DATA SHEET

GPLB30A

LCD CONTROLLER

JAN. 07, 2008

Version 1.4

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LCD CONTROLLER

1. GENERAL DESCRIPTION

The GPLB30A, an 8-bit CMOS microprocessor, contains 2752 bytes working RAM, 96K bytes ROM, 7 I/Os, interrupt/wakeup controller, UART for serial communication, Serial SRAM interface and Bus memory interface for memory expansion, and automatic display controller/driver for LCD. It also features one PWM driver with two audio channels to produce attractive sound effects easily. Its large ROM area can be used to store both program and audio data. The built-in UART speeds up data transmission between two devices. Furthermore, a SLEEP (power-down) function is also built in to extend power life. The GPLB30A is designed with state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

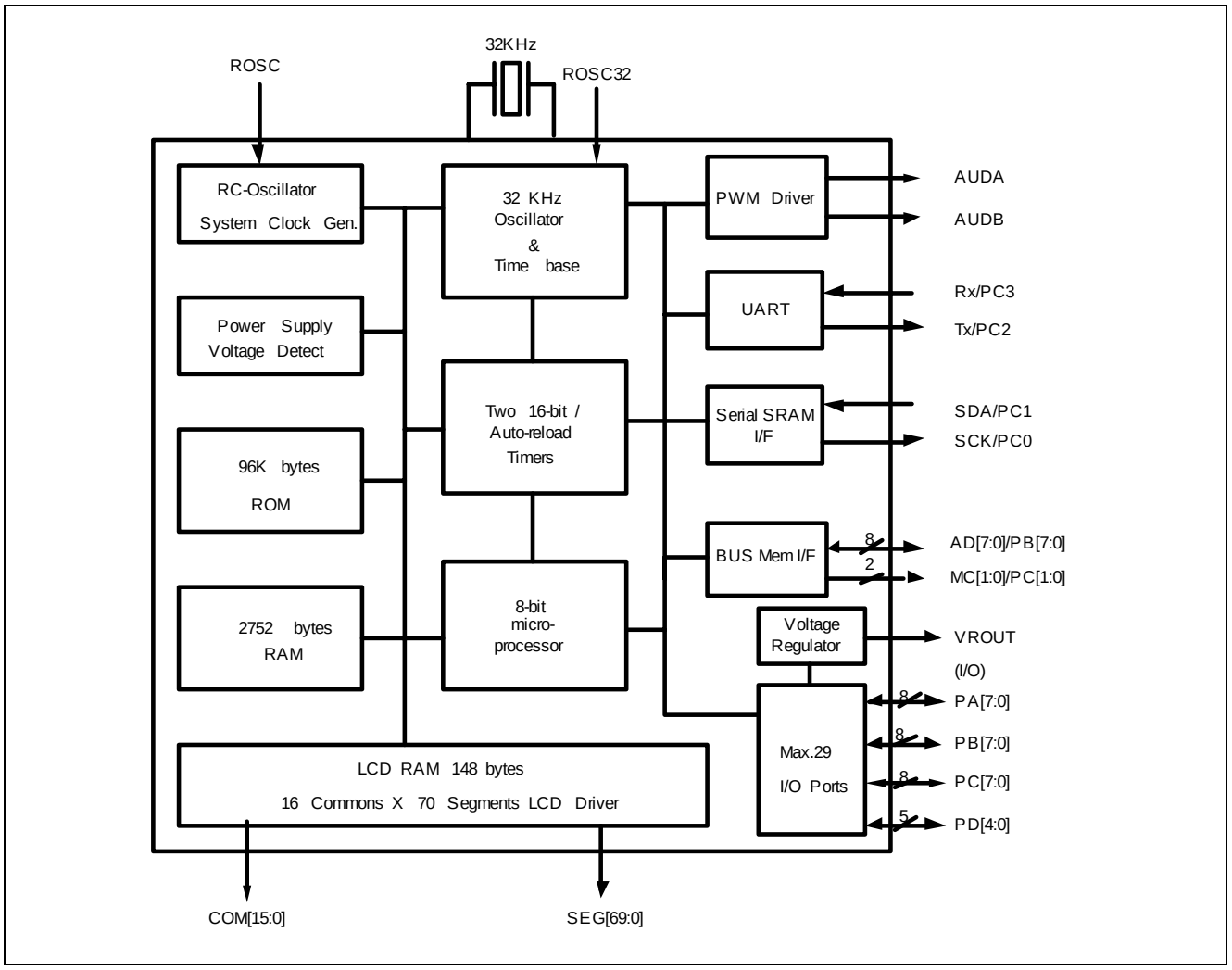
2. FEATURES

- Built in 8-bit processor
  - **2752 bytes SRAM**
  - **96K bytes ROM**
  - Max. operating speed: 4.0MHz @ 2.4V - 3.6V
    5.0MHz @ 3.6V - 5.5V
  - CPU clock is software programmable, can be /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
  - Provides 6 wake-up sources
  - Provides 7 interrupt sources
- Universal Asynchronous Receiver and Transmitter (UART)
- Serial SRAM interface
- Bus memory interface
- Built-in voltage regulator for external memory devices
- Key scan function
  - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
  - **Up to 70 segments, up to 16 commons, maximum 1120 dots**
  - 1/5 bias; 1/16 duty capability
  - **140 bytes dedicated LCD RAM**
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 32-level contrast control (2.45V - 5.75V, in 1/5 bias)
- **Power saving SLEEP mode**
- **Low Voltage Detector**
  - **8-level 2.9V - 2.2V/4.35V - 3.3V detection**
  - **2.2V Low voltage reset**
- **Peripherals**
  - **Max. 29 I/O pins (PA[7:0], PB[7:0], PC[7:0], PD[4:0])**
    . Dedicated I/Os: PA[0:4]
    . Shared pin I/Os:
    PA[5:7]/SEG[69:67]
    PB[0:7]/BMI AD BUS[0:7]/SEG[64:57]
    PC[0:1]/BMI MC[0:1]/SSRAM SDA, SCK
    PC[2:3]/UART Tx/Rx/SEG[66:65]
    PC[4:7]/SEG[56:53]
    PD[0:4]/SEG[52:48]
  - 32.768KHz oscillator circuit for RTC
  - RC-oscillator (only one resistor is needed)
  - Two 16-bit reloadable timer/counters
  - **8-bit DAC resolution, 2-channel PWM audio outputs**
  - Watchdog Timer for reliable operation
- Low power consumption:
  - 600μA typical @ 3.0V, F_{CPU} = 1.0MHz, F_{OSC} = 4.0MHz
  - 25μA typical halt current @ 3.0V
  - <1μA typical standby current @ 3.0V
- Wide operating voltage range:
  - 2.4V - 3.6V
  - 3.6V - 5.5V

3. APPICATION FIELD

- Handheld game
- Scientific calculator
- Talking calculator, Talking clock
- Talking instrument controller
- General speech synthesizer
- Data bank

4. BLOCK DIAGRAM



Note1: PA[5:7] share pins with SEG[69:67] (mask option).
Note2: PB[0:7] share pins with SEG[64:57] (mask option).
Note3: PC[0:1] share pins with Bus memory interface MC[0:1]. Also share pins with Serial SRAM interface SCK/SDA.
Note4: PC[2:3] share pins with UART Tx/Rx. Also share pins with SEG[66:65].
Note5: PC[4:7] share pins with SEG[56:53] (mask option).
Note6: PD[0:4] share pins with SEG[52:48] (mask option).

5. SIGNAL DESCRIPTIONS

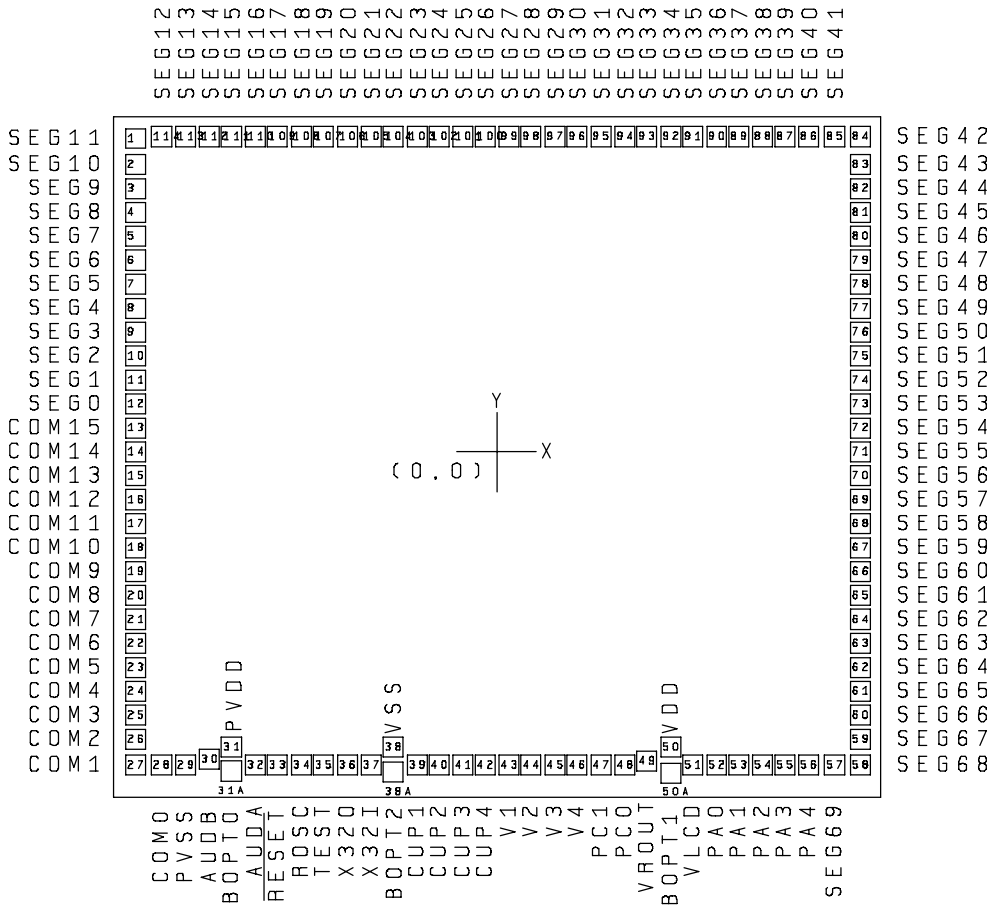
Total: 114 pins

Mnemonic	PIN No.	Type	Description
SEG11 - 0	1 - 12	O	LCD driver segment output. SEG15 - 0 share pin with key scan port.
SEG47 - 12	79 - 114	O	
SEG69 - 67 / PA5 - 7	57 - 59	I/O	SEG69 - 67 optioned to PA5 - 7.
SEG66 - 65 / PC2 - 3 / Tx, Rx	60 - 61	I/O	SEG66 - 65 optioned to PC2/Tx, PC3/Rx.
SEG64 - 57 / PB0 - 7	62 - 69	I/O	SEG64 - 57 optioned to PB0 - 7.
SEG56 - 53 / PC4 - 7	70 - 73	I/O	SEG56 - 53 optioned to PC4 - 7(PortC 4, 5 shared with Ext-I, Ext-ck).
SEG52 - 48 / PD0 - 4	74 - 78	I/O	SEG52 - 48 optioned to PD0 - 4.
COM15 - 0	28 - 13	O	LCD driver common output.
PA4 - 0	56 - 52	I/O	Port A is a bi-directional I/O port, which can be software programmed as wake up I/O.
PC0 / MC0 / SCK PC1 / MC1 / SDA	48 47	I/O	Port C is a bi-directional I/O port. Share pin with Bus Extender MC1 - 0. Also share pin with SDA/SCK.
ROSC	34	I	R-oscillator input, connect to VDD through a resistor.
$\overline{\text{RESET}}$	33	I	System reset input, low active.
AUDA, AUDB	32, 30	O	PWM audio output.
X32I	37	I	32.768KHz crystal input or connects to VDD through a resistor (option).
X32O	36	O	32.768KHz crystal output.
TEST	35	I	Test input.
VROUT	48	P	Internal regulator output. Enable or disable via bonding option. Should be connected to VDD if internal Regulator is disabled.
CUP4 - 1	42 - 39	P	LCD voltage generation. Charge pump capacitor inter-connection pins.
VLCD	51	P	LCD voltage generation.
V4 - 1	46 - 43	P	LCD voltage generation.
VDD	50	P	Power supply voltage input.
VSS	38	P	Ground reference.
PVDD	31	P	PWM driver power.
PVSS	29	P	PWM driver ground reference.
BOPT0 BOPT1	31A 50A	B	Internal regulator output voltage select option pin (internally pull-low)*.
BOPT2	38A	B	Internal regulator enable/disable option pin (internally pull-high)*.

Legend: I = Input, O = Output, P = Power, B = Bonding option

Note*: See bonding option section for details.

5.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.
Note2: Pin VROUT should be connected to VDD if internal Regulator is disabled.

6. FUNCTIONAL DESCRIPTIONS

6.1. Memory

The GPLB30A contains 96K-byte ROM and 2752-byte SRAM. Cooperating with Generalplus bus extender, GPBA01B, the external memory, either RAM or ROM, can be extended up to 4MB. Serial SRAM interface is also provided in GPLB30A, thus SRAM space can be extended by using Generalplus Serial SRAM, GPRS256B or GPRS512C.

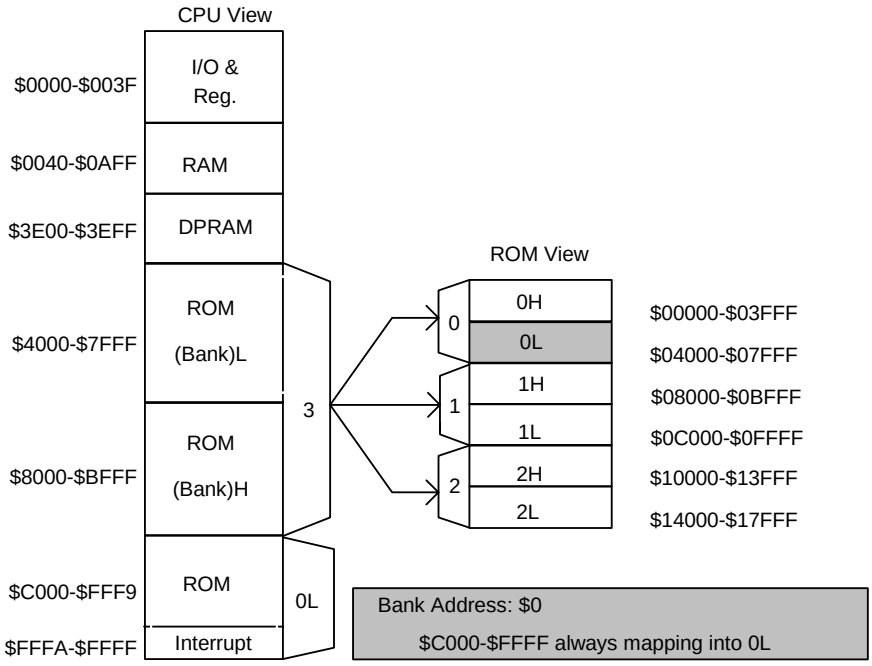
6.2. Map of Memory and I/Os

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



1. $4000-$BFFF can be external memory if MEXT ($07.7) =1 and Bank port ($00.7)=1.
2. $C000-$FFFF can be external memory if MEXT ($07.7) =1 and EXC($0b.1)=1.
3. User program should start from $C800. $C000-$C7FF is the test program area.
4. User program interrupt vector: $FFFA ~ $FFFF.
5. Test program interrupt vector: $FFF2 ~ $FFF7.

6.3. Operating States

There are three operation modes involved in GPLB30A/31A: standby, halt and operating. The following table shows the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

6.3.1. Operating mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest current.

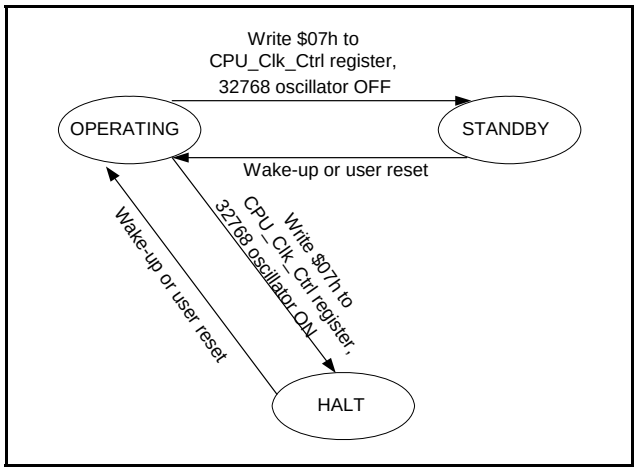
6.3.2. Standby mode

Write “07H” to P_04H_CPU_Clk_Ctrl Register ($04) and turn off 32768Hz oscillator to activate standby mode. The standby mode is a mode where the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

6.3.3. Halt mode

Write “07H” to P_04H_CPU_Clk_Ctrl Register ($04) but still keeps 32768Hz oscillator running to enter halt mode. In halt mode, CPU clock halts and waits for an event (key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPLB30A state diagram:



GPLB30A State Diagram

6.4. Speech and Melody

For speech synthesis, the GPLB30A provides several timer interrupts for a precise sampling frequency. The sound data can be stored into ROM and be played back. Several algorithms are recommended for high fidelity and good compression of sound such as PCM and ADPCM.

For melody synthesis, the GPLB30A provides a dual tone mode. Once in the dual tone mode, users only need to program the tone frequency for each channel by writing to the timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically.

6.5. LCD Controller/Driver

The GPLB30A contains an 1120-dot LCD controller/driver. A programmer is able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768 oscillator running. The LCD driver in GPLB30A supports 1/16 duty and 1/5 bias.

6.6. LCD Voltage Generation

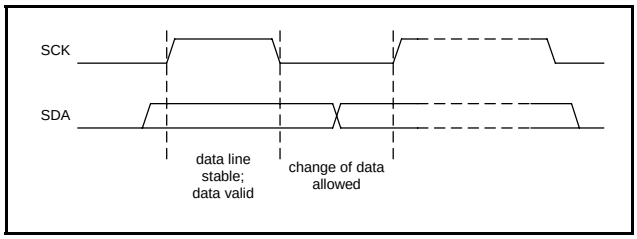
The GPLB30A offers a voltage regulator and a charge-pumping circuit. The voltage regulator provides a reference voltage (V2) for the charge-pumping circuit to generate VLCD. Users can get the desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 2.45V to 5.75V with 32 levels.

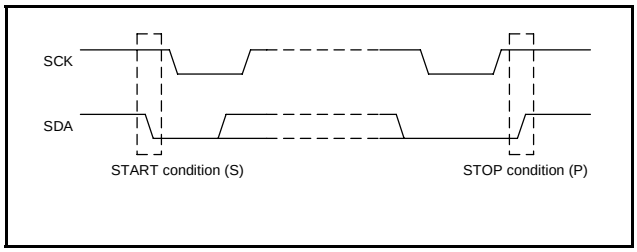
6.7. PWM Output

Internally, the GPLB30A has a pair of PWM drivers, supporting two sound channels. Each channel is able to play speech or tone individually. The PWM drivers can directly drive speaker or buzzer without buffer or amplification circuit.

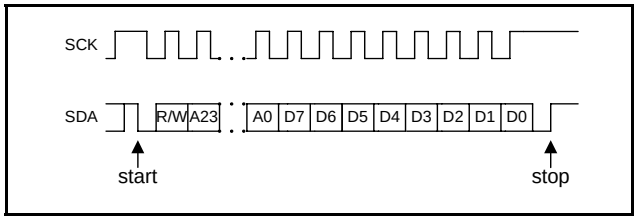
6.8. Serial SRAM Interface

The Serial SRAM interface is able to expand the data storage SRAM. The Control Registers are ranged from $30-$36. Note that The pins of SDA and SCK are shared with PC [1:0] and therefore, users should set PC[1:0] as Serial SRAM interface by writing to Port $27[1:0].

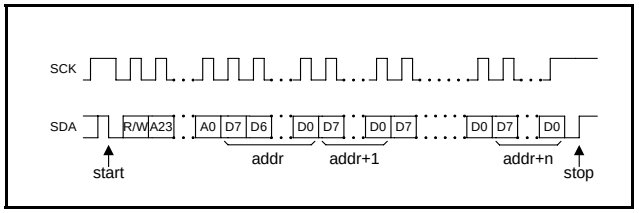




6.8.1. Read/Write timing



6.8.2. Continuous Read/Write timing



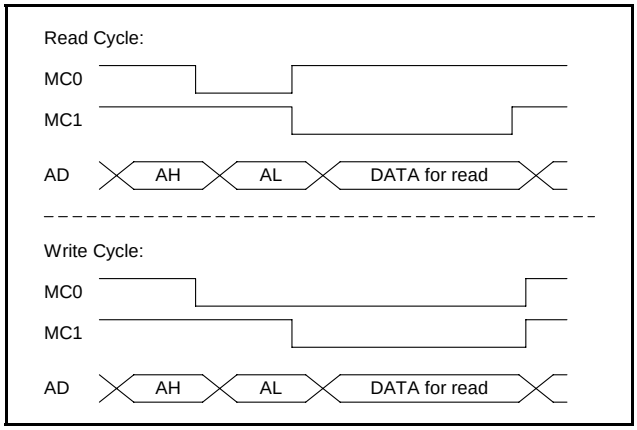
6.9. Bus Memory Interface

A built-in Bus memory interface is available on GPLB30A. Through the use of Bus memory interface, user can expand the memory space by using a external Bus memory (SRAM, mask ROM or Flash). The Bus memory interface includes 10 signal

pins: MC1, MC0 and AD BUS[7:0] which shared pin with port B. Before using the Bus memory interface, users should set MEXT=1 ($03.7) and BANK register ($0), then access address $4000-BFFF to read or write data from external bus memory. Note that when using Bus memory interface, CPU clock setting can not be set as F_{OSC}/1, should be /2 or slower.

MC1	MC0	AD BUS [7:0]
L	L	Data for Write
L	H	Data for Read
H	L	AL (Address Low byte)
H	H	AH (Address High byte)

The simple timing relation is as follows:



6.10. Voltage Regulator

The GPLB30A offers a voltage regulator, which supplies power source for external memory devices. The voltage regulator can output four voltage levels, 2.5V/2.6V/2.7V/3.0V via bonding option. The output voltage level should be properly selected based on the electrical characteristics of external memory devices involved.

6.11. Asynchronous Serial Interface (UART)

The GPLB30A supports a 1-channel UART for serial communications. The bit-rate is up to 115.2kbps. UART operation is controlled by UART command registers. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be configured in the command registers. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt activates when a byte is received or transmitted. Reading the status register informs whether the interrupt is generated by Rx or Tx. Frame, overrun and parity errors are detected as each byte is received and all error status can be read from status register.

The UART supports clock auto calibration. If auto calibration is selected, standard baud rate from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to the baud rate control registers. The supported baud rates and their minimum R-oscillator clock frequency requirements are shown in the table below.

Baud Rate(bps)	Min. Frosc(Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto calibration is not selected, users can get desired baud rates by writing appropriate values to pre-scalar registers. Non-standard baud rates can be obtained by this method. In the non-calibration mode, users should understand that the R-oscillator frequency may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

6.12. Low Voltage Detection

The GPLB30A provides an 8-level (Software programmable) low voltage detector to detect low voltage events. Users can turn on the low detection to monitor VDD periodically to check if it is lower than the given value. In addition, if LV NMI is enabled, a NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops below 2.2V. *When LVR function is enabled, care must be taken not to turn off 32kHz crystal oscillator. Otherwise an unexpected reset may occur when 32kHz crystal is being turned on again.*

6.13. Key Scan Function

GPLB30A supports key scan function. The LCD driver will generate a key strobe signal in the period of every common. When PA received this strobe signal, a wake-up is issued. Then users can send the key scan signal through SEG[15:0] to determine the location of the depressed key.

6.14. Watchdog Timer (WDT)

An on chip watchdog timer is also available in the GPLB30A. The WDT is designed to recover the system from abnormal operation. In some cases, if WDT is not cleared for one second, the WDT will generate a system reset to restart system. If WDT

is enabled, the WDT should be cleared every 0.5 second to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.15. Bonding Options

6.15.1. Voltage regulator

- Enable
- Disable

6.15.2. Regulator output selection

- 2.5V
- 2.6V
- 2.7V
- 3.0V

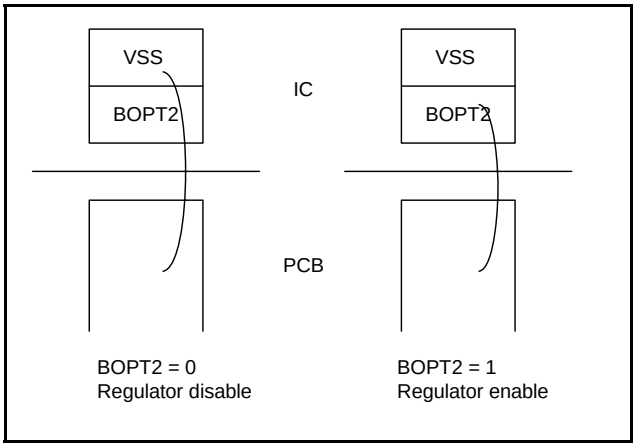


Figure1: Bonding option for regulator Enable/Disable

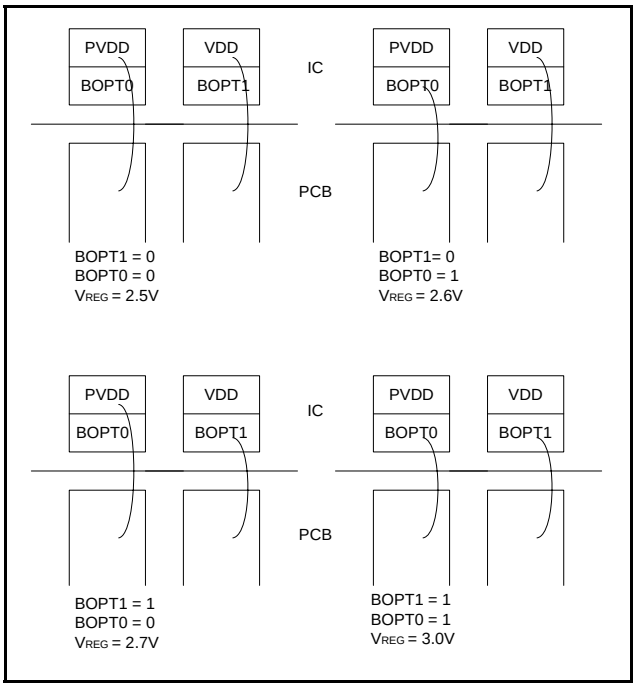


Figure2: Bonding option for regulator output voltage select

6.16. Mask Options

6.16.1. 32768 oscillator

- X'TAL
- R-oscillator

6.16.2. Watchdog timer

- Enable
- Disable

6.16.3. PA[5:7]/SEG[69:67]

Each port/segment can be optioned as I/O or LCD segment individually.

6.16.4. PA[2:3]/Tx,Rx/SEG[66:65]

Each port/segment can be optioned as I/O or LCD segment individually.

6.16.5. PB[0:7]/SEG[64:57]

Each port/segment can be optioned as I/O or LCD segment individually.

6.16.6. PC[4:7]/SEG[56:53]

Each port/segment can be optioned as I/O or LCD segment individually.

6.16.7. PD[0:4]/SEG[52:48]

Each port/segment can be optioned as I/O or LCD segment individually.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to + 60℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

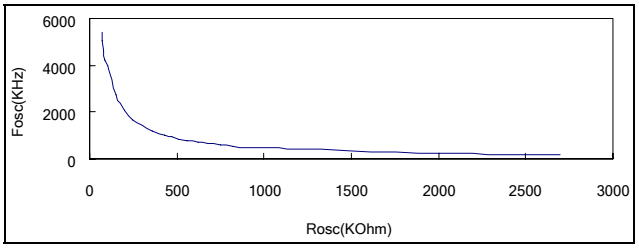
7.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	600	-	μA	F_{CPU} = 1.0MHz @ 3.0V F_{OSC} = 4.0MHz, no load
Halt Current	I_{HALT1}	-	18	-	μA	VDD = 3.0V, 32K X'tal ON, Maximum VLCD, Strobe on, Pump clock =32KHZ, no LCD panel
Halt Current	I_{HALT2}	-	9.0	-	μA	VDD = 3.0V, 32K X'tal ON, Maximum VLCD, Strobe off, Pump clock =4KHZ, no LCD panel
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, all off
Audio Output Current	I_{OH}	-	-20	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-40	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Audio Output Current	I_{OL}	-	20	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	40	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	1.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	2.45	-	5.75	V	VDD = 3.0V, 1/5 bias, no load
Regulator Output Voltage	V_{REG}	-	2.5	-	V	Output voltage is selected by bonding option
		-	2.6	-		
		-	2.7	-		
		-	3.0	-		
Regulator Output Voltage Drop	V_{RDROP}	-	-	100	mV	I_L = 1.0mA, VDD = 3.6V
OSC Resistor	R_{OSC}	-	200K	-	Ω	F_{OSC} = 2.0MHz @ 3.0V
CPU Clock	F_{CPU}	-	-	4.0	MHz	F_{CPU} = F_{OSC}/1 @ 2.4V
		-	-	5.0	MHz	F_{CPU} = F_{OSC}/1 @ 3.6V

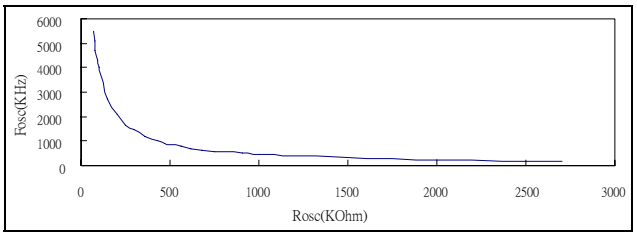
Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

7.3. The Relationships between the R_{OSC} and the F_{CPU}

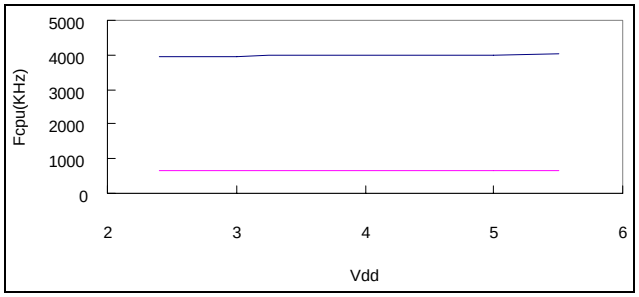
7.3.1. VDD = 3.0V, T_A = 25℃



7.3.2. VDD = 4.5V, T_A 25℃

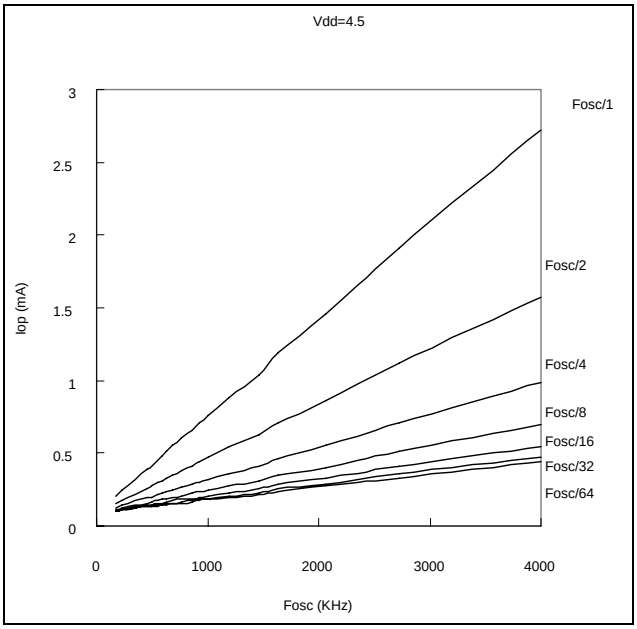


7.4. The Relationships between the F_{CPU} and the VDD



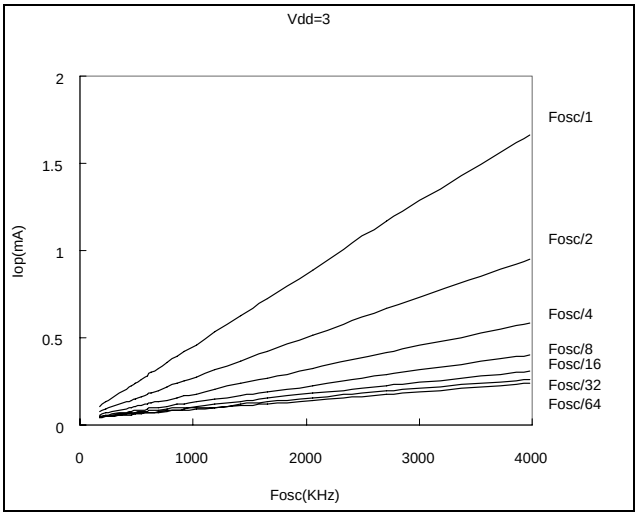
7.5. The Relationships between the F_{CPU} and the I_{OP}

7.5.1. When VDD = 4.5V



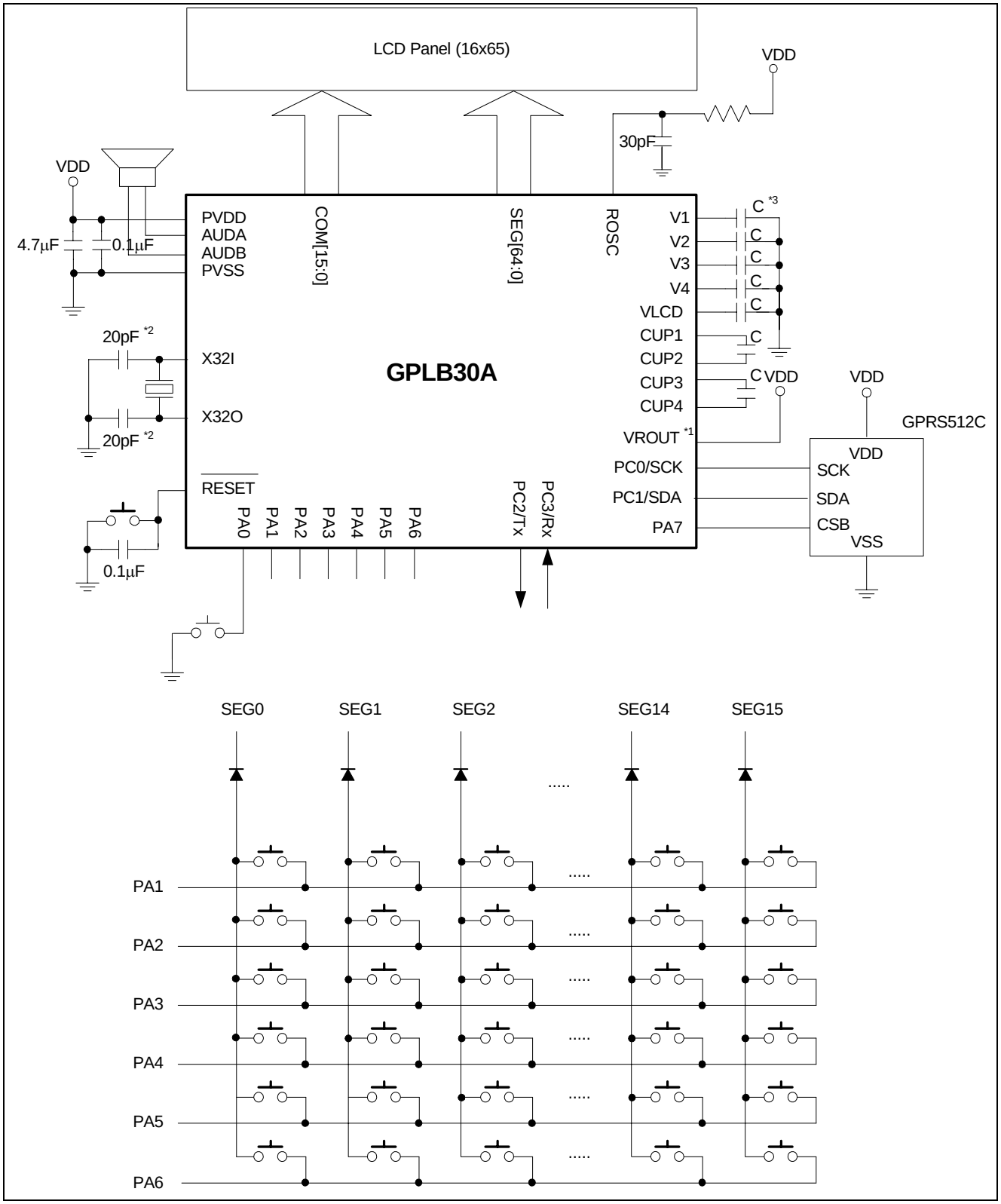
7.6. The Relationships between the F_{CPU} and the I_{OP}

7.6.1. When VDD = 3.0V



8. APPLICATION CIRCUITS

8.1. 1040 Dots LCD Driver, 65 Segments × 16 Commons, 1/5 Bias with External Serial SRAM, Regulator Disabled- (1)

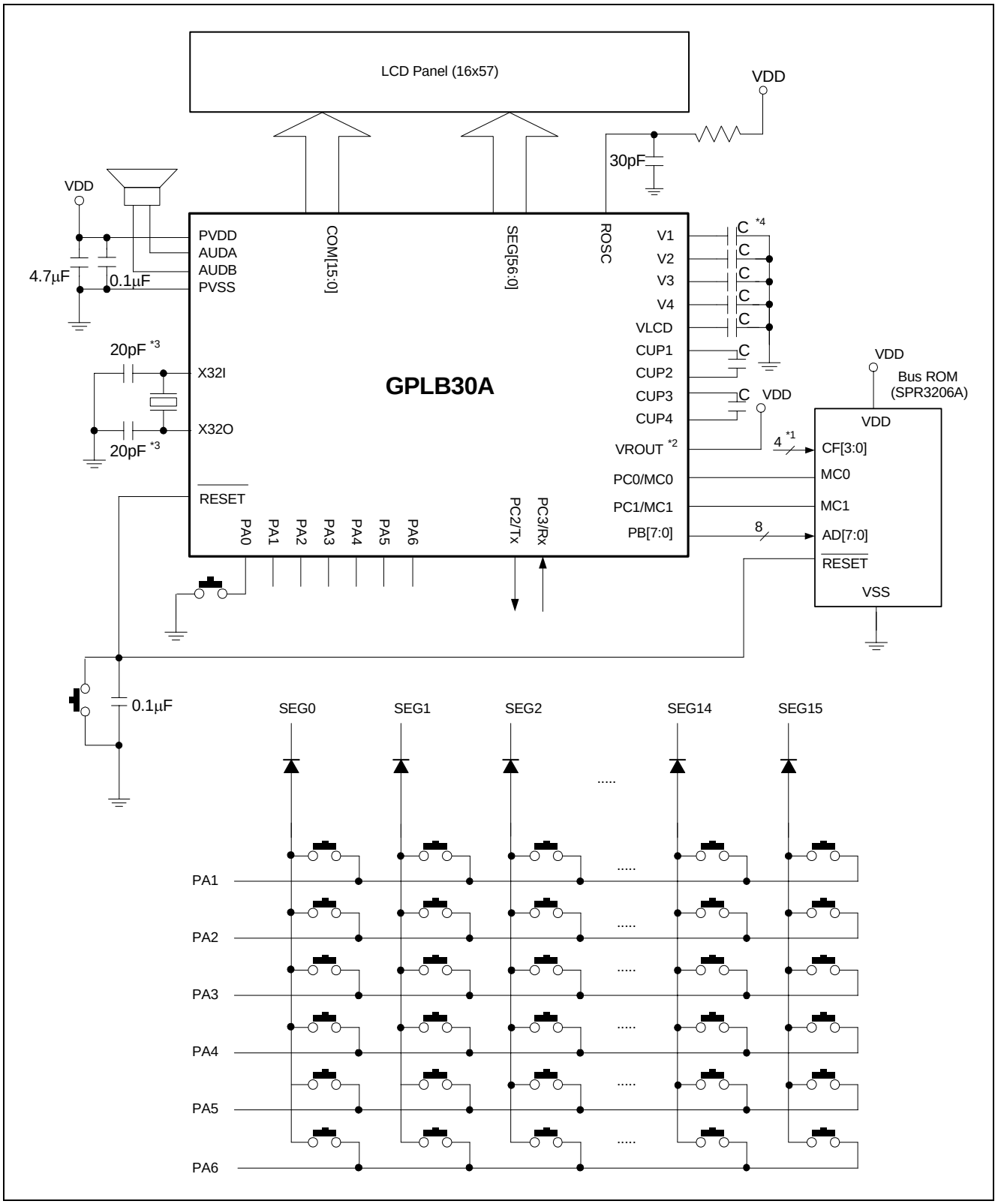


Note*1: Pin VROUT should be connected to VDD if internal Regulator is disabled.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*3: The value of the capacitance(C) would range from 0.1μF to 4.7μF to stable the output voltage.

8.2. 912 Dots LCD Driver, 57 Segments × 16 Commons, 1/5 Bias with External Bus ROM, Regulator Disabled - (2)



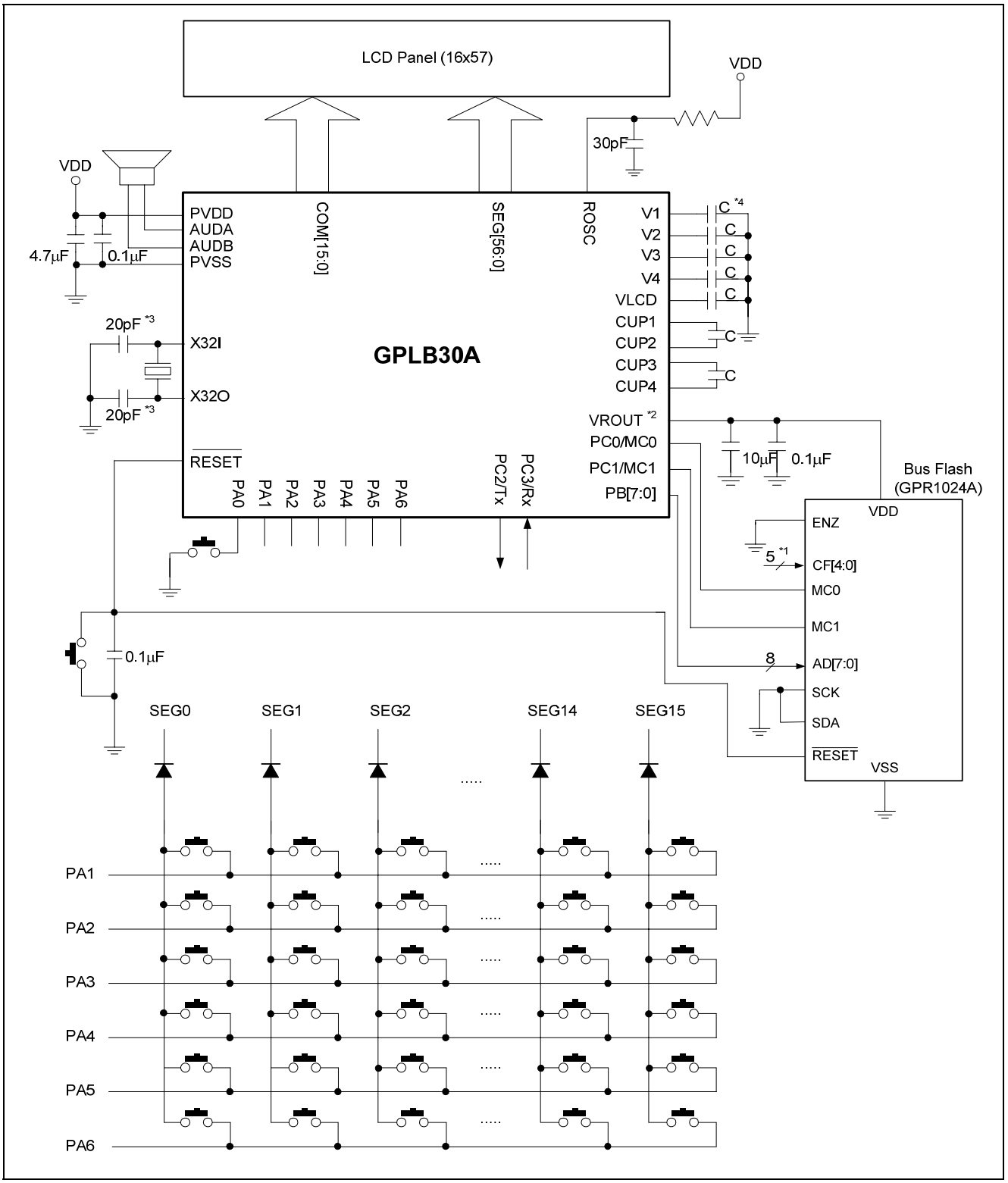
Note*1: Detail settings of these pins please refer to the data sheet of SPR3206A.

Note*2: Pin VROUT should be connected to VDD if internal Regulator is disabled.

Note*3: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*4: The value of the capacitance(C) would range from 0.1μF to 4.7μF to stable the output voltage.

8.3. 912 Dots LCD Driver, 57 Segments × 16 Commons, 1/5 Bias with External Bus Flash, Regulator Enabled - (3)



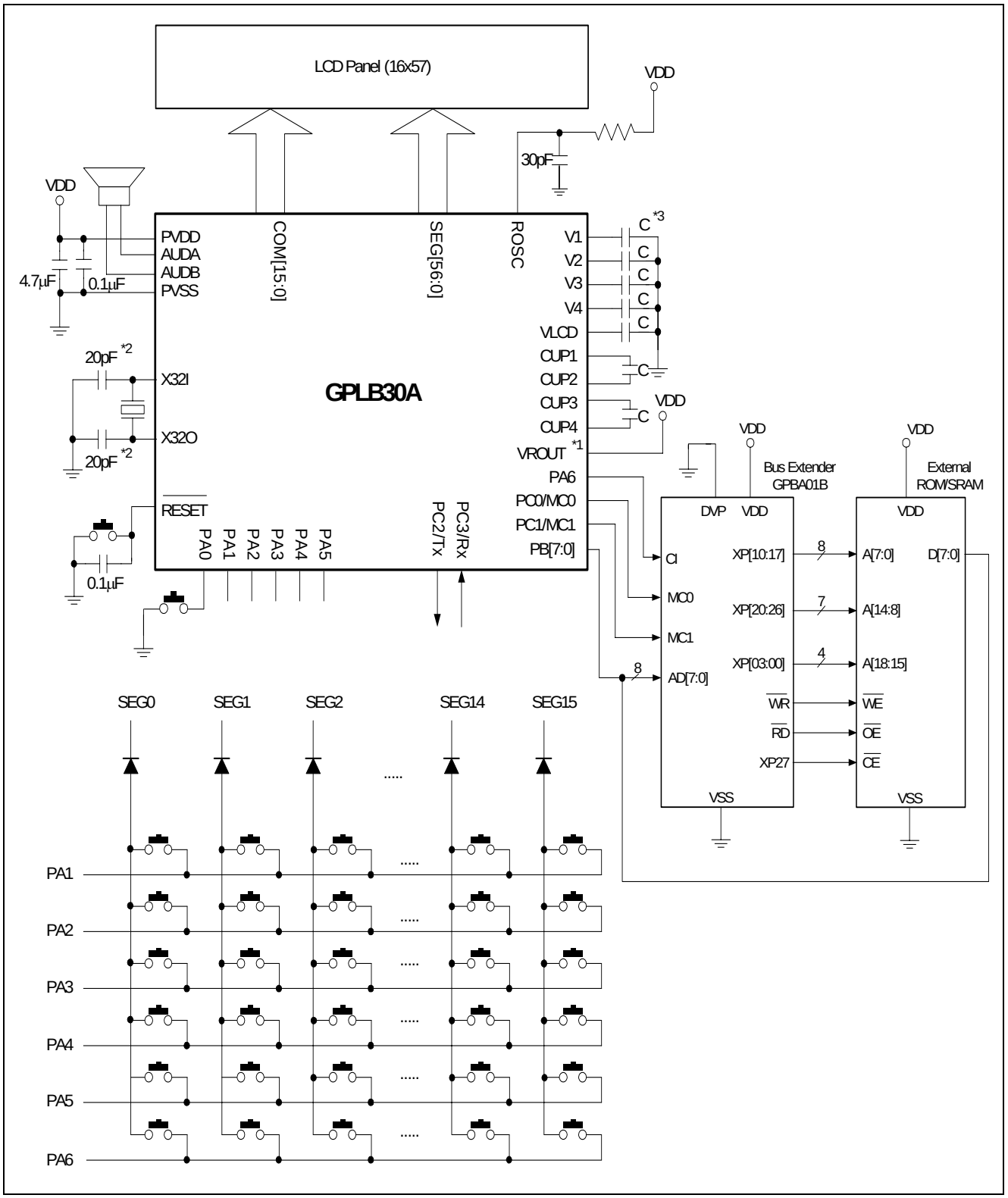
Note*1: Detail settings of these pins please refer to the data sheet of GPR1024A.

Note*2: Pin VROUT should be connected to VDD if internal Regulator is disabled.

Note*3: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*4: The value of the capacitance(C) would range from 0.1μF to 4.7μF to stable the output voltage.

8.4. 912 Dots LCD Driver, 57 Segments × 16 Commons, 1/5 Bias with Bus Extender, Regulator Disabled - (4)

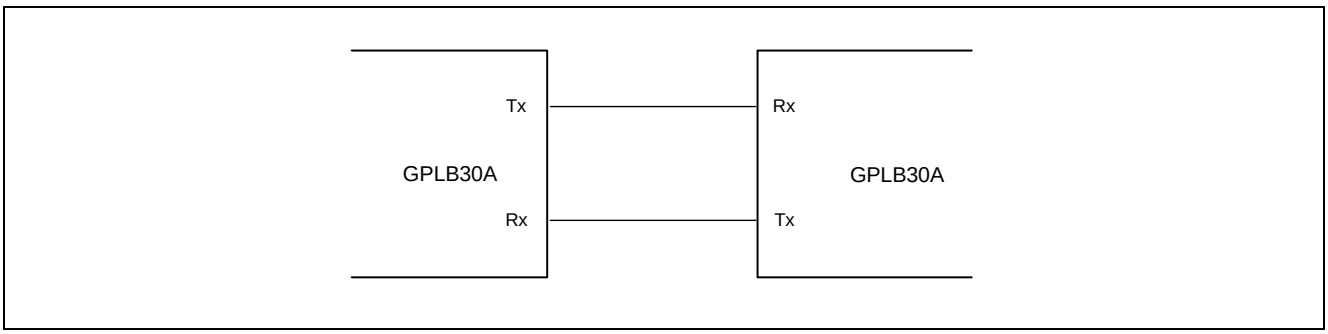


Note*1: Pin VROUT should be connected to VDD if internal Regulator is disabled.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*3: The value of the capacitance(C) would range from 0.1µF to 4.7µF to stable the output voltage.

8.5. Serial Communications between two GPLB30As - (5)



9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPLB30A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
JAN. 07, 2008	1.4	Modify the diagrams in section 8. APPLICATION CIRCUITS.	13 - 17
DEC. 12, 2006	1.3	Modify the description to section 6.12.	8
DEC. 12, 2005	1.2	1. Modify port C shared pin to section 4 and 5. 2. Modify the descriptions to section 6.1 and 8.	2, 3 4, 10
APR. 18, 2005	1.1	1. Modify application circuit: (1) A capacitor with 30pF should be added on the net ROSC pin. The pictures should be modified are located at the section 8. application circuits. 2. Correct pin type in section 5 3. Correct dedicated LCD RAM: 148 to 140	10 - 14 2 1
MAR. 10, 2005	1.0	Original Note: The GPLB30A data sheet v1.0 is a continued version of SPLB30A data sheet v0.5.	18