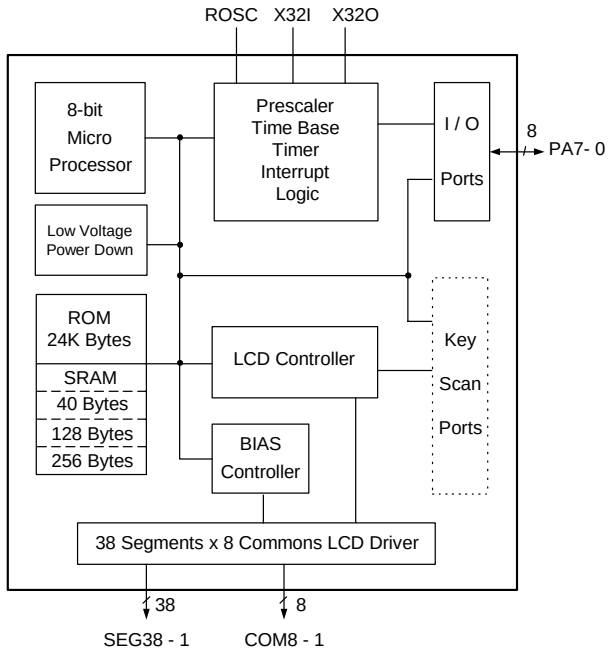
304 DOTS DATA BANK

1. GENERAL DESCRIPTION

GPLB21C is an 8-bit CMOS microprocessor with advanced processing technology and mechanisms by Generalplus. It includes 2K-bytes working RAM, 22K-bytes ROM, 8 I/Os, an interrupt controller, a timer and a LCD controller/driver. The 22K-byte ROM provides proper space for LCD graphic data. The 256 bytes of CPU working SRAM is available to users for programming and data storage. The GPLB21C is capable of driving sophisticated functions and displaying remarkable LCD graphics. A Sleep (power-down) feature is also built-in to reduce power consumption. The GPLB21C is a high-end micro-controller that includes, not only the latest technology, but also the full commitment and support of Generalplus. Clearly the most suitable solution for your product needs.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit CPU (CPU14B)
- 22K bytes ROM
- 40 bytes dual port SRAM for 38 x 8 LCD display buffer
- 128 bytes SRAM for CPU working space
- 256 bytes SRAM for data
- 8 I/O ports
- LCD controller/driver (1/4 bias, V_{OP} = VDD, Type-B)
  - . 38 x 8 (304 dots)
  - . 38 x 6 (228 dots)
- Built-in R-oscillator and 32.768KHz crystal oscillator
- 8-bit Reloadable timer/counter with pre-scaler
- NMI controller with following sources
  - . 2Hz for RTC
  - . 128Hz
  - . Key (PA7 - 0)
  - . Counter overflow
- Halt and Standby mode
- Low Voltage Power Down (LVPD)
- Wide operating range: 2.4V - 3.6V @ 1.0MHz
  3.6V - 5.5V @ 1.0MHz
- Power saving sleep mode

4. APPLICATION FIELD

- Hand held games
- Pet games
- Educational games, etc.

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	9	I	Power supply input
VSS	22	I	GND
RESET	11	I	System reset input (internal pull-high), low active
TEST	61	I	Test input (internal pull-low), high active
X32I	13	I	32.768 KHz crystal input
X32O	12	O	32.768 KHz crystal output
ROSC	10	I	R-oscillator input, connect a resistor to VDD through a resistor
PA7 - 0	21 - 14	I/O	Input / output port
COM8 - 1	8 - 1	O	LCD common output. COM7, COM8 can be reassigned as IOZ6, IOZ7 bi-directional I/O port.
SEG38 - 1	23 - 60	O	LCD segment output. See note 1 below.

Note1: SEG16 - 1 can be used as keyboard scan output pins by software programming register ($007E).

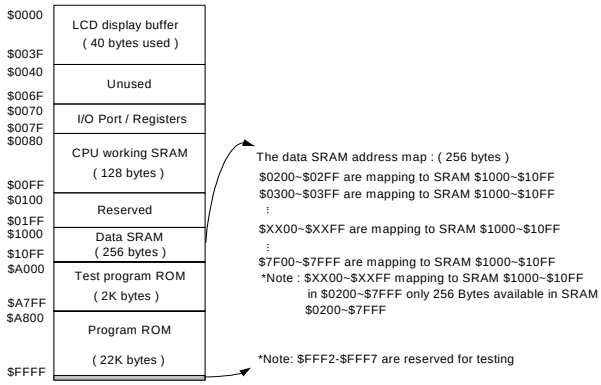
Note2: When the ROSC mode is selected, pin X32I should be connected to VSS and pin X32O should be floating.

Key scan options are as follows:

Key scan port No.	Key scan assignment options	($ 007E) bit 2, bit 1, bit 0
1 - 8	SEG8 - 1 or SEG16 - 9	1, 0, 1 1, 1, 0
9 - 16	SEG16 - 1	1, 1, 1

6. FUNCTIONAL DESCRIPTIONS

6.1. ROM Area



6.2. Mask Options

6.2.1. 32K from Crystal / R-osc with prescaler

When the crystal mode is selected, the system time base, LCD timing, and auto-strobe signal is generated form the 32.768KHz crystal oscillator. The R-osc option is provided to support system timebase, LCD timing, and auto-strobe signal without 32.768KHz crystal oscillator. When the R-osc mode is selected, the signals and timings will be generated from pre-scaler. By programming register ($007C), users can get a suitable clock (R-osc) to replace the 32.768 KHz clock. Bit-5 of register ($007A) can also turn off this clock.

6.3. LCD Mapping and Specification

SRAM space ($00H - $3F) is allocated for LCD display buffer. To display a pattern on the LCD, the user simply writes the corresponding bits as display buffer. The following table shows the mapping between LCD and display buffer.

	SEG8 - 1 (b7 - b0)	SEG16 - 9 (b7 - b0)	SEG24 - 17 (b7 - b0)	SEG32 - 25 (b7 - b0)	SEG38 - 33 (b5 - b0)
COM1	07H	06H	05H	04H	03H
COM2	0FH	0EH	0DH	0CH	0BH
COM3	17H	16H	15H	14H	13H
COM4	1FH	1EH	1DH	1CH	1BH
COM5	27H	26H	25H	24H	23H
COM6	2FH	2EH	2DH	2CH	2BH
COM7	37H	36H	35H	34H	33H
COM8	3FH	3EH	3DH	3CH	3BH

The GPLB21C supports LCD's with the following characteristics:

Duty: 1/6 or 1/8

Bias: 1/4; V_{LCD} = VDD

V_1 = VDD * 3/4

V_2 = VDD * 2/4

V_3 = VDD * 1/4

VEE = GND

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 6.0V
Input Voltage Range	V_{IN}	-0.5V to VDD + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

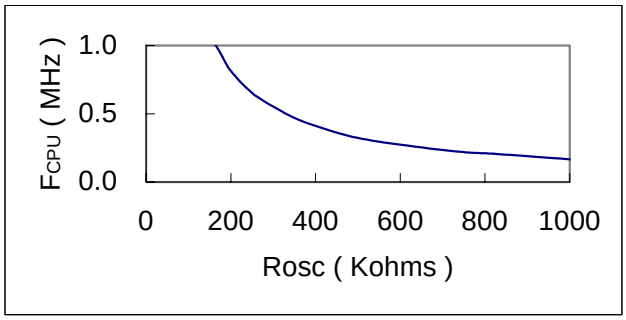
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	160	-	μA	F_{CPU} = 500KHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V, 32768Hz OFF
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I (PA5 - 0)	I_{OH}	-	-1.0	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I (PA5 - 0)	I_{OL}	-	1.0	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Output High I (PA7 - 6)	I_{OH}	-	-2.5	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I (PA7 - 6)	I_{OL}	-	2.5	-	mA	VDD = 3.0V, V_{OL} = 1.0V
OSC Resistor	R_{OSC}	-	330	-	Kohm	F_{CPU} = 500KHz @ 3.0V
CPU Clock	F_{CPU}	-	-	1.0	MHz	VDD = 3.0V

7.3. DC Characteristics (VDD = 4.5V, T_A = 25℃)

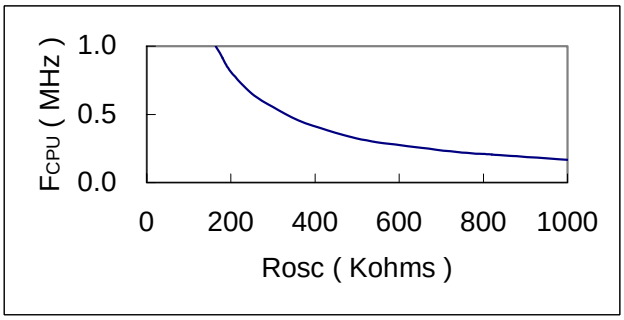
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	400	-	μA	F_{CPU} = 500KHz @ 4.5V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 4.5V, 32768Hz OFF
Input High Level	V_{IH}	3.0	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 4.5V
Output High I (PA5 - 0)	I_{OH}	-	-1.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PA5 - 0)	I_{OL}	-	1.0	-	mA	VDD = 4.5V, V_{OL} = 0.8V
Output High I (PA7 - 6)	I_{OH}	-	-3.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PA7 - 6)	I_{OL}	-	3.0	-	mA	VDD = 4.5V, V_{OL} = 0.8V
OSC Resistor	R_{OSC}	-	330	-	Kohm	F_{CPU} = 500KHz @ 4.5V
CPU Clock	F_{CPU}	-	-	1.0	MHz	VDD = 4.5V

7.4. The Relationship between the R_{OSC} and the F_{CPU}

7.4.1. VDD = 3.0V, T_A = 25℃

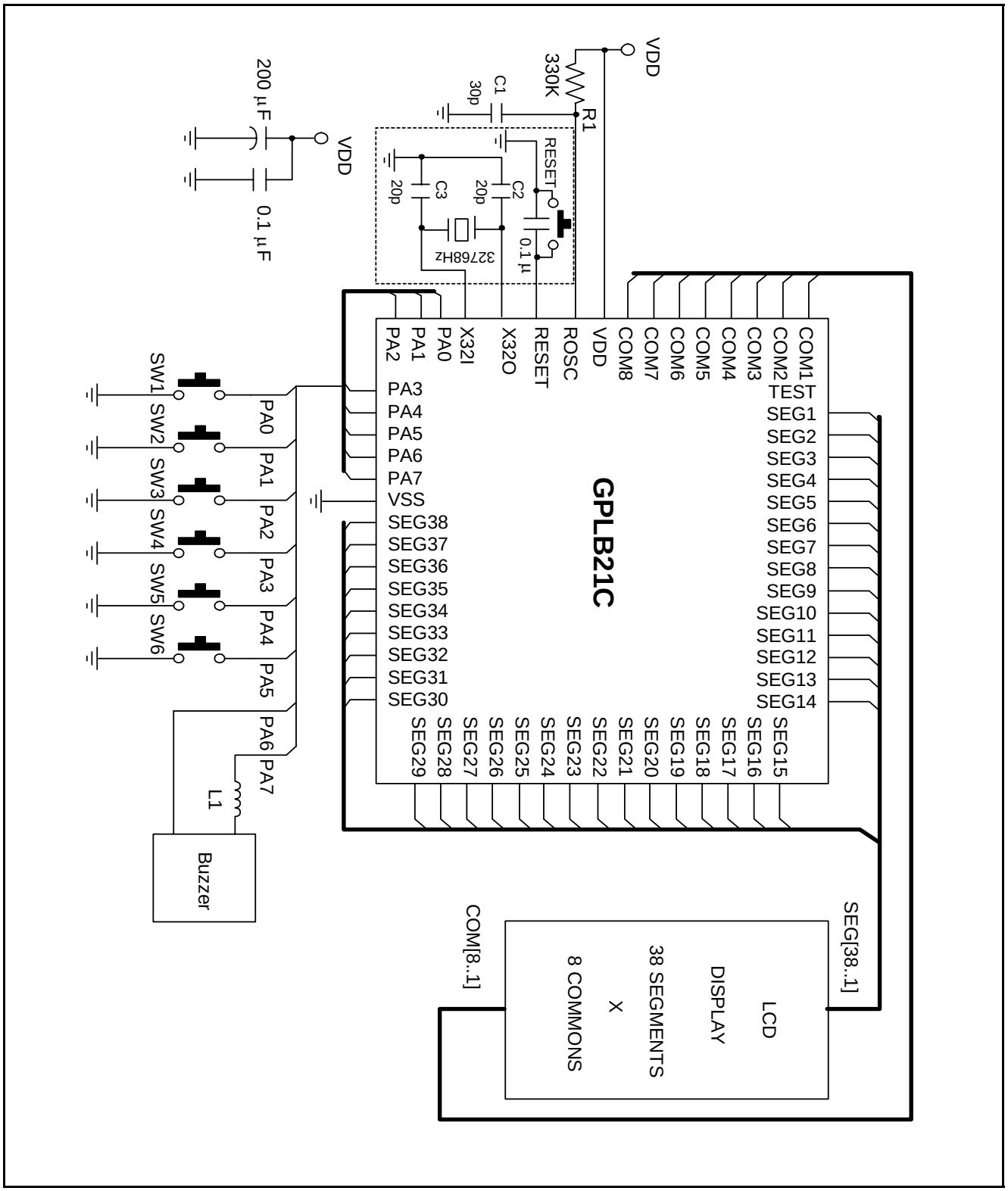


7.4.2. VDD = 4.5V, T_A = 25℃

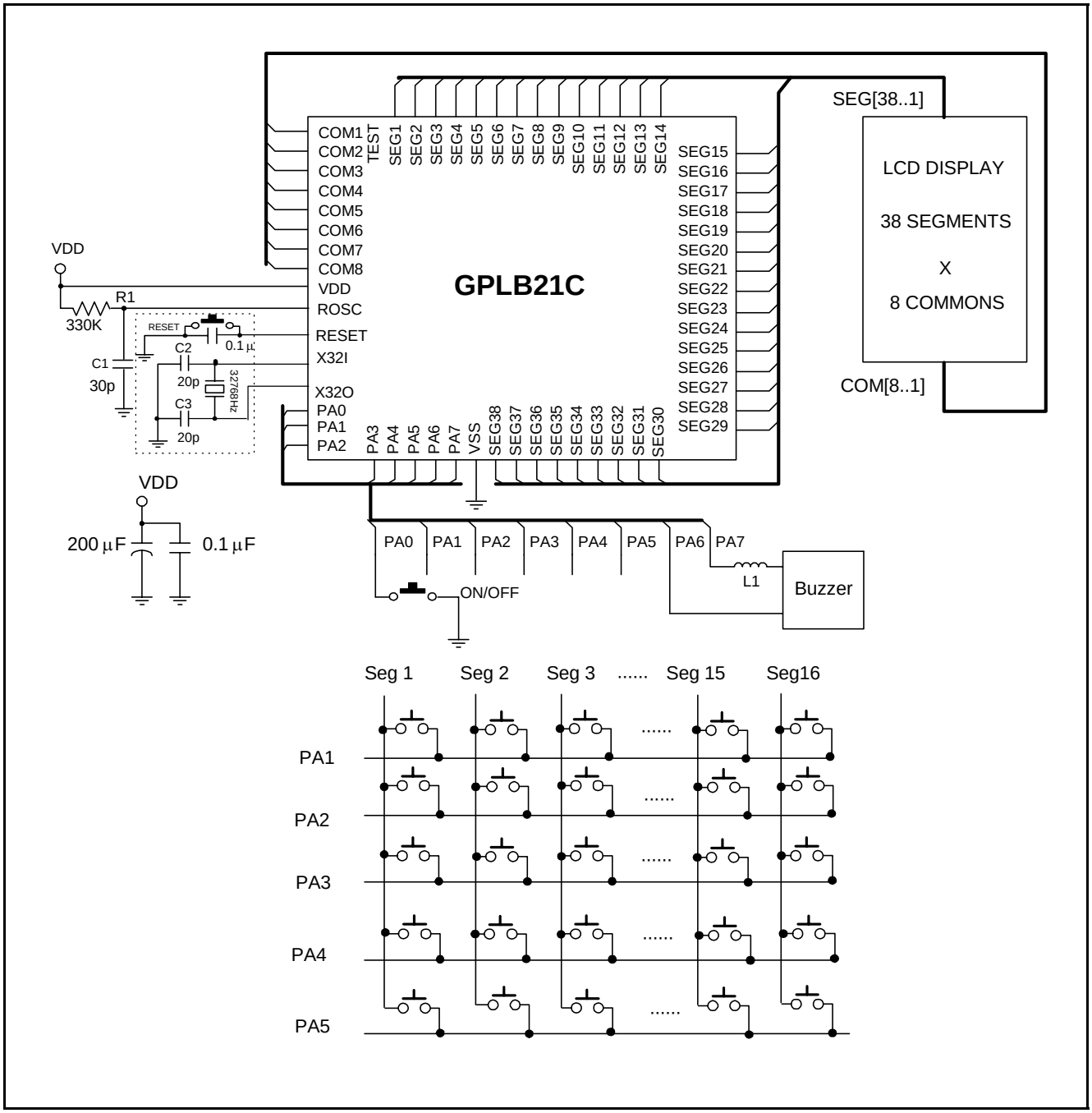


8. APPLICATION CIRCUITS

8.1. Application Circuit - (1)



8.2. Application Circuit - (2)



Note1: In the CRYSTAL mode, the 32768Hz crystal oscillator generates an accurate time base. The Crystal mode requires the installation of a 32768Hz crystal oscillator.

Note2: In the ROSC mode, a suitable time base is generated from the R-Oscillator. A 32768Hz crystal oscillator does not need to be installed.

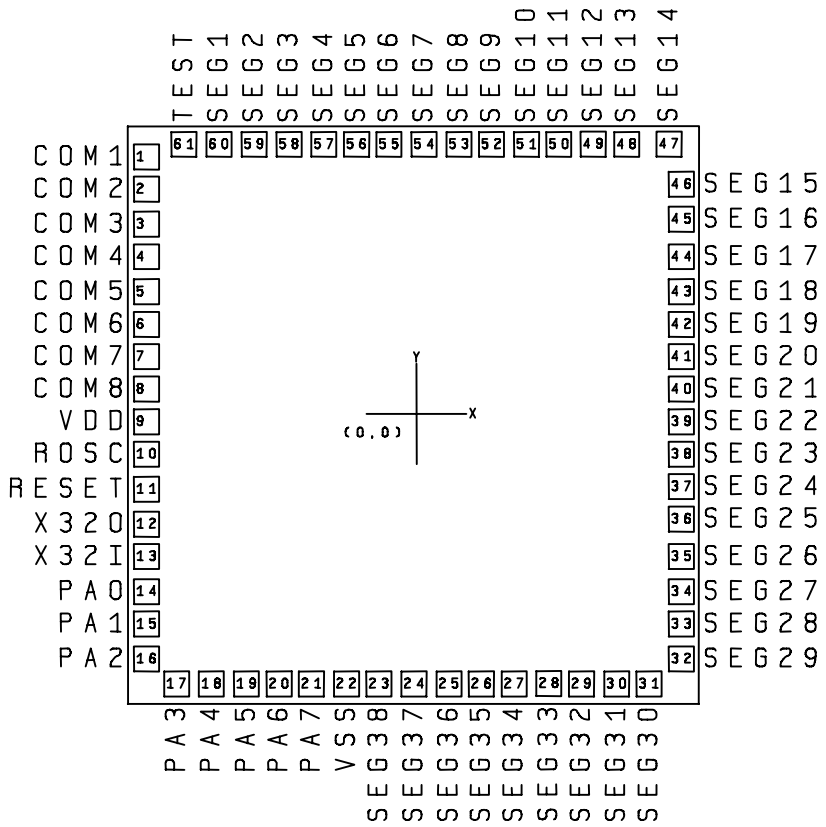
Note3: To avoid noise interference on the PCB around R-Oscillator and crystal circuit, the following installation guidelines are suggested:

1). R1 and C1 should be placed as near as possible to the ROSC pin.

2). C2, C3 and the Crystal should be placed as near as possible to X32I and X32O. A shielding by ground is suggested.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
GPLB21C-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z)..

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	COM1	-1050	989	32	SEG29	1052	-980
2	COM2	-1050	854	33	SEG28	1052	-840
3	COM3	-1050	719	34	SEG27	1052	-700
4	COM4	-1050	584	35	SEG26	1052	-560
5	COM5	-1050	449	36	SEG25	1052	-420
6	COM6	-1050	319	37	SEG24	1052	-285
7	COM7	-1050	189	38	SEG23	1052	-155
8	COM8	-1050	59	39	SEG22	1052	-25
9	VDD	-1050	-71	40	SEG21	1052	105
10	ROSC	-1050	-206	41	SEG20	1052	235
11	RESET	-1050	-341	42	SEG19	1052	365
12	X32O	-1050	-476	43	SEG18	1052	495
13	X32I	-1050	-611	44	SEG17	1052	635
14	PA0	-1050	-746	45	SEG16	1052	775
15	PA1	-1050	-881	46	SEG15	1052	915
16	PA2	-1050	-1016	47	SEG14	1038	1114
17	PA3	-929	-1115	48	SEG13	887	1115
18	PA4	-794	-1115	49	SEG12	747	1115
19	PA5	-659	-1115	50	SEG11	607	1115
20	PA6	-524	-1115	51	SEG10	467	1115
21	PA7	-389	-1115	52	SEG9	327	1115
22	VSS	-254	-1115	53	SEG8	192	1115
23	SEG38	-119	-1115	54	SEG7	57	1115
24	SEG37	16	-1115	55	SEG6	-78	1115
25	SEG36	151	-1115	56	SEG5	-213	1115
26	SEG35	286	-1115	57	SEG4	-348	1115
27	SEG34	421	-1115	58	SEG3	-488	1115
28	SEG33	556	-1115	59	SEG2	-628	1115
29	SEG32	691	-1115	60	SEG1	-768	1115
30	SEG31	826	-1115	61	TEST	-908	1115
31	SEG30	961	-1115				

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 08, 2005	1.0	Original Note: The GPLB21C data sheet v1.0 is a continued version of SPLB21C data sheet v1.2.	11