DATA SHEET

GPFA120C1

128K Music Synthesizer

Jul. 14, 2015

Version 1.0

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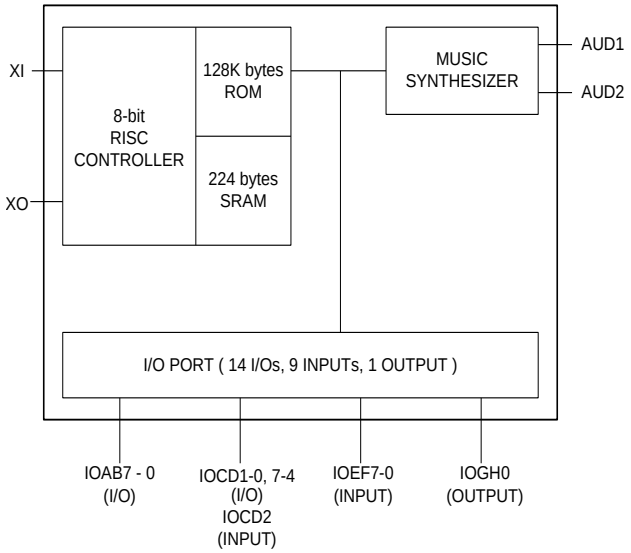
128K MUSIC SYNTHESIZER

1. GENERAL DESCRIPTION

The GPFA120C1, a fully CMOS integrated circuit, adopts the advanced design and processing technology to integrate an 8-bit RISC processor, an 8-channel music synthesizer, 128K bytes program ROM, 224 bytes working SRAM, timer/counter and I/Os interface in a single chip. The sound processing logic is a unique approach to implement high quality melody effect and to simulate all types of musical instruments by programming the tone ROM and controlling the envelope slope to each channel. Each channel can also be defined as a speech channel to generate percussion, animal sound, gunshot, explosion, and many PCM-based special sound effects along with the major music rhythm.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 8 channel speech / melody
- Operating voltage: 2.4V - 5.5V
- 14 general inputs / outputs
- 9 input pins, 1 output pin
- Two audio output pins
- Watchdog mode
- 224 bytes SRAM
- 128K bytes program ROM
- Power down mode
- Stereo function
- Crystal OSC or R_{OSC}, up to 14.318MHz.
- Power ON reset
- Volume control
- Key wakeup capability
- Low voltage reset

4. APPLICATION FIELDS

- Electric piano
- Music clock
- Music box
- Children’s storybook

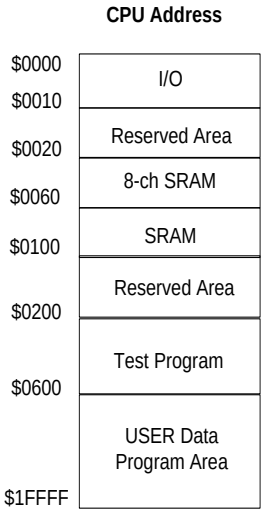
5. PAD ASSIGNMENT AND SIGNAL DESCRIPTION

5.1. Signal Description

Mnemonic	Type	Description
VDD	I	Positive supply voltage
VSS	I	Ground input
XI	I	Crystal oscillator input or R_{OSC} input
XO	O	Crystal oscillator output
$\overline{\text{RESET}}$	I	Reset input, active low, internal pull high
SLEEP	O	Sleep output
TEST	I	Test pin, internal pull low, NC
VM	I	Capacitor input ,should connect it with one 1uF capacitor to AVSS
AUD1 AUD2	O	Audio output
IOCD2 IOEF7 - 0	I	Data input pins
IOAB7 - 0	I/O	Programmable input/output pins
IOCD7 - 6 IOCD5 - 4 IOCD1 - 0	I/O	Programmable input/output pins
IOGH0	O	Programmable output pins
AVSS	I	Analog VSS
AVDD	I	Analog VDD

6. FUNCTION DESCRIPTION

6.1. Memory Mapping

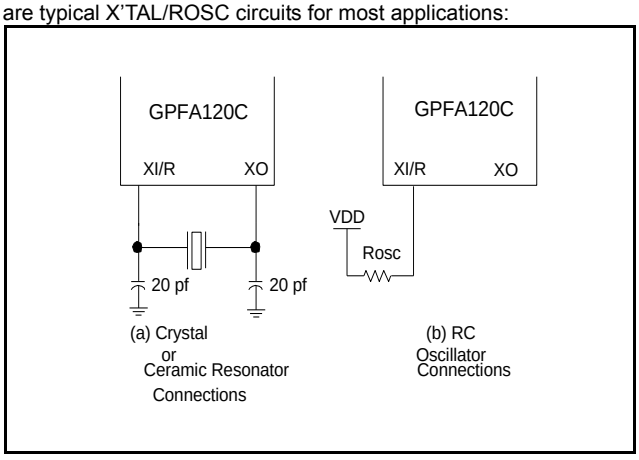


6.2. CPU

The 8-bit micro-processor in GPFA120C1 is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (same as 6502 instruction structure). GPFA120C1 is capable of running up to 7.16MHz depending on specification of the application.

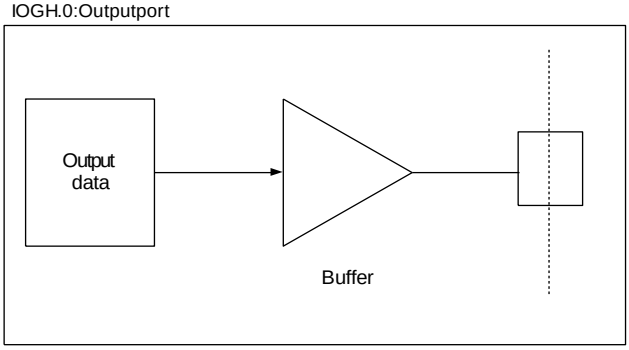
6.3. Oscillator

The GPFA120C1 supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator through mask option. The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:

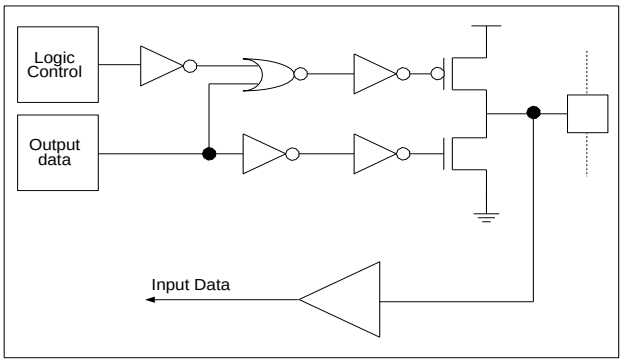


6.4. I/O Port Configuration

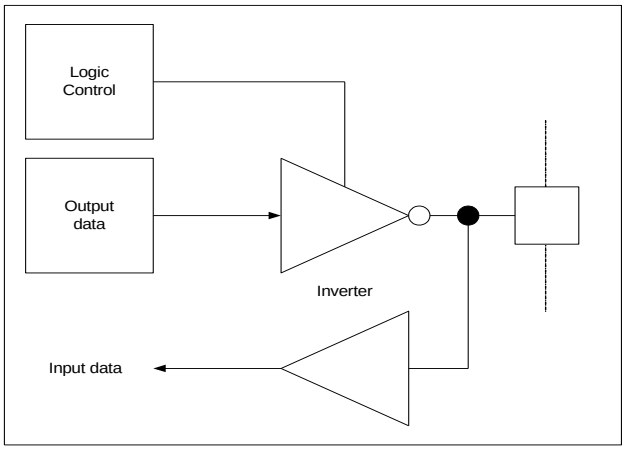
IOGH.0:Outputport



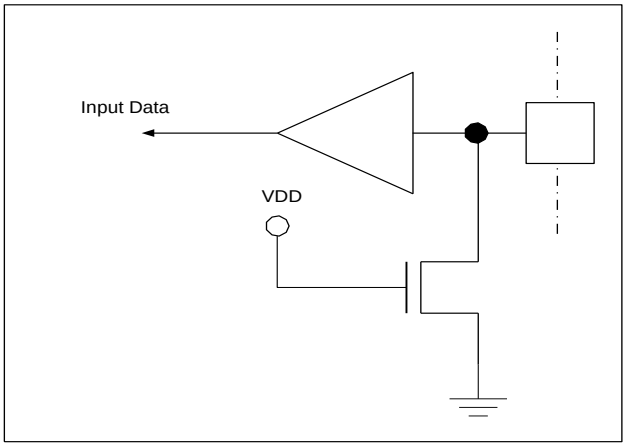
IOCD. 4,5,6,7: Input Output port



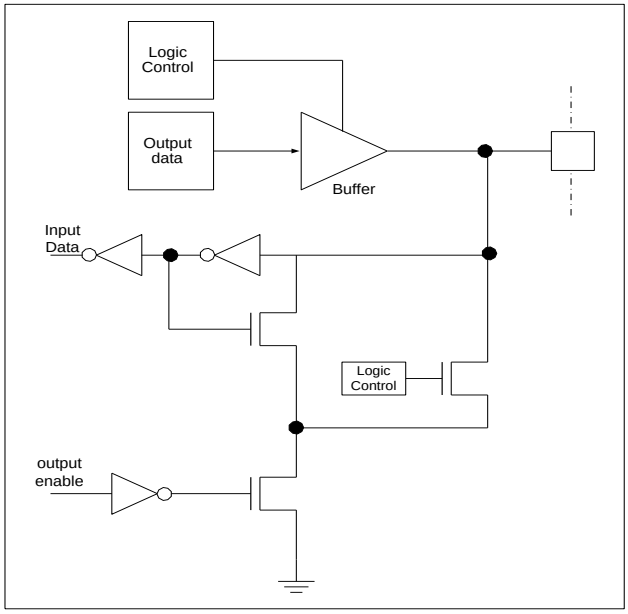
IOCD.0: Input Output Port



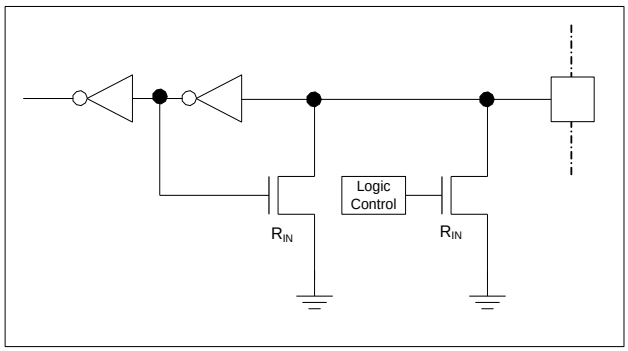
IOCD.2: Input Port



IOAB.0 - 7, IOCD1: Input Output port



IOEF.0-7: Input Port



6.5. Key Wake-up

CPU's wakeup from sleep mode requires a wakeup signal to turn the system clock on. The key wakeup can be used for wakeup sources.

6.6. Interrupt

The GPFA120C1 has two interrupt modes: FIQ (Fast Interrupt Request) and IRQ (Interrupt Request). The priority of FIQ is higher than that of IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt source. The interrupt controller handles 7 INTs sources, which are depicted in the following table.

Interrupt Source	Priority
Channel 3 interrupt	IRQ
Channel 2 interrupt	IRQ
Channel 1 interrupt	IRQ
Channel 0 interrupt	FIQ/IRQ (by program)*
T11 interrupt (system CLK/4096)	IRQ
T8 interrupt (system CLK/512)	IRQ
External interrupt	IRQ

Note: *User can set the priority to be FIQ or IRQ by program.

6.7. Generation of Speech and Melody

The fixed address of RAM area $0020 - $005F is designed as address pointers and a data buffer for the 8-channel speech/melody generation. When a channel is defined as speech, we should set the 16-bit address pointer pointing to the ROM area. The data can be sent directly to DA in direct output mode. The EA register controls the volume of the speech for each AUD output. If the channel is defined as a melody channel, we should set the channel to normal speech mode, fetch the chord and decode the note first. After that, we should set that channel to melody mode that selects the tone ROM for programming and controlling the envelope to choose an instrument. Then play the data to DA buffer in synchronous rhythm with the change of the time base (tempo).

6.8. Stop Clock Mode

GPFA120C1 supports a power saving mode for those applications requiring very low standby current. Simply enable the wakeup sources, and then stop the CPU clock by writing the SLPSTAR register. CPU will enter standby mode, and RAM and I/O retain at their previous states until wakeup again.

6.9. Volume Control Function

A volume control function provides 8-bit volume controller for voltage D/A output control. The volume level can be controlled through software.

6.10. Low Voltage Reset

The GPFA120C1 has a Low Voltage Reset (LVR) function. In general, the CPU system becomes unstable and malfunctions under low voltage condition. With the unique design of Low Voltage Reset in GPFA120C1, it's able to reset all functions into the initial operational (stable) state if the power voltage drops below certain operating voltage.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to VDD + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Ratings table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. DC Characteristics

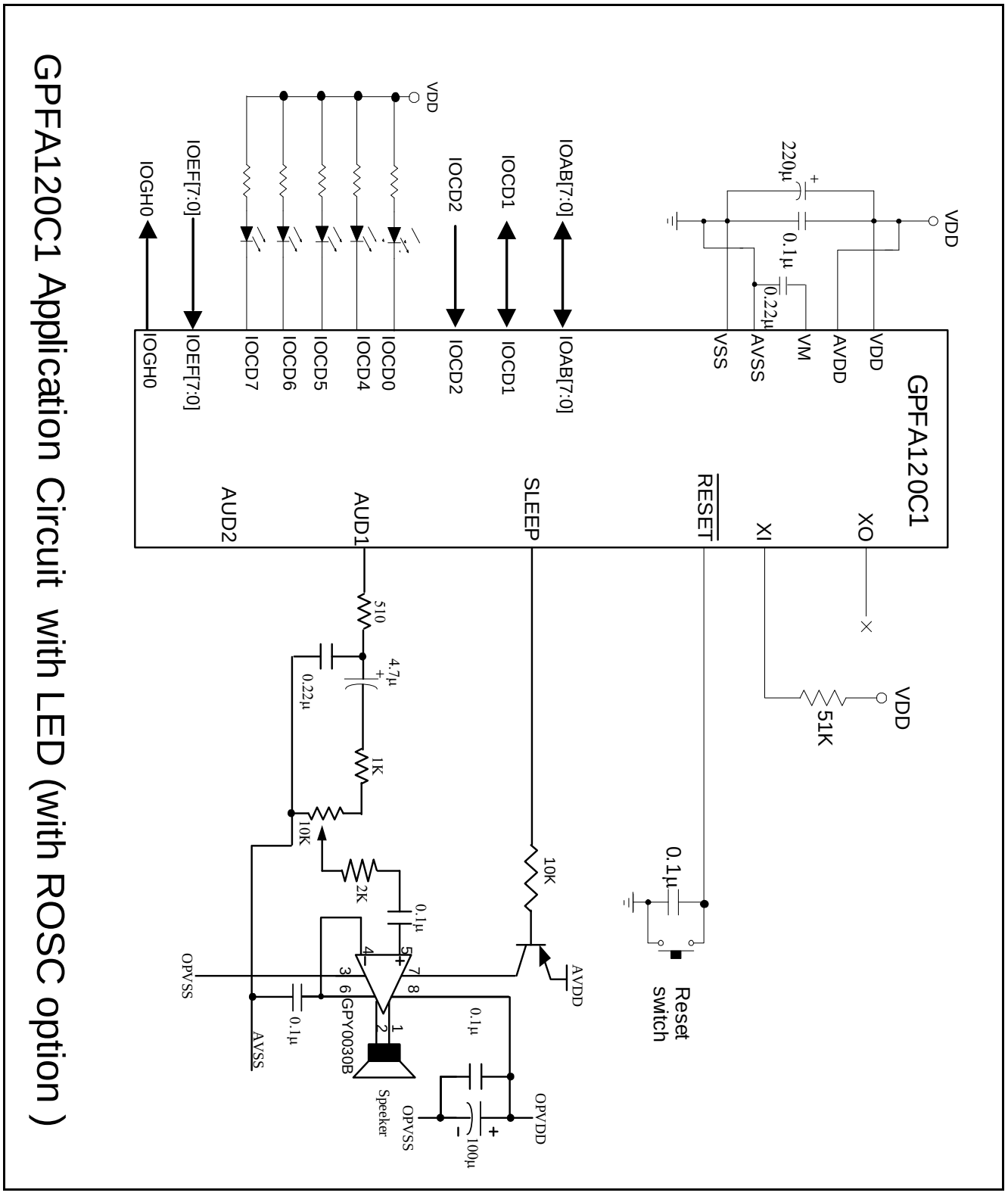
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	8.8	-	mA	F_{CPU} = 7.16MHz @ 5.0V, no load
		-	4.0	-	mA	F_{CPU} = 7.16MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	3.0	μA	VDD = 5.0V
OSC Frequency	F_{OSC2}	-	-	14.318	MHz	VDD = 5.0V
Audio Output Voltage	V_{AUD}	-	-	0.9*VDD	V	-
Input High Level	V_{IH}	0.7VDD	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3VDD	V	-
Output High Current (IOAB[7:0], IOCD[7:4], IOCD[1:0], IOGH0)	I_{OH}	-	-11	-	mA	VDD = 5.0V, V_{OH} = 4.2V
		-	-6	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (IOAB[7:0], IOCD1, IOGH0)	I_{OL}	-	30	-	mA	VDD = 5.0V, V_{OL} = 0.8V
		-	14	-	mA	VDD = 3.0V, V_{OL} = 0.5V
LED Sink Current (IOCD0,IOCD[7:4])	I_{OL}	-	40	-	mA	VDD = 5.0V, V_{OL} = 1.0V
		-	18	-	mA	VDD = 3.0V, V_{OL} = 0.6V
Input Pull-Low Resistor (IOEF[7:0])	R_{PL}	-	120	-	K-Ohm	VDD = 5.0V, VIN = VDD
		-	250	-	K-Ohm	VDD = 3.0V, VIN = VDD
CPU Clock	F_{CPU}	-	-	7.16	MHz	F_{CPU} = F_{OSC2} /2, R_{OSC} = 51KΩ

8. APPLICATION CIRCUITS

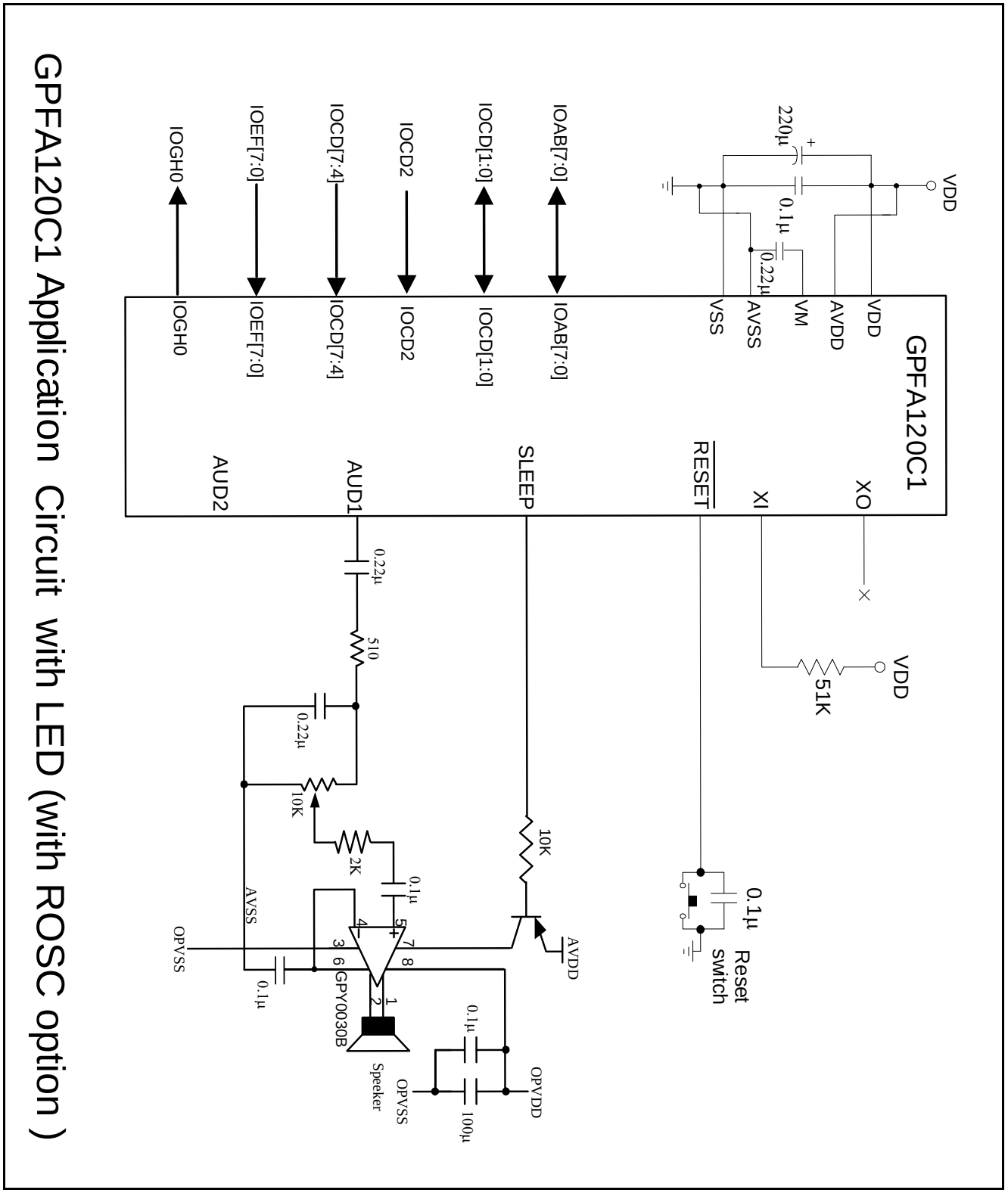
8.1. GPFA120C1 Application Circuits with R_{OSC} Option

8.1.1. Application circuit - (1)

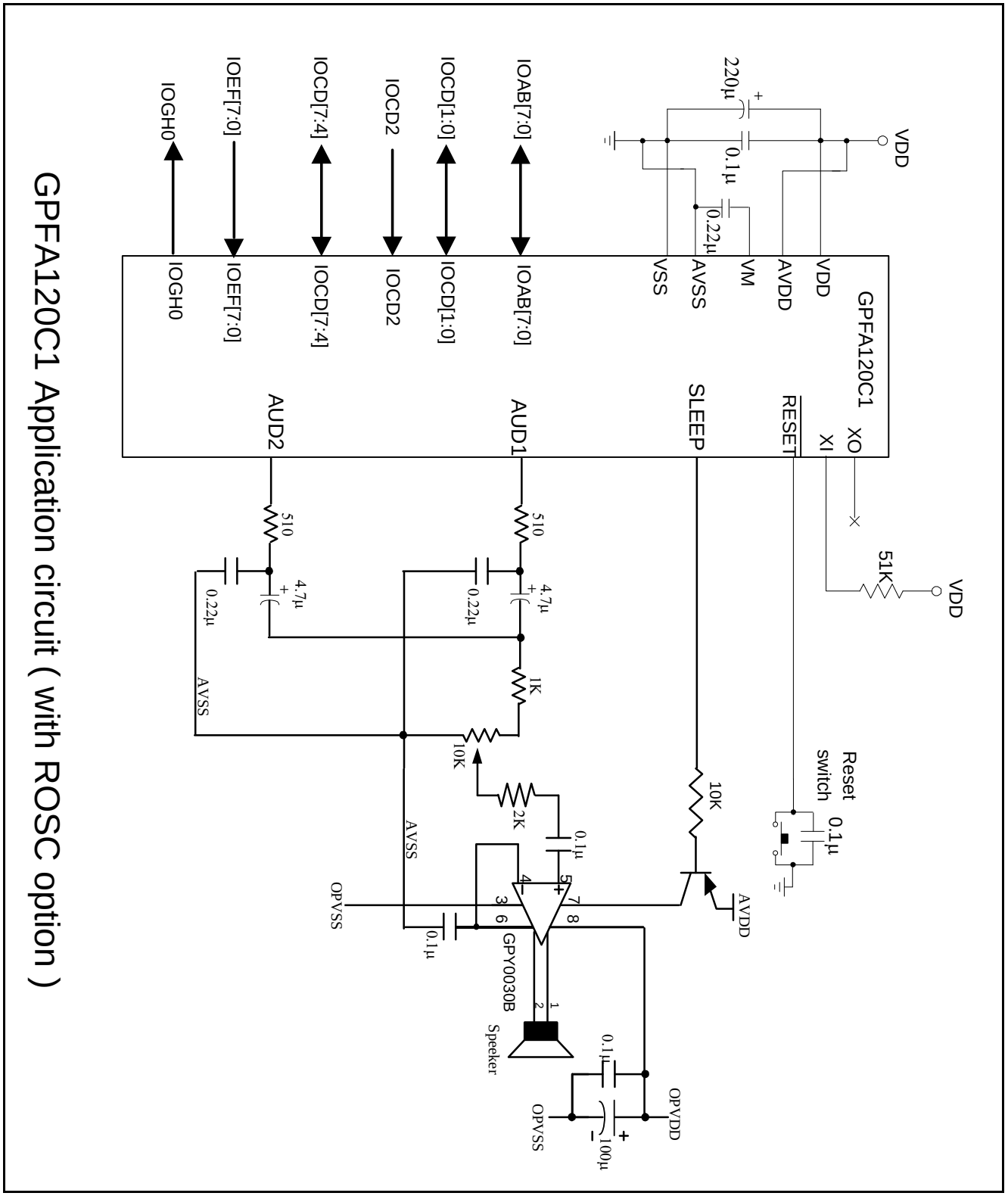
GPFA120C1 Application Circuit with LED (with ROSC option)



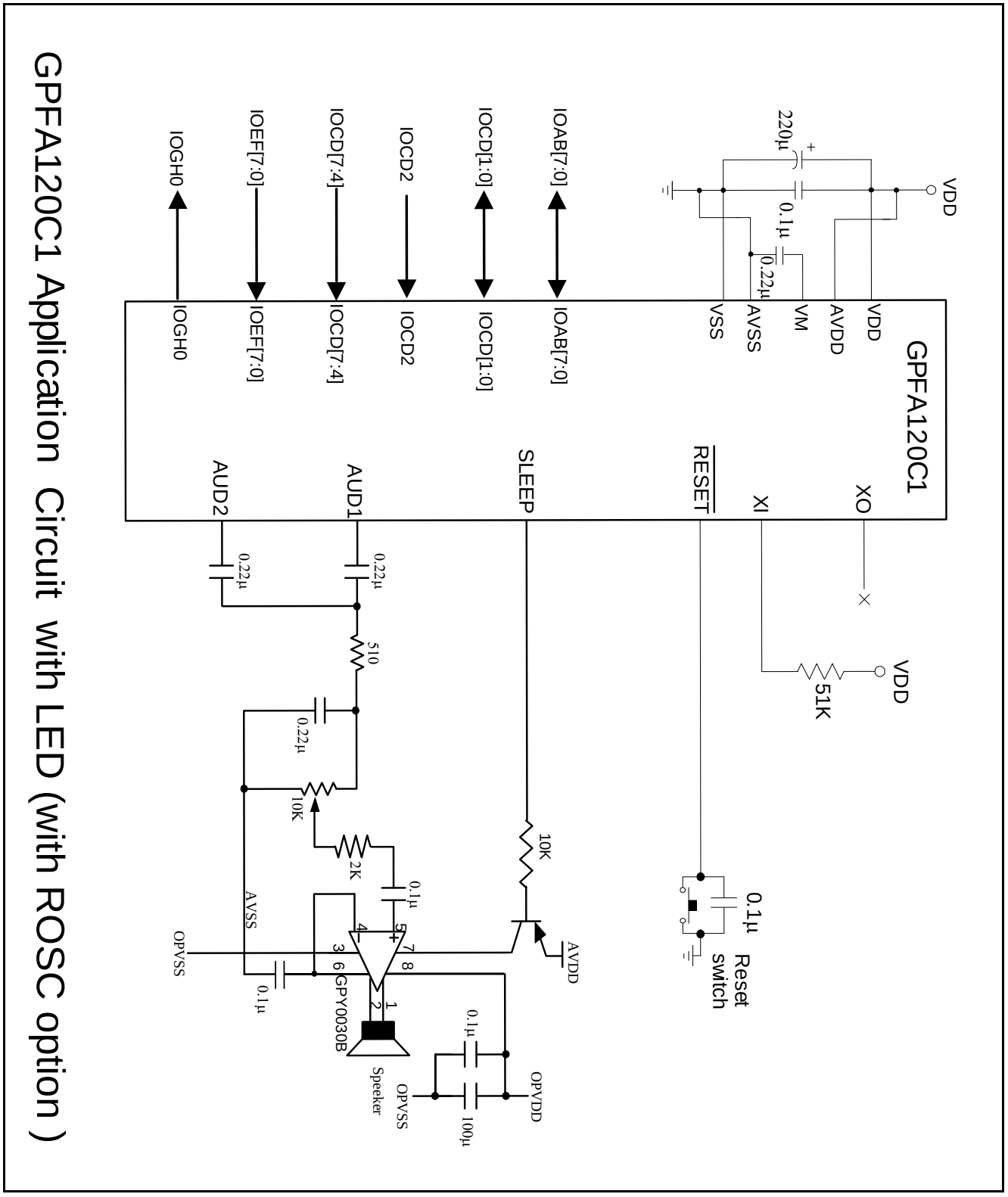
8.1.2. Application circuit - (2)



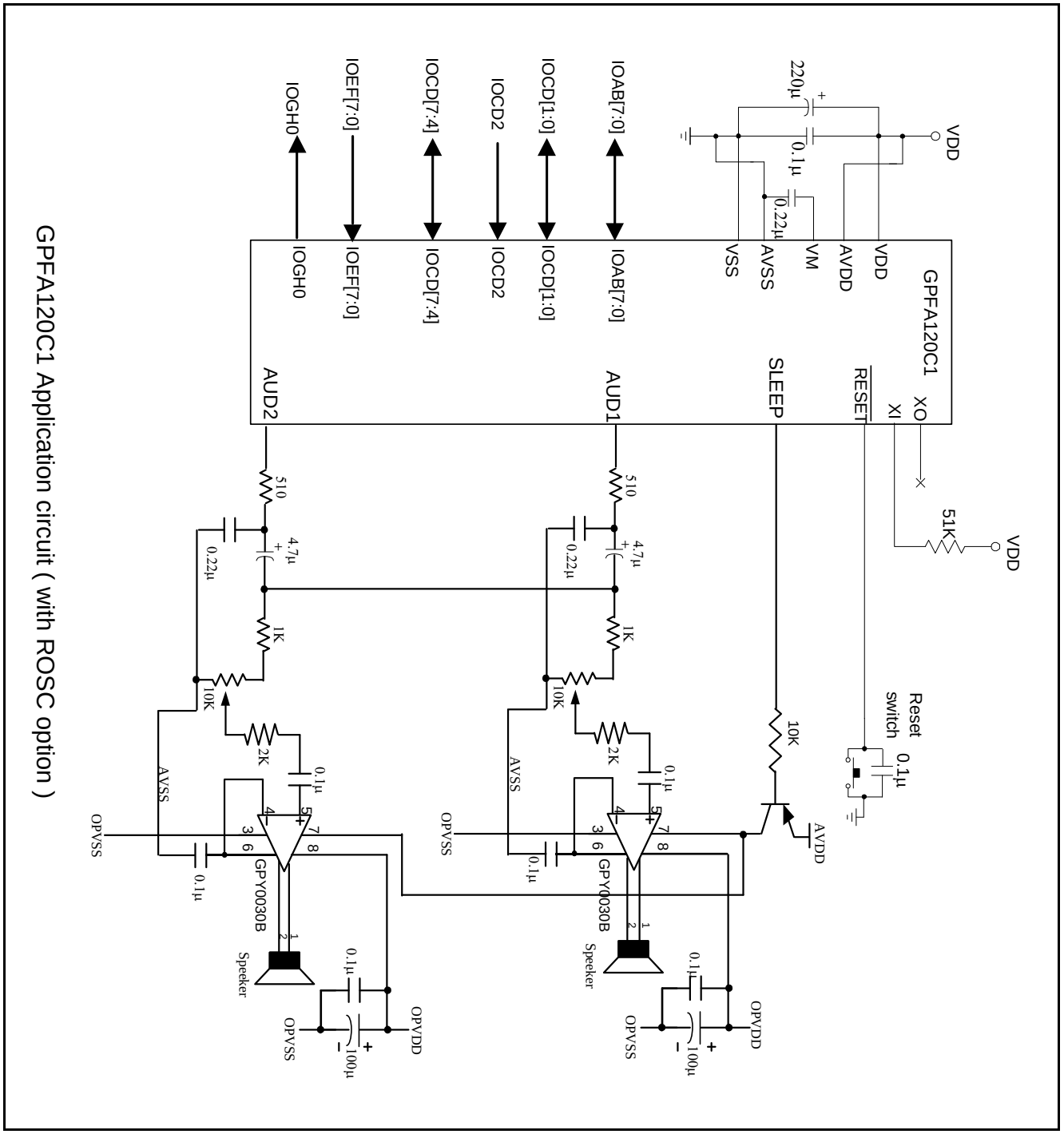
8.1.3. Application circuit - (3)



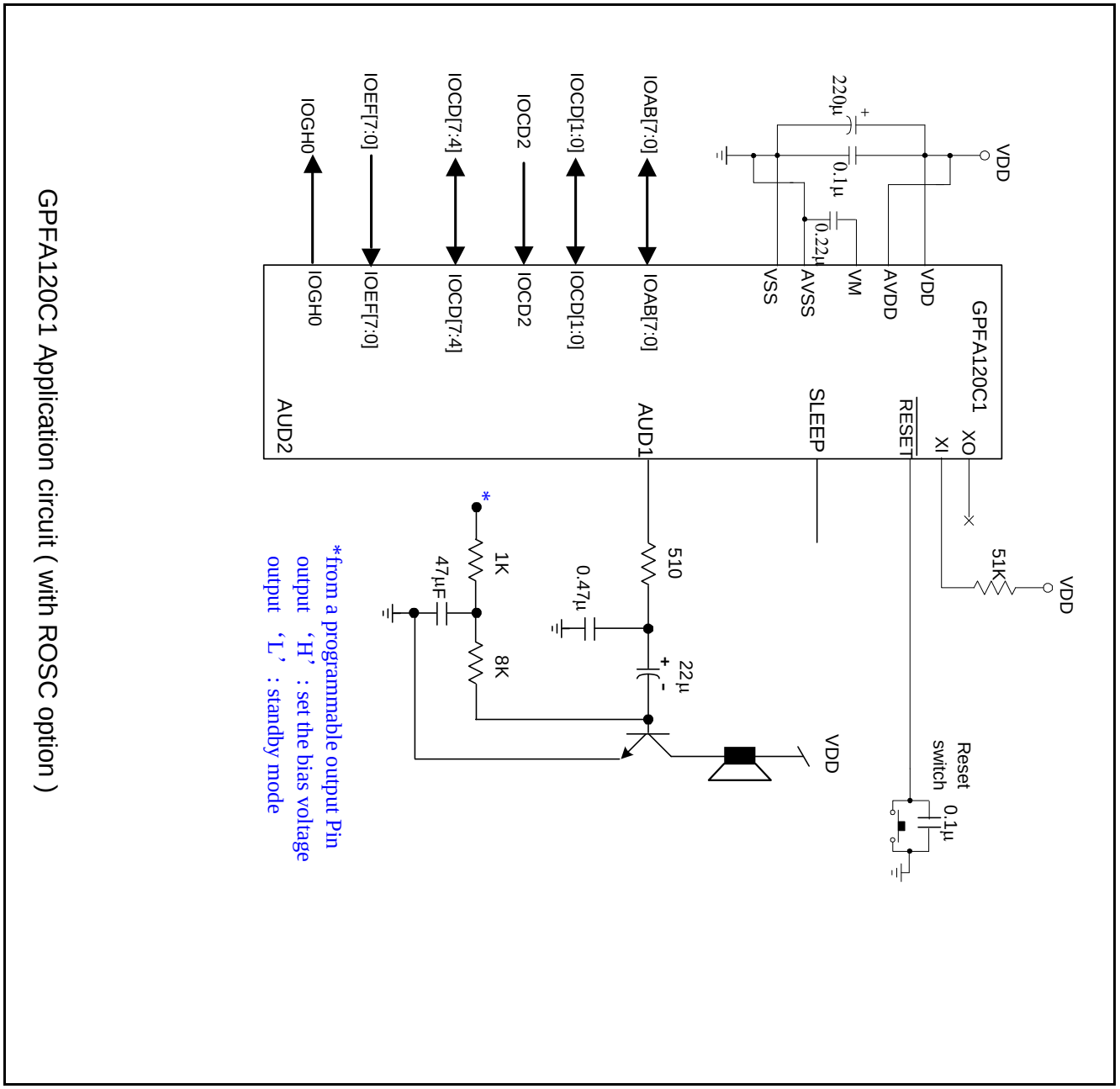
8.1.4. Application circuit - (4)



8.1.5. Application circuit - (5)

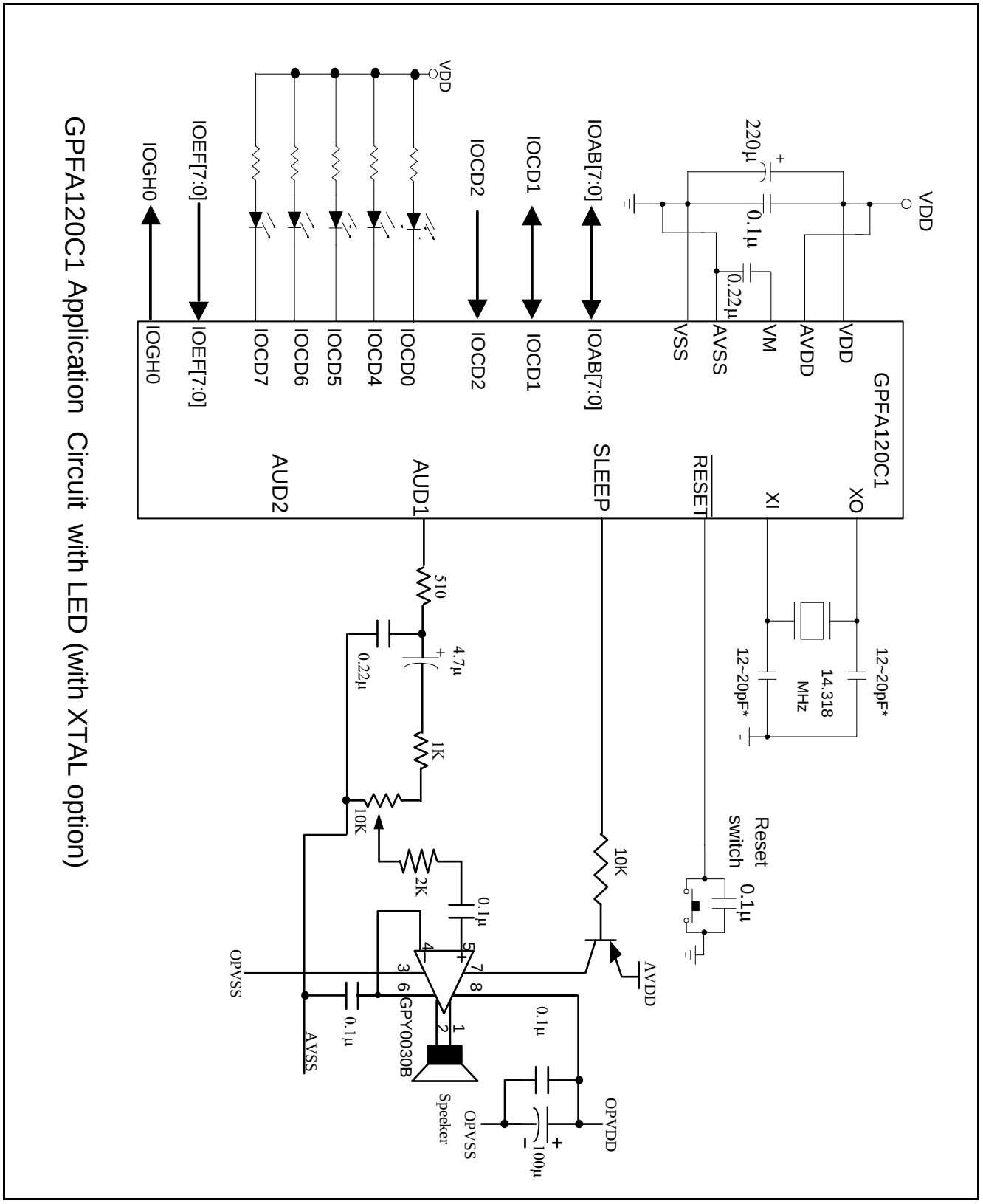


8.1.6. Application circuit - (6)



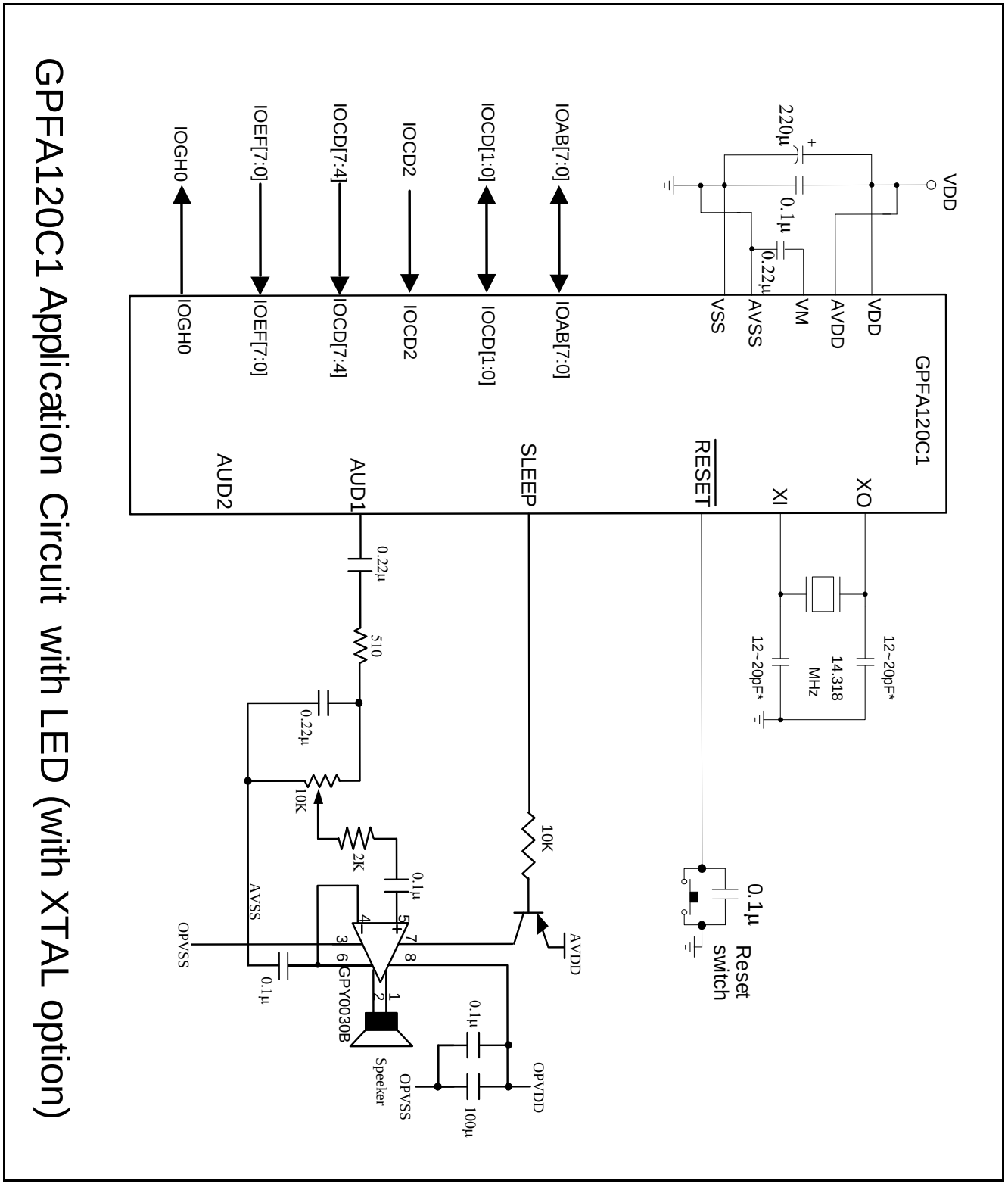
8.2. GPFA120C1 Application Circuits with Crystal Option

8.2.1. Application circuit - (1)



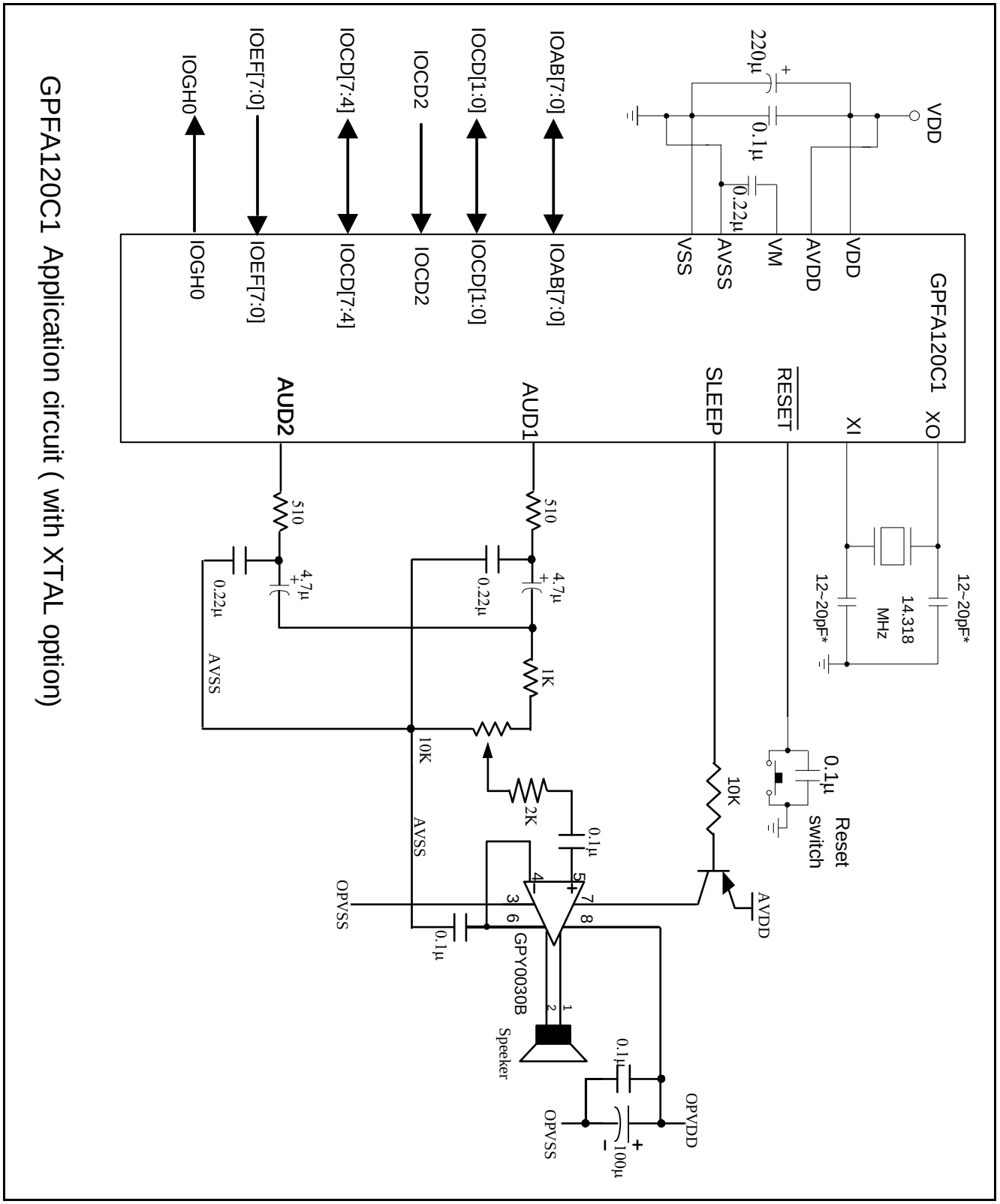
Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.2.2. Application circuit - (2)



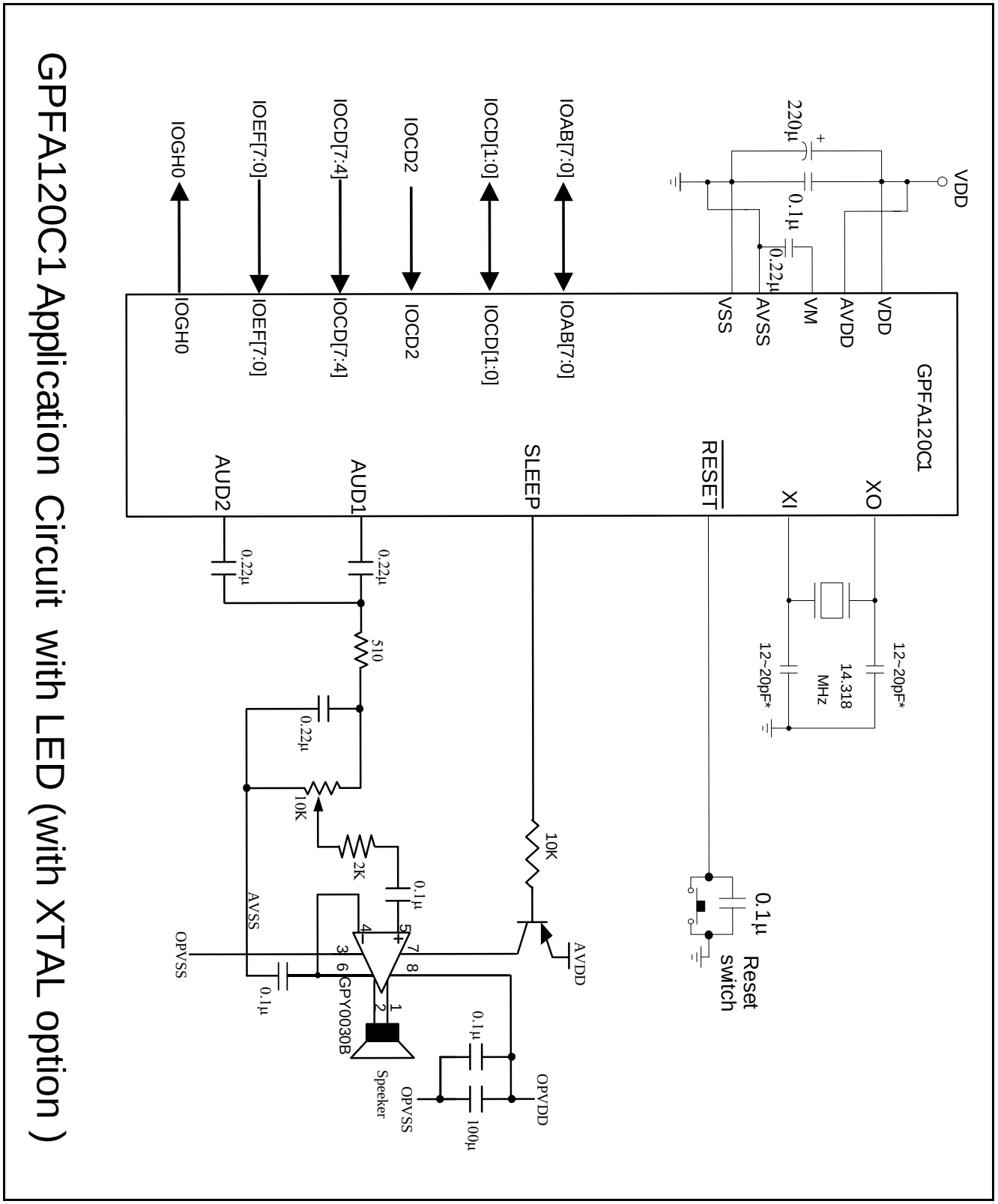
Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.2.3. Application circuit - (3)

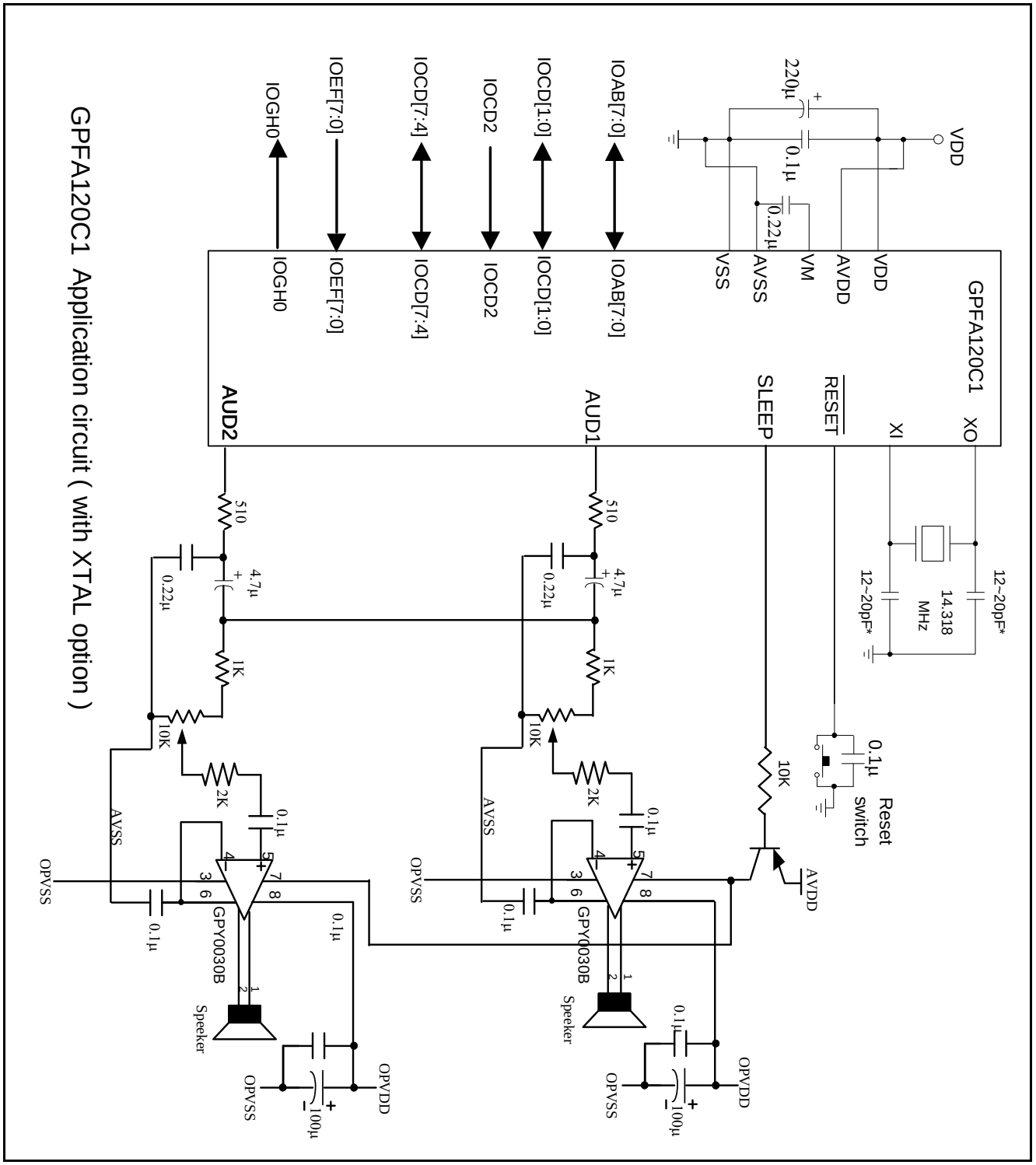


Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.2.4. Application circuit - (4)

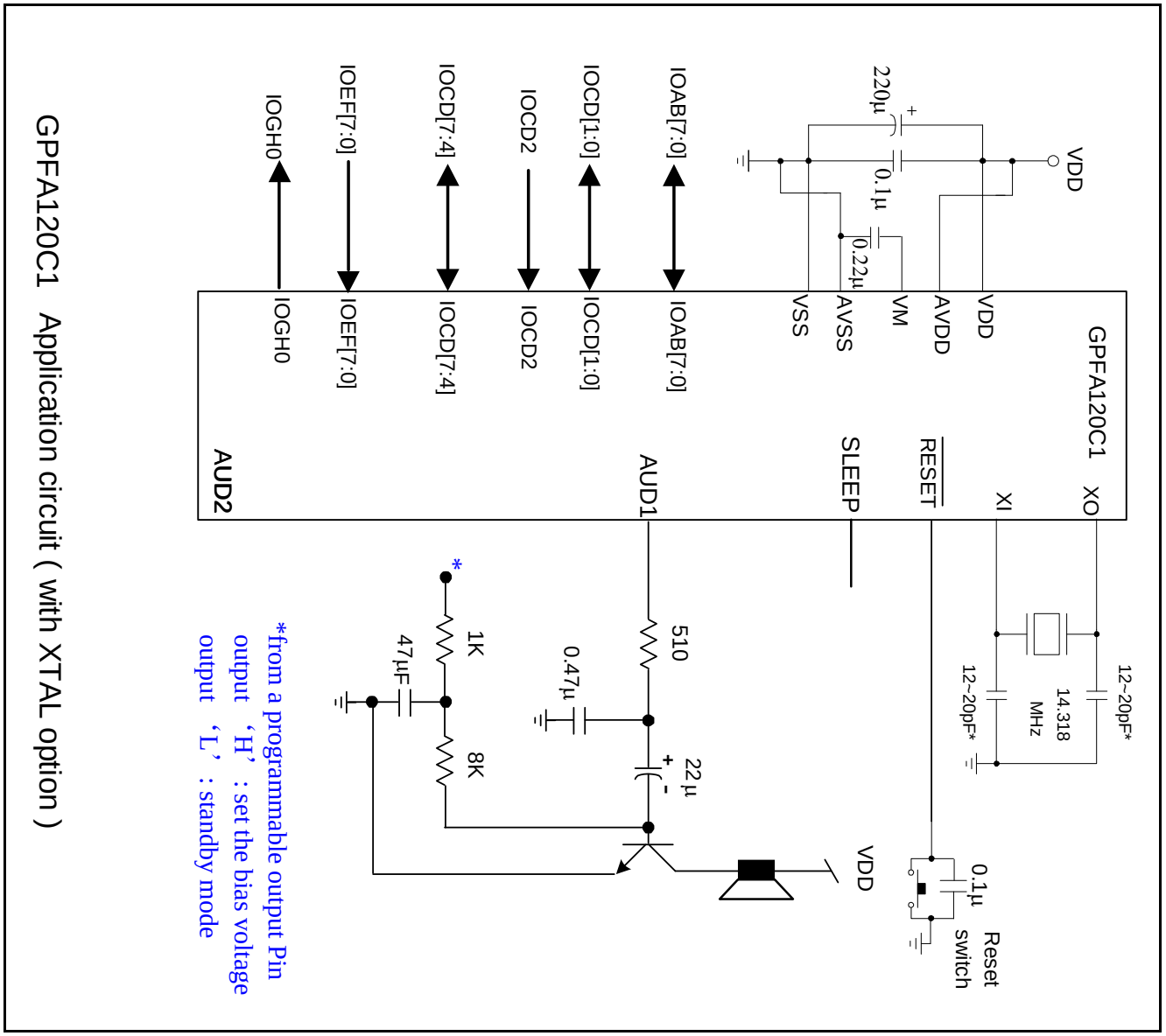


8.2.5. Application circuit - (5)



Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.2.6. Application circuit - (6)



Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPFA120C1-NnnV-A	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

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11. REVISION HISTORY

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