DATA SHEET

GPCE2P064B

16-bit Sound Controller

Apr. 07, 2015

Version 1.2

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16-BIT SOUND CONTROLLER

1 GENERAL DESCRIPTION

GPCE2P064B, a 16-bit architecture sound controller, features the newest 16-bit microprocessor, *μ'nSP*™ (pronounced as *micro-n-SP*). This high processing speed assures the *μ'nSP*™ is capable of handling complex digital signal processes easily and rapidly. Therefore, the GPCE2P064B is applicable to the areas of digital sound process and voice recognition. The operating voltage of 2.4V through 5.5V and speed of 0.16MHz through 49.152MHz yield the GPCE2P064B to be easily used in varieties of applications. The memory capacity includes a 32K-word OTP ROM plus a 2K-word working SRAM. Other features include 20 programmable multi-functional I/Os, three 16-bit timers/counters, 32KHz clock, Low Voltage Reset/Detection, four channels 12-bit ADC (one channel built-in MIC amplifier with auto gain controller), one 14-bit DAC with push-pull amplifier and many others.

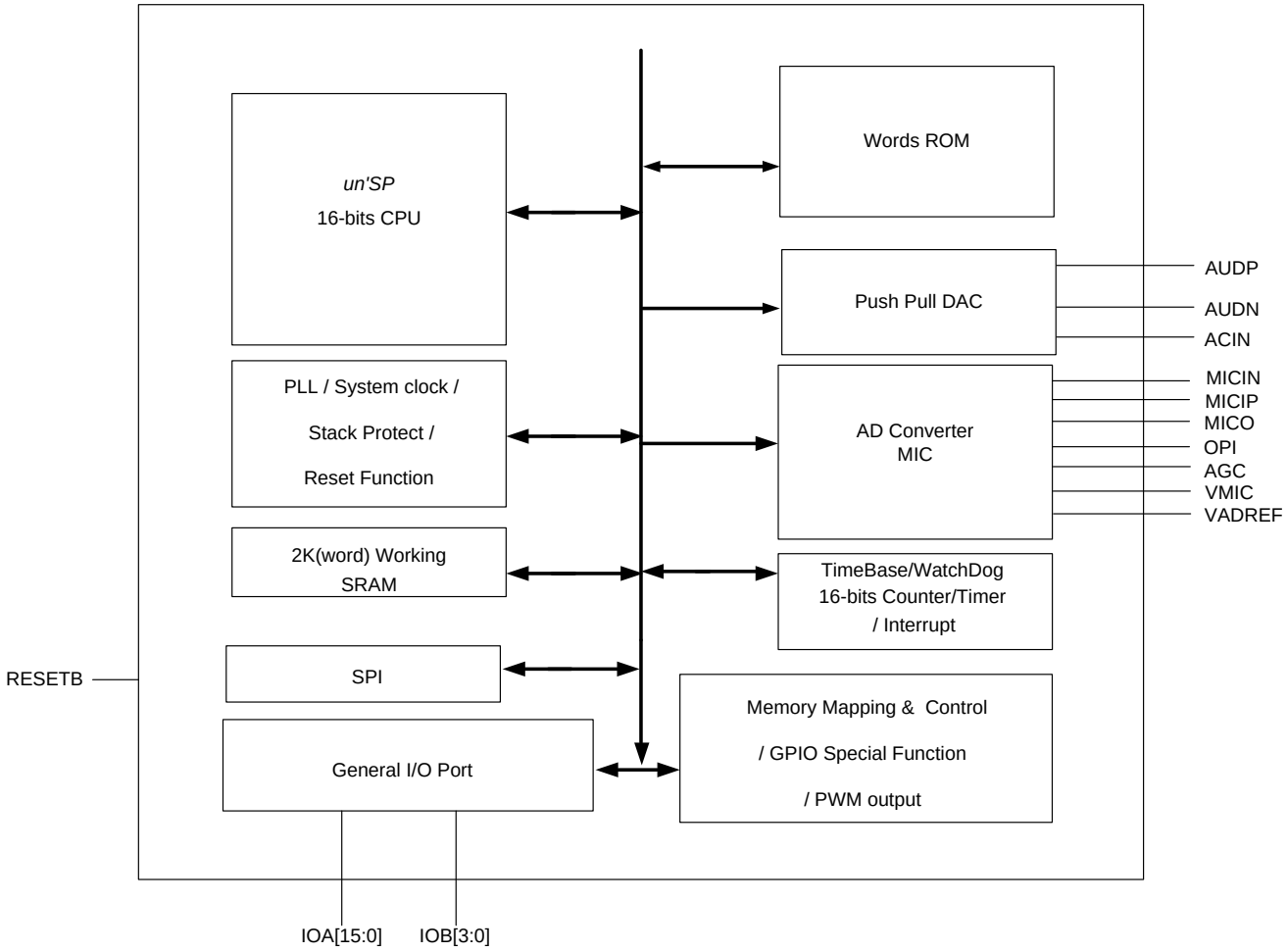
2 FEATURES

- 16-bit *μ'nSP*™ microprocessor
- CPU Clock: 0.16MHz - 49.152MHz
- Operating Voltage: 2.4V - 5.5V
- Power regulator built-in with input voltage: 2.4~5.5V, output voltage: 2.4~3.0V
- IO PortA & B Operating Voltage: 2.4V - 5.5V
- 32K-word fast speed OTP ROM
- 2K-word working SRAM
- Software-based audio processing
- Two sets of 14-bit software channel with noise filter, mixer and scalar to play high quality sound
- Standby mode for power saving
- Three 16-bit timers/counters
- One 14-bit DAC with push-pull amplifier. Supports cascade mode
- 20 general I/Os (bit programmable)
- Key wakeup function (IOA0 - 15)
- PLL feature for system clock
- 32kHz internal resistor oscillator selected.
- Four channels 12-bit AD converter
- ADC
- Built-in microphone amplifier and AGC or PGA function selected
- Low voltage reset and low voltage detection
- Watchdog Enable (option)
- One SPI serial interface I/O

3 APPLICATION FIELD

- Voice Recognition Products
- Intelligent Interactive Talking Toys
- Advanced Educational Toys
- Kids Learning Products
- Kids Storybook
- General Speech Synthesizer
- Long Duration Audio Products
- Recording / Playback Products

4 BLOCK DIAGRAM



5 SIGNAL DESCRIPTIONS

5.1 Signal Pin

5.1.1 All Pins and LQFP64 pin descriptions

Mnemonic	PIN No. (LQFP64)	Type	Description
PORT A, Port B			
IOA[15:0]	37-30,27-20	I/O	IOA[15:0]: bi-directional I/O ports It can be programmed as wakeup I/O pins
IOB [3:0]	18-15	I/O	IOB [3:0]: bi-directional I/O ports Under OTP ROM programming mode, IOB2→SCK, IOB3→SDA.
Power & GND			
VDD_IOA	29	P	Power VDD for Port A
VSS_IO	28	G	Power GND for IO Port
VDD_IOB	19	P	Power VDD for Port B
V3_ADC	7	P	Power VDD for AD
VSS_ADC	6	G	Power GND for AD
V3_REGO	63	P	3V power output from regulator
VDD_REG	62	P	Positive supply for regulator(2.4V~5.5V)
VSS_REG	64	G	Ground reference for regulator
VDD_DAC	54	P	Positive 5V supply for push-pull DAC
VDD_PDAC	50	P	Positive 5V supply for push-pull DAC post driver
VSS_DAC	53	I	Ground reference for push-pull DAC
VSS_ PDAC	48,52	I	Ground reference for push-pull DAC post driver
OPTION			
TEST	5	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
VPP	1	I	High voltage during OTP programming. NC at the normal run.
EPM	2	I	Program control input. Connect to VDDIN during OTP programming. NC at normal run
DAC			
AUDP	49	O	Audio output of push pull DAC
AUDN	51	O	Audio output of push pull DAC
ACIN	55	U	Audio analog mixer in
ADC			
MICP	14	I	MIC amplifier input positive (Internal Floating)
MICN	13	I	MIC amplifier input negative (refer to application circuit)
MICOUT	12	O	MIC amplifier output (refer to application circuit)
OPI	11	I	Audio amplifier negative input (refer to application circuit)
AGC	10	IO	AGC by pass filter (refer to application circuit)
VMIC	8	O	Microphone power supply
VADREF	9	O	AVREF_DA reference pin
PLL			
VCOIN	3	I	PLL low pass filter input
Other Signal			
RESETB	4	I	System reset pin (active low)

5.1.2 SOP24 (HS101) pin descriptions

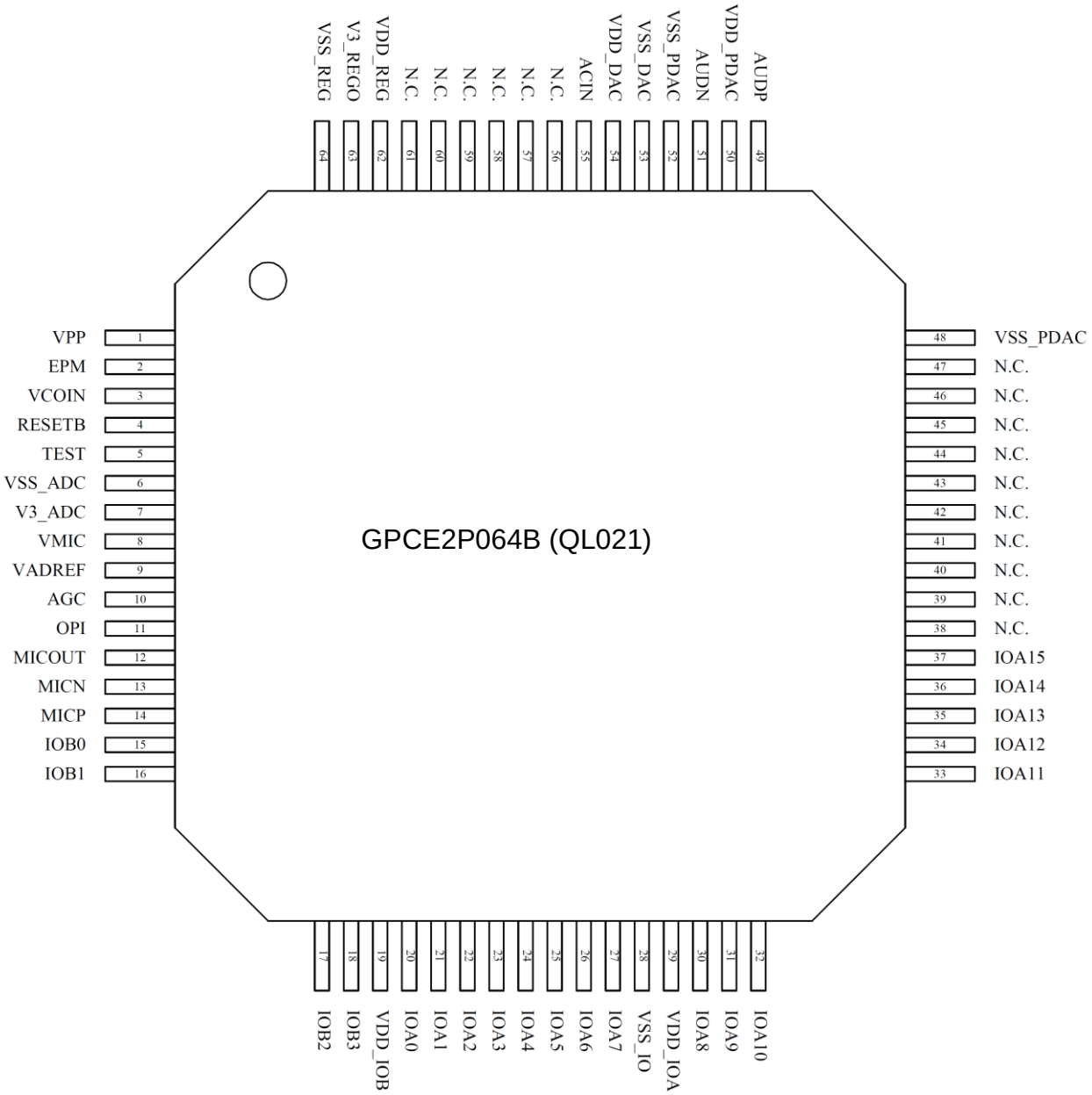
Mnemonic	PIN No. (HS101)	Type	Description
PORT A, Port B			
IOA[0] IOA[12] IOA[13] IOA[14] IOA[15]	14 15 16 17 18	I/O	IOA : bi-directional I/O ports It can be programmed as wakeup I/O pins
IOB [2] IOB [3]	11 12	I/O	IOB : bi-directional I/O ports Under OTP ROM programming mode, IOB2→SCK, IOB3→SDA.
Power & GND			
VDD_IOA	19	P	Power VDD for Port A
VDD_IOB	13	P	Power VDD for Port B
V3_ADC	9	P	Power VDD for AD
VSS_ADC	8	G	Power GND for AD
V3_REGO	1	P	3V power output from regulator
VDD_REG	24	P	Positive supply for regulator(2.4V~5.5V)
VSS_REG	2	G	Ground reference for regulator
VDD_PDAC	22	P	Positive 5V supply for push-pull DAC post driver
VSS_ PDAC	20	I	Ground reference for push-pull DAC post driver
OPTION			
TEST	7	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
VPP	3	I	High voltage during OTP programming. NC at the normal run.
EPM	4	I	Program control input. Connect to VDDIN during OTP programming. NC at normal run
DAC			
AUDP	21	O	Audio output of push pull DAC
AUDN	23	O	Audio output of push pull DAC
ADC			
VADREF	10	O	AVREF_DA reference pin
PLL			
VCOIN	5	I	PLL low pass filter input
Other Signal			
RESETB	6	I	System reset pin (active low)

5.1.3 SOP24 (HS102) pin descriptions

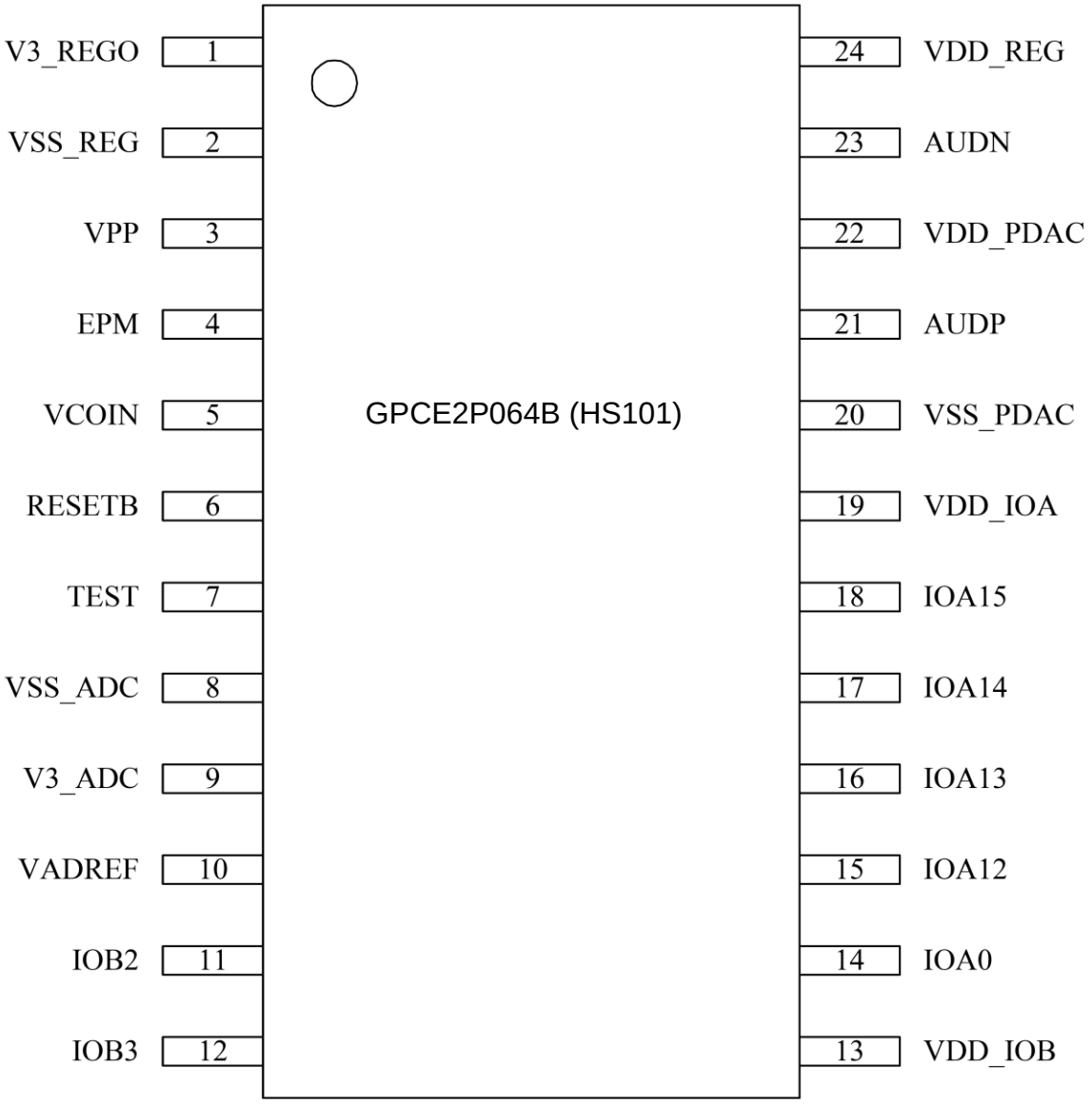
Mnemonic	PIN No. (HS102)	Type	Description
PORT A, Port B			
IOA[0]	14	I/O	IOA : bi-directional I/O ports It can be programmed as wakeup I/O pins
IOA[1]	15		
IOA[12]	16		
IOA[14]	17		
IOA[15]	18		
IOA[13]	19		
IOA[8]	20		
IOA[7]	22		
IOA[6]	23		
IOA[3]	24		
IOB[0]	9	I/O	IOB : bi-directional I/O ports Under OTP ROM programming mode, IOB2→SCK, IOB3→SDA.
IOB[1]	10		
IOB[2]	11		
IOB[3]	12		
Power & GND			
VDD_IOA	21	P	Power VDD for Port A
VDD_IOB	13	P	Power VDD for Port B
V3_REGO	3	P	3V power output from regulator
VDD_REG	4	P	Positive supply for regulator(2.4V~5.5V)
VSS_REG	5	G	Ground reference for regulator
OPTION			
TEST	8	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
VPP	2	I	High voltage during OTP programming. NC at the normal run.
EPM	1	I	Program control input. Connect to VDDIN during OTP programming. NC at normal run
PLL			
VCOIN	6	I	PLL low pass filter input
Other Signal			
RESETB	7	I	System reset pin (active low)

5.2 PIN Map

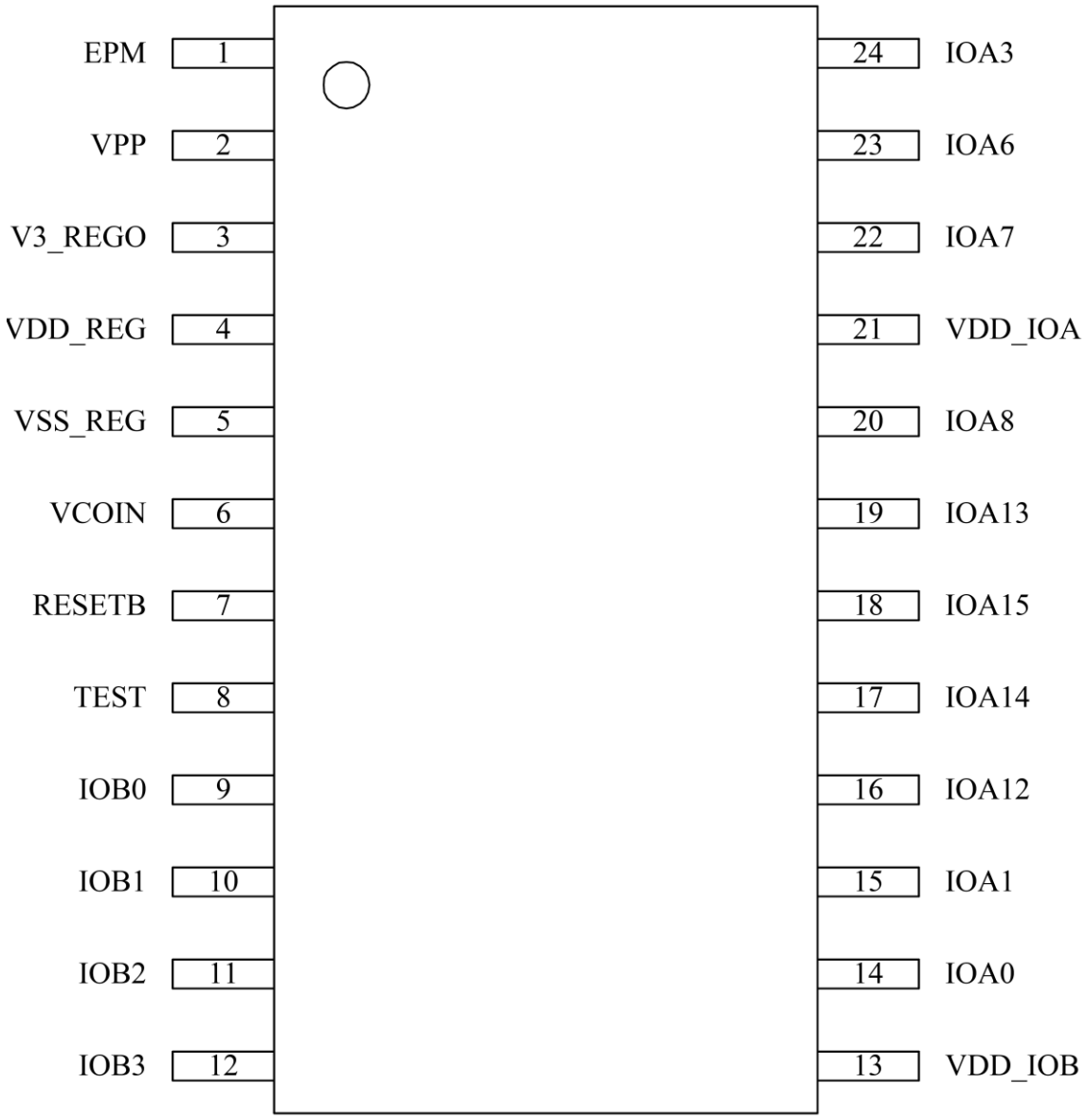
5.2.1 LQFP64



5.2.2 SOP24 (HS101)



5.2.3 SOP24 (HS102)



6 FUNCTION DESCRIPTIONS

6.1 CPU

The GPCE2P064B is equipped with a 16-bit μ'nSP™, the newest 16-bit microprocessor (pronounced as micro-n-SP). Eight registers are involved in μ'nSP™: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK.

6.2 Memory

6.2.1 SRAM

The amount of SRAM is 2K-word (including Stack), ranged from $0000 through $07FF with access speed of two CPU clock cycles.

6.2.2 OTP ROM

GPCE2P064B features a 32K-word high-speed OTP ROM.

6.3 PLL, Clock, Power Mode

6.3.1 PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (32kHz) and to pump the frequency from 20.48MHz to 49.152MHz for system clock (F_{OSC}). The default PLL frequency is 24.576MHz.

6.3.1.1 System clock

Basically, the system clock is provided by PLL and programmed by the Port_SystemClock (R/W) to determine the clock frequency for system. The default system clock F_{OSC} = 24.576MHz and CPU clock is F_{OSC}/8 if not specified. The initial CPU clock is Fosc/8 after system wakes up and adjusts to desired CPU clock via programming the Port_SystemClock (R/W). This avoids ROM reading failure when system awakes.

6.3.1.2 32KHz clock

The 32KHz clock is normally used in watch, clock or other time related products. A 2Hz (0.5 seconds) function is loaded in GPCE2P064B. It counts the time as well as to wake CPU up whenever 2Hz occurs. Since the clock is generated each 0.5 seconds, time can be traced by the number of 32KHz occurrences. In addition, GPCE2P064B supports 32KHz internal resistor oscillator in normal mode and auto-power-saving mode.

6.4 Standby Mode

The GPCE2P064B features a power savings mode (or called standby mode) for low power applications. To enter standby mode, the desired key wakeup port (IOA[15:0]) must be configured to input first. And read the Port_IOA_Data to latch the IOA state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing $5555 into Port_System_Sleep(W) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states until CPU being awakened. The wakeup sources in GPCE2P064B include KEY wakeup (IOA[15:0]), 32KHz wakeup, FIQ and IRQ0 - IRQ7. After GPCE2P064B is awakened, CPU will continue to execute the program from where it slept. Programmer can also enable or disable the 32kHz when CPU is in standby mode.

6.5 Low Voltage Detection and Low Voltage Reset

6.5.1 Low voltage detection (LVD)

The Low Voltage Detection (LVD) reports the circumstance of present voltage. There are four LVD levels to be selected: 2.6V, 2.8V, 3.0V and 3.2V. Those levels can be programmed via P_LVD_Ctrl. As an example here, suppose LVD is given 2.8V. When the voltage drops below 2.8V, the b12 of P_LVD_Ctrl is read as HIGH. In such state, program can be designed to response this condition.

6.5.2 Low voltage reset

In addition to the LVD, the GPCE2P064B has another important function, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR level. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below LVR level. The LVR will reset all functions to the initial operational (stable) states when the voltage drops below LVR level.

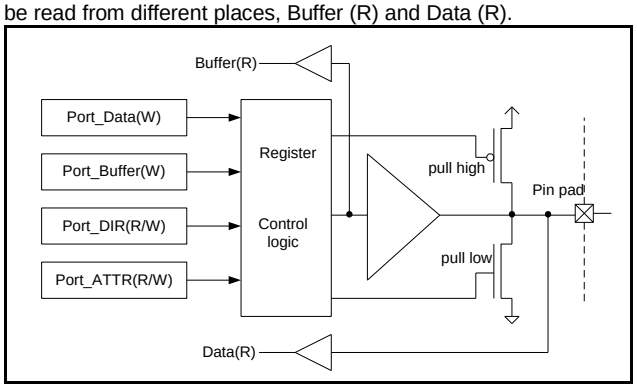
6.6 Interrupt

The GPCE2P064B has 13 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is a high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

6.7 I/O

Two I/O ports are built in GPCE2P064B - PortA and PortB, total has 20 bit-programmable I/Os. The PortA is a general purpose I/O with programmable wakeup capability, i.e. IOA [15:0] is the

key wakeup port. To activate key wakeup function, latch data on Port_IOA_Data and enable the key wakeup function. Wakeup is triggered when the PortA state is different from at the time latched. Furthermore, the I/O ports can be operated at 5V level, higher than the CPU core which is a 3V level system. Suppose system operating voltage is running at 3.3V, VDDIO (power for I/O) operates from 3.3V to 5.5V. In such condition, the I/O pad is capable of operating from 0V through VDDIO. The following diagram is an I/O schematic. Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R).



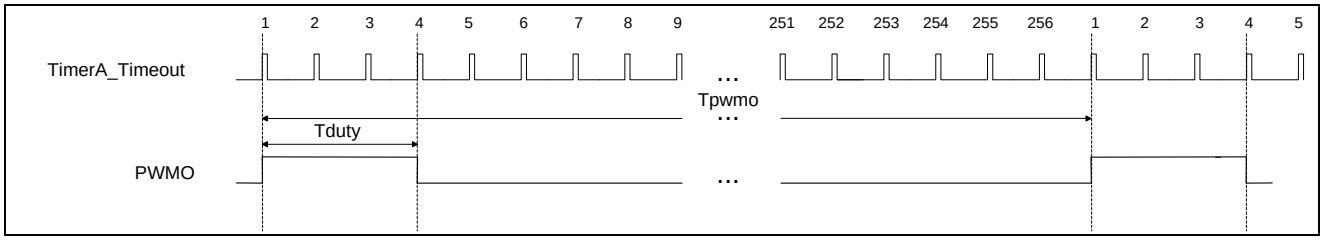
In addition to a general purpose I/O port function, PortA/B also shares/carries some special functions.

6.8 Timer / Counter

GPCE2P064B provides three 16-bit timers/counters - TimerA, TimerB and TimerC or so called universal counters. The clock source of Timer A/B/C are from clock source Input 1 and clock source Input 2 (see below table) which perform AND operation to form the varieties of combinations. When timer overflows, a timeout signal (TAOUT) is sent to CPU interrupt module to generate a timer interrupt signal. In addition, Timer A/B/C hardware interrupt events can be used to latch the DAC audio output and trigger ADC conversion.

6.9 IO PWM

One IO PWMs which duty is selected from 1/256 to 254/256. Example the below figure is a 3/256-duration cycle. The PWMO waveform is made by selecting a pulse width through Port_PWM_Ctrl. As a result, each 256 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.



6.10 Timebase

Timebase, generated by 32kHz crystal oscillator, is a combination of frequency selection. Furthermore, timebase generates 4KHz, 2KHz, 512Hz, 64Hz, 16Hz and 2Hz interrupt sources for Real-Time-Clock

6.11 Sleep Mode, Wakeup, and Watchdog

6.11.1 Sleep and wakeup modes

1) Sleep: After power-on reset, IC starts running until a sleep command is issued. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.
2) Wakeup: CPU awaking from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The FIQ/IRQ signal makes CPU to complete the wakeup process and initialization.

6.11.2 Watchdog Reset

The GPCE2P064B provides another important feature, watchdog reset. If the watchdog function is enabled, a reset signal is generated to reset system when watchdog counter is overflow.
The purpose of watchdog is to monitor whether the system operates normally. Within a certain period, watchdog register must be cleared. If it is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again.

6.12 Soft Reset Protection

Software reset. Writing $5555 into P_System_Reset will reset the whole system similar to hardware reset (pull low RESETB pin), except a flag will set on in P_System_LVD_Ctrl(R/W).

6.13 ADC (Analog to Digital Converter) / DAC

The GPCE2P064B has eight channels 12-bit ADC (Analog to

Digital Converter). The function of an ADC is to convert analog signal to digital signal, e.g. a voltage level into a digital word. The four channels of ADC can be four channels of line-in from IOB [3:0] or one channel microphone (MIC) input through amplifier PGA controller, and AGC controller. The MIC amplifier circuit is capable of reducing common mode noise by transmitting signals through differential MIC Inputs (MICN, MICP). Moreover, an external resistor can be applied to adjust microphone gain and time of AGC operating. The AD needs to select source of line-in before conversion. The ADC take pad(VDD_ADC) as voltage reference.

6.14 SPI

A Serial Peripheral Interface (SPI) controller is built in GPCE2P064B to facilitate communicating with other devices and components. There are four control signals on SPI - SPICS (IOA12), SPICK (IOA13), SDO (IOA14), and SDI (IOA15).

6.15 Audio Algorithm

The following speech types can be used in GPCE2P064B: PCM, SACM_S200, SACM_S480, SACM_S530, SACM_A1600, SACM_A1601, SACM_A1800, SACM_A3400pro, SACM_A3600, SACM_DVR520, SACM_DVR1600, SACM_DVR1800, SACM_DVR3200, and SACM_DVR4800. For melody synthesis, the GPCE2P064B supports SACM_MS01 (FM) and SACM_MS02 (wave-table) synthesizers.

7 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 4.0V
PortA/B Pad Supply Voltage	V_{IO}	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see DC Electrical Characteristics.

7.2 DC Characteristics (V3_REGO = 3.0V, VDDIO = 4.5V (PortA & B), TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REG	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	13	-	mA	F_{OSC} = 49.152MHz, AD, DAC disable, no load
Standby Current	I_{STB}	-	-	5	μA	Disable 32KHz, Disable PLL(F_{OSC})
				10	μA	Enable 32KHz,Disable PLL(F_{OSC})
Input High Level	V_{IH}	0.7VDD_{IO}	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3VDD_{IO}	V	-
Output High Current	I_{OH}	-	-20	-	mA	V_{OH} = 0.7VDDIO
Output Low Current (PA[3:0], PB[3:0])	I_{OL}	-	20	-	mA	V_{OL} = 0.3VDDIO
Output Low Current (PA[7:4])	I_{OL}	-	40	-	mA	V_{OL} = 0.3VDDIO
Input Pull-Low Resister (PA15:0)	R_{PL}	-	120	-	KΩ	V_{IN} = VDDIO
Input Pull-Low Resister (PB[3:0])	R_{PL}	-	1200	-	KΩ	V_{IN} = VDDIO
Input Pull-High Resister (PA15:0)	R_{PH}	-	110	-	KΩ	V_{IN} = VSS
Internal ROSC frequency deviation	⊿F/F	-3%	32768	+3%	HZ	V3_REGO = 3.0V

7.3 DC Characteristics (V3_REGO = 3.0V, VDDIO = 3.3V (PortA & B), TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	-
Operating Current	I_{OP}	-	13	-	mA	F_{OSC} = 49.152MHz, AD, DAC disable, no load
Standby Current	I_{STB}	-	-	3	μA	Disable 32KHz, Disable PLL(F_{OSC})
				6	μA	Enable 32KHz,Disable PLL(F_{OSC})
Input High Level	V_{IH}	0.7VDD_{IO}	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3VDD_{IO}	V	-
Output High Current	I_{OH}	-	-11	-	mA	V_{OH} = 0.7VDDIO

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output Low Current (PA[3:0], PB[3:0])	I_{OL}	-	11	-	mA	V_{OL} = 0.3VDDIO
Output Low Current (PA[7:4])	I_{OL}	-	25	-	mA	V_{OL} = 0.3VDDIO
Input Pull-Low Resister (PA15:0)	R_{PL}	-	120	-	KΩ	V_{IN} = VDDIO
Input Pull-Low Resister (PB[3:0])	R_{PL}	-	1200	-	KΩ	V_{IN} = VDDIO
Input Pull-High Resister (PA15:0, PB3:0)	R_{PH}	-	110	-	KΩ	V_{IN} = VSS
Internal ROSC frequency deviation	⊿F/F	-3%	32768	+3%	HZ	V3_REGO = 3.0V

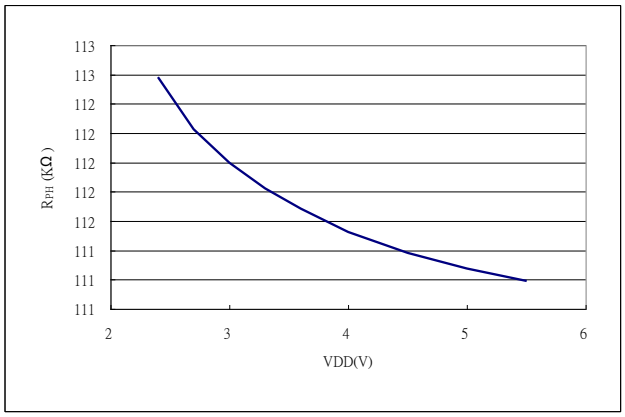
7.4 DAC Characteristics (VDD_DAC = 5.0V, TA = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
THD+n (5V @0.6W)	-	-	1	-	%
Noise at No Signal	-	-	-97	-	dBr A
Dynamic Range(-60dB)	-	-	-82	-	dBr A

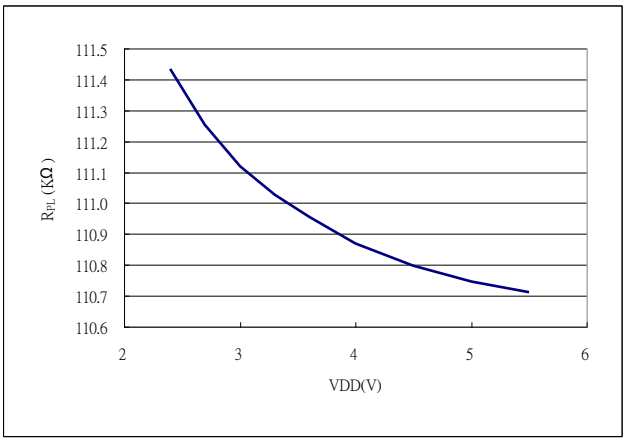
7.5 Regulator Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage	VDD_REG	2.4	-	5.5	V	
Maximum Current Output	IREGO	-	-	40	mA	VDD_REG (Regulator in)= 4.5V,△VDD (Regulator out) <100mV
Output Voltage	V3_REGO	2.85	3.0	3.15	V	VDD_REG > 3.2V and V3_REGO is 3.0V
Standby Current	IRGES	-	2.5	-	uA	

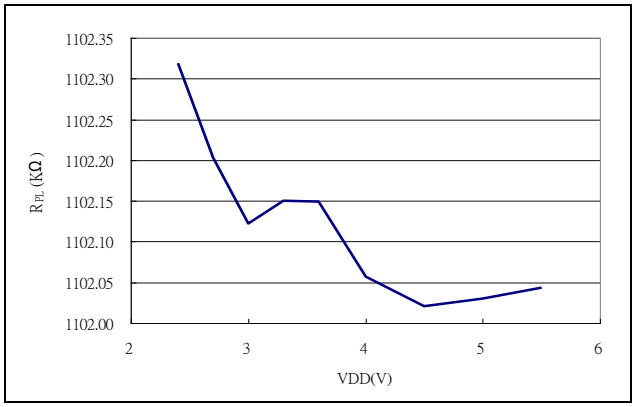
7.6 Pull High Resister and VDDIO



7.7 Pull Low Resister and VDDIO (Normal PAD)

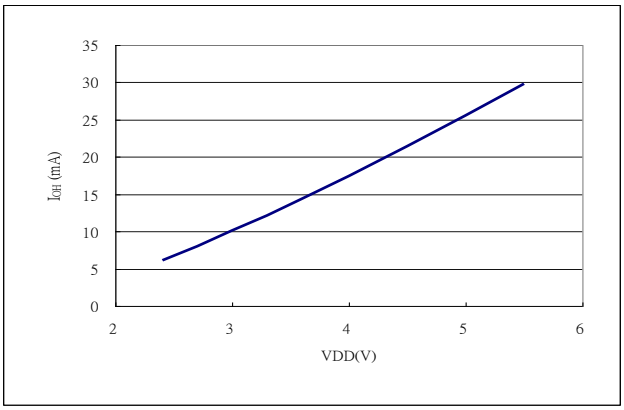


7.8 Pull Low Resister and VDDIO (IOB[3:0] PAD with input high)



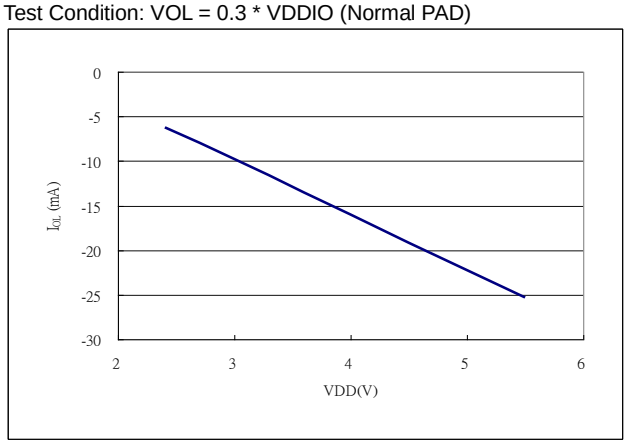
7.9 I/O Output High Current I_{OH} and VDDIO

Test Condition: VOH = 0.7 * VDDIO



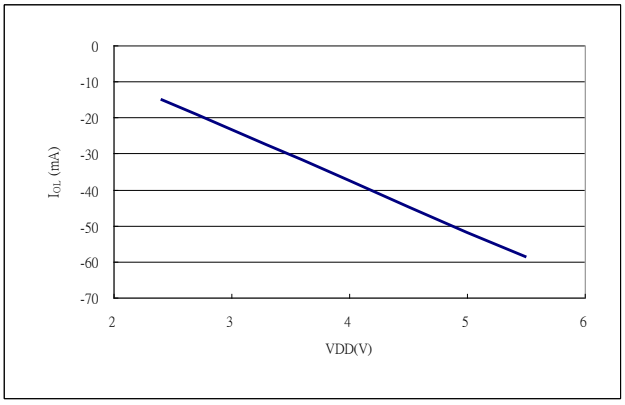
7.10 I/O Output Low Current I_{OL} and VDDIO (Normal Pad)

Test Condition: VOL = 0.3 * VDDIO (Normal PAD)

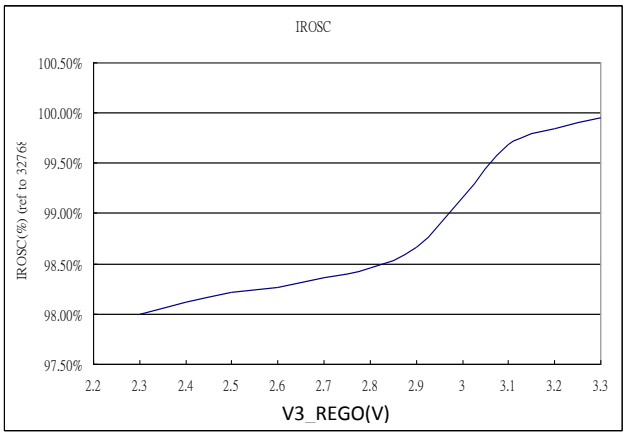


7.11 I/O Output Low Current I_{OL} and VDDIO (High driving pad)

Test Condition: VOL = 0.3 * VDDIO (High Driving PAD)

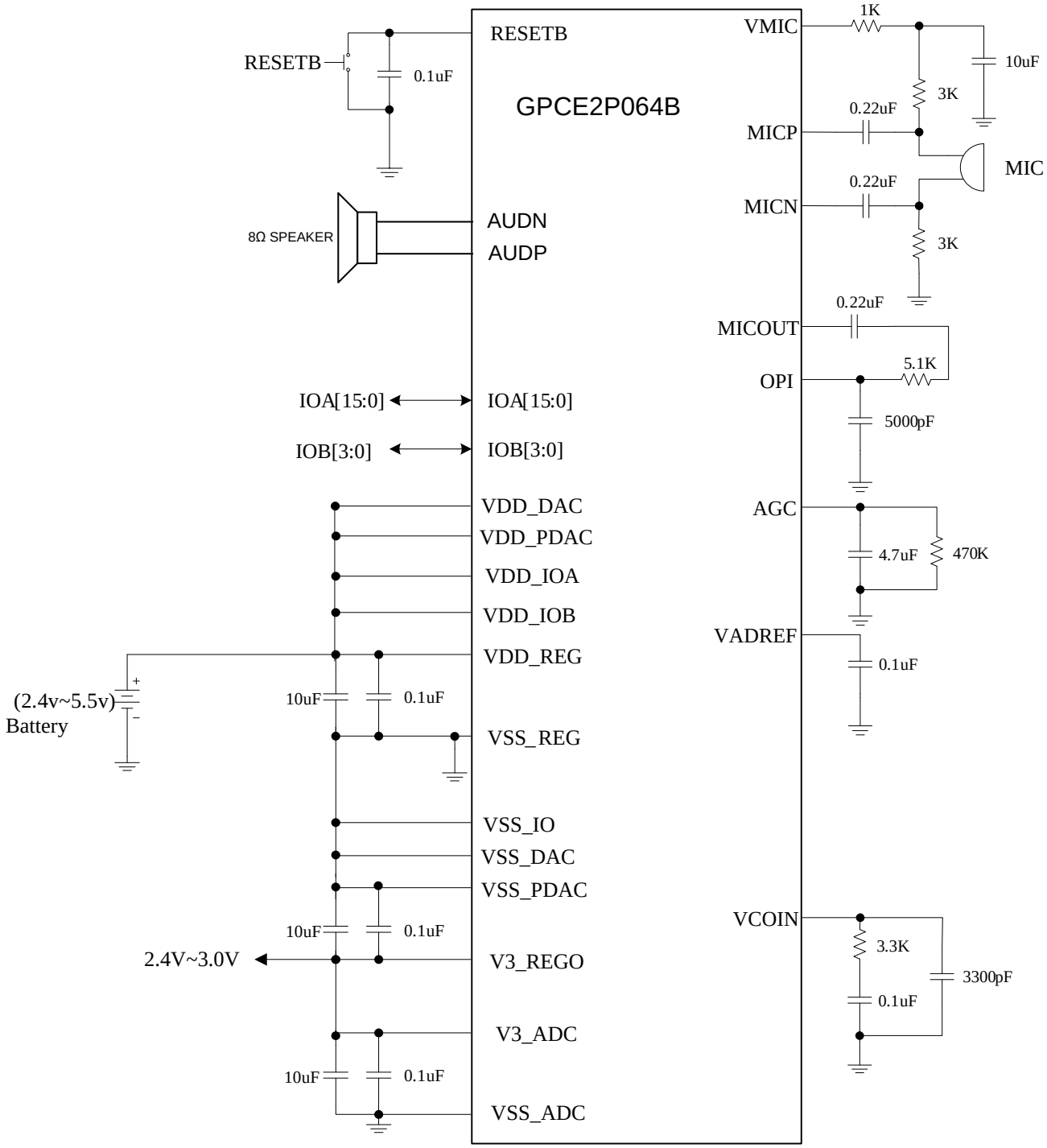


7.12 Internal ROSC and V3_REGO



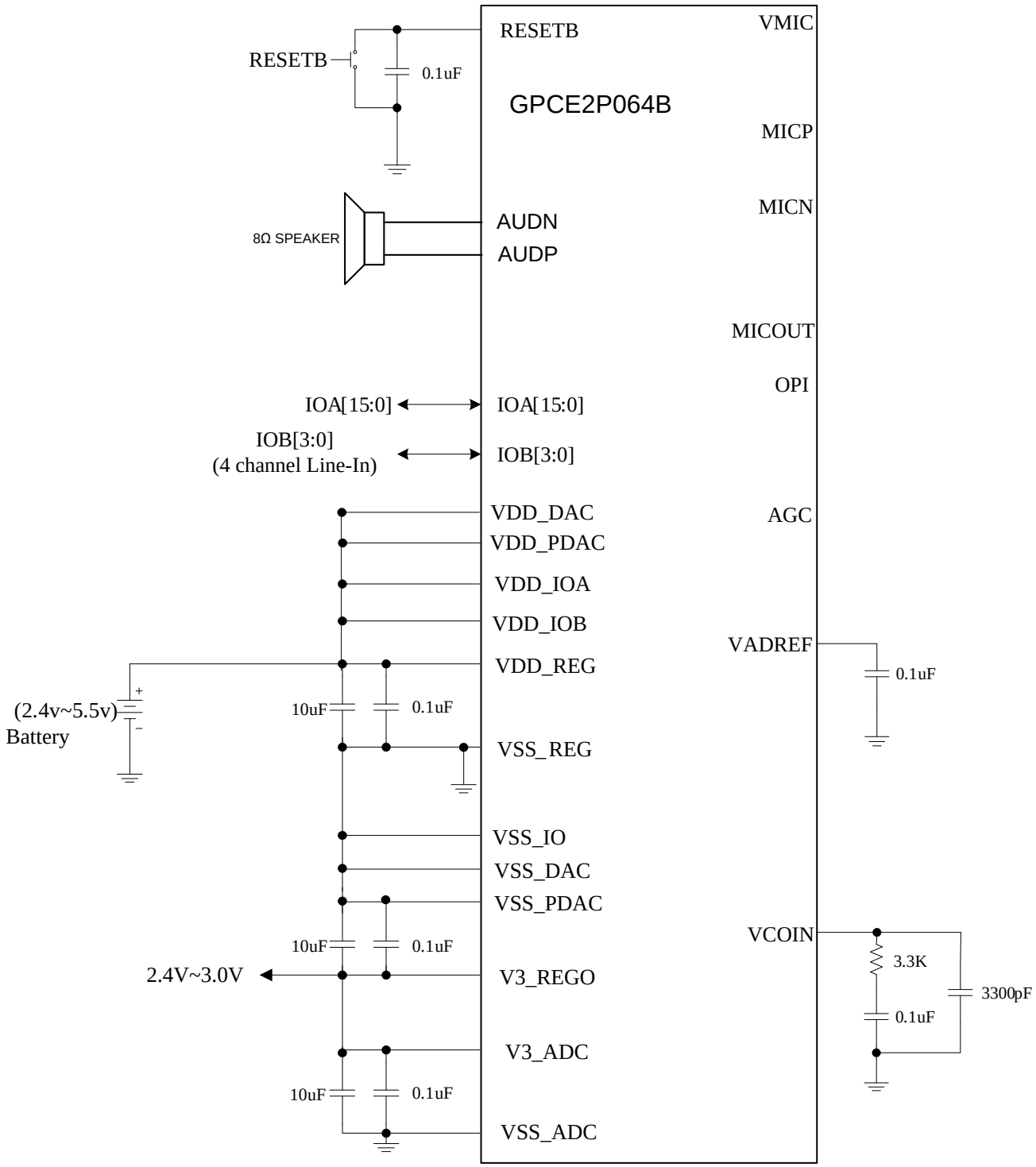
8 APPLICATION CIRCUITS

8.1 Application Circuit with MIC_IN Selected



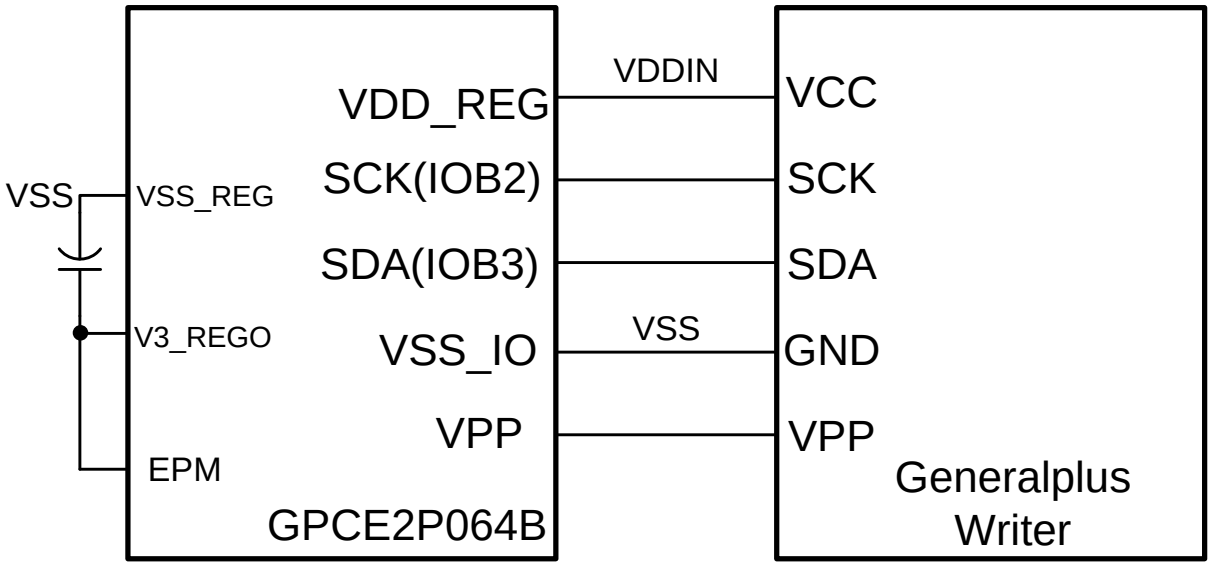
Note: V3_REGO is output of built-in regulator with maximum current 40mA. It is recommended that only use it for internal power pad.

8.2 Application Circuit with LINE-IN Selected



Note: V3_REGO is output of built-in regulator with maximum current 40mA. It is recommended that only use it for internal power pad.

8.3 OTP ROM Programming Circuit



9 PACKAGE/PAD LOCATIONS

9.1 Ordering Information

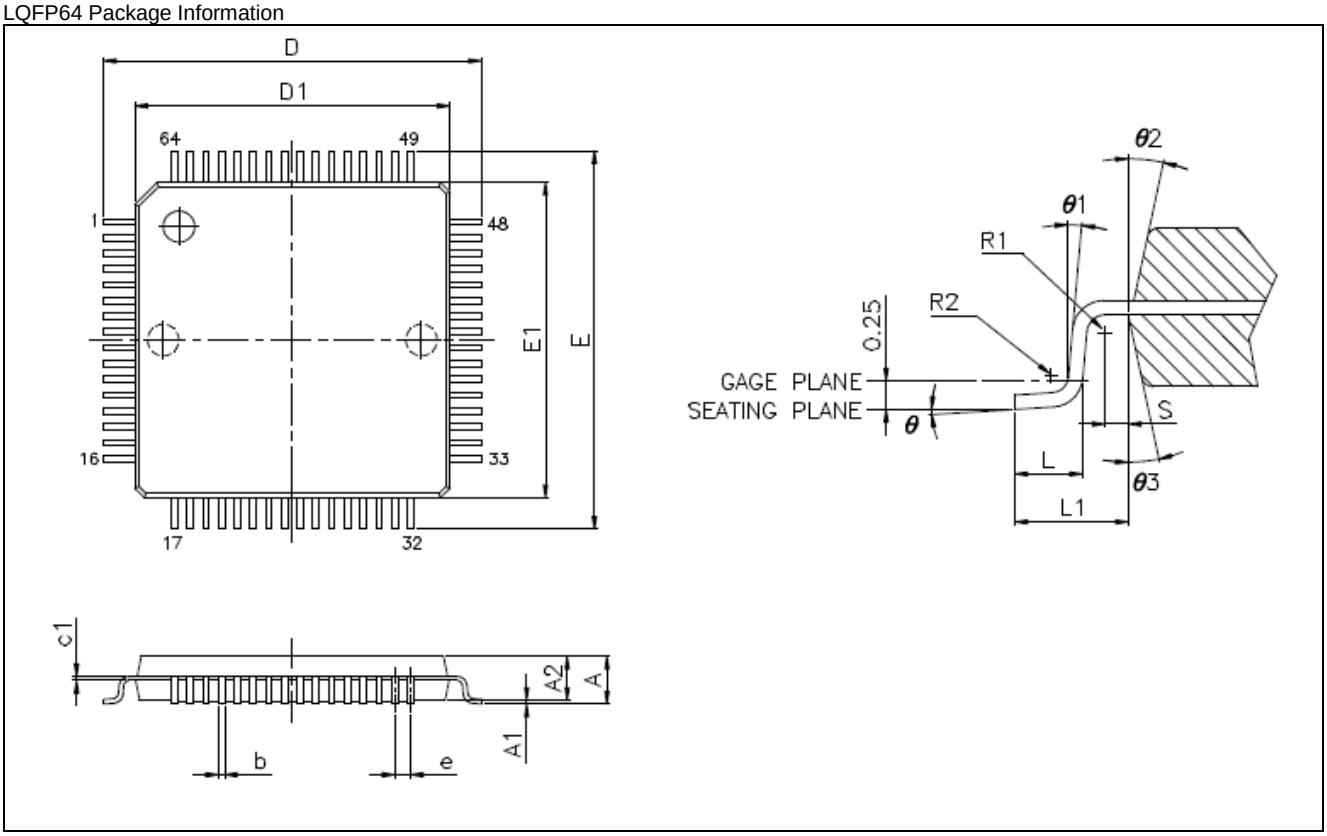
Product Number	Package Type
GPCE2P064B-NnnV-C	Chip form
GPCE2P064B-NnnV-QL02x	Halogen Free Package – LQFP64
GPCE2P064B-NnnV-HS10x	Halogen Free Package – SOP24

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

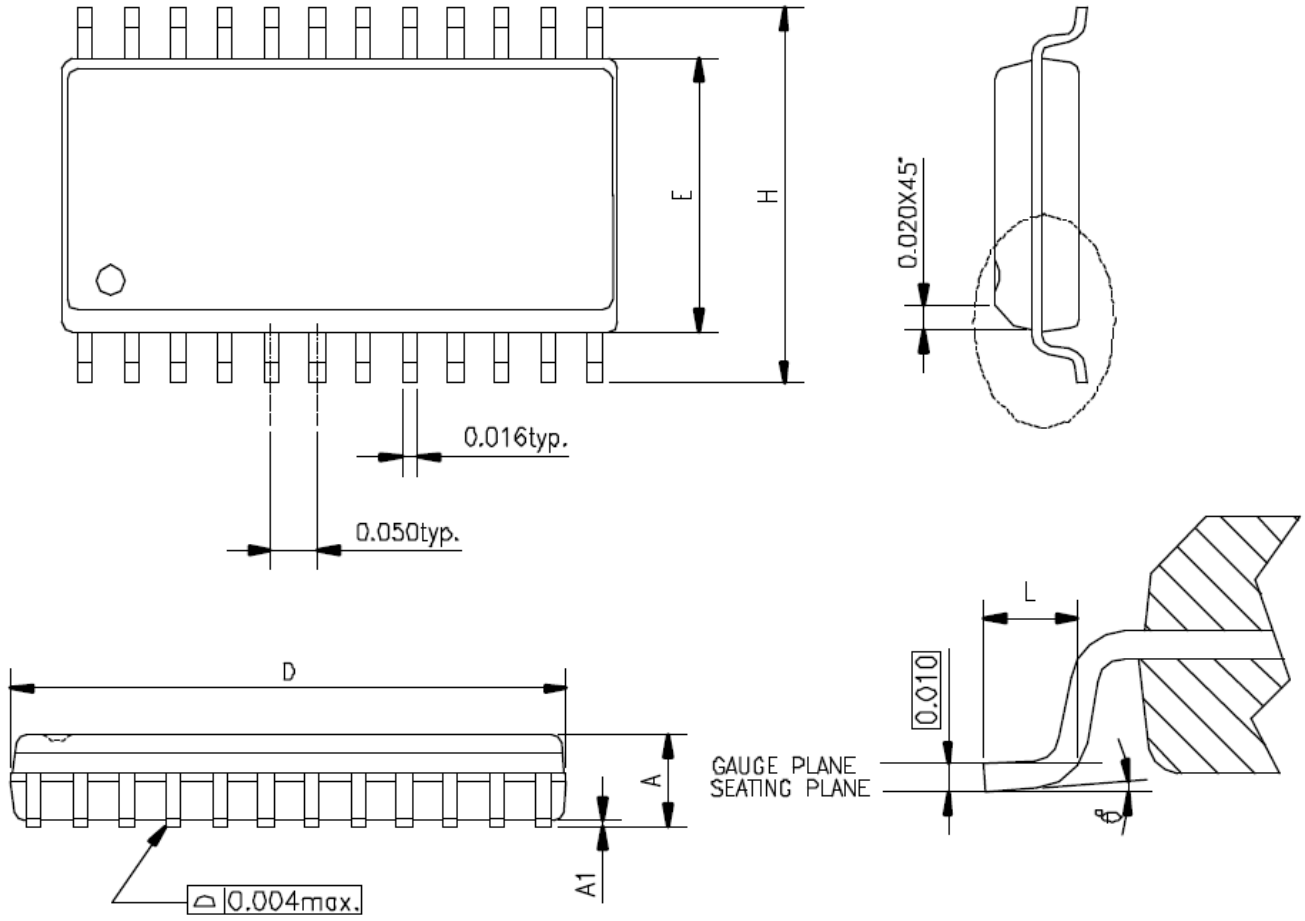
Note3: Package form number (x = 1 - 9, serial number).

LQFP64 Package Information



Symbol	Dimension in mm		
	Min.	Typ.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	-	0.16
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20 REF		
θ	3.5° REF		
θ1	5.0° REF		
θ2	12° REF		
θ3	12° REF		
R1	0.16 REF		
R2	0.15 REF		

9.2 SOP24 Package Information



Symbol	Dimension in INCH		
	Min.	Typ.	Max.
A	0.093	0.099	0.104
A1	0.004	-	0.012
D	0.599	0.600	0.614
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0	-	8

10 DISCLAIMER

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11 REVISION HISTORY

Date	Revision #	Description	Page
Apr. 07, 2015	1.2	Modify 5.1, 5.2, for package SOP24	25
Dec. 25, 2013	1.1	1. Rename : “V33_REG” to “V3_REGO”, “V33_ADC” to “V3_ADC” 2. Correct the value of V3_REGO at P2,P12,P13,P16 and P17	23
Sep. 25, 2013	1.0	Original	23