DATA SHEET

GPCE256A

Sound Controller with
128 K x 16 MASK ROM

OCT. 02, 2013

Version 1.3

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SOUND CONTROLLER WITH 128 K x 16 MASK ROM

1. GENERAL DESCRIPTION

The GPCE256A is equipped with the newest 16-bit CPU *μ'nSP*® (read as "micro-n-SP") designed by SUNPLUS. It's high processing speed empowered the *μ'nSP™ ISA 1.3* capable of handling sophisticated digital signal processes (DSP) computation easily. The wide range of CPU speed, from 0.1875MHz to 48MHz, makes the GPCE256A to be easily applied in different kinds of applications. The built-in memory contains 128K-word mask ROM and 2K-word working SRAM. Other features including 32 programmable multi-functional I/Os, three 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection, eight channels of 12-bit ADC (one channel built-in MIC amplifier with Auto Gain Controller). One very important feature is GPCE256A built-in very high quality, one 16-bit DACs, this provides GPCE256A being able to output very high quality sound and music. Another two IO PWM outputs provide the convenience of generating some duty-cycle wave form signals. A power saving mode, halt mode, is designed to only stop CPU clock but reserve others. To save even more power, a sleep mode is available to stop all clocks. These two modes can be awakened from the I/O or interrupt source triggers.

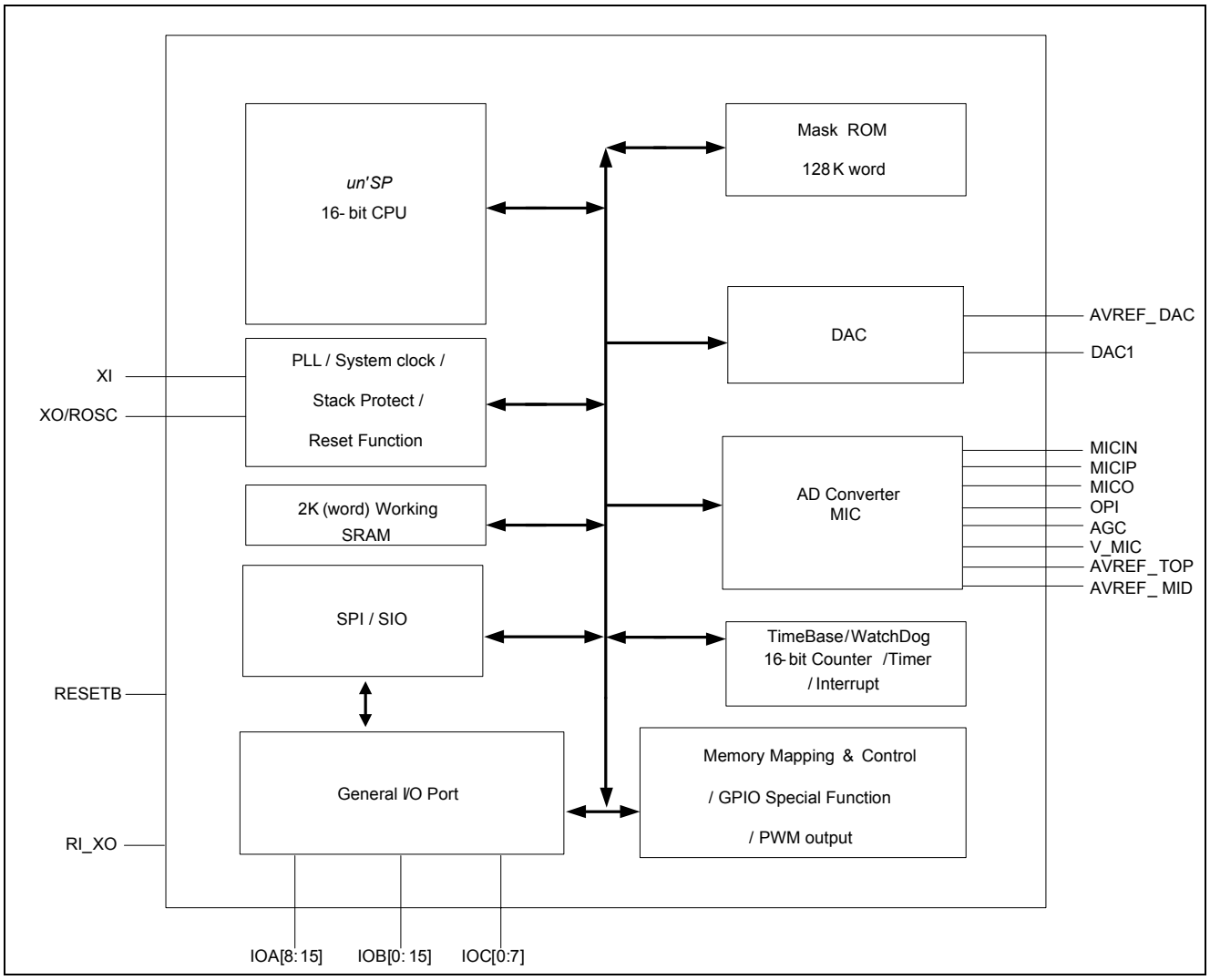
2. APPLICATION FIELD

- Intelligent interactive talking toys
- Advanced educational toys
- General speech synthesizer
- Long duration audio products

3. FEATURES

- 16-bit *μ'nSP™ ISA 1.3* microprocessor
- CPU clock: 0.1875MHz - 48MHz@6MHz crystal
- 128K-word mask ROM
- 2K-word CPU working SRAM
- Chip operating voltage: 2.7V - 3.6V
- IO operating voltage: 2.7V - 5.5V
- Total of 32 programmable IOs including IOA(8 pins), IOB(16 pins) and IOC(8 pins)
- Crystal Resonator & R-oscillator
- Standby mode (Clock Stop mode) for power savings
- Halt mode (only stops CPU clock) for power savings
- Three 16-bit timers/counters and One RTC
- One 16-bit DAC output
- Eight channels of 12-bit AD converter
- Wakeup source from IOA key, TIMER/RTC
- 32768Hz Real Time Clock (RTC)
- ADC external top reference voltage
- One Generalplus Serial interface I/O (SIO)
- One SPI serial interface I/O
- Built-in microphone amplifier and AGC function
- Low voltage reset and low voltage detection
- Watchdog function

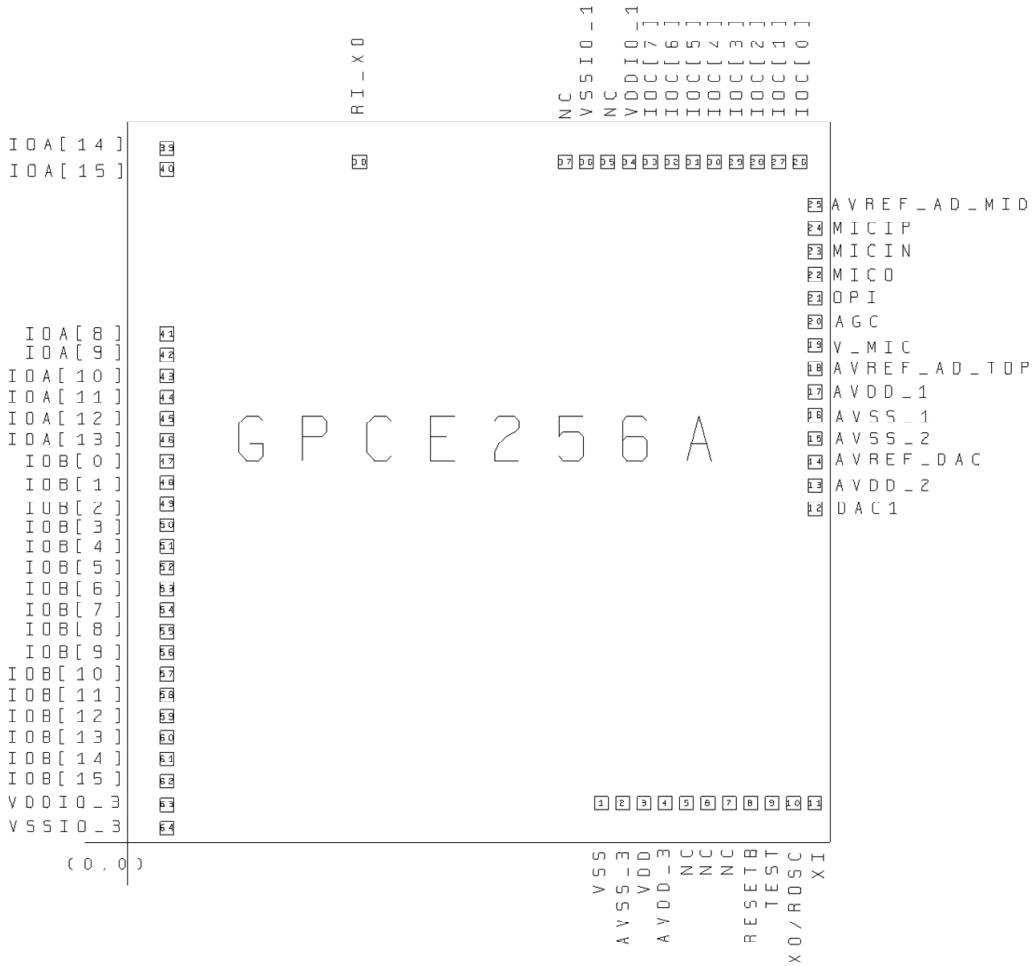
4. BLOCK DIAGRAM



5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
Port A, Port B, Port C & Port D			
IOA [15:8]	39 - 46	I/O	IOA [15:8]: bi-directional I/O ports. It can be programmed as wakeup I/O pins.
IOB [15:0]	47 - 62	I/O	IOB [15:0]: bi-directional I/O ports.
IOC [7:0]	26 - 33	I/O	IOC [7:0]: bi-directional I/O ports.
Power & GND			
VDDIO_1	34	P	Positive power supply for IOC [7:0].
VSSIO_1	36	G	Ground reference for IOC [7:0].
VDDIO_3	63	P	Positive power supply for IOA [15:8], IOB [15:0].
VSSIO_3	64	G	Ground reference for IOA [15:8], IOB [15:0].
AVDD_1	17	P	Positive power supply for analog circuit including ADC & MIC.
AVSS_1	16	G	Ground reference for analog circuit including ADC & MIC.
AVDD_2	13	P	Positive power supply for analog circuit including DAC.
AVSS_2	15	G	Ground reference for analog circuit including DAC.
AVDD_3	4	P	Positive power supply for analog circuit including PLL, ROSC and OSC.
AVSS_3	2	G	Ground reference for analog circuit including PLL, ROSC and OSC.
VDD	3	P	Positive power supply for digital circuit.
VSS	1	G	Ground reference for digital circuit.
CLK System/ ICE Interface			
XI	11	I	Oscillator crystal input.
XO / ROSC	10	O	Oscillator crystal output / ROSC-input at ROSC mode.
Option			
TEST	9	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low).
RI_XO	38	I	ROSC/Crystal selection pin, high is Crystal and low is R-oscillator (Pad internal pull high).
DAC			
DAC1	12	O	Audio DAC1 output.
AVREF_DAC	14	O	DAC reference pin.
ADC			
MICIP	24	I	MIC amplifier input positive (Internal Floating).
MICIN	23	I	MIC amplifier input negative (refer to application circuit).
MICO	22	O	MIC amplifier output (refer to application circuit).
OPI	21	I	Audio amplifier negative input (refer to application circuit).
AGC	20	IO	AGC by pass filter (refer to application circuit).
V_MIC	19	O	Microphone power supply.
AVREF_TOP	18	I	AVREF_TOP input (ADC maximum value voltage) (refer to application circuit).
AVREF_MID	25	O	AVREF_TOP/2 output with buffer (~ ADC middle value voltage) (refer to application circuit).
Other Signal			
RESETB	8	I	System reset pin (active low) (internal 47Kohm pull high resistor).
NC	5, 6, 7, 35, 37		
Total: 64 pads			

5.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure the IC functions properly, please bond all VDD and VSS pins.

Note3: The 0.1uF capacitor between VDD and VSS should be placed to IC as closed as possible.

6. FUNCTIONAL DESCRIPTION

6.1. CPU

The GPCE256A is equipped with the newest 16-bit CPU *μ'nSP*® (read as "micro-n-SP") designed by SUNPLUS. Thirteen registers are available in *μ'nSP*®: R1 ~ R4 (General-purpose registers), SR1 ~ SR4 (Secondary Bank Registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP), SR (Segment Register) and FR (Flag Register). It provides interrupts including thirteen FIQs (Fast Interrupt Request) and fourteen IRQs (Interrupt Request), plus one software-interrupt, BREAK.

Moreover, a high performance hardware multiplier with the capability of FIR filter calculation is also built-in to reduce the software multiplication loading.

6.2. Memory

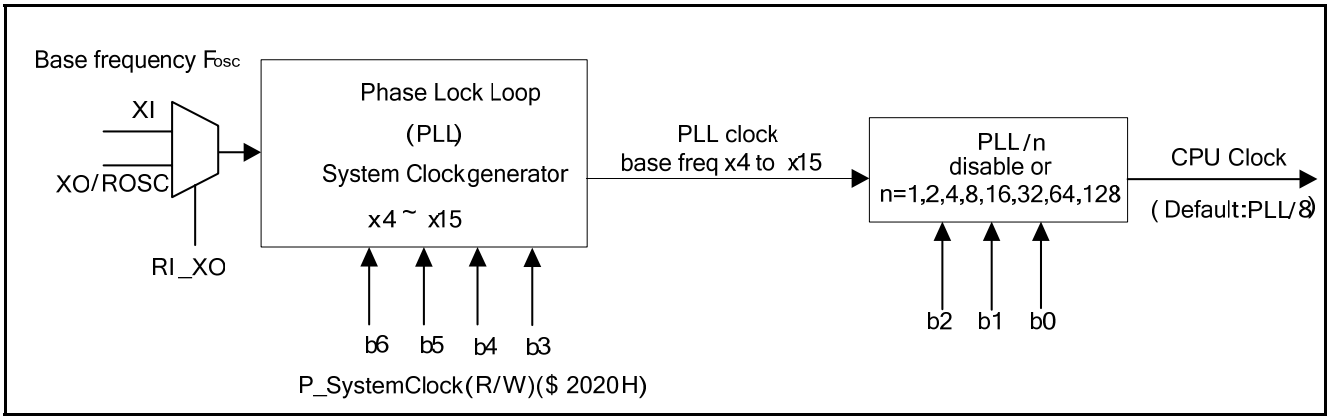
6.2.1. SRAM

The amount of SRAM is 2K-word (including Stack) ranged from $0000 through $07FF with two CPU-clock cycles access speed.

6.2.2. Mask ROM

Mask ROM size is 128K words and its address is mapped from $004000 to $023FFF. This mask ROM is a high-speed memory, with 60ns access time. The mask option on GPCE256A is described below.

OPTION_WDOG_EN: enable or disable watchdog reset.



6.3. PLL, Clock, Power Saving Mode

6.3.1. PLL (Phase Lock Loop)

The purpose of PLL is to provide stable output frequency which reference a base frequency (from crystal). The PLL frequency gain (output frequency / input frequency) ranges from 4 to 15. Suppose base frequency is 6MHz and PLL frequency gain selects 8, the output frequency of PLL is 48MHz.

6.3.1.1. System clock

Basically, the system clock is provided by PLL and programmed by the P_SystemClock to determine the clock frequency for system. The default PLL clock (PLL) pumps to $6*F_{OSC}$, that is 36MHz using 6MHz crystal and CPU clock will also be 36MHz if PLL/8 not specified.

6.3.1.2. 32768Hz RTC

The Real Time Clock (RTC) is normally used in watch, clock or other timing-based applications. A 2Hz-RTC (0.5 second) function is available in GPCE256A. The RTC counts the time as well as to wake CPU up whenever RTC occurs. Time can be traced by the numbers of RTC occurrence. In addition, GPCE256A supports 32768Hz oscillator in strong mode and weak mode for power savings. In strong mode, 32768Hz OSC circuit in GPCE256A always runs at the highest power consumption. On the other hand, 32768Hz OSC in GPCE256A circuit run less power consumption in weak mode, but it must use a high-standard 32768Hz external crystal such as SEIKO SSP_T6 or Microcrystal CC5V-T1A.

6.4. Power Saving Mode

The GPCE256A features a power savings mode (or called standby mode) for low power applications. To enter standby mode, the desired key wakeup port(IOA[15:8]) must be configured to input first. And read the P_IOA_Data to latch the IOA state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing $5555 into P_SystemSleep(W) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states until CPU being awakened. The wakeup sources in GPCE256A include KEY wake up (IOA[15:8]), RTC wakeup, and IRQ1 – IRQ7. After GPCE256A is awakened, CPU will

continue to execute the program from the location it slept. Programmer can also enable or disable the 32768Hz RTC when CPU is in standby mode.

6.5. CPU Halt Mode

The GPCE256A features a CPU halt mode for power savings. In this mode, the CPU clock is turned off.

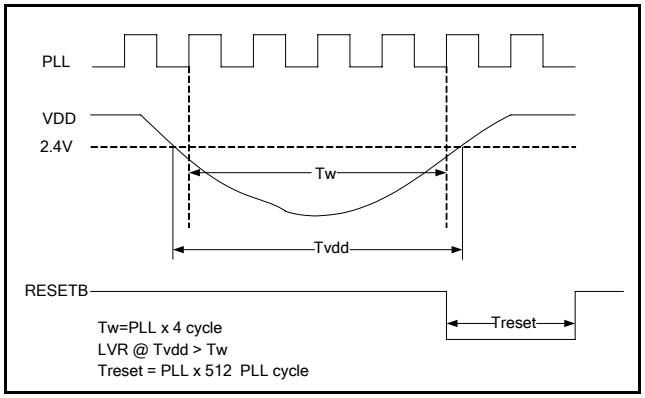
6.6. Low Voltage Detection and Low Voltage Reset

6.6.1. Low Voltage Detection (LVD)

The Low Voltage Detect (LVD) reports the circumstance of present voltage. There are four LVD levels to be selected: 2.6V, 2.8V, 3.0v and 3.2V. Those levels can be programmed via P_LVD_Ctrl. As an example, suppose LVD is given to 2.8V. When the voltage drops below 2.8V, the b12 of P_LVD_Ctrl is read as HIGH. In such state, program can be designed to react this condition.

6.6.2. Low Voltage Reset (LVR)

In addition to the LVD, the GPCE256A provides another important feature, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below 2.4V for 4 consecutive PLL system clock cycles. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below 2.4V. Using LVR, it will reset all functions to the initial operational (stable) states when the voltage drops below 2.4V. The LVR function is always on in GPCE256A. A LVR timing diagram is given as follows:



6.6.3. Watchdog reset

The GPCE256A provides another important feature, watchdog reset. With the watchdog function, a reset signal is generated to reset system when watchdog counter is overflow and the mask option of OPTION_WDOG_EN is enabled.

The purpose of watchdog is to monitor whether the system operates normally. Within a certain period, watchdog register must be cleared. If it is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again.

6.6.4. Soft reset protection

Software reset. Writes $5555 into P_System_Reset will reset the whole system like hardware reset (pull low RESETB pin), except a flag will set on in P_System_LVD_Ctrl(R/W).

6.6.5. Stack access protection

GPCE256A will reset when stack operation (example push or pop) of CPU accesses the SRAM that is not in the defined range. The defined stack range uses stack top (P_Stack_Top) and bottom (P_Stack_Bottom) control register.

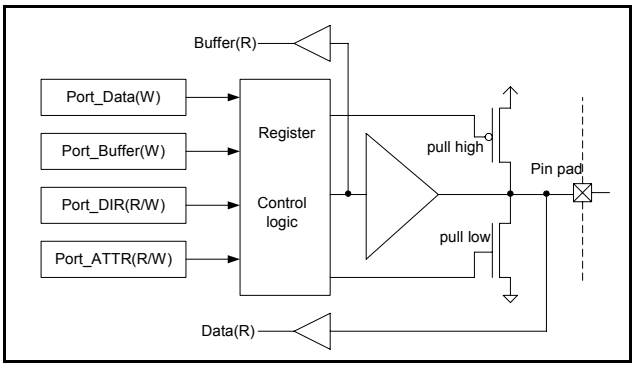
6.7. Interrupt

The GPCE256A has 14 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

Interrupt Source	Interrupt Name / FIQ Name	IRQ Priority
Timer A	IRQ0_TMA/FIQ_TMA	1(High)
Timer B	IRQ1_TMB/FIQ_TMB	2
Timer C	IRQ2_TMC/FIQ_TMC	3
SPI	IRQ3_SPI/FIQ_SPI	4
SIO	IRQ3_SIO	5
Key wakeup	IRQ5_KEY/FIQ_KEY	6
EXT1	IRQ5_EXT1/FIQ_EXT1	7
EXT2	IRQ5_EXT2/FIQ_EXT2	8
4096Hz	IRQ6_4KHz/FIQ_4KHz	9
2048Hz	IRQ6_2KHz/FIQ_2KHz	10
512Hz	IRQ6_512Hz/FIQ_512Hz	11
64Hz	IRQ7_64Hz/FIQ_64Hz	12
16Hz	IRQ7_16Hz_FIQ_16Hz	13
2Hz	IRQ7_2Hz/FIQ_2Hz	14(Low)

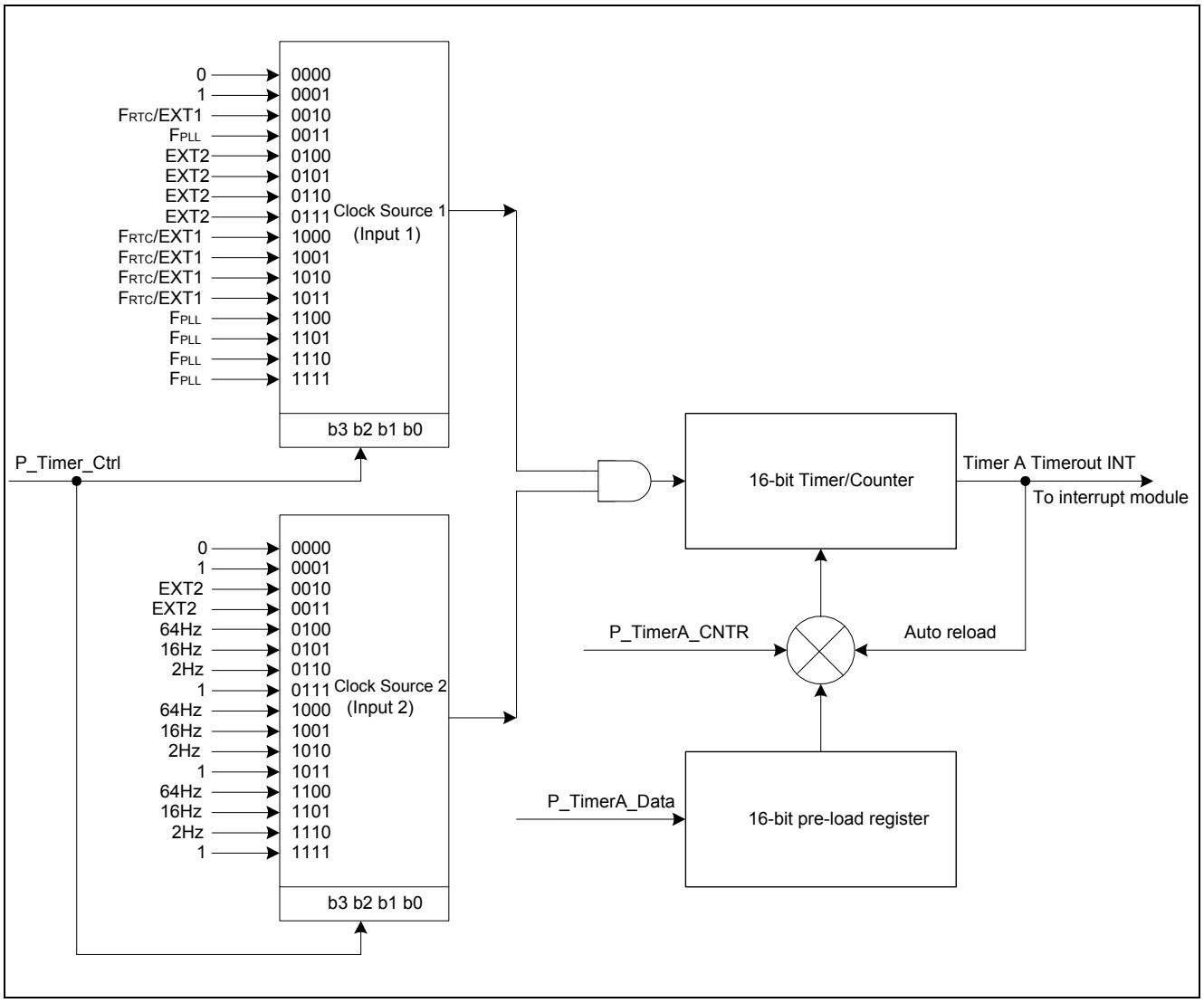
6.8. I/O

Three I/O ports are built in GPCE256A - PortA, PortB and PortC, total has 32 bit-programmable I/Os. The PortA is a general purpose I/O with programmable wakeup capability, i.e. IOA [15:8] is the key wakeup port. To activate key wakeup function, latch data on P_IOA_Data and enable the key wakeup function. Wakeup is triggered when the PortA state is different from at the time latched. Furthermore, the I/O ports can be operated at 5V level, higher than the CPU core which is a 3V level system. Suppose system operating voltage is running at 3.3V, then VDDIO (power for I/O) operates from 3.3V to 5.5V. In such condition, the I/O pad is capable of operating from 0V through VDDIO. The following diagram is an I/O schematic. Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R).



In addition to a general purpose I/O port function, PortA/B/C also shares/carries some special functions. A summary of PortA/B/C special functions is listed as follows:

Port	Special Function	Function Description
IOA8	APWMO1	TimerA PWM output
IOA9	BPWMO1	TimerB PWM output
	IROUT	IR Output
IOA10	Feedback Output2	Work with IOA11 by adding a RC circuit between them to get an OSC to EXT2 interrupts
IOA11	Feedback Input2	-
	EXT2	External interrupt source 2
IOA12	Feedback Output1	Work with IOA13 by adding a RC circuit between them to get an OSC to EXT1 interrupt
IOA13	Feedback Input1	-
	EXT1	External interrupt source 1
IOA14	RTCO	Real time clock output
IOA15	RTCI	Real time clock input
IOB6	APWMO2	TimerA PWM output
IOB7	BPWMO2	TimerB PWM output
IOB10	SDA	Serial interface data
IOB11	SCK	Serial interface clock
IOB12	CS	SPI chip select
IOB13	CK	SPI clock
IOB14	DI	SPI data input
IOB15	DO	SPI data output
IOC0	AN0	ADC Channel 0
IOC1	AN1	ADC Channel 1
IOC2	AN2	ADC Channel 2
IOC3	AN3	ADC Channel 3
IOC4	AN4	ADC Channel 4
IOC5	AN5	ADC Channel 5
IOC6	AN6	ADC Channel 6
IOC7	AN7	ADC Channel 7


0 0000
1 0001
FRTC/EXT1 0010
FPLL 0011
EXT2 0100
EXT2 0101
EXT2 0110
EXT2 0111
FRTC/EXT1 1000
FRTC/EXT1 1001
FRTC/EXT1 1010
FRTC/EXT1 1011
FPLL 1100
FPLL 1101
FPLL 1110
FPLL 1111
Clock Source 1
(Input 1)
b3 b2 b1 b0
P_Timer_Ctrl
0 0000
1 0001
EXT2 0010
EXT2 0011
64Hz 0100
16Hz 0101
2Hz 0110
1 0111
64Hz 1000
16Hz 1001
2Hz 1010
1 1011
64Hz 1100
16Hz 1101
2Hz 1110
1 1111
Clock Source 2
(Input 2)
b3 b2 b1 b0
16-bit Timer/Counter
Timer A Timerout INT
To interrupt module
P_TimerA_CNTR
Auto reload
P_TimerA_Data
16-bit pre-load register

Refer to the above table, the configuration of IOA10, IOA11, IOA12, and IOA13 involves feedback function that an OSC frequency can be obtained from EXT1 (EXT2) by simply adding a RC circuit between IOA10 (IOA12) and IOA11 (IOA13).

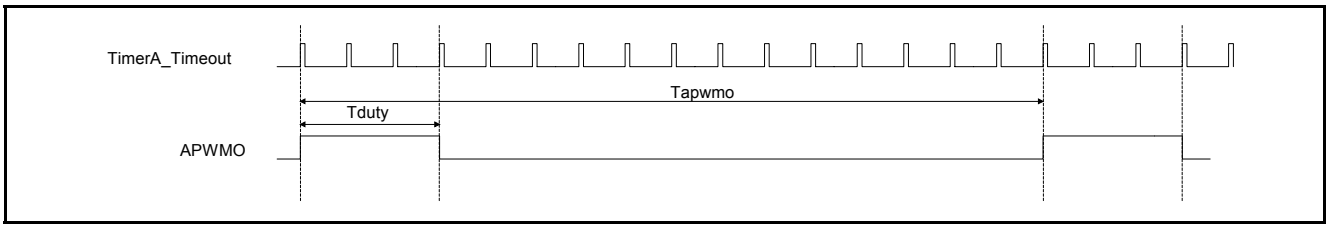
6.9. Timer/Counter

GPCE256A provides three 16-bit timers/counters - TimerA, TimerB and TimerC, or so called universal counters. The clock source of Timer A/B/C are from clock source Input 1 and clock source Input 2 (see below table) which perform AND operation to form the varieties of combinations. When timer overflows, a timeout signal (TAOUT) is sent to CPU interrupt module to generate a timer interrupt signal. In addition, Timer A/B/C hardware interrupt events can be used to latch the DAC audio output and trigger ADC conversion.

Example to Timer A, sending a write signal into TMA_CNT, the value of TMA_DATA (value=N) will reload into TMA_CNT and set an appropriated clock source. Timer wills up-count from N, N+1, N+2… 0XFFFF. An INT signal is generated at the moment of timer rolling over from “0xFFFF” to “0x0000”, and an INT signal is processed by INT controller immediately. At the same time, N will be reloaded into TMA_CNT and start counting again.

In Timer A, the clock Input 1 is a high frequency source and clock Input 2 is a low frequency clock source. The combination of clock Input 1 and 2 provides varieties of speeds to TimerA/CounterA - “1” representing pass signal (not gating), and “0” meaning timer deactivated. For instance, if Input 1=”1”, the clock is depending on Input 2. If Input 1=”0”, the TimerA is deactivated. The EXT1/ETX2 is the external clock source 1 and external clock source 2.

TMXSEL	Input 1	Input 2
0000	‘0’	‘0’
0001	‘1’	‘1’
0010	F_{RTC} / EXT1	EXT2
0011	F_{PLL}	EXT2
0100	EXT2	64Hz
0101	EXT2	16Hz
0110	EXT2	2Hz
0111	EXT2	‘1’
1000	F_{RTC} / EXT1	64Hz
1001	F_{RTC} / EXT1	16Hz
1010	F_{RTC} / EXT1	2Hz
1011	F_{RTC} / EXT1	‘1’
1100	F_{PLL}	64Hz
1101	F_{PLL}	16Hz
1110	F_{PLL}	2Hz
1111	F_{PLL}	‘1’



6.9.1. IO PWM

Two IO PWMs which duty is selected from 1/16 to 14/16. Example the above figure is a 3/16-duration cycle. The APWMO waveform is made by selecting a pulse width through P_APWM_Ctrl. As a result, each 16 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.

6.9.2. Timebase

Timebase, generated by 32768Hz crystal oscillator, is a combination of frequency selection. Furthermore, timebase generates 4KHz, 2KHz, 512Hz, 64Hz, 16Hz and 2Hz interrupt sources (FIQ6/IRQ6, FIQ7/IRQ7) for Real-Time-Clock.

6.10. Sleep Mode, Wakeup, Halt Mode, and Watchdog

6.10.1. Sleep and wakeup modes

1) Sleep: After power-on reset, IC starts running until a sleep command is issued. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.
2) Wakeup: CPU awaking from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The FIQ/IRQ signal makes CPU to complete the wakeup process and initialization. The CPU wakeup source is given in the following table.

Wakeup Source
Timer A interrupt
Timer B interrupt
Timer C interrupt
EXT1/EXT2/KEY
RTC

3) Halt mode: Halt mode for power saving. In this mode, CPU clock is turned off.

6.11. ADC (Analog to Digital Converter)

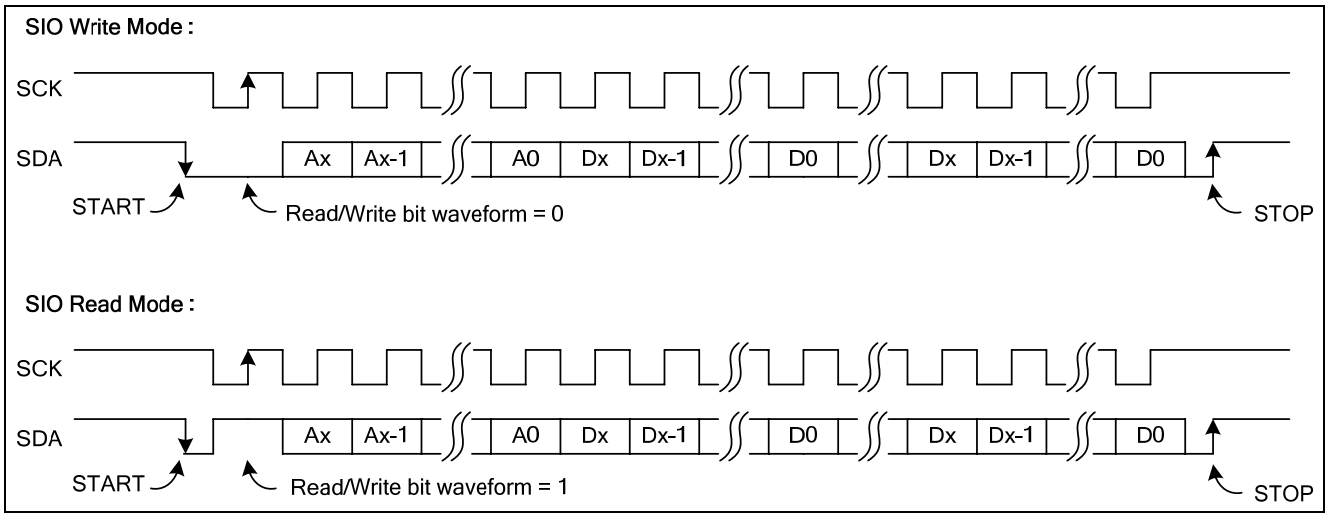
The GPCE256A has eight channels of 12-bit A/D (Analog to Digital Converter). The function of an A/D converter is to convert analog quality signal, e.g. a voltage into a digital word or input source, can be eight channels line-in from IOC [7:0] or one channel microphone input through amplifier and AGC controller. The MIC amplifier circuit is capable of reducing common mode noise by transmitting signals through MIC fully differential Input. Moreover, an external resistor can be applied to adjust microphone gain and time of AGC operating. The AD needs to select source of line-in before converting. The ADC is able to choose the external or internal (=AVDD) top reference voltage.

6.12. 16 Bits DAC Audio Driver

The GPCE256A provide one 16-bit DAC for audio outputs, the pin name is DAC1.

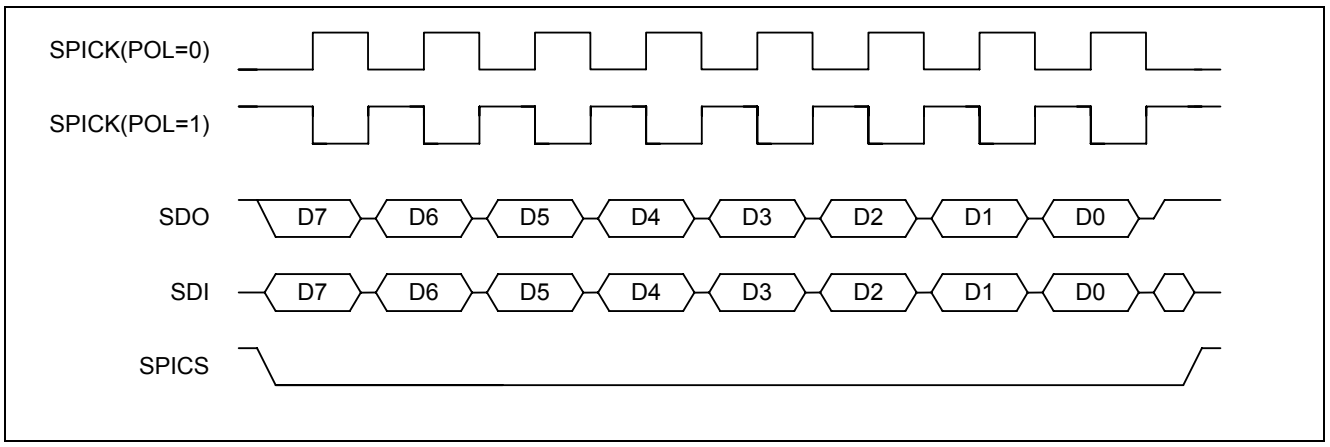
6.13. Serial Interface I/O (SIO)

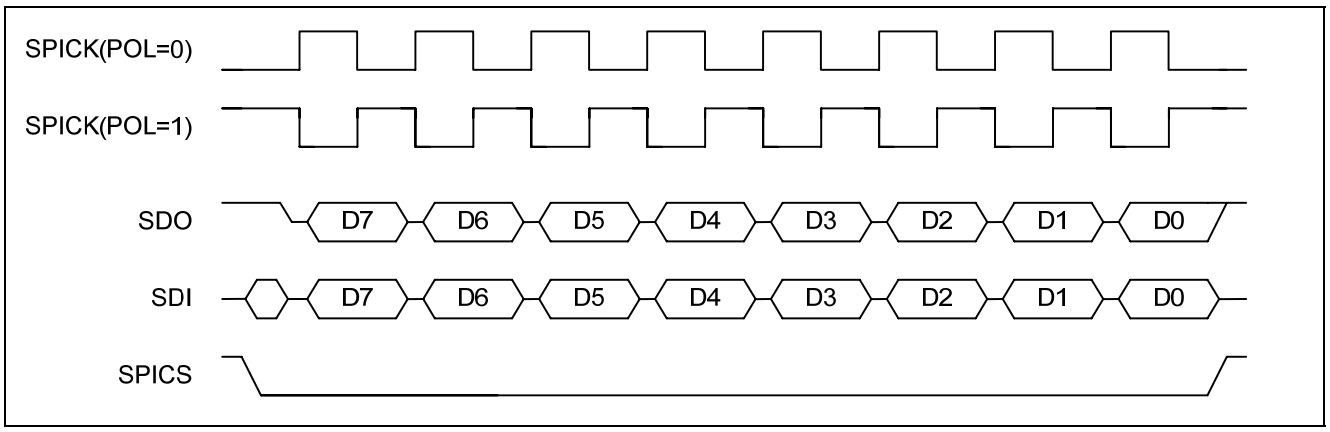
Serial interface I/O offers a one-bit serial interface that communicates with other devices. This serial interface is capable of transmitting or receiving data via two I/O pins, IOB11 (SCK) and IOB10 (SDA).



6.14. SPI

A Serial Peripheral Interface (SPI) controller is built in GPCE256A to facilitate communicating with other devices and components. There are four control signals on SPI - SPICS (IOB12), SPICK (IOB13), SDI (IOB14), and SDO (IOB15).





6.15. Audio Algorithm

The following speech types can be used in GPCE256A: PCM, LOG PCM, SACM_S200, SACM_S480, SACM_S530, SACM_S720, SACM_A1600, SACM_A1601, SACM_A3200, SACM_A3600, SACM_DVR1600 (Digital Voice Recorder), and SACM_DVR4800.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Min.	Max.	Unit
IO PAD Supply Voltage	VDDIO	-0.3	6.0	V
Analog Supply Voltage	AVDD	-0.3	4.0	V
Core Supply Voltage	VDD	-0.3	4.0	V
Input Voltage Range	V_{IN}	-0.3	VDDIO + 0.5	V
ESD Protection(HBM)	V_{ESD}	2K	-	V
Operating Temperature Range	T_A	0	+60	℃
Storage Temperature Range	T_{STO}	-50	+150	℃

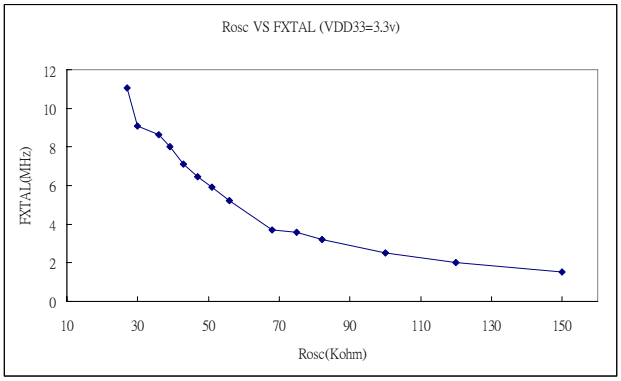
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.3V, VDDIO = 5V, T_A = 25℃)

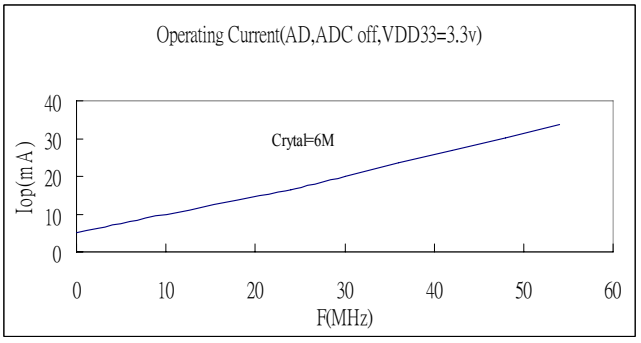
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage (IO)	VDDIO	VDD	5.0	5.5	V	IO VDD
Operating Voltage (Analog)	AVDD	2.7	3.3	3.6	V	3.3V for analog power
Operating Voltage (Core)	VDD	2.7	3.3	3.6	V	3.3V for core power
Operating Current	I_{OP}	-	30	-	mA	PLL = 48MHz, AD, DAC disable, no loading ; VDD = 3.3v; VDDIO=5.0v
Standby Current	I_{STB}	-	-	2	μA	Disable 32KHz crystal
Input High Level	V_{IH}	0.7 VDDIO	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3 VDDIO	V	-
IO Output High Current	I_{OH}	-	-6.9	-	mA	V_{OH} = 0.9 × VDDIO
IO Output Low Current	I_{OL}	-	12.1	-	mA	V_{OL} = 0.1 × VDDIO
Input Pull-Low Resistor (IOA, IOB, IOC)	R_{PL}	-	147	-	KΩ	V_{IN} = VDDIO
Input Pull-High Resistor (IOA, IOB,IOC)	R_{PH}	-	200	-	KΩ	V_{IN} = VSS

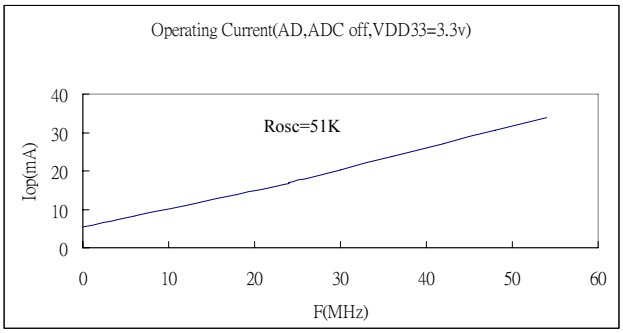
7.2.1. R-OSC frequency vs. resistor

7.2.1.1. VDD = 3.3V, VDDIO = 5V, T_A = 25℃



7.2.1.2. Operation current (VDD = 3.3V, VDDIO = 5V, T_A = 25℃)





7.3. ADC Characteristics (AVDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
ADC Line_In Input Voltage Range from IOC[7:0]	VINL (Note 1)	VSS-0.3	-	AVDD+0.3	V
ADC Microphone Input Voltage Range	VINM	VSS-0.3	-	AVDD+0.3	V
External ADC Top Voltage	VEXTREF (Note 2)	2.0	-	AVDD+0.3	V
Resolution of ADC	RESO	-	-	12	bits
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 4)	-	60	-	dB
Effective Number of Bit	ENOB (Note 5)	-	9.6	-	bits
Integral Non-Linearity of ADC	INL	-	±3.0		LSB (Note 3)
Differential Non-Linearity of ADC	DNL (Note 6)	-	±1.0	-	LSB
No Missing Code		-	12	-	Bits
MAX ADC Clock		-	-	3	MHz
AD Conversion Rate	F_{CONV}	-	-	150K	Hz

Note1: Internal protection diodes clamp the analog input to AVDD and VSS. These diodes allow the analog input to swing from (VSS-0.3V) to (AVDD+0.3V) without causing damage to the devices.

Note2: The ADC performance is limited by the system's noise level, so the GPCE256A just guarantee with the 8-bit accuracy when AVREF_TOP is 2V.

Note3: LSB means Least Significant Bit. With VINL=3V, 1LSB=3V/2^12= 0.732 mV.

Note4: The SINAD testing condition at VINLp-p=3.1V, F_{CONV}=48KHz, Fin=1KHz Sine waves at AVDD=3.3V from the IOC [7:0] input.

Note5: ENOB= (SINAD-1.76)/6.02.

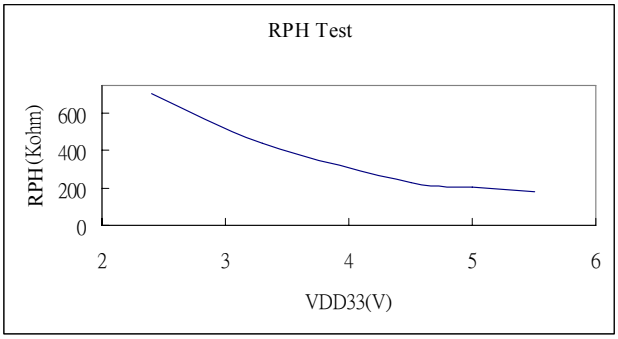
Note6: The ADC of GPCE256A can guarantee no missing code.

7.4. DAC Characteristics (AVDD = 3.3V, T_A = 25℃)

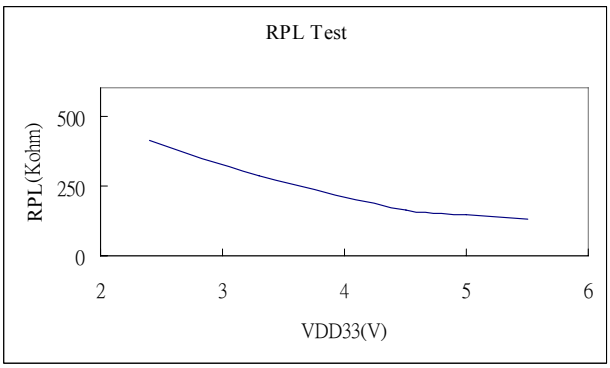
Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
Resolution of DAC	RESO	-	16	-	bit
Signal to Noise Ratio of DAC	SNR	-	90	-	dB
Dynamic Range	DR	-	85	-	dB
Sample Rate	F_S	-	200K	-	Hz
THD+N at FS (Note 1)	F_{OUT}=0.997KHz	-	-60	-	db
Output Loading	RL	125	-	-	ohm
Output Range	Input=Full Scale	-	60%	-	AVDD

Note1: The THD+N testing condition at AVDD=3.3, F_s=48KHz, Fin=0.997KHz input at RL=125 ohm.

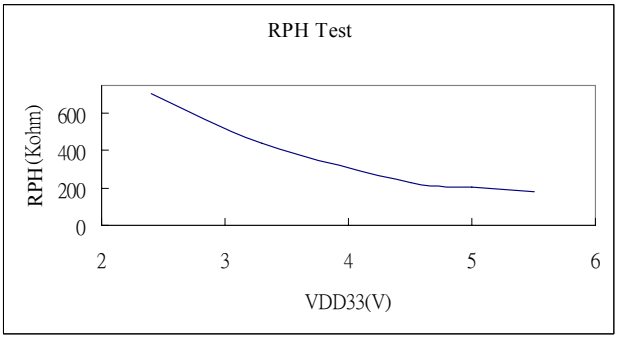
7.4.1. Pull high resister and VDDIO



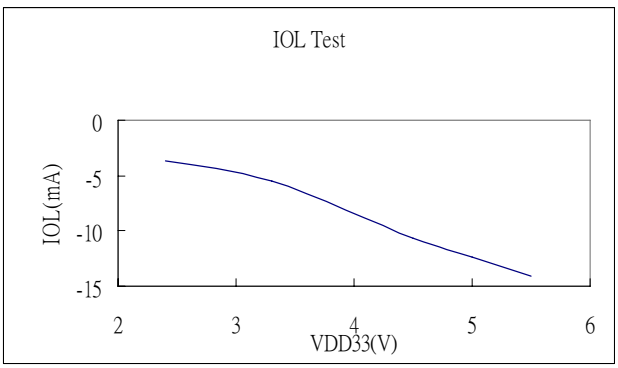
7.4.2. Pull low resister and VDDIO



7.4.3. I/O output high current I_{OH} and V_{OH}

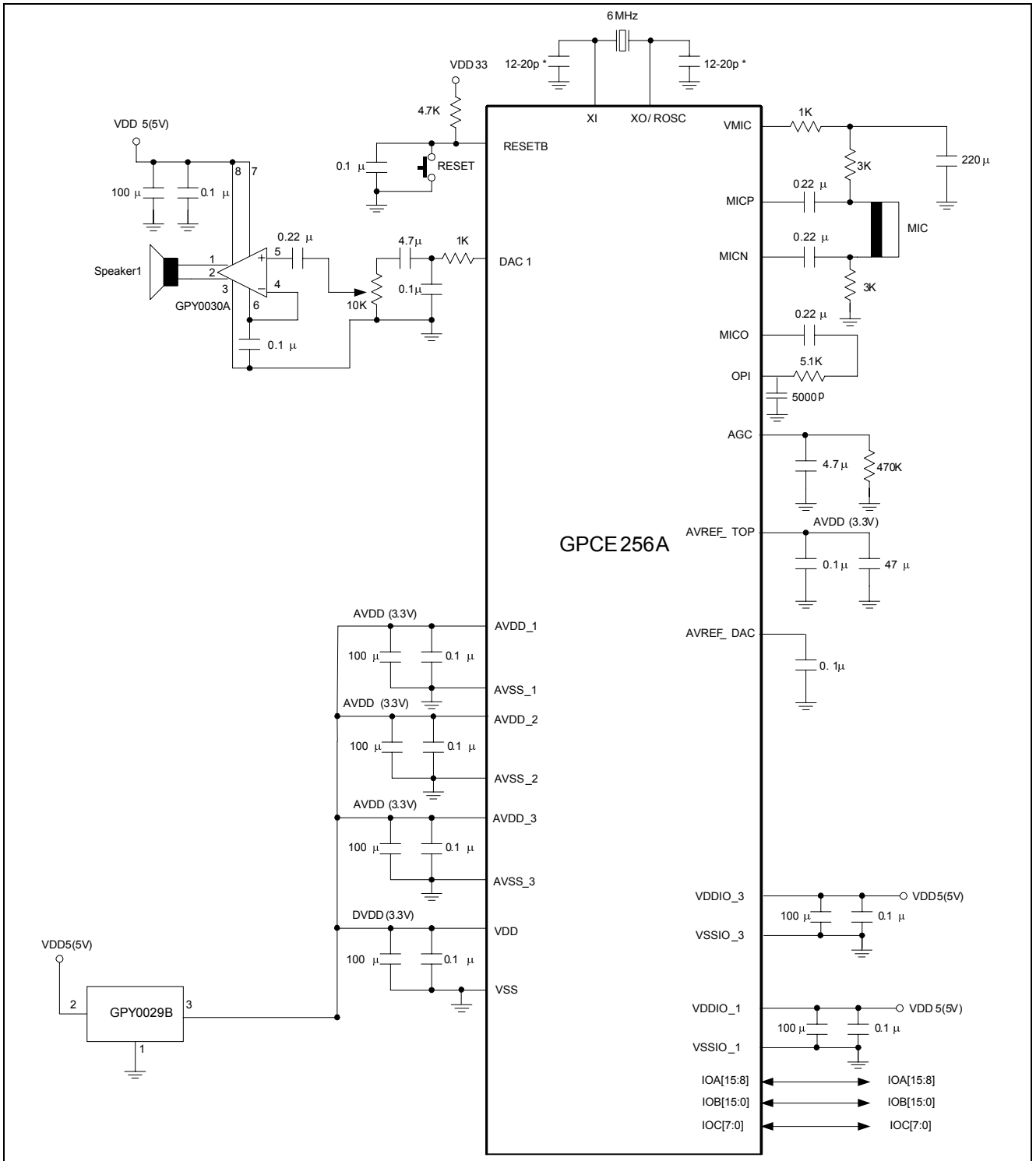


7.4.4. I/O output low current I_{OL} and V_{OL}



8. APPLICATION CIRCUITS

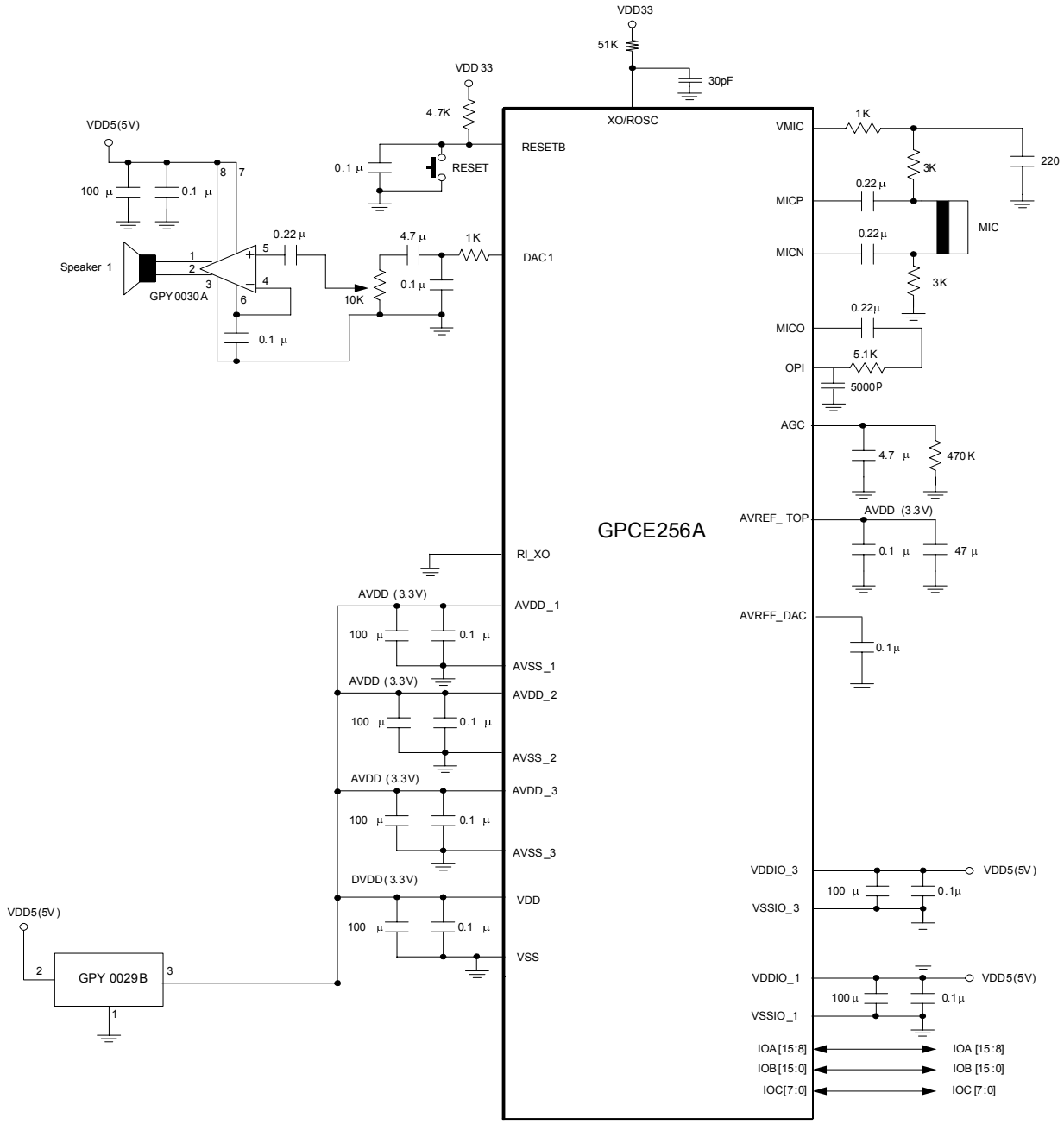
8.1. Application Circuit 1 (with Crystal, DAC Output)



GPCE256A Application Circuit audio amplifier with Crystal and DAC output

Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.2. Application Circuit 2 (with R-oscillator, DAC Output)



GPCE256A Application Circuit audio amplifier with R -oscillator and DAC output

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPCE256A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 02, 2013	1.3	Add COMAIR logo to the cover page	
NOV. 02, 2009	1.2	1. Modify 3.FEATURES. 2. Modify 7.2 DC Characteristics.	3 14
JUL.17, 2007	1.1	1. Modify the “Application Circuit 1 (with Crystal, DAC Output)” in section 8.1. 2. Modify the “Application Circuit 2 (with R-oscillator, DAC Output)” in section 8.2.	16 17
FEB. 26, 2007	1.0	1. Modify the “FEATURES” to section 3. 2. Add “ELECTRICAL SPECIFICATIONS” to section 7.	3 13
DEC. 05, 2006	0.1	Preliminary version.	17