DATA SHEET

GPCDXLXXXA

Multi-Channel Sound Controller with DC-DC Booster

Jun 18, 2013

Version 1.1

Table of Contents

PAGE

MULTI-CHANNEL SOUND CONTROLLER WITH DC-DC BOOSTER

1.GENERAL DESCRIPTION

The GPCDXLXXXA features an internal ROM, 512-byte working SRAM, three 12-bit timers, 24 general I/Os with multi-channel input and one 14-bit DAC with amplifier. The microprocessor implements software based on audio processing, functional control and others. For audio processing, melody and speech can be mixed into one output. The GPCDXLXXXA is featured maximum two sets software channel and a high performance SPU voice engine to play voice with ADPCM/PCM data. It is designed for wide input voltage range (1.0V~3.6V), and the circuit works at a programmable pumped voltage (3.0V~4.5V). In addition, GPCDXLXXXA features sleep mode for power savings. It can be awakened from sleep mode by interrupt sources or changing IO's state. There is also a Serial Peripheral Interface (SPI) controller built-in GPCDXLXXXA to facilitate communication with other devices and components.

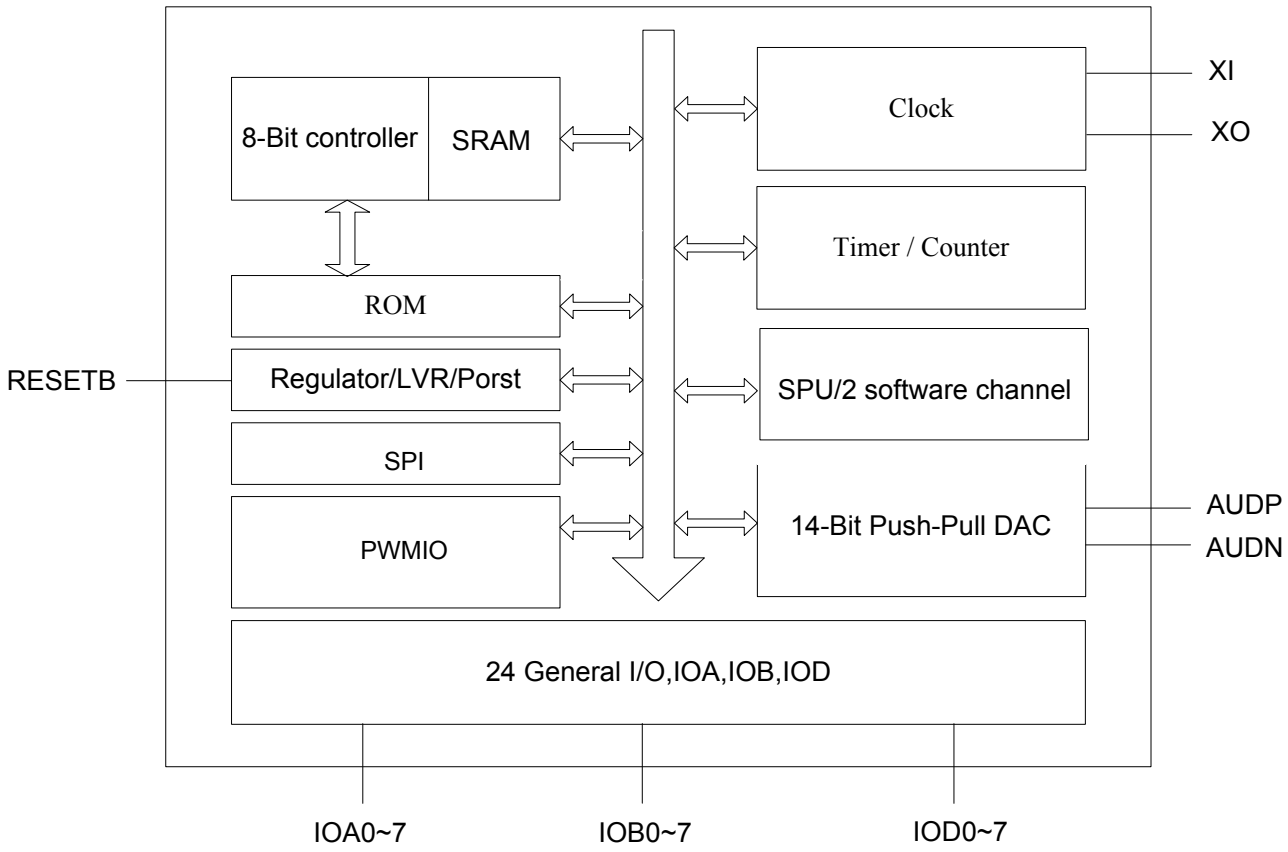
2.FEATURES

- Input Voltage: 1.0V ~ 3.6V
- Programmable pumped voltage:
  One-battery selected: 3.3V ~ 4.2V
  Two-battery selected: 3.3V ~ 4.5V
- CPU speed: Max. 8MHz
- F_{OSC} = Max. 16MHz (2 x CPU clock)
- RAM size: Max. 512 bytes
- Three 12-bit timer/counter, TMA with capture and comparison function, TMB/ TMC with comparison function only (Programmable and Auto Reload)
- Clock source with ROSC or XTAL (option)
- Sleep mode to reduce power consumption
- Key change wake-up function
- IRQs & NMI interrupts
- Watchdog function (option)
- 3.0V regulator output
- Low Voltage Reset
- 24 bit-programmable general I/Os
- Eight I/Os with high sink current for LED application
- All general IOs with 1M pull-low function to prevent current leakage from error key touch
- One 14-bit DAC with amplifier for direct drive speaker
- SPU (Sound Processing Unit) engine can output audio data with 14-bit resolution to perform high quality voice/melody
- IR PWM Output
- Hardware PWMIO supports four LED outputs with 256-level brightness control
- Real-time clock
- Multi-channel SPU engine with ADPCM/PCM wavetable
- Maximum two sets of 14-bit software channel with noise filter to play high quality sound
- SPI master interface
- Built-in Battery Voltage Detect (BVD) / Low Voltage Detect (LVD) function

3.APPLICATION FIELD

- Talking instrument controller
- General music synthesizer
- General purpose controller
- High end toy controller
- Intelligent education toys
- And more

4.BLOCK DIAGRAM



5. GPCDXLXXXA FAMILY AND DIFFERENT FEATURES LIST

Body	ROM size	SPU Channel	Software Channel
GPCD9L340A	1MB	8	1
GPCD9L300A	912KB	8	1
GPCD9L270A	832KB	8	1
GPCD9L220A	672KB	8	1
GPCD6L340A	1MB	4	2
GPCD6L300A	912KB	4	2
GPCD6L270A	832KB	4	2
GPCD6L220A	672KB	4	2
GPCD3L340A	1MB	1	2

6. SIGNAL DESCRIPTIONS

6.1. Signal Description for GPCDXLXXXA

Mnemonic	Type	Description	Note
IO PORT			
IOA7-0	I/O	Bi-directional IO ports, can be wakeup pins	IOA3-0 high sink
IOB7-0	I/O	Bi-directional IO ports, can be wakeup pins	IOB3-0 high sink
IOD7-0	I/O	Bi-directional IO ports, can be wakeup pins	
Clock related			
XO	O	Oscillator crystal output	Keep floating at ROSC mode
XI	I	Oscillator crystal input/ROSC input	
Power/Ground PAD			
VDD_IN	P	Power from battery (1.0V~3.6V)	
VSS_IN	G	Ground reference for battery	
VDD_DCO1,VDD_DCO2	P	Power output from DC-DC booster (3.3V~4.5V)	VDD_DCO1, VDD_DCO2 are shorted on PCB
VSS_DC1,VSS_DC2	G	Ground reference for DC-DC booster output	VSS_DC1, VSS_DC2 are shorted on PCB
VDD_RGO	P	regulator power output (3.0V)	For core power
VDD_RGI	P	regulator power input	Connect to VDD_DCO1/VDD_DCO2
VDD_IO	P	Power for all IO ports (3.3V~4.5V)	VDD_IO cannot be smaller than VDD_CORE
VSS_IO	G	Ground reference for all IO ports	
VDD_CORE	P	Power for core circuit	Connect to VDD_RGO
VSS_CORE	G	Ground reference for core circuit	
VDD_DAC	P	Power for DAC	Connect to VDD_DCO1/VDD_DCO2
VSS_DAC	G	Ground reference for DAC	
VDD_AMP	P	Power for audio amplifier	Connect to VDD_DCO1/VDD_DCO2
VSS_AMP	G	Ground reference for audio amplifier	
VDD_DRV	P	Power for audio output driver	Connect to VDD_DCO1/VDD_DCO2
VSS_DRV	G	Ground reference for audio output driver	
Others			
RESETB	I	External reset pin (active low)	Internal pull-high
TEST	I	For Generalplus test mode. NC for normal application.	Internal pull-low
LX1	I	inductor connection for DC-DC (1st group)	
LX2	I	inductor connection for DC-DC (2nd group)	
AUDP	O	Audio output-P	
AUDN	O	Audio output-N	
MICIN	I	Line-In / Microphone input	

7. FUNCTIONAL DESCRIPTIONS

7.1. SRAM

The 512-byte SRAM (including Stack) area is located in $000000~$0002FF.

7.2. ROM

GPCDXLXXXA is capable of accessing internal 1MB ROM. The ROM size is depicted in following table:

Body	ROM Size	ROM Address
GPCD9L340A	1MB	0x00840~0xFFFFF
GPCD9L300A	912KB	0x00840~0xE3FFF
GPCD9L270A	832KB	0x00840~0xCFFFF
GPCD9L220A	672KB	0x00840~0xA7FFF
GPCD6L340A	1MB	0x00840~0xFFFFF
GPCD6L300A	912KB	0x00840~0xE3FFF
GPCD6L270A	832KB	0x00840~0xCFFFF
GPCD6L220A	672KB	0x00840~0xA7FFF
GPCD3L340A	1MB	0x00840~0xFFFFF

7.3. Low Voltage Reset

The GPCDXLXXXA provides another important feature - Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR level.

7.4. Interrupt

The GPCDXLXXXA has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls fifteen IRQs and seven NMIs. A NMI cannot be interrupted by any other IRQs.

7.5. Hardware PWMIO

Hardware PWMIO supports four LED outputs from IOB0~3(or IOA0~3) with brightness control of 256 levels. The clock source of PWMIO can be selected by user's request.

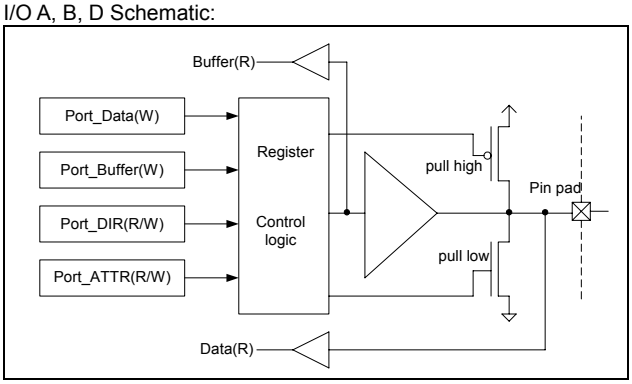
7.6. I/O

The purpose of input and output port is to communicate with other devices. Maximum 24 programmable I/O ports are built-in for GPCDXLXXXA, including Port A, B and D. All ports are general I/Os with programmable wake-up capability. In addition, these ports also provide some special functions in certain pins. Please refer to following figure for more information about **IO Sharing**.

7.6.1. I/O Configuration

The following diagram represents the I/O schematic.

I/O A, B, D Schematic:



Port_Data and Port_Buffer are written into the same register but reading from different node. To activate key wakeup function, user should latch data on IOX_Data and enable the key wakeup function. Wakeup is triggered when the port's state is different from the latched data.

A summary of IO sharing is listed as following.

IO Sharing

	IOA								IOB							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
High sink					V	V	V	V					V	V	V	V
PWMIO													V	V	V	V
IR(Output)									V							
External INT										V						
External Clock		V(TMC)	V(TMB)	V(TMA)												
RTC											V	V				
IIS out/in	V(in)	V(in)	V(in)			V(out)	V(out)	V(out)								
QD					V(qd2)	V(qd2)	V(qd1)	V(qd1)								
CC		TMC	TMB	TMA						TMC	TMB	TMA				
1M pull low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

	IOD							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Wake up	V	V	V	V	V	V	V	V
SPI					V(rx)	V(tx)	V(ck)	V(cs)
1M pull low	V	V	V	V	V	V	V	V

***Note: QD means quadrature decoder, CC means Capture/Comparison.**

7.7. Timer/Counter (Timer A/Timer B/Timer C)

Three 12-bit timers are embedded in GPCDXLXXXA: Timer A, Timer B and Timer C. These timers all have a 12-bit up counter, a preloaded register, and programmable clock sources. Timer A/B can also be the clock source of the software channel. The clock source of each timer can be set individually. Two clock sources including CPU clock and external clock can be selected individually or their combination to be timer's clock source. Besides, capture and comparison function are supported by TMA. Comparison is supported by TMB and TMC.

7.8. Sleep, Wakeup and Watchdog

7.8.1. Sleep and Wakeup

Sleep mode saves power by stopping clock while device is not in use. When entering into sleep mode, the device runs from operating mode to standby mode. Wake-up from sleep mode is to turn back to operating mode.

1) Sleep: after power-on reset, IC starts working until a sleep command is given. When a sleep signal is accepted, IC will turn off system clock and enter into sleep mode.

2) Wake-up: while a wakeup source is generated, GPCDXLXXXA wakes up from sleep mode. While wake-up is completed, program counter will continue to execute the next command.

7.8.2. Watchdog

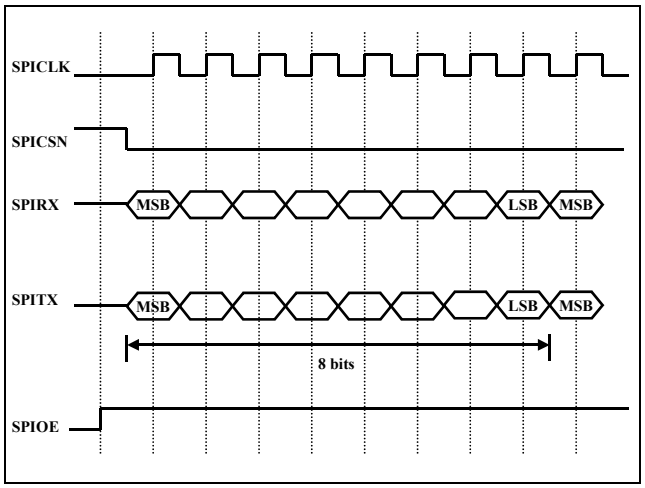
If the watchdog function is enabled, a reset signal is generated to reset system when watchdog counter is overflow.

7.9. Speech and DAC

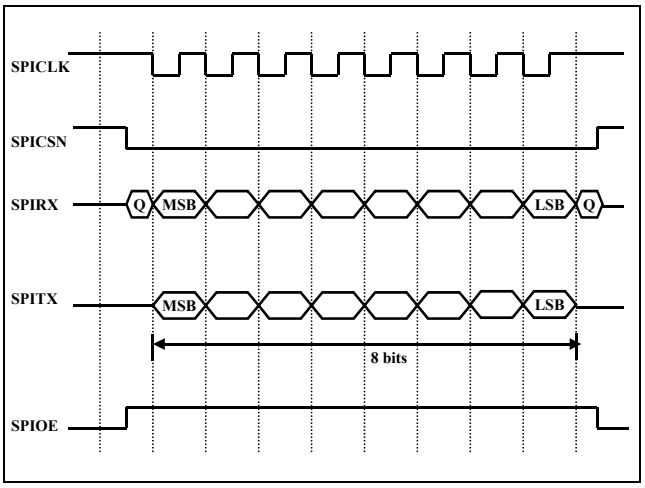
The GPCDXLXXXA uses a high performance SPU voice engine to achieve multi-channel voice with ADPCM/PCM. A hardware multiplier is also embedded in this SPU for software usage. Moreover, there is maximum two sets 14-bit DAC with amplifier for direct audio output.

7.10. SPI Controller

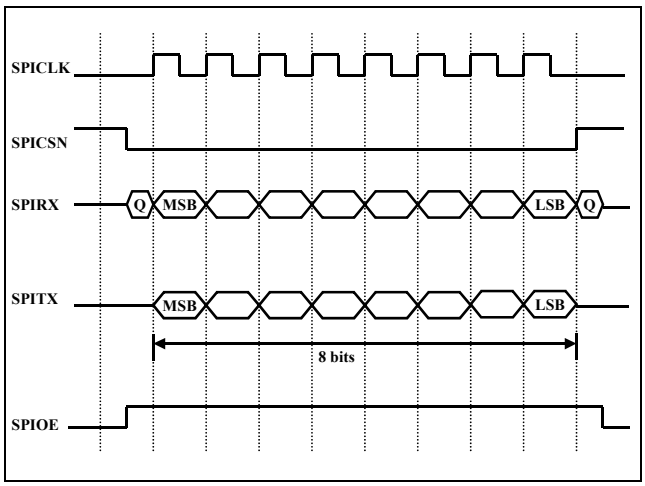
A Serial Peripheral Interface (SPI) controller is built in GPCDXLXXXA to facilitate communication with other devices and components. There are four control signals on SPI: SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO); these four signals are shared with PortD0, PortD1, PortD2, and PortD3. While SPI module is enabled by corresponding control bits, these four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of timing are presented as follows:



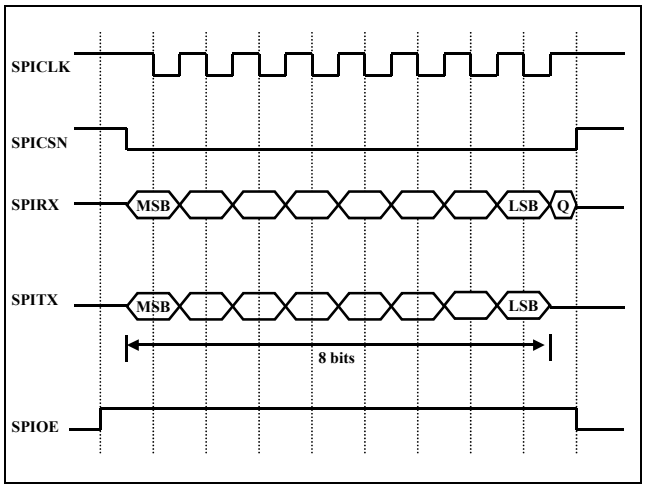
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 1, SPH=1



Master Mode, SPO = 0, SPH=1



Master Mode, SPO = 1, SPH=0

7.11. DC-DC Booster

The GPCDXLXXXA can be supplied wide input voltage (1.0V~3.6V) and work with a programmable pumped voltage. Inside the chip, it is implemented a group of high efficient DC-DC booster circuit. The DC-DC booster circuit pumps input voltage to 3.3V~4.5 that supplies chip as working voltage.

7.12. Battery Voltage Detect / Low Voltage Detect

The GPCDXLXXXA is built-in Battery Voltage Detect (BVD) function. The battery voltage level can be read back by program. Furthermore, user can set low voltage level and get the Low Voltage Detect (LVD) flag by program.

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see DC Electrical Characteristics.

8.2. AC Characteristics (TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC}	-	-	16.0	MHz	VDD_IN = 1.0V - 3.6V

8.3. Power Characteristics

8.3.1. One battery selected, TA = 25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.) *	VDD_IN	1.0	-	-	V	I(VDD_DCO)=80mA@VDD_DCO=3.3V I(VDD_DCO)=30mA@VDD_DCO=4.2V L=15uH/0.5W (Color Code Inductance)
Input Voltage (Max.)	VDD_IN	-	-	1.8	V	
Operating Voltage** (pump voltage)	VDD_DCO	3.3	-	4.2	V	
Operating Current-1	I_{OP-1}	-	20	-	mA	VDD_IN=1.5V, VDD_DCO=3.3V F_{CPU} = 8MHz , DAC on, no load
		-	30	-	mA	VDD_IN=1.5V, VDD_DCO=4.2V F_{CPU} = 8MHz , DAC on, no load
Operating Current-2	I_{OP-2}	-	13	-	mA	VDD_IN=1.5V, VDD_DCO=3.3V F_{CPU} = 8MHz , DAC off, no load
		-	20	-	mA	VDD_IN=1.5V, VDD_DCO=4.2V F_{CPU} = 8MHz , DAC off, no load
Standby Current	I_{STBY}	-	-	5.0	μA	VDD_IN = 1.5V

*As I(VDD_DCO) is greater than the value of test condition; VDD_DCO can be observed voltage drop.

**VDD_DCO is the pumped voltage. It is greater than or equal to input voltage. It is possible to be lower with heavy loading under operating.

8.3.2. Two battery selected, TA = 25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.) *	VDD_IN	1.3	-	-	V	I(VDD_DCO)=40mA@VDD_DCO=3.3V I(VDD_DCO)=15mA@VDD_DCO=4.5V L=15uH/0.5W (Color Code Inductance)
Input Voltage (Max.)	VDD_IN	-	-	3.6	V	
Operating Voltage**	VDD_DCO	3.3	-	4.5		
Operating Current-1	I_{OP-1}	-	10	-	mA	VDD_IN=3.0V, VDD_DCO=3.3V F_{CPU} = 8MHz , DAC on, no load
		-	15	-	mA	VDD_IN=3.0V, VDD_DCO=4.5V F_{CPU} = 8MHz , DAC on, no load

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current-2	I_{OP-2}	-	6	-	mA	VDD_IN=3.0V, VDD_DCO=3.3V F_{CPU} = 8MHz , DAC off, no load
		-	9	-	mA	VDD_IN=3.0V, VDD_DCO=4.5V F_{CPU} = 8MHz , DAC off, no load
Standby Current	I_{STBY}	-	-	10.0	μA	VDD15 = 3.0V

*As I(VDD_DCO) is larger than the value of test condition; VDD_DCO can be observed voltage drop.

**VDD_DCO is the pumped voltage. It is greater than or equal to input voltage. It is possible to be lower with heavy loading under operating.

8.4. Regulator Characteristics (TA=25℃)

Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Input Voltage	VDD_RGI	2.3	-	5.5	V	
Maximum Current Output	I_{VDD_RGO}	-	-	30	mA	
Output Voltage*	VDD_RGO	2.7	-	3.3	V	VDD_RGI > 3.0V*

*As VDD_RGI is smaller than 3.0V+△V, V_{VDD_RGO}=VDD_RGI-△V (△V ~ 0.1V-0.4V as I_{VDD_RGO}=30mA)

8.5. DC Characteristics

8.5.1. VDD_IO=3.3V, TA=25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input High Level	V_{IH}	0.7*VDD_IO	-	VDD_IO	V	-
Input Low Level	V_{IL}	VSS_IO	-	0.3*VDD_IO	V	-
Output High Current (IOA[7:0]/IOB[7:0]/IOD[7:0])	I_{OH}	-	6	-	mA	VDD_IO =3.3V, V_{OH} =0.7*VDD_IO
Output Low Sink Current (IOA[7:4]/IOB[7:4]/IOD[7:0])	I_{OL1}	-	9	-	mA	VDD_IO =3.3V, V_{OL} =0.3*VDD_IO
Output Low Sink Current (IOA[3:0]/IOB[3:0])	I_{OL2}	-	18	-	mA	VDD_IO =3.3V, V_{OL} =0.3*VDD_IO
Input Pull-Low Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PL}	-	100	-	Kohm	VDD_IO =3.3V, V_{in} =VDD_IO
High Input Pull-Low Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PL2}	-	850	-	Kohm	VDD_IO =3.3V, V_{in} =VDD_IO
Input Pull-High Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PH}	-	100	-	Kohm	VDD_IO =3.3V, V_{in} =VSS_IO

8.5.2. VDD_IO =4.5V, TA=25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input High Level	V_{IH}	0.7*VDD_IO	-	VDD_IO	V	-
Input Low Level	V_{IL}	VSS_IO	-	0.3*VDD_IO	V	-
Output High Current (IOA[7:0]/IOB[7:0]/IOD[7:0])	I_{OH}	-	10	-	mA	VDD_IO =4.5V, V_{OH} =0.7*VDD_IO
Output Low Sink Current (IOA[7:4]/IOB[7:4]/ IOD[7:0])	I_{OL1}	-	16	-	mA	VDD_IO =4.5V, V_{OL} =0.3*VDD_IO

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output Low Sink Current (IOA[3:0]/IOB[3:0])	I_{OL2}	-	31	-	mA	VDD_IO =4.5V, V_{OL} =0.3*VDD_IO
Input Pull-Low Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PL1}	-	100	-	Kohm	VDD_IO =4.5V, V_{in} =VDD_IO
High Input Pull-Low Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PL2}	-	850	-	Kohm	VDD_IO =4.5V, V_{in} =VDD_IO
Input Pull-High Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PH}	-	100	-	Kohm	VDD_IO =4.5V, V_{in} =VSS_IO

8.6. DAC Characteristics

8.6.1. One battery selected, VDD_IN=1.5V VDD_DCO=3.3V, R_L=8Ω, f=1KHz, TA=25℃

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	Bit
THD+n (3.3V@0.175W)	-	-	0.4	-	%
Noise at No Signal	-	-	-84	-	dBr A
Dynamic Range(-60dB)	-	-	-78	-	dBr A

8.6.2. Two battery selected, VDD_IN=3.0V VDD_DCO=4.5V, R_L=8Ω, f=1KHz, TA=25℃

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	Bit
THD+n (4.5V@0.35W)	-	-	0.3	-	%
Noise at No Signal	-	-	-84	-	dBr A
Dynamic Range(-60dB)	-	-	-75	-	dBr A

8.7. Pump Efficiency

8.7.1. One battery selected, VDD_IN=1.5V, T_A = 25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency (L=15uH/0.5W)	Eff.	-	80	-	%	I(VDD_DCO)=30mA; VDD_DCO=3.3V
		-	70	-	%	I(VDD_DCO)=100mA; VDD_DCO=3.3V

*Use Color Code Inductance

8.7.2. Two battery selected, VDD_IN=3.0V, T_A = 25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency (L=15uH/0.5W)	Eff.	-	81	-	%	I(VDD_DCO)=50mA; VDD_DCO=4.5V
		-	75	-	%	I(VDD_DCO)=200mA; VDD_DCO=4.5V

*Use Color Code Inductance

8.8. VDD_IN v.s. Supplied Current (I(VDD_DCO))

8.8.1. One battery selected, TA = 25℃

VDD_IN (V)	I(VDD_DCO) (mA)	Condition
1.0	80	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)
1.2	130	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)
1.5	200*	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)

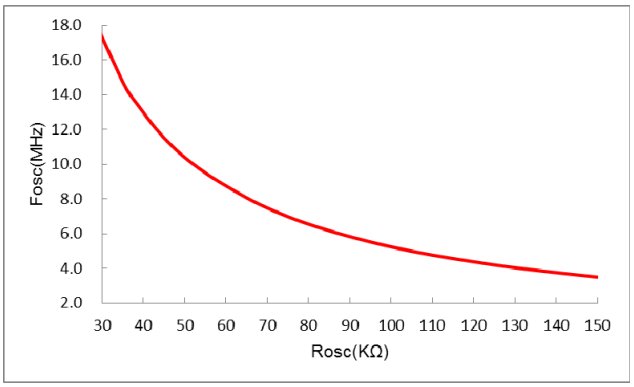
*The max measured current of I(VDD_DCO) is 200mA only.

8.8.2. Two battery selected, TA = 25℃

VDD_IN (V)	I(VDD_DCO) (mA)	Condition
1.5	10	VDD_DCO=4.5V ; L=15uH/0.5W (Color Code Inductance)
2.4	200*	VDD_DCO=4.5V ; L=15uH/0.5W (Color Code Inductance)

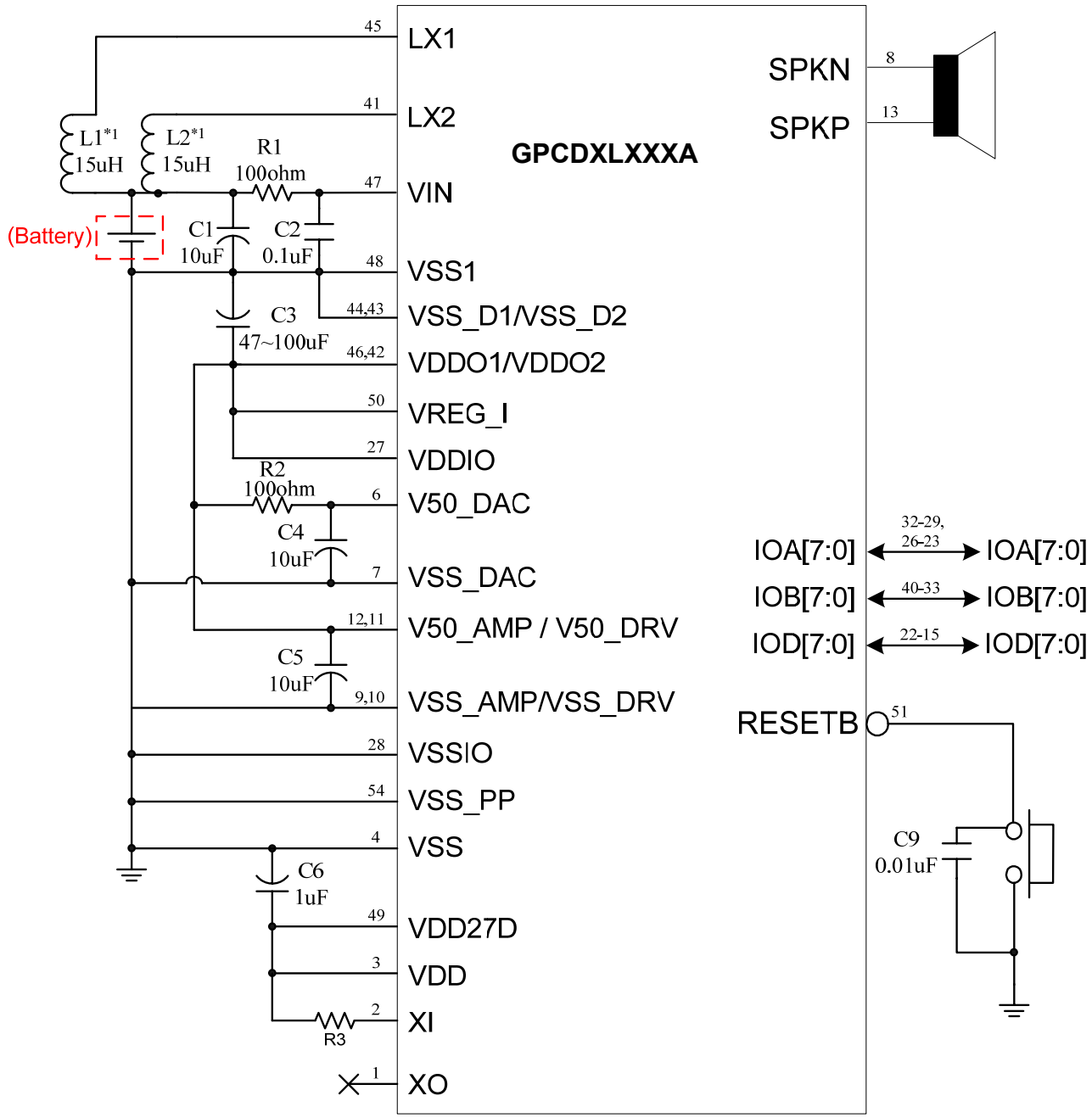
*The max measured current of I(VDD_DCO) is 200mA only.

8.9. The Relationship between R_{osc} and F_{osc} (TA=25℃)



9.APPLICATION CIRCUITS

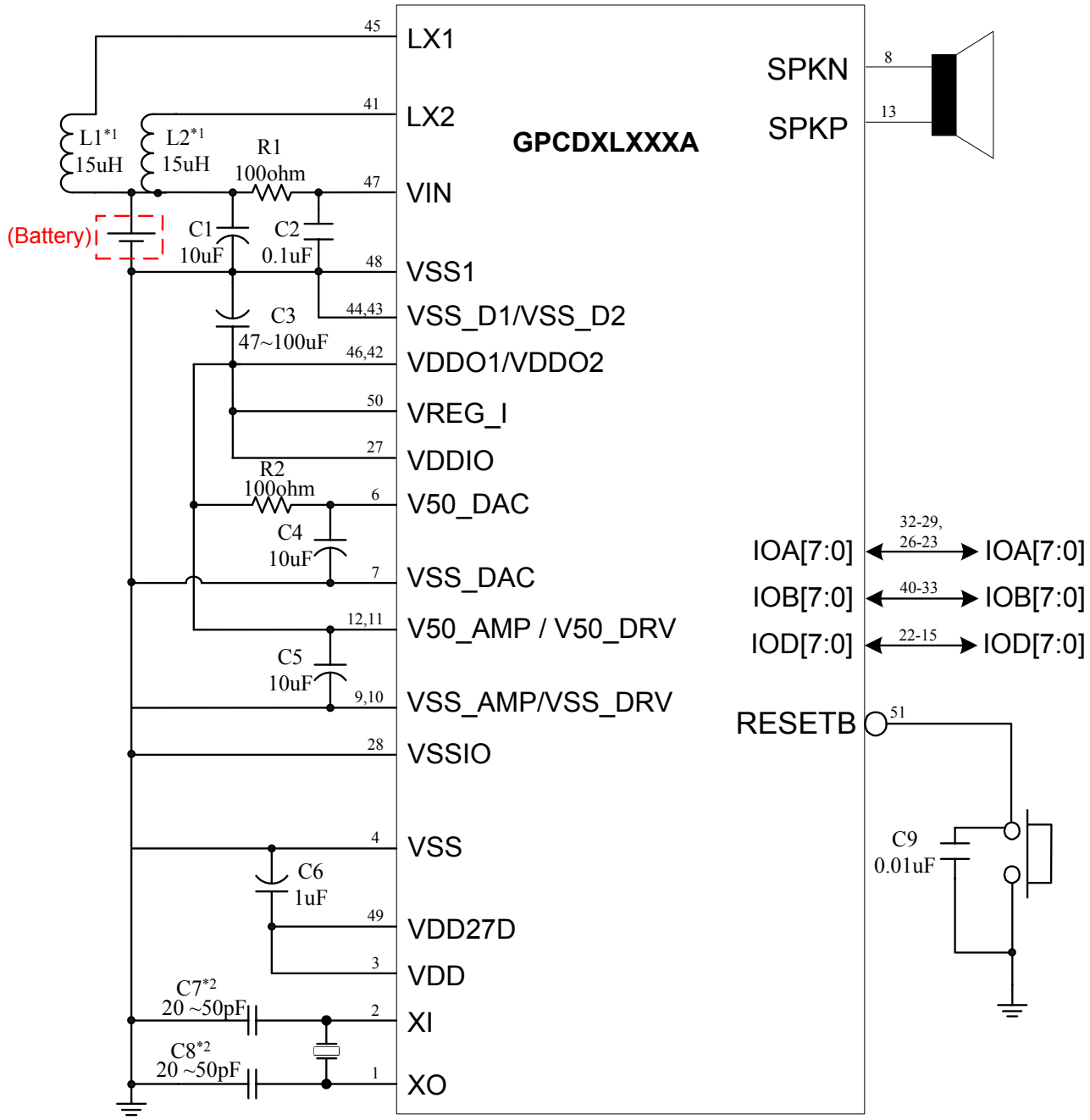
9.1. GPCDXLXXXA Application Circuit with R_{OSC}-Mode



Note:

1. L1 and L2 should be as close as to VDD_IN/LX1/LX2 as possible. Please use inductance with lower resistance to gain higher efficiency. **15uH/0.5W@IDC(max)>250mA, ESR<1.5ohm is recommended.**
2. The value of C3 is dependent on the loading of application. Generally, 47uF should be enough. C3 should be as close as possible to VDD_DCO1/VDD_DCO2.
3. C4 should be as close as possible to VDD_DAC/VSS_DAC.
4. C5 should be as close as possible to VDD_AMP/VDD_DRV and VSS_AMP/VSS_DRV.
5. The capacitance of C9 can not be large than 0.01uF.

9.2. GPCDXLXXXA Application Circuit with XTAL-Mode



Note:

1. L1 and L2 should be as close as to VDD_IN/LX1/LX2 as possible. Please use inductance with lower resistance to gain higher efficiency. **15uH/0.5W@IDC(max)>250mA, ESR<1.5ohm is recommended.**
2. The values of C7/C8 are for design guidance only; different values may be needed for different crystal/resonator used.
3. The value of C3 is dependent on the loading of application. Generally, 47uF should be enough. C3 should be as close as possible to VDD_DCO1/VDD_DCO2.
4. C4 should be as close as possible to VDD_DAC/VSS_DAC.
5. C5 should be as close as possible to VDD_AMP/VDD_DRV and VSS_AMP/VSS_DRV.
6. The capacitance of C9 can not be large than 0.01uF.

10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPCDXLXXXA-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page
Jun 18, 2013	1.1	Add “GPCD3L340A”.	5,7
May 23, 2013	1.0	Original	18