DATA SHEET

GPC3XXXAx/Bx/Cx/Dx

3-channel Sound Controller

Aug. 28, 2017

Version 2.3

Table of Contents

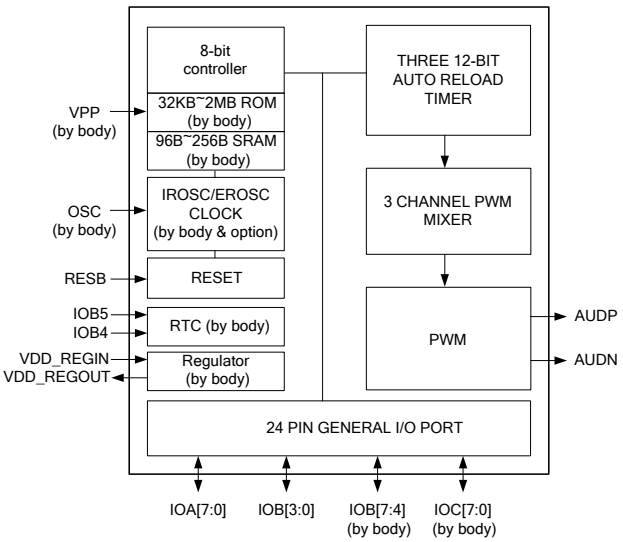
PAGE

3-CHANNEL SOUND CONTROLLER

1. GENERAL DESCRIPTION

The GPC3XXXAx/Bx/Cx/Dx is embedded with an 8-bit processor, 32K~2M bytes ROM or OTP ROM (by body), 96~256 bytes SRAM, three 12-bit timer/counters, 12~24 general I/Os, a 3-channel mixer, a pair of 12-bit PWM outputs and a real time clock (by body). In audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range and has a Low Voltage Reset function and a sleep mode to save more power. It can be awakened from sleep mode by interrupt sources or IO's state changes. GPC3XXXAx/Bx/Cx/Dx is one of the most suitable speech engines in the industry for vocal applications.

2. BLOCK DIAGRAM



3. FEATURES

■ Wide Operating Voltage: 2.0V/2.1V * - 5.5V (by body)

***** The lowest operating voltage depends on LVR (Low Voltage Reset) level. Typical LVR voltage is 2.0V/2.1V (by body), but with +/- 0.1V deviation possibility

■ Working Voltage with 6MHz system clock: 2.2V ** - 5.5V

Working Voltage with 8MHz system clock: 2.4V ** - 5.5V

****** The system clock would start to slow down at lowest working voltage (6MHz at 2.2V, 8MHz at 2.4V); please refer to the Frequency vs. VDD curve on page 16 and page 17

■ ROM size: 32K~2M bytes (by body option)

■ RAM size: 96 ~256 bytes (by body option)

■ Built-in internal or external RC oscillator (by body option)

■ Built-in internal RC oscillator 8MHz or 6MHz(code option)

■ Approx. 10~680 seconds speech @6KHz sampling rate with 4-bit ADPCM (by body option)

■ Standby mode (Clock Stop mode) for power savings. Max. 2.0uA ~ 5.0uA @ 4.5V (by body option)

■ Bit programmable 12~24 general I/Os(by body option)

■ Four I/Os with high sink current for LED application

■ All general IOs provide 1M pull-low function to prevent current leakage while pressing the key (IOs to VDD)

■Three 12-bit timer/counters

■ Seven or eight IRQs & 1 NMI interrupt (by body option)

■ Two or three wake-up sources (by body option)

■ Feedback function (by body option)

■ Low Voltage Reset (LVR) function

■ Watchdog function

■ IR function

■ RTC function (by body option)

■ Four sets of hardware PWMIO supporting LED outputs with brightness control of 256-level

■ A 3-channel mixer with melody or ADPCM/PCM input

■ A pair of PWM outputs with volume control

4. APPLICATION FIELD

■ Talking instrument controller

■ General music synthesizer

■ High-end toy controller

■ Intelligent education toys

■ And more

5. GPC3XXXAx/Bx/Cx/Dx FAMILY AND FEATURE LIST

Body	GPC3680A	GPC3540A	GPC3480A	GPC3420A	GPC3341A	-
Voice Duration	680 Sec.	540 Sec.	480 Sec.	420 Sec.	340 Sec.	-
Working Voltage	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.1~5.5V	2.0~5.5V	-
RAM Size	128B	128B	128B	128B	128B	-
ROM Size	2MB	1632KB	1440KB	1280KB	1024KB(OTP)	-
Clock Source	IROSC	IROSC	IROSC	IROSC	IROSC	-
IO Pin	24 (IOA/B/C)	24 (IOA/B/C)	24 (IOA/B/C)	24 (IOA/B/C)	24 (IOA/B/C)	-
High sink IO	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]	-
Hardware PWMIO	V	V	V	V	V	-
IR	V	V	V	V	V	-
RTC	V	V	V	V	V	-
PWM Volume control	V	V	V	V	V	-
Feedback function	X	X	X	X	X	-
IRQ Interrupt	8	8	8	8	8	-
NMI interrupt	1	1	1	1	1	-
Wakeup source	3	3	3	3	3	-
Body	**GPC3340A/B**	**GPC3256A/B**	**GPC3340C/D**	**GPC3256C**	**GPC3170A/B/A1/ B1**	**GPC3120A/B/A1**
Voice Duration	340 Sec.	256 Sec.	340 Sec.	256 Sec.	170 Sec.	120 Sec.
Working Voltage	2.0~5.5V	2.0~5.5V	2.0~5.5V	2.0~5.5V	2.0~5.5V	2.0~5.5V
RAM Size	128B	128B	128B	128B	128B	128B
ROM Size	1024KB	768KB	1024KB	768KB	512KB	384KB
Clock Source	IROSC	IROSC	IROSC	IROSC	IROSC	IROSC
IO Pin	24 (IOA/B/C)	24 (IOA/B/C)	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)
High sink IO	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]
Hardware PWMIO	V	V	V	V	V	V
IR	V	V	V	V	V	V
RTC	V	V	V	V	V	V
PWM Volume control	V	V	V	V	V	V
Feedback function	X	X	X	X	X	X
IRQ Interrupt	8	8	8	8	8	8
NMI interrupt	1	1	1	1	1	1
Wakeup source	3	3	3	3	3	3

Note1: Only 1M Ohm pull low R is available on IOA[7:0] for **GPC3340B~GPC3092B, GPC3340D, and GPC3170B1.**

Body	GPC3106A/B/A1	GPC3092A/B/A1	GPC3080A	GPC3072A	GPC3063A	GPC3052A
Voice Duration	106 Sec.	92 Sec.	80 Sec.	72 Sec.	63 Sec.	52 Sec.
Working Voltage	2.0~5.5V	2.0~5.5V	2.0~5.5V	2.0~5.5V	2.0~5.5V	2.0~5.5V
RAM Size	128B	128B	128B	128B	128B	128B
ROM Size	320KB	288KB	256KB	224KB	192KB	160KB
Clock Source	IROSC	IROSC	IROSC	IROSC	IROSC	IROSC
IO Pin	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)
High sink IO	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]
Hardware PWMIO	V	V	V	V	V	V
IR	V	V	V	V	V	V
RTC	V	V	V	V	V	V
PWM Volume control	V	V	V	V	V	V
Feedback function	X	X	X	X	X	X
IRQ Interrupt	8	8	8	8	8	8
NMI interrupt	1	1	1	1	1	1
Wakeup source	3	3	3	3	3	3
Body	**GPC3040A/B**	**GPC3030A/B**	**GPC3026A/B**	**GPC3010A**	**GPC3011C**	**GPC3010C**
Voice Duration	40 Sec.	30 Sec.	26 Sec.	10 Sec.	10 Sec.	10 Sec.
Working Voltage	2.0~5.5V	2.0~5.5V	2.0~5.5V	2.0~5.5V	2.0~5.5V	2.0~5.5V
RAM Size	96B	96B	96B	128B	256B	256B
ROM Size	128KB	96KB	80KB	32KB	32KB(OTP)	32KB
Clock Source	IROSC	IROSC	IROSC	IROSC	IROSC/EROSC	IROSC/EROSC
IO Pin	12 (IOA/B[3:0])	12 (IOA/B[3:0])	12 (IOA/B[3:0])	16 (IOA/B)	16 (IOA/B)	16 (IOA/B)
High sink IO	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]	IOB[3:0]
Hardware PWMIO	V	V	V	V	V	V
IR	V	V	V	V	V	V
RTC	X	X	X	X	X	X
PWM Volume control	V	V	V	V	V	V
Feedback function	X	X	X	RC/XTAL	RC/XTAL	RC/XTAL
IRQ Interrupt	7	7	7	7	7	7
NMI interrupt	1	1	1	1	1	1
Wakeup source	2	2	2	2	2	2

6.SIGNAL DESCRIPTIONS

6.1. Signal Descriptions for GPC3680A~ GPC3026A, GPC3340B~ GPC3092B, GPC3040B~ GPC3026B, GPC3340C/D, GPC3256C, GPC3170A1~ GPC3092A1, GPC3170B1

PIN Name	Type	Description
IO Port		
IOA[7：0]	I/O	IOA[7：0] is a bi-directional I/O port, can be software programmed as wakeup I/O. 1Mohm || 100Kohm feedback pull low resistor (only 1M ohm feedback pull low resistor is available for **GPC3340B~GPC3092B , GPC3340D, GPC3170B1**) IOA7 shares its pad with IR output IOA1 shares its pad with external clock input IOA0 shares its pad with external interrupt input
IOB[7：0]	I/O	IOB[7：0] is a bi-directional I/O port, can be software programmed as wakeup I/O. 1Mohm || 100Kohm feedback pull low resistor IOB5 shares its pad with XTAL 32KHz input IOB4 shares its pad with XTAL 32KHz output IOB[3：0] shares its pad with 256-level PWM output, high sink current **IOB[7：4] is NOT available for GPC3040A/B~GPC3026A/B**
IOC[7：0]	I/O	IOC[7：0] is a bi-directional I/O port, can be software programmed as wakeup I/O. 1Mohm || 100Kohm feedback pull low resistor **IOC[7：0] is NOT available for GPC3170A~GPC3026A, GPC3170B~GPC3092B, GPC3040B~GPC3026B, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1.**
Power & Ground PAD		
CVDD	P	Power supply voltage input for internal circuit
CVSS	G	Ground reference for internal circuit
VDDIO	P	Power supply voltage input for GPIO PAD, must be equal to CVDD
VSSIO	G	Ground reference for GPIO PAD
PVDD	P	PWM driver power, can be greater than or equal to CVDD & VDDIO **(refer to Note3 and Note4）**
PVSS	G	PWM driver ground reference
Others		
RESB	I	System reset input, low active (with pull high)
TEST	I	Test pin input, high active (with pull low), and please DON'T bond the TEST pin.
AUDP、AUDN	O	PWM output

Total: 34 pins

Legend: I = Input　O = Output　P = Power　G = Ground

Note1: To ensure IC functions properly, please bond all of VDD and VSS pins.
Note2: CVDD must be equal to VDDIO.
Note3: PVDD can be greater than or equal to CVDD & VDDIO for GPC3680A~GPC3052A, GPC3340B~GPC3092B, GPC3040B~GPC3026B, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1.
Note4: PVDD must be equal to CVDD & VDDIO for GPC3040A~GPC3026A.
Note5: Please DO NOT bond TEST pin.
Note6: IOC[7：0] is NOT available for GPC3170A/B~GPC3026A/B, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1.
Note7: IOB[7：4] is NOT available for GPC3040A/B~GPC3026A/B.
Note8: Only 1Mohms pull low resistor is available on IOA[7：0] for GPC3340B~GPC3092B, GPC3340D, GPC3170B1.

6.2. Signal Descriptions for GPC3341A

PIN Name	Type	Description
IO Port		
IOA[7：0]	I/O	Bi-directional I/O port, can be software programmed as a wake-up I/O. 1Mohm || 100K feedback Pull Low resistor IOA7 shares its pad with IR Output, IOA3 shares its pad with SDA in serial programming cycle. IOA2 shares its pad with SCK in serial programming cycle. IOA1 shares its pad with External Clock Input. IOA0 shares its pad with External Interrupt Input.
IOB[7：0]	I/O	Bi-directional I/O port, can be software programmed as a wake-up I/O. 1Mohm || 100K feedback Pull Low resistor. IOB5 shares its pad with XTAL 32KHz Input. IOB4 shares its pad with XTAL 32KHz Output. IOB[3：0] shares its pad with 256-level PWM Output, high sink current.
IOC[7：0]	I/O	Bi-directional I/O port, can be software programmed as a wake-up I/O. 1Mohm || 100K feedback Pull Low resistor
Power & Ground PAD		
VDD_REGOUT	O	Regulator output pin
VDD_REGIN	P	Regulator input pin
CVSS	G	Ground reference
VPP	P	High voltage during programming, NC at the normal run
VDDIO	P	Power supply voltage input
VSSIO	G	Ground reference
PVDD	P	PWM driver power
PVSS	G	PWM driver ground reference
Others		
RESB	I	System reset input, low active with pull-high
EPM	I	Program control pin, NC at the normal run
TEST	I	Test pin input, high active (with pull low) and please DON'T bond the TEST pin.
NC	I	DON'T bond the NC pin.
AUDP, AUDN	O	PWM audio output

Total: 38 Pins

Legend: I = Input O = Output P = Power G = Ground

Note1: To ensure that the IC is functioned properly, please bond all VDD and VSS pins.
Note2: VDD_REGIN should be equal to VDDIO.
Note3: PVDD should be higher than or equal to VDD_REGIN & VDDIO.
Note4: please DON'T bond NC pin.
Note5: please DON'T bond TEST pin.

6.3. Signal Descriptions for GPC3010A/3010C

PIN NAME	TYPE	DESCRIPTION
IO Port		
IOA[7：0]	I/O	IOA[7：0] is a bi-directional I/O port, can be software programmed as wakeup I/O. 1Mohm || 100Kohm feedback pull low resistor IOA7 shares its pad with IR output. IOA1 shares its pad with external clock input. IOA0 shares its pad with external interrupt input. IOA[2：1] shares its pad with feedback function.
IOB[7：0]	I/O	IOB[7：0] is a bi-directional I/O port, can be software programmed as wakeup I/O. 1Mohm || 100Kohm feedback pull low resistor. IOB[3：0] shares its pad with 256-level PWM output, high sink current.
Power & Ground PAD		
VDD_REGOUT	O	Regulator output
VREF	I	Reference voltage of analog circuit, must be connected to VDD_REGOUT
VDD_REGIN	P	Power supply regulator voltage input
VSS	G	Ground reference
PVDD	P	PWM driver power, can be greater than or equal to VDD_REGIN
PVSS	G	PWM driver ground reference
Others		
RESB	I	System reset input, low active (with pull high)
NC	I	Please DON'T bond NC pin (**only for GPC3010A).**
OSC	I	Frequency control pin for external oscillator, with resistor to VDD_REGIN (**only for GPC3010C).**
TEST	I	Test pin input, high active (with pull low), and please DON'T bond the TEST pin.
AUDP, AUDN	O	PWM output

Total: 27 Pins

Legend: I = Input O = Output P = Power G = Ground

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: PVDD can be greater than or equal to VDD_REGIN.
Note3: Please DON'T bond TEST pin.
Note4: NC pin is only for GPC3010A, and please DON'T bond NC pin.
Note5: OSC pin is only for GPC3010C.

6.4. Signal Descriptions for GPC3011C

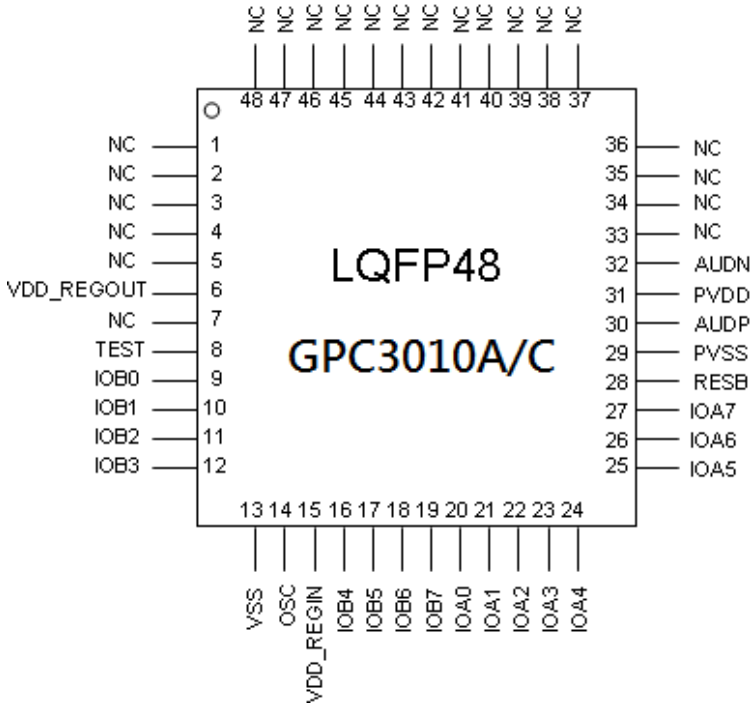
PIN NAME	PIN NO.	TYPE	DESCRIPTION
	IO Port		
IOA[7：0]	27-20	I/O	IOA[7：0] is a bi-directional I/O port, can be software programmed as wakeup I/O. 1Mohm || 100Kohm feedback pull low resistor IOA7 shares its pad with IR output. IOA1 shares its pad with external clock input. IOA0 shares its pad with external interrupt input. IOA[2：1] shares its pad with feedback function.
IOB[7：0]	19-16, 12-9	I/O	IOB[7：0] is a bi-directional I/O port, can be software programmed as wakeup I/O. 1Mohm || 100Kohm feedback pull low resistor IOB[3：0] shares its pad with 256-level PWM output, high sink current.
	Power & Ground PAD		
VDD_REGOUT	6	O	Regulator output
VPP	7	I	Power to OTP ROM, should be supplied from GPC3011C writer in program mode and be connected to VDD_REGOUT in read mode
VDD_REGIN	15	P	Power supply regulator voltage input
VSS	13	G	Ground reference
PVDD	31	P	PWM driver power can be higher than or equal to VDD_REGIN.
PVSS	29	G	PWM driver ground reference
	Others		
RESB	28	I	System reset input, low active (with pull high)
OSC	14	I	Frequency control pin for external oscillator, with resistor to VDD_REGIN
TEST	8	I	Test pin input, high active (with pull low)
AUDP, AUDN	30, 32	O	PWM output

Total: 27 Pins

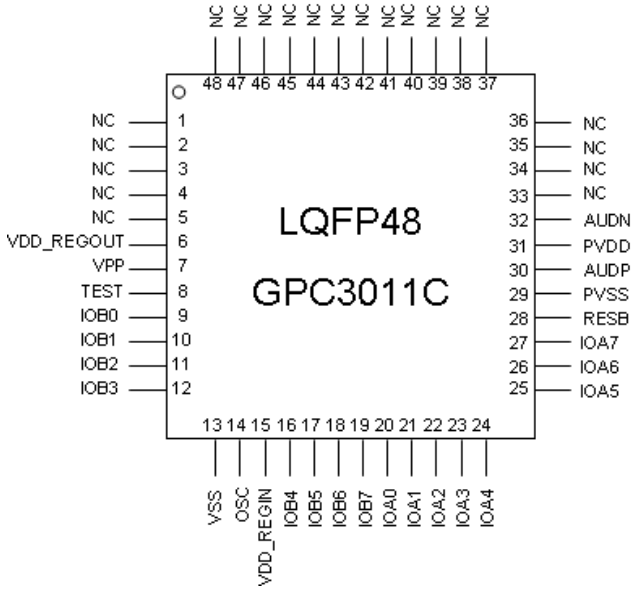
Legend: I = Input O = Output P = Power G = Ground

Note1: PVDD can be greater than or equal to VDD_REGIN.

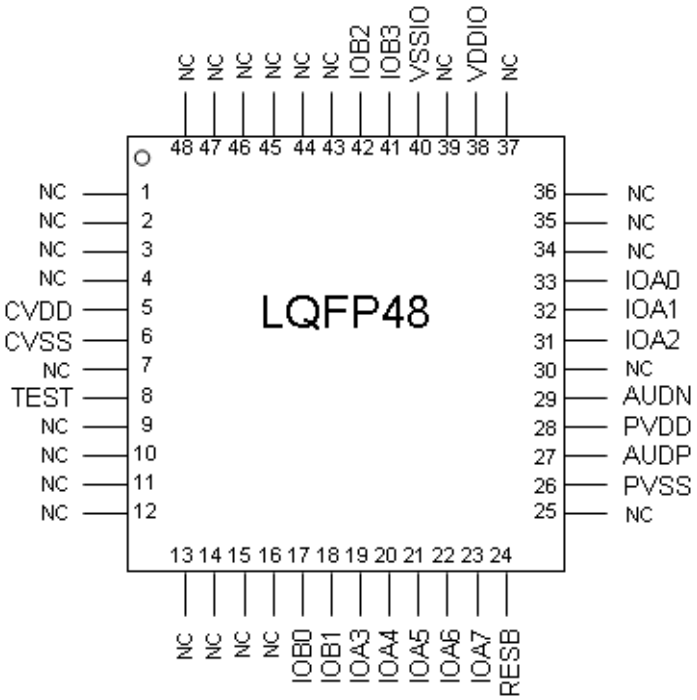
6.5. LQFP48 pin map for GPC3010A/C



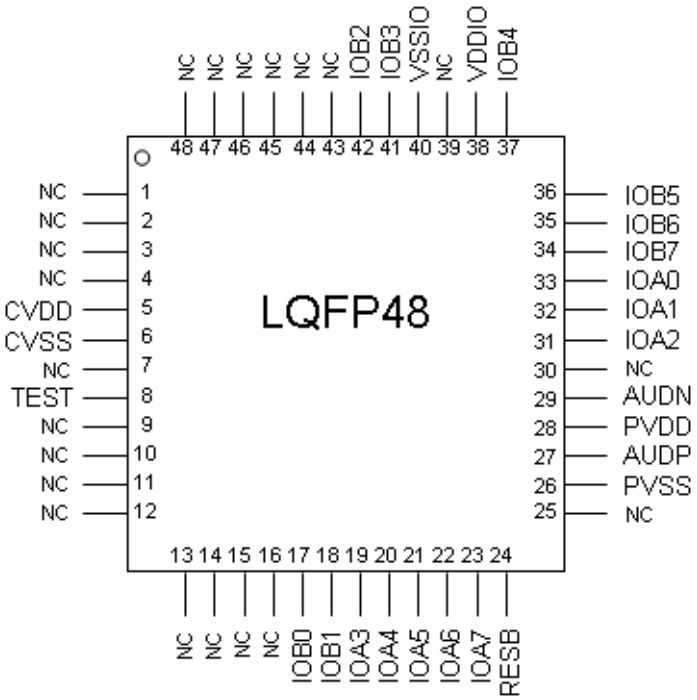
6.6. LQFP48 pin map for GPC3011C



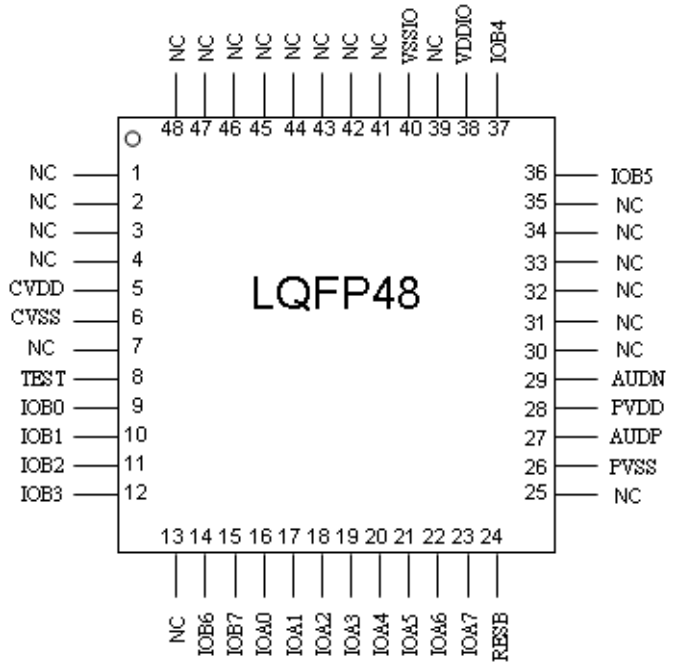
6.7. LQFP48 pin map for GPC3040A/B, GPC3030A/B, GPC3025A/B



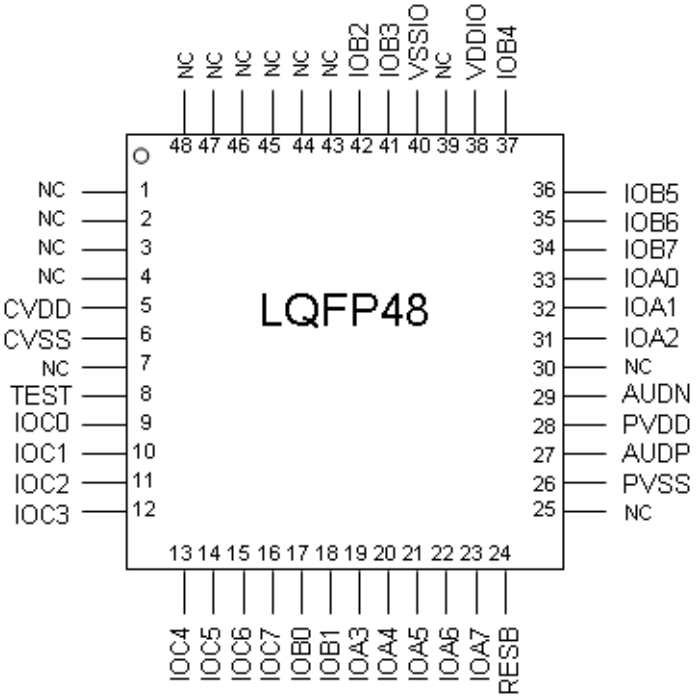
6.8. LQFP48 pin map for GPC3080A, GPC3072A, GPC3063A, GPC3052A



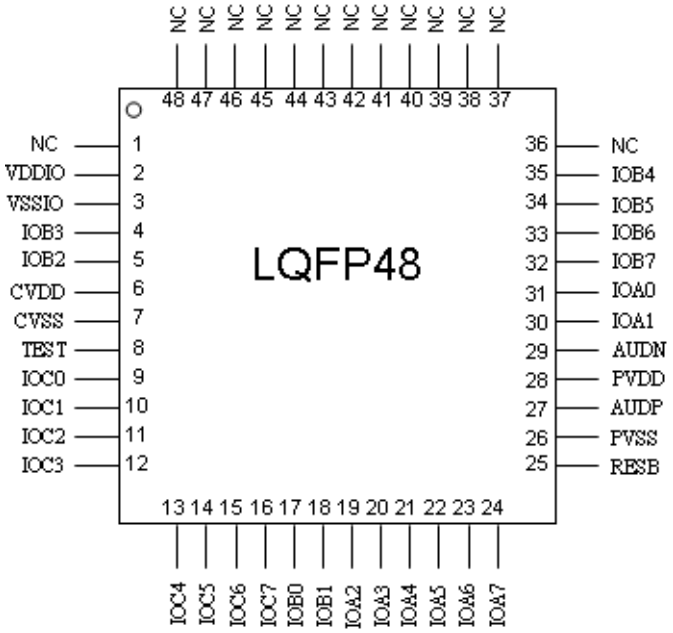
6.9. LQFP48 pin map for GPC3170Ax/Bx, GPC3120Ax/Bx, GPC3106Ax/Bx, GPC3092Ax/Bx



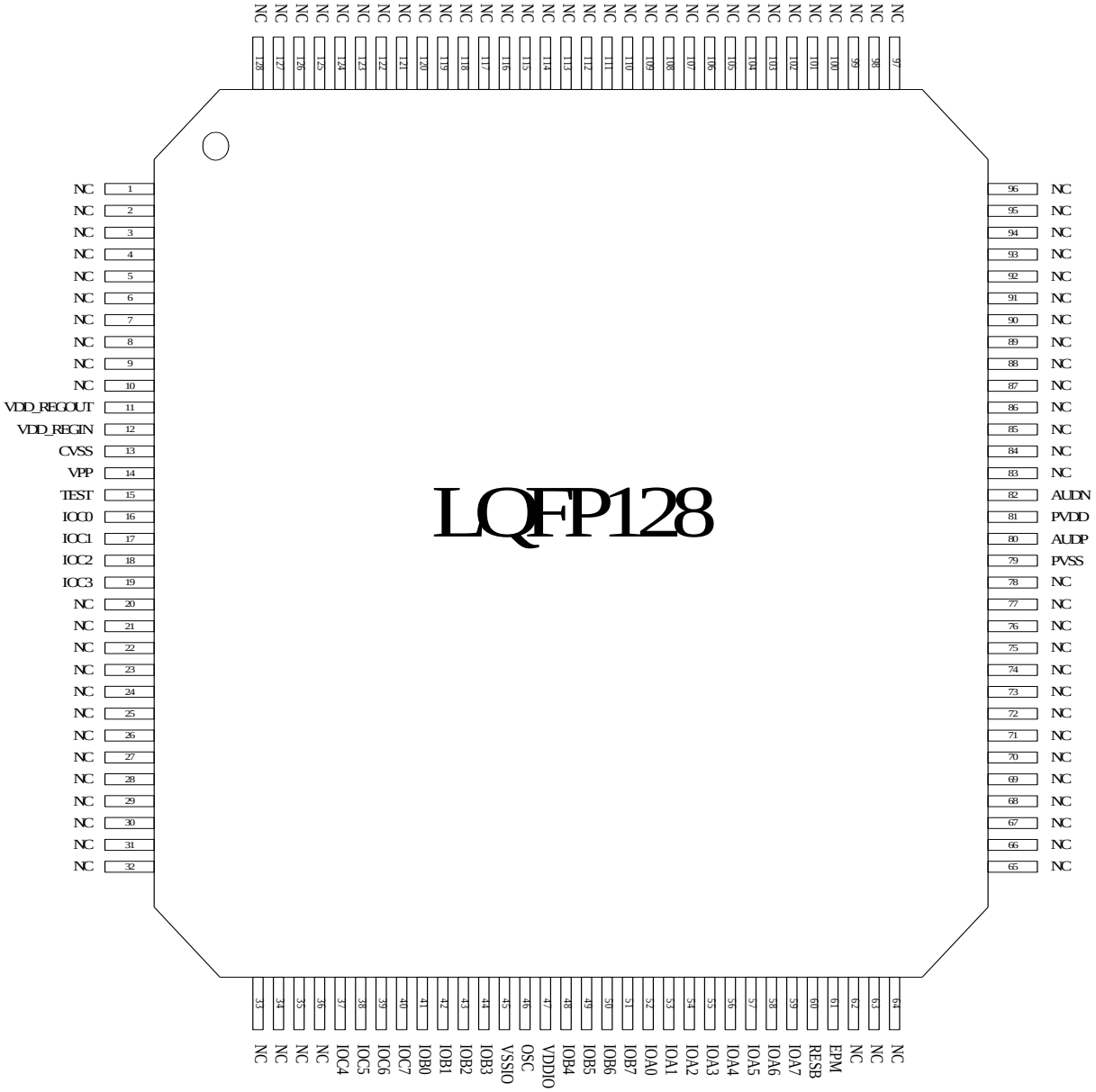
6.10. LQFP48 pin map for GPC3340A/B, GPC3256A/B



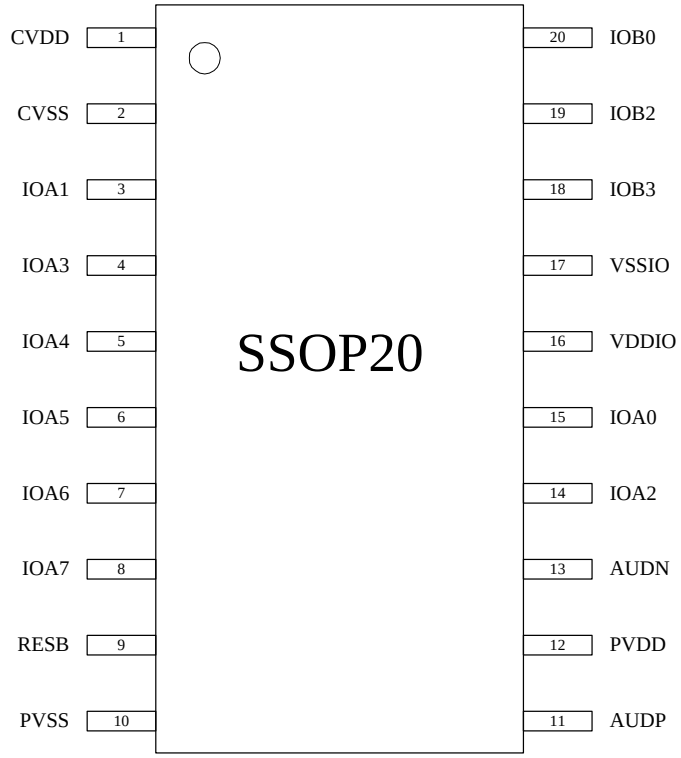
6.11. LQFP48 pin map for GPC3680A, GPC3540A, GPC3480A, GPC3420A



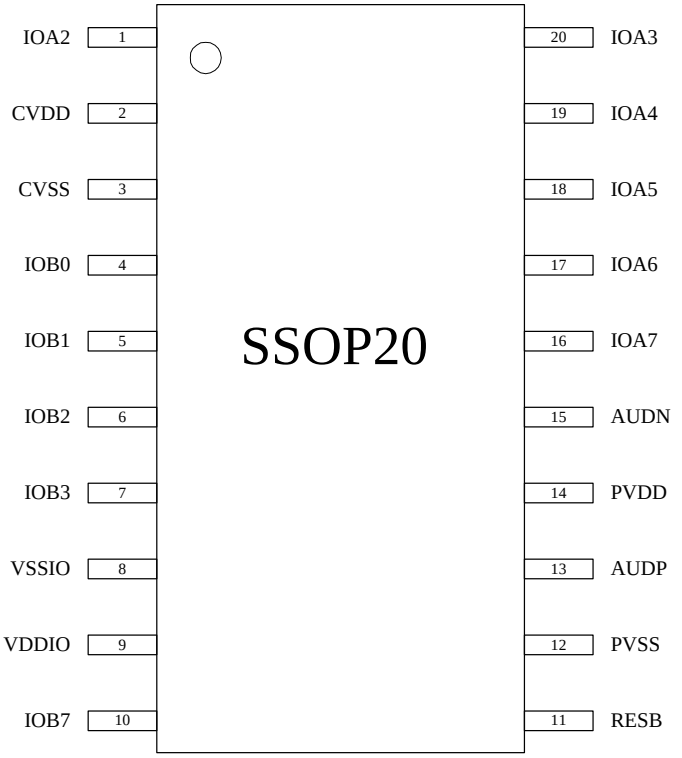
6.12. LQFP128 pin map for GPC3341A



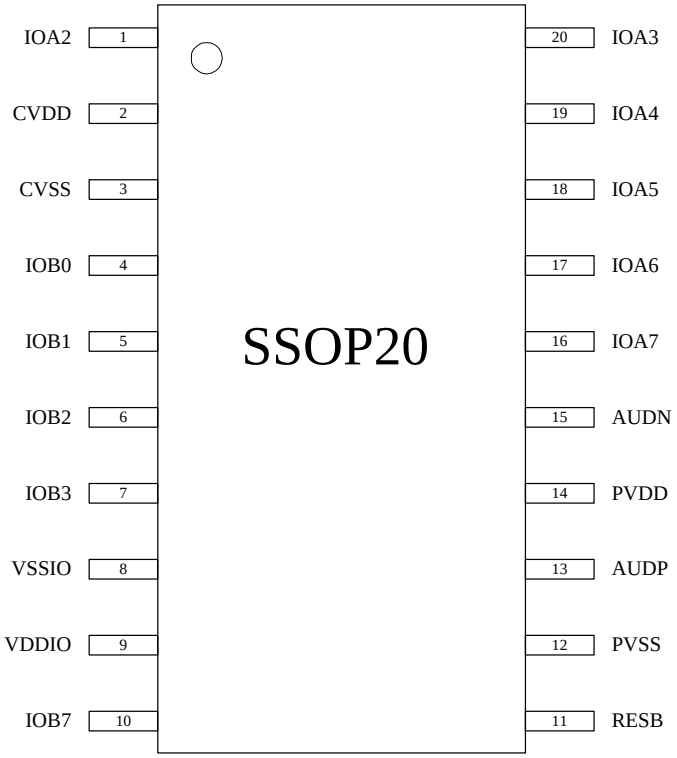
6.13. SSOP20 pin map for GPC3040A/B, GPC3030A/B, GPC3025A/B



6.14. SSOP20 pin map for GPC3080A, GPC3072A, GPC3063A, GPC3052A



6.15. SSOP20 pin map for GPC3170Ax/Bx, GPC3120Ax/Bx, GPC3106Ax/Bx, GPC3092Ax/Bx



7. FUNCTIONAL DESCRIPTIONS

7.1. CPU

The microprocessor in GPC3XXXAx/Bx/Cx/Dx is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of generating a clearer speech and music as well as achieving the best performance.

7.2. RAM Area

The total RAM size is **128-byte** (including stack) for GPC3680A~GPC3052A, GPC3340B~GPC3092B, GPC3010A, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1 and GPC3170B1, starting from address $0080 through $00FF ($0080 - $00FF mapping to $0180 - $01FF).

The total RAM size is **96-byte** (including stack) for GPC3040A/B~GPC3026A/B, starting from address $00A0 through $00FF ($00A0 - $00FF mapping to $01A0 - $01FF).

The total RAM size is **256-byte** (including stack) for GPC3011C/ GPC3010C, starting from address $0080 through $017F ($0100 - $017F mapping to $0180 - $01FF).

7.3. ROM Area

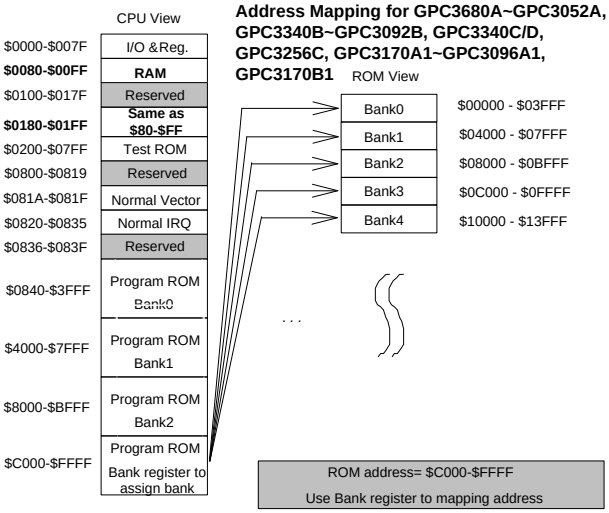
The GPC3XXXAx/Bx/Cx/Dx provides a 32K~2M bytes ROM or OTP ROM (by body option) that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register; choose bank, and access address to fetch data.

Body	ROM size	ROM Address
GPC3680A	2MB	0x00840~0x1FFFFF
GPC3540A	1632KB	0x00840~0x197FFF
GPC3480A	1440KB	0x00840~0x167FFF
GPC3420A	1280KB	0x00840~0x13FFFF
GPC3340A/B/C/D	1024KB	0x00840~0x0FFFFF
GPC3341A	1024KB	0x00840~0x0FFFFF
GPC3256A/B/C	768KB	0x00840~0x0BFFFF
GPC3170A/B/A1/B1	512KB	0x00840~0x07FFFF
GPC3120A/B/A1	384KB	0x00840~0x05FFFF
GPC3106A/B/A1	320KB	0x00840~0x04FFFF
GPC3092A/B/A1	288KB	0x00840~0x047FFF
GPC3080A	256KB	0x00840~0x03FFFF
GPC3072A	224KB	0x00840~0x037FFF
GPC3063A	192KB	0x00840~0x02FFFF
GPC3052A	160KB	0x00840~0x027FFF
GPC3040A/B	128KB	0x00840~0x01FFFF
GPC3030A/B	96KB	0x00840~0x017FFF

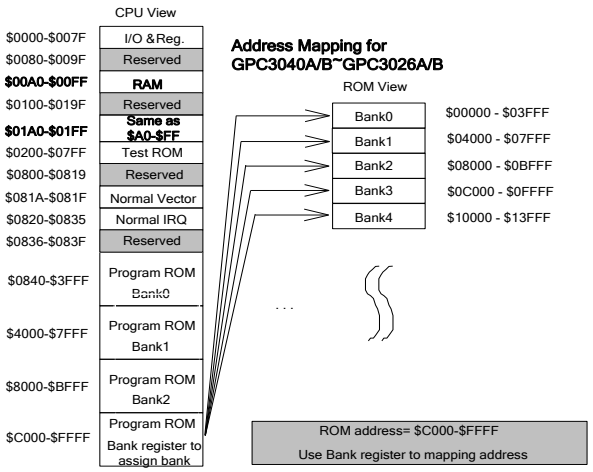
Body	ROM size	ROM Address
GPC3026A/B	80KB	0x00840~0x013FFF
GPC3010A	32KB	0x00840~0x007FFF
Body	**ROM size**	**ROM Address**
GPC3011C	32KB	0x00840~0x007FFF
GPC3010C	32KB	0x00840~0x007FFF

7.4. Map of Memory and I/Os

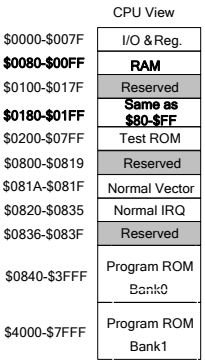
7.4.1. Mapping for GPC3680A~GPC3052A, GPC3340B~GPC3092B, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1



7.4.2. Mapping for GPC3040A/B~GPC3026A/B

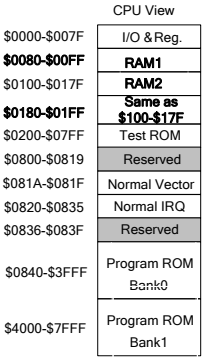


7.4.3. Mapping for GPC3010A



Address Mapping for GPC3010A

7.4.4. Mapping for GPC3011C/GPC3010C



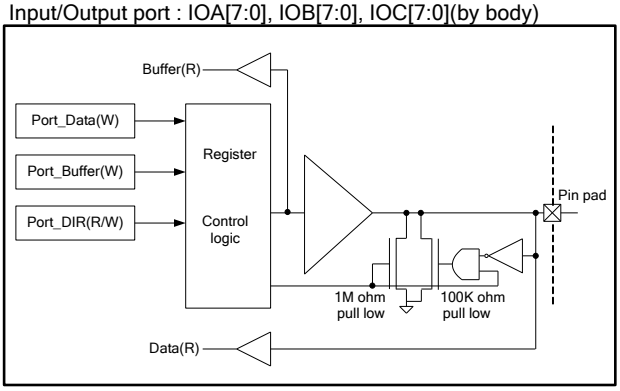
Address Mapping for GPC3011C / GPC3010C

7.5. I/O Port

There are 12 ~ 24 IOs (IOA[7:0], IOB[7:0] and IOC[7:0]) in the GPC3XXXAx/Bx/Cx/Dx (by body), which are bit-controlled IOs. These IOs can be programmed as input (pure input or pull-low) or output buffer. In pull-low input, the IOs generate less impedance to achieve a better noise immunity. While pressing the key (IOs to VDD), a higher impedance retains to save DC power. All 12~24 IOs (by body), are wake-up sources in the GPC3XXXAx/Bx/Cx/Dx. IOA7 can be programmed as an IR transmitter. IOA1 can be programmed as an external clock source. IOA0 can be programmed as an external interrupt source, and IOB5, IOB4 can be programmed as a 32KHz crystal clock generator by adding external components (by body). IOB[3:0] can sink high current to drive high brightness LED. In GPC3341A, IOA3 shares pad with SDA, and IOA2 shares with SCK in serial programming cycle. In GPC3010A/GPC3011C/GPC3010C, IOA[2:1] can also be programmed as feedback function with IOA2 connecting to the input of inverter and IOA1 connecting to the output of inverter. With feedback function, RC or XTAL oscillation can be implemented. For mode flexible application, IO wakeup and ECK as TMA clock source are also available when feedback function enable. Refer the programming guide for more detail information about feedback function.

IO port configuration:

Input/Output port : IOA[7:0], IOB[7:0], IOC[7:0](by body)



7.6. Hardware PWMIO

Hardware PWMIO supports four LED outputs from IOB[3:0] with brightness control of 256 levels. The clock source of PWMIO can be selected by user's request.

7.7. Power Saving Mode

The GPC3XXXAx/Bx/Cx/Dx includes a power saving mode (Standby mode) for those applications that require low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. All 12~24 IOs (by body), RTC(8Hz/2Hz) (by body), external interrupt(IOA0) are wake-up sources in the GPC3XXXAx/Bx/Cx/Dx. After GPC3XXXAx/Bx/Cx/Dx wakes up, the internal CPU will continue to execute program.

7.8. RTC (Real Time Clock)

GPC3XXXAx/Bx/Cx/Dx (by body) provides two RTC (real time clock) sources: 2Hz, 8Hz. The RTC sources can be used for time counting or system awaking. Each RTC occurs, the system wakes up and users can use this signal for time counting. In addition, GPC3XXXAx/Bx/Cx/Dx supports 32768Hz OSC in auto mode, the first one second runs at strong mode (consumes the highest power) and then switch to weak mode automatically to save power.

***Note: RTC is NOT available for GPC3040A/B~GPC3026A/B, GPC3010A, GPC3011C, GPC3010C.**

7.9. Watchdog

The purpose of watchdog is to monitor whether the system operates normally. Within a certain period of time, watchdog must be cleared. It prevents the system from incorrect code execution by generating a system reset when software fails to clear watchdog flag within 1 second. Watchdog function can be removed by option in GPC3XXXAx/Bx/Cx/Dx series.

7.10. Low Voltage Reset

The GPC3XXXAx/Bx/Cx/Dx has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctions under low voltage condition. With the unique design of Low Voltage Reset in GPC3XXXAx/Bx/Cx/Dx, it is able to reset all functions to the initial operational (stable) state if the power voltage drops below certain operation voltage.

7.11. Interrupt

The GPC3XXXAx/Bx/Cx/Dx has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller provides 7 or 8 IRQs (by body) and 1 NMI. A NMI cannot be interrupted by any other IRQs.

Interrupt Source	Priority
TIMER A	NMI
TIMER A	IRQ1
TIMER B	IRQ2
TIMER C	IRQ3
TB1	IRQ4
TB2	IRQ5
RTC(by body)	IRQ6
KEY	IRQ7
EXT	IRQ8

***Note: RTC is NOT available for GPC3040A/B~GPC3026A/B, GPC3010A, GPC3011C, GPC3010C.**

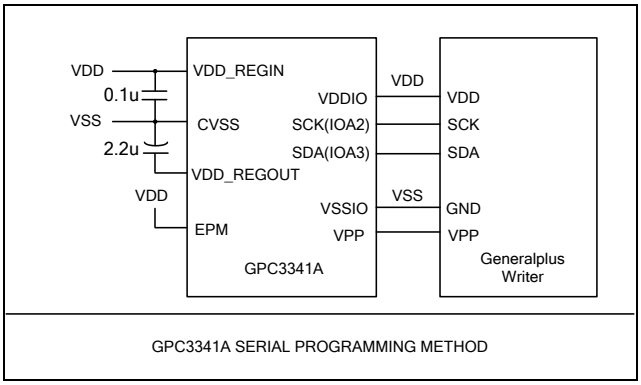
7.12. Timer/Counter

The GPC3XXXAx/Bx/Cx/Dx has three 12-bit timer/counters, TMA, TMB, and TMC respectively. In the timer mode, TMA, TMB, and TMC are re-loadable up-counters. When timer overflows from $0FFF to $0000, the carry (overflow) signal will make user's preset value be loaded into timer automatically and count up again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

7.13. Speech and Melody

In speech synthesis, GPC3XXXAx/Bx/Cx/Dx uses NMI for an accurate sampling frequency. Users can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, ADPCM, SACMA3400, and A3400Pro.

7.14. OTP Programming Circuit for GPC3341A



GPC3341A SERIAL PROGRAMMING METHOD

Note1: Don't connect any component with IOA2 and IOA3 when programming.

Note2: Connect EPM to VDD during OTP programming cycle, and keep it floating in normal run.

Note3: Connect VPP to Writer during OTP programming cycle, and keep it floating in normal run.

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	(VSS-0.3V) to (V_+ + 0.3V)
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-65℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

8.2. DC Characteristics (TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Min. Operating Voltage	VDD*min	2.0	2.1	2.2	V	**For GPC3680A/540A/480A/420A**
		1.9	2.0	2.1	V	**For Others**
Max. Operating Voltage	VDD max	-	-	5.5	V	
Low Voltage Reset Level	V^*_{LVR}	2.0	2.1	2.2	V	**For GPC3680A/540A/480A/420A**
		1.9	2.0	2.1	V	**For Others**
Operating Current	I_{OP}	-	2.5	-	mA	F_{CPU} = 6MHz @ 3.0V, PWM output off **For GPC3680A/540A/480A/420A**
		-	4	-	mA	F_{CPU} = 6MHz @ 3.0V, PWM output off **For GPC3341A**
		-	2	-	mA	F_{CPU} = 6MHz @ 3.0V, PWM output off **For Others**
		-	5	-	mA	F_{CPU} = 6MHz @ 4.5V, PWM output off **For GPC3680A/540A/480A/420A/341A**
		-	2.5	-	mA	F_{CPU} = 6MHz @ 4.5V, PWM output off **For GPC3010A/011C/010C**
		-	4	-	mA	F_{CPU} = 6MHz @ 4.5V, PWM output off **For Others**
Halt Current	I^{**}_{HALT}	-	4	-	uA	VDD = 3.0V, XTAL32K ON **NOT available for GPC3040A/B~GPC3026A/B, GPC3010A/011C/010C**
		-	8	-	uA	VDD = 4.5V, XTAL32K ON **NOT available for GPC3040A/B~GPC3026A/B , GPC3010A/011C/010C**
Standby Current	I_{STBY}	-	-	5	uA	VDD = 3.0V, **For GPC3341A/010A/011C/ 010C**
		-	-	3	uA	VDD = 3.0V, **For GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1.**
		-	-	2	uA	VDD = 3.0V, **For Others**
		-	-	5	uA	VDD = 4.5V, **For GPC3341A/010A/011C/ 010C**
		-	-	3	uA	VDD = 4.5V, **For GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1.**
		-	-	2	uA	VDD = 4.5V, **For Others**

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
GPIO Input High Level (IOA, IOB, IOC)	V_{IH}	0.7VDD	-	-	V	VDD = 3.0V
		0.7VDD	-	-	V	VDD = 4.5V
GPIO Input Low Level (IOA, IOB, IOC)	V_{IL}	-	-	0.3VDD	V	VDD = 3.0V
		-	-	0.3VDD	V	VDD = 4.5V
Output High Current (IOA, IOB, IOC)	I_{OH}	-	5	-	mA	VDD = 3.0V, V_{OH} = 0.7*VDD
		-	10	-	mA	VDD = 4.5V, V_{OH} = 0.7*VDD
Output Low Current (IOA, IOB[7:4], IOC)	I_{OL}	-	10	-	mA	VDD = 3.0V, V_{OL} = 0.3*VDD
		-	20	-	mA	VDD = 4.5V, V_{OL} = 0.3*VDD
Output Low Current (IOB[3:0])	I_{OL}	-	20	-	mA	VDD = 3.0V, V_{OL} = 0.3*VDD
		-	40	-	mA	VDD =4.5V, V_{OL} = 0.3*VDD
Input Pull Low Resistor (IOA, IOB, IOC)	R_L	-	200, 2000	-	Kohm	VDD = 3.0V, IO = 0V 2000Kohms for IOA in GPC3340B~ GPC3092B and 200Kohms for others
		-	100, 1000	-	Kohm	VDD = 4.5V, IO = 0V 1000Kohms for IOA in GPC3340B~ GPC3092B and 100Kohms for others
Input Pull Low Resistor (IOA, IOB, IOC)	R_L	-	2000	-	Kohm	VDD = 3.0V, IO = 3.0V
		-	1000	-	Kohm	VDD = 4.5V, IO = 4.5V
PWM Driver Current	I_{PWM}	-	180	-	mA	VDD = 3.0V, 8 Ohms load
		-	280	-	mA	VDD = 4.5V, 8 Ohms load
Frequency deviation by voltage drop	⊿F/F	-	2	-	%	$\frac{Fosc(4.5v) - Fosc(2.4v)}{Fosc(4.5v)}$ F_{CPU} = 6MHz **For GPC3011C/010C EROSC**
		-	2	-	%	$\frac{Fosc(3.0v) - Fosc(2.4v)}{Fosc(3.0v)}$ F_{CPU} = 6MHz **For GPC3680A/540A/480A/420A IROSC**
		-	2	-	%	$\frac{Fosc(3.0v) - Fosc(2.4v)}{Fosc(3.0v)}$ F_{CPU} = 8MHz **For GPC3680A/540A/480A/420A IROSC**
		-	2	-	%	$\frac{Fosc(4.5v) - Fosc(3.0v)}{Fosc(4.5v)}$ F_{CPU} = 6MHz **For GPC3680A/540A/480A/420A IROSC**
		-	2	-	%	$\frac{Fosc(4.5v) - Fosc(3.0v)}{Fosc(4.5v)}$ F_{CPU} = 8MHz **For GPC3680A/540A/480A/420A IROSC**
		-	2	-	%	$\frac{Fosc(4.5v) - Fosc(2.4v)}{Fosc(4.5v)}$ F_{CPU} = 6MHz,**For GPC3341A~GPC3010A/011C/010C IROSC**

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
		-	2	-	%	$\frac{Fosc(4.5v)-Fosc(2.4v)}{Fosc(4.5v)}$ F_{CPU} = 8MHz,**For GPC3341A~GPC3010A/ 011C/010C IROSC**
		-	2	-	%	$\frac{Fosc(4.5v)-Fosc(2.4v)}{Fosc(4.5v)}$ F_{CPU} = 6MHz, **For GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1 IROSC**
		-	2	-	%	$\frac{Fosc(4.5v)-Fosc(2.4v)}{Fosc(4.5v)}$ F_{CPU} = 8MHz, **For GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1 IROSC**
Frequency lot deviation	⊿F/F	-7	-	7	%	$\frac{Fosc(3.0v)-6MHz}{6MHz}$ F_{CPU} = 6MHz @ 3.0V, Rosc=51Kohm **For GPC3011C/010C EROSC**
		-7	-	7	%	$\frac{Fosc(4.5v)-6MHz}{6MHz}$ F_{CPU} = 6MHz @ 4.5V, Rosc=51Kohm **For GPC3011C/010C EROSC**
		-3	-	3	%	$\frac{Fmax(3.0v)-Fmin(3.0v)}{Fmax(3.0v)}$ F_{CPU} = 6MHz @ 3.0V,**For IROSC**
		-3	-	3	%	$\frac{Fmax(3.0v)-Fmin(3.0v)}{Fmax(3.0v)}$ F_{CPU} = 8MHz @ 3.0V,**For IROSC**
		-3	-	3	%	$\frac{Fmax(4.5v)-Fmin(4.5v)}{Fmax(4.5v)}$ F_{CPU} = 6MHz @ 4.5V,**For IROSC**
		-3	-	3	%	$\frac{Fmax(4.5v)-Fmin(4.5v)}{Fmax(4.5v)}$ F_{CPU} = 8MHz @ 4.5V,**For IROSC**

***Note:** VDDmin may have +/-0.1V variation due to process issue.

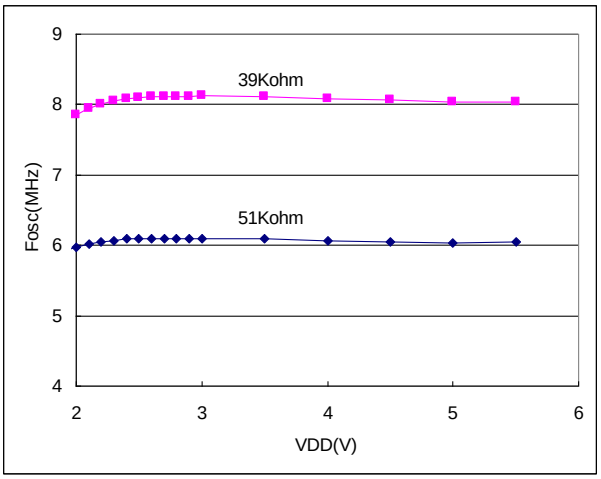
****Note:** Halt mode is **NOT** available for **GPC3040A/B~GPC3026A/B, GPC3**010A/011C/010C.

8.3. (3volt) External Oscillator R Relative F_{osc} Table for GPC3011C/010C (the table is only for reference)

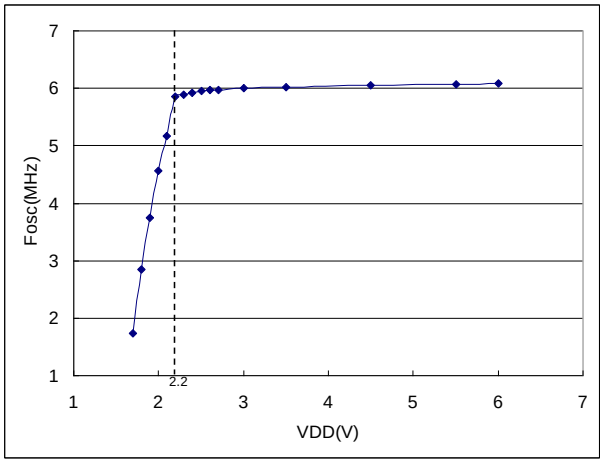
R(Kohm)	39	51	75
F_{osc} (MHz)	8	6	4

8.4. The Relationship between the FOSC and VDD

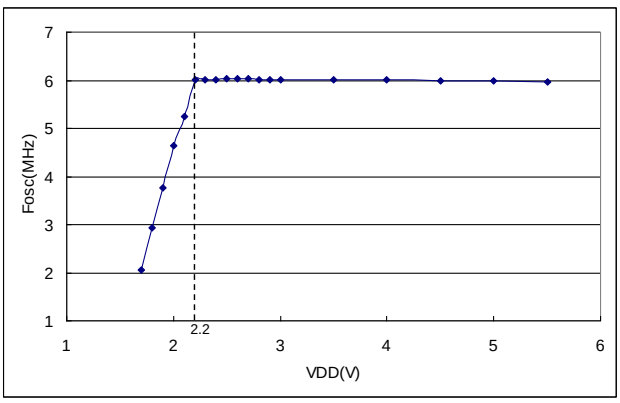
8.4.1. Frequency vs. VDD (external R_{OSC}) For GPC3011C/010C



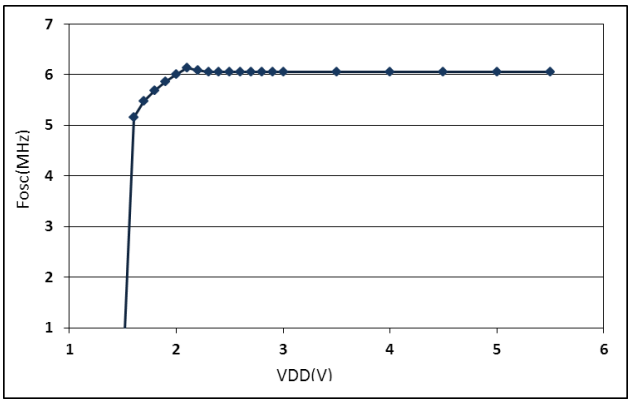
8.4.2. Frequency vs. VDD (build-in 6MHz ROSC) For GPC3680A/540A/480A/420A



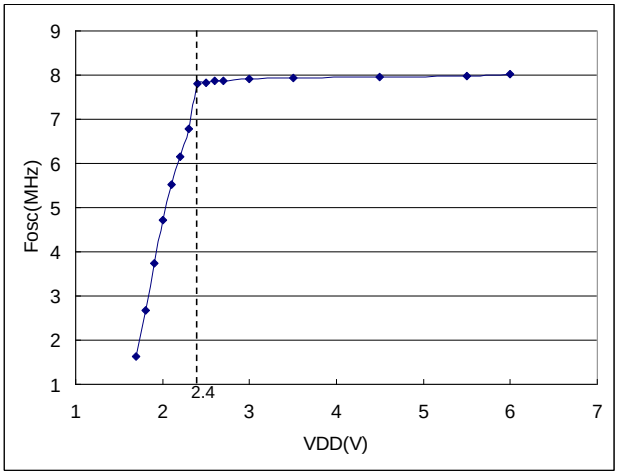
8.4.3. Frequency vs. VDD (build-in 6MHz ROSC) For GPC3341A~GPC3026A



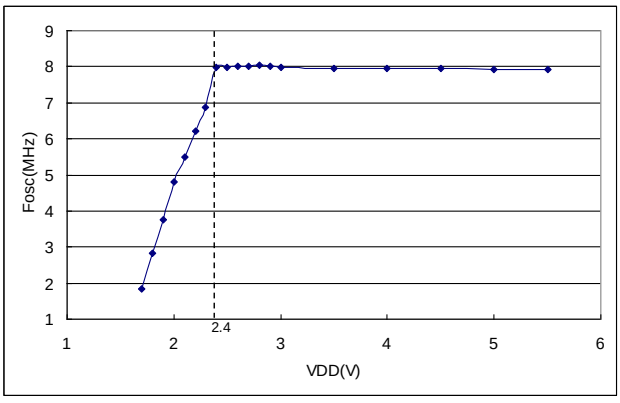
8.4.4. Frequency vs. VDD (build-in 6MHz ROSC) For GPC3010A/011C/010C



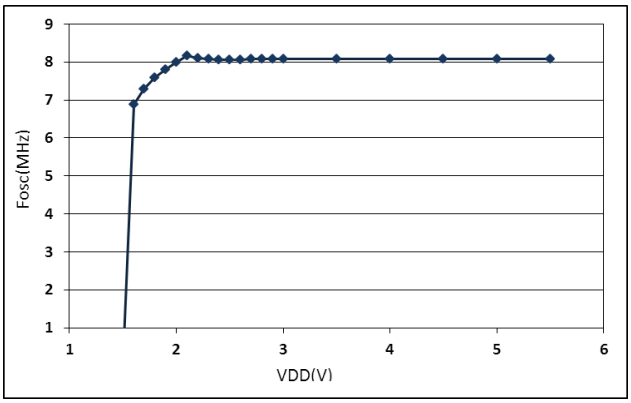
8.4.5. Frequency vs. VDD (build-in 8MHz R_{OSC}) For GPC3680A/540A/480A/420A



8.4.6. Frequency vs. VDD (build-in 8MHz ROSC) For GPC3341A~GPC3026A, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1

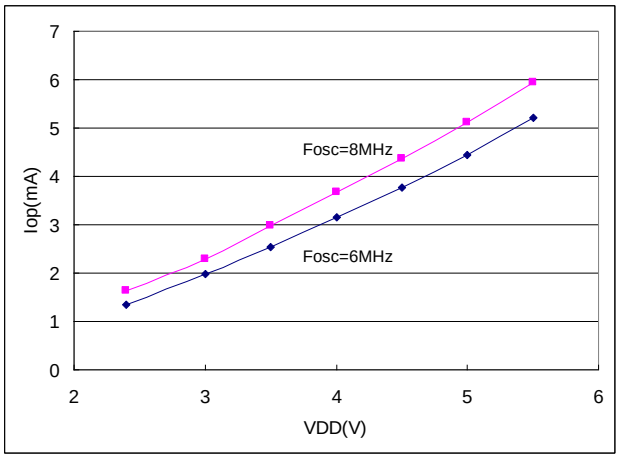


8.4.7. Frequency vs. VDD (build-in 8MHz ROSC) For GPC3010A/011C/010C

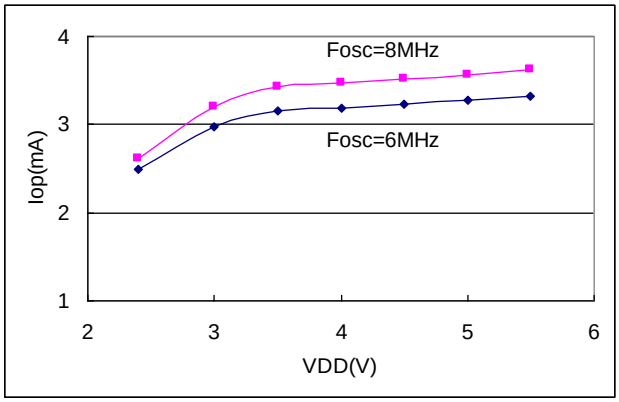


8.5. The Relationship between the VDD and I_{OP} (PWM output off)

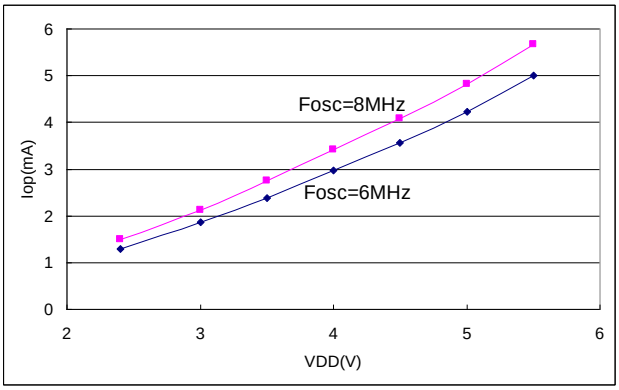
8.5.1. Operating Current vs. VDD (build-in R_{OSC}) For GPC3680A/540A/480A/420A



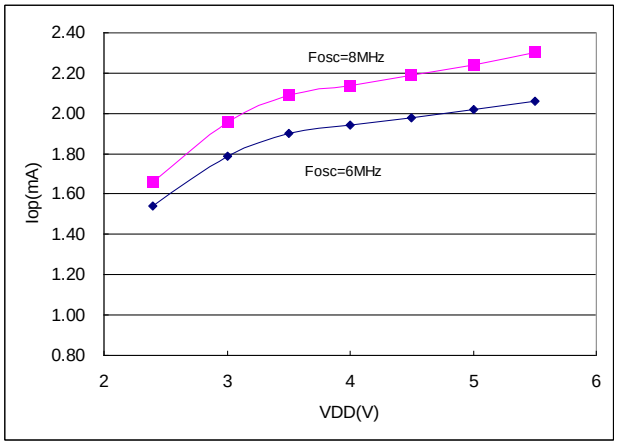
8.5.2. Operating Current vs. VDD (build-in R_{OSC}) For GPC3341A



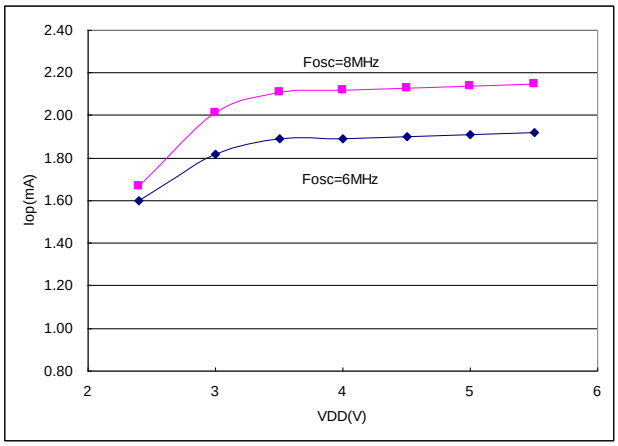
8.5.3. Operating Current vs. VDD (build-in R_{OSC}) For GPC3340A ~GPC3026A, GPC3340B ~GPC3092B, GPC3040B ~GPC3026B, GPC3340C/D~GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1



8.5.4. Operating Current vs. VDD (external R_{OSC}) For GPC3011C/010C

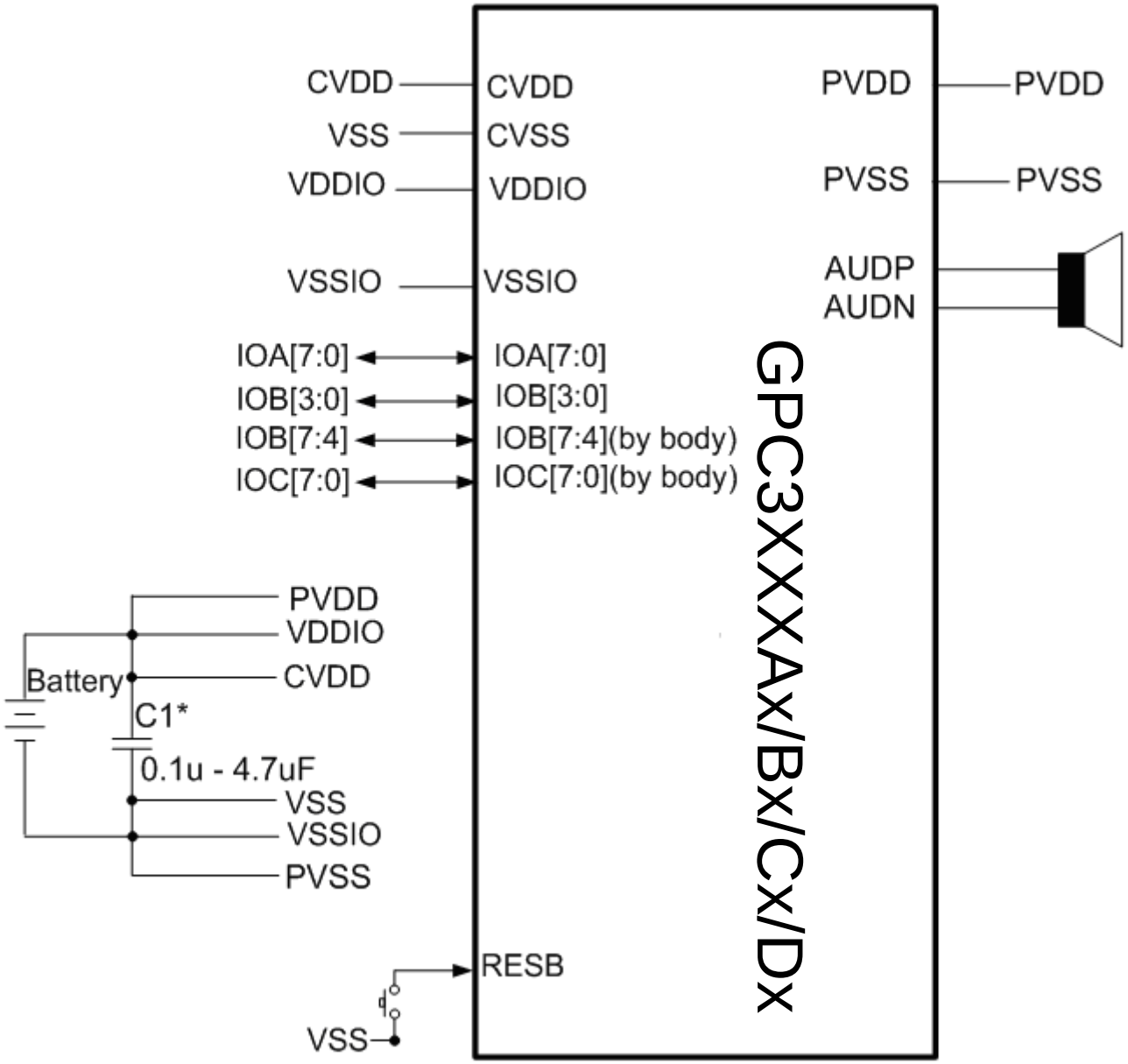


8.5.5. Operating Current vs. VDD (build-in R_{OSC}) For GPC3010A/011C/010C



9. APPLICATION CIRCUITS

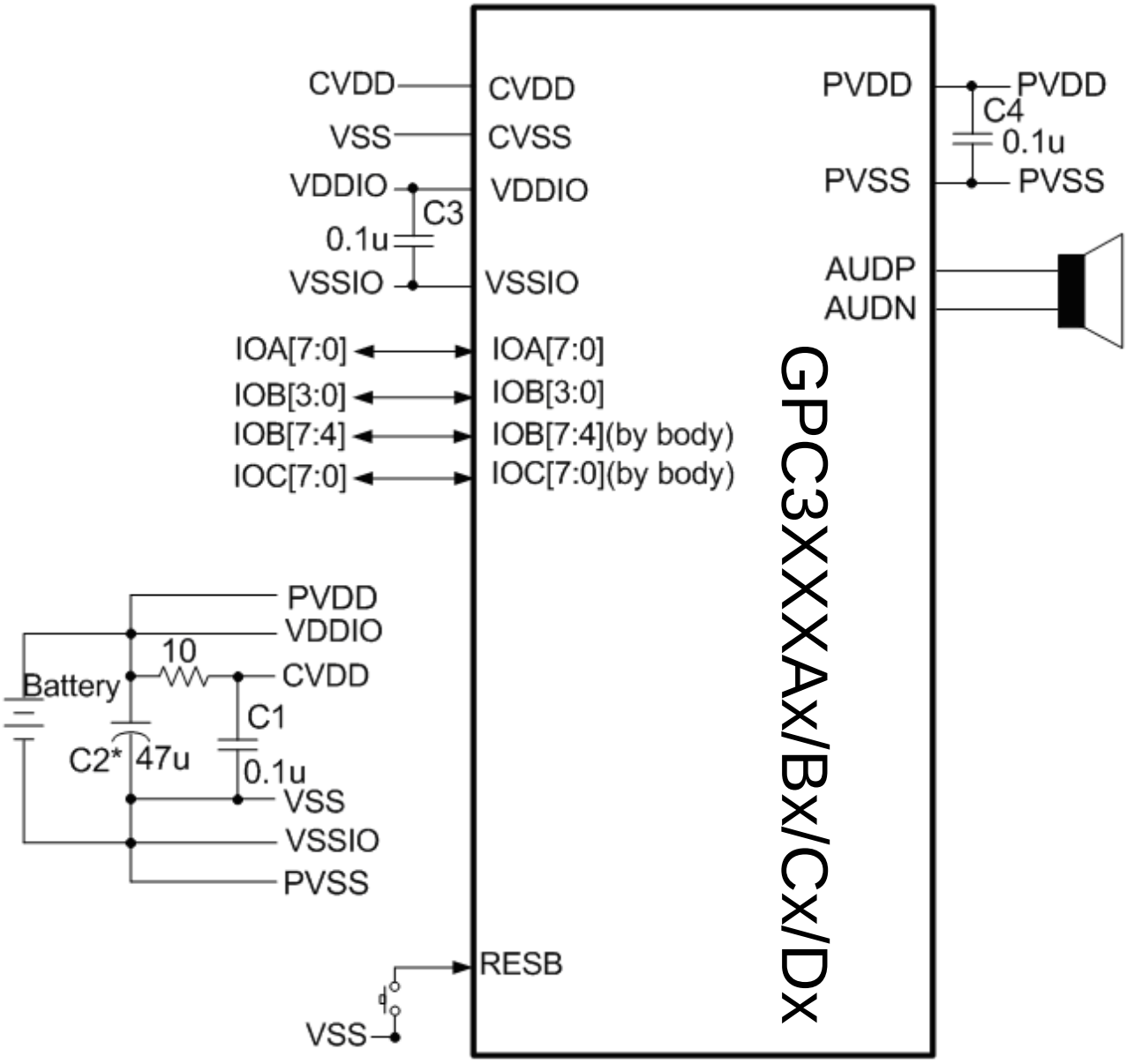
9.1. Application Circuits with Low Loadings for GPC3680A~GPC3026A, GPC3340B~GPC3092B, GPC3040B~GPC3026B, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1.



PCB Layout Guidelines:

1. CVDD, VDDIO and PVDD must be connected to power input port directly rather than the branch of each other.
2. CVDD must be equal to VDDIO.
3. PVDD **can be greater than or equal to** CVDD and VDDIO **for GPC3680A~GPC3052A, GPC3340B~GPC3092B, GPC3040B~GPC3026B, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1.**
4. PVDD **MUST be equal** to CVDD and VDDIO **for GPC3040/030A/026A.**
5. CVSS, VSSIO and PVSS must be connected to ground input directly rather than the branch of each other.
6. Capacitor (used for XTAL32K) is proposed to be 12~20 pF **for GPC3680A~GPC3052A, GPC3340B~GPC3092B, NOT available for GPC3040A/B~GPC3026A/B**.
7. When using two batteries, C1 is suggested to be 0.1uF~4.7uF, and should be increased in a high-volume application.
8. **Only 1Mohms pull low resistor is available on IOA[7：0] for GPC3340B~GPC3092B, GPC3340D, GPC3170B1.**

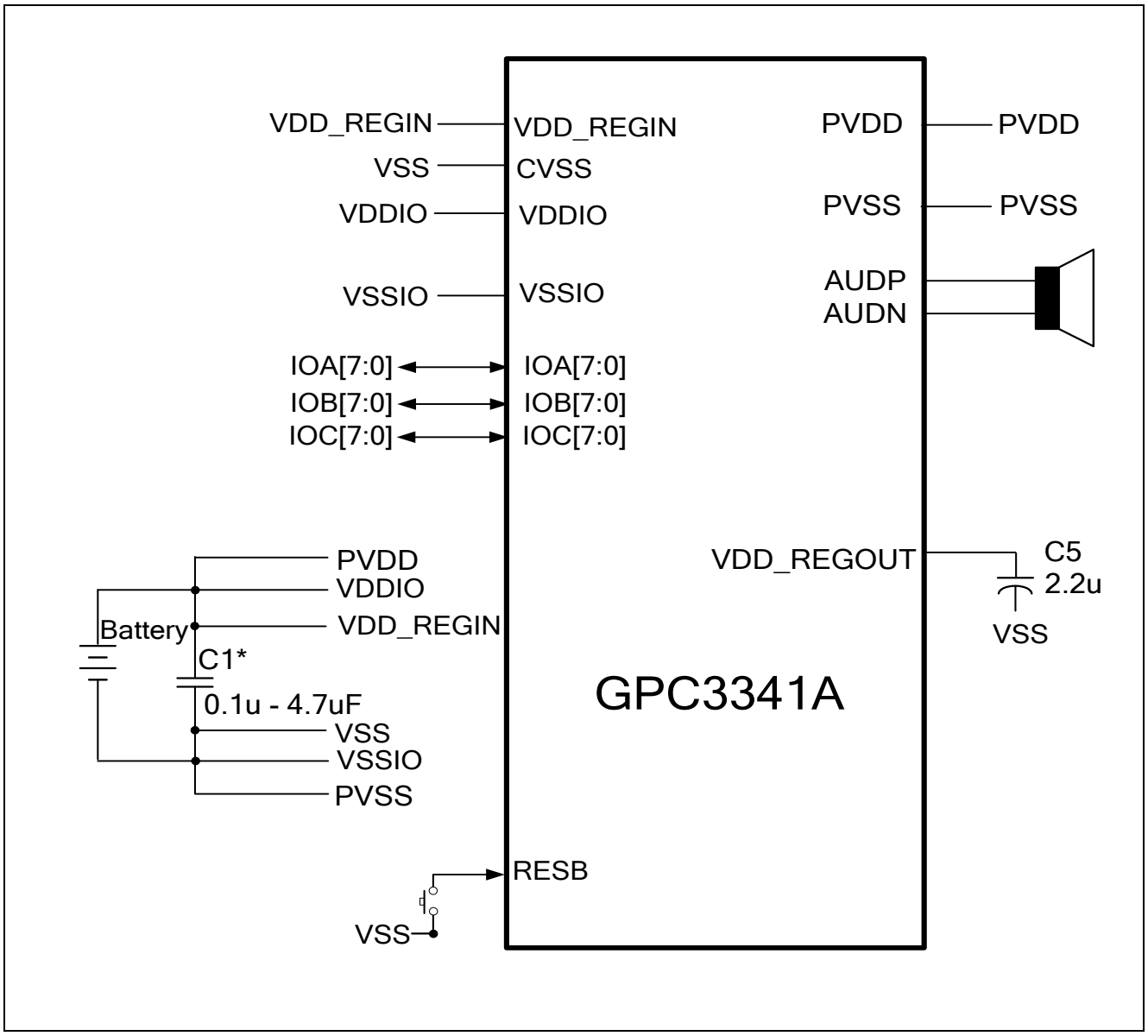
9.2. Application Circuits with Heavy Loadings (such as motor, high brightness LED) for GPC3680A~GPC3026A, GPC3340B~GPC3092B, GPC3040B~GPC3026B, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1.



PCB Layout Guidelines:

1. CVDD, VDDIO and PVDD must be connected to power input port directly, rather than the branch of each other.
2. CVDD must be equal to VDDIO.
3. PVDD **can be greater than or equal to** CVDD and VDDIO **for GPC3680A~GPC3052A, GPC3340B~GPC3092B, GPC3040B~GPC3026B, GPC3340C/D, GPC3256C, GPC3170A1~GPC3092A1, GPC3170B1.**
4. PVDD **MUST be equal** to CVDD and VDDIO **for GPC3040/030A/026A.**
5. CVSS, VSSIO and PVSS must be connected to ground input directly rather than the branch of each other.
6. Capacitor (used for XTAL32K) is proposed to be 12~20 pF **for GPC3680A~GPC3052A, GPC3340B~GPC3092B, but not available for GPC3040A/B~GPC3026A/B**.
7. The typical value of C2 is 47uF, and should be modified in different loading.
8. **Only 1M-Ohm pull low resistor is available on IOA[7：0] for GPC3340B~GPC3092B, GPC3340D, GPC3170B1.**

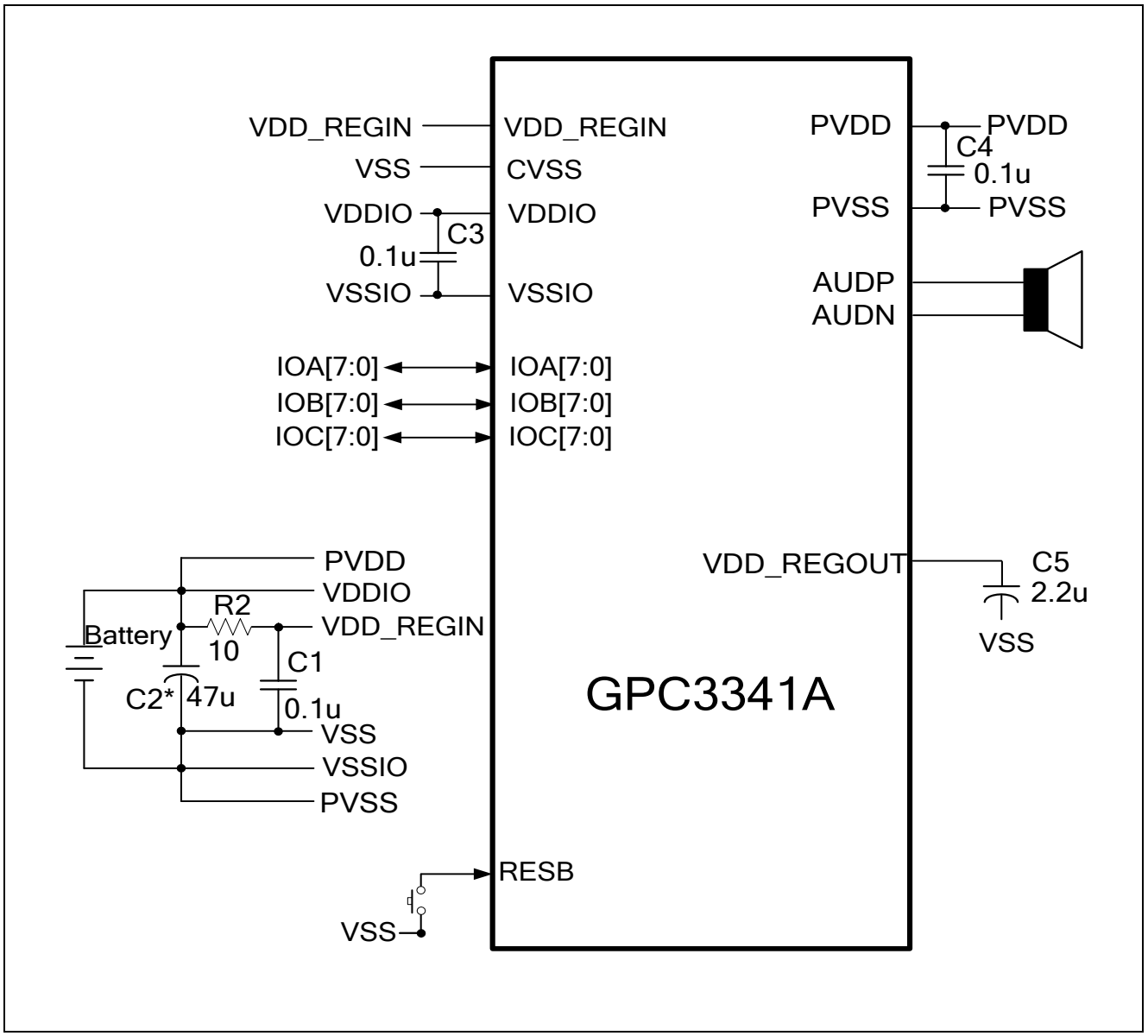
9.3. Application Circuit with Low Loading for GPC3341A



PCB Layout Guidelines:

1. VDD_REGIN, VDDIO and PVDD should be connected to power input port directly rather than the branch of each other.
2. VDD_REGIN should be equal to VDDIO.
3. PVDD should be greater than or equal to VDD_REGIN and VDDIO.
4. CVSS, VSSIO and PVSS should be connected to ground input directly rather than the branch of each other.
5. When using two batteries, C1 should be 0.1uF~4.7uF and should be increased for a high-volume application.

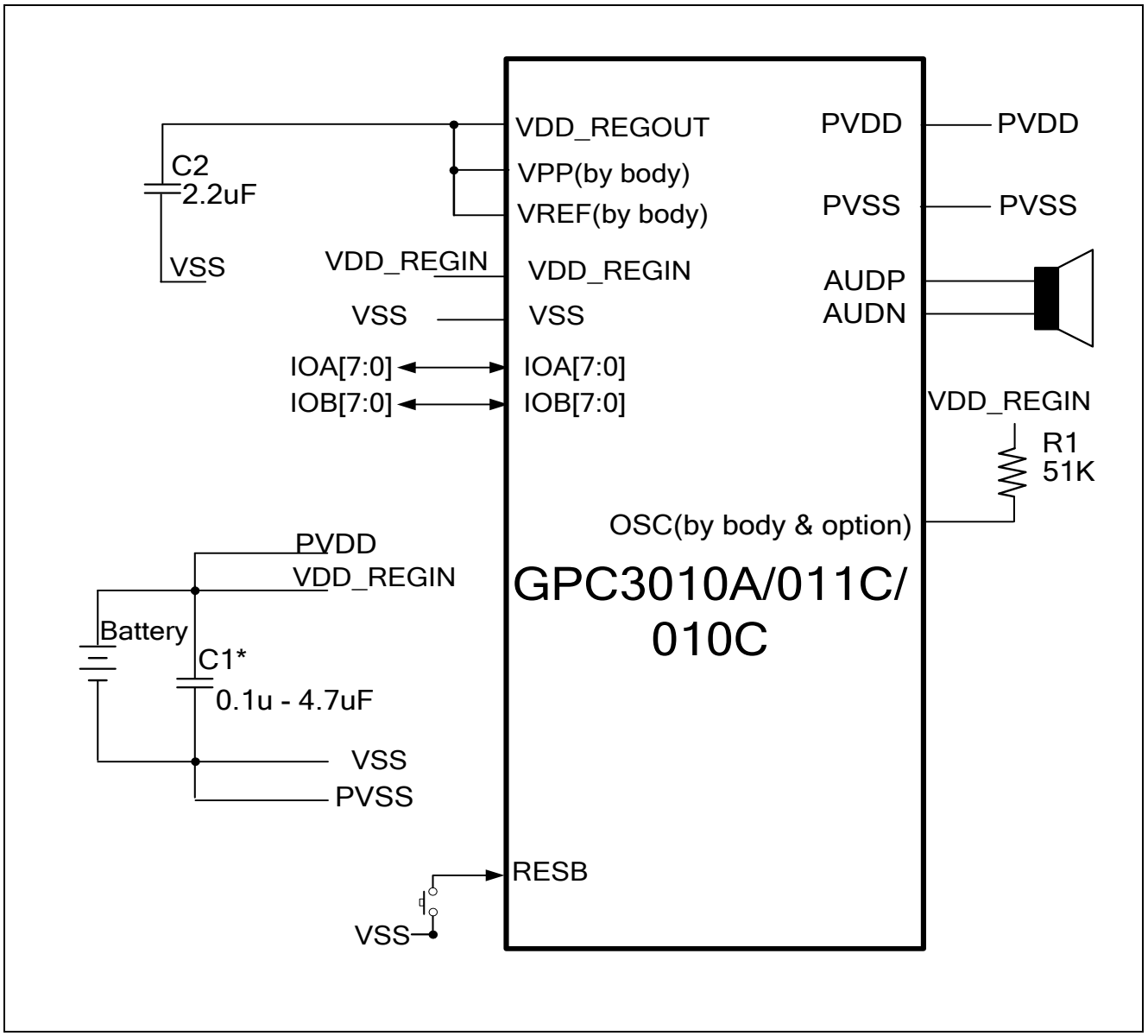
9.4. Application Circuits with Heavy Loading (such as motor, high brightness LED) for GPC3341A



PCB Layout Guidelines:

1. VDD_REGIN, VDDIO and PVDD should be connected to power input port directly rather than the branch of each other.
2. VDD_REGIN should be equal to VDDIO.
3. PVDD should be greater than or equal to VDD_REGIN and VDDIO.
4. CVSS, VSSIO and PVSS should be connected to ground input directly rather than the branch of each other.
5. The typical value of C2 is 47uF, and should be adjusted if different loading is applied.

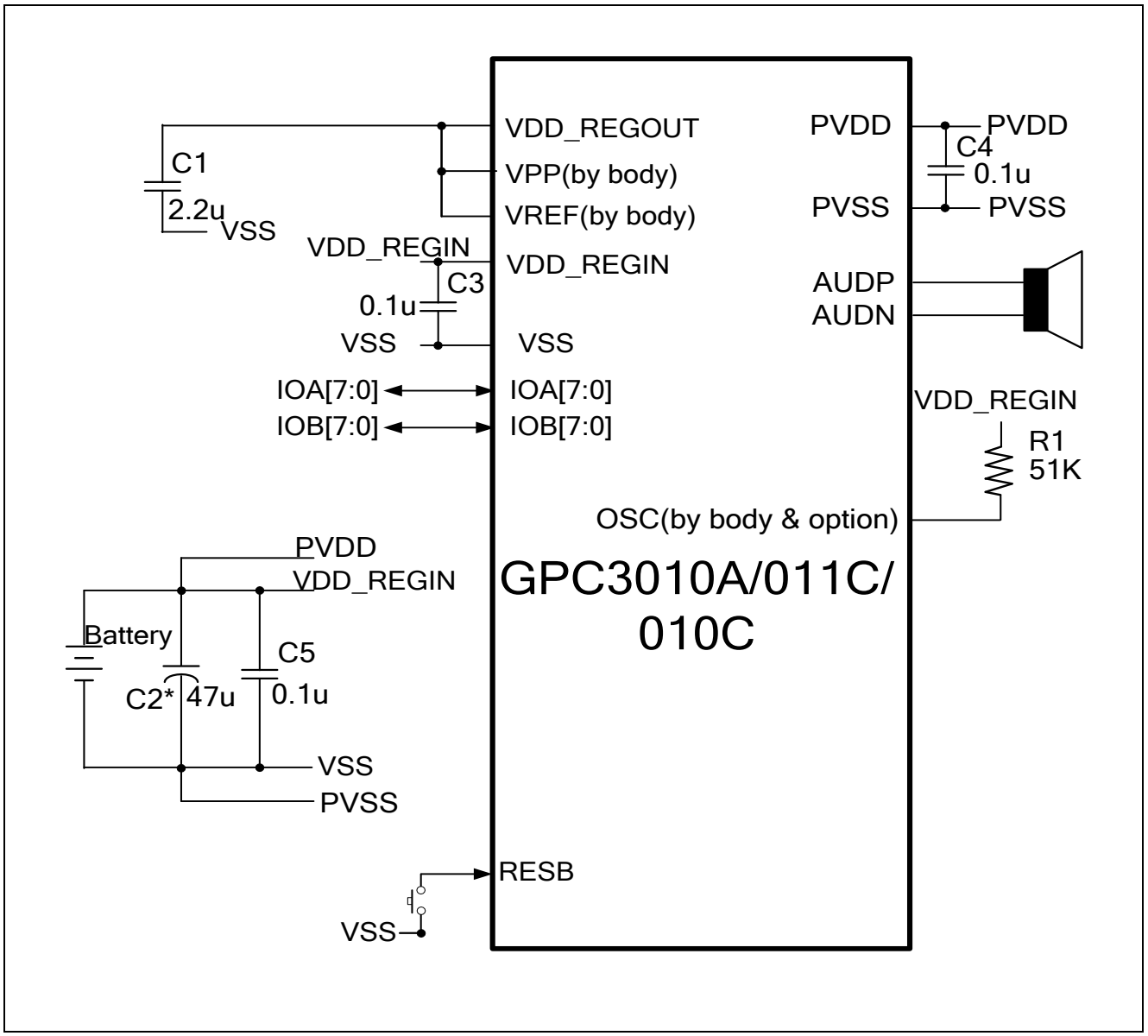
9.5. Application Circuits with Low Loading for GPC3010A/011C/010C



PCB Layout Guidelines:

1. VDD_REGIN and PVDD must be connected to power input port directly rather than the branch of each other.
2. PVDD can be higher than or equal to VDD_REGIN.
3. VSS and PVSS must be connected to ground input directly rather than the branch of each other.
4. C1 is suggested to 0.1uF~4.7uF, and should be increased for a high-volume application.

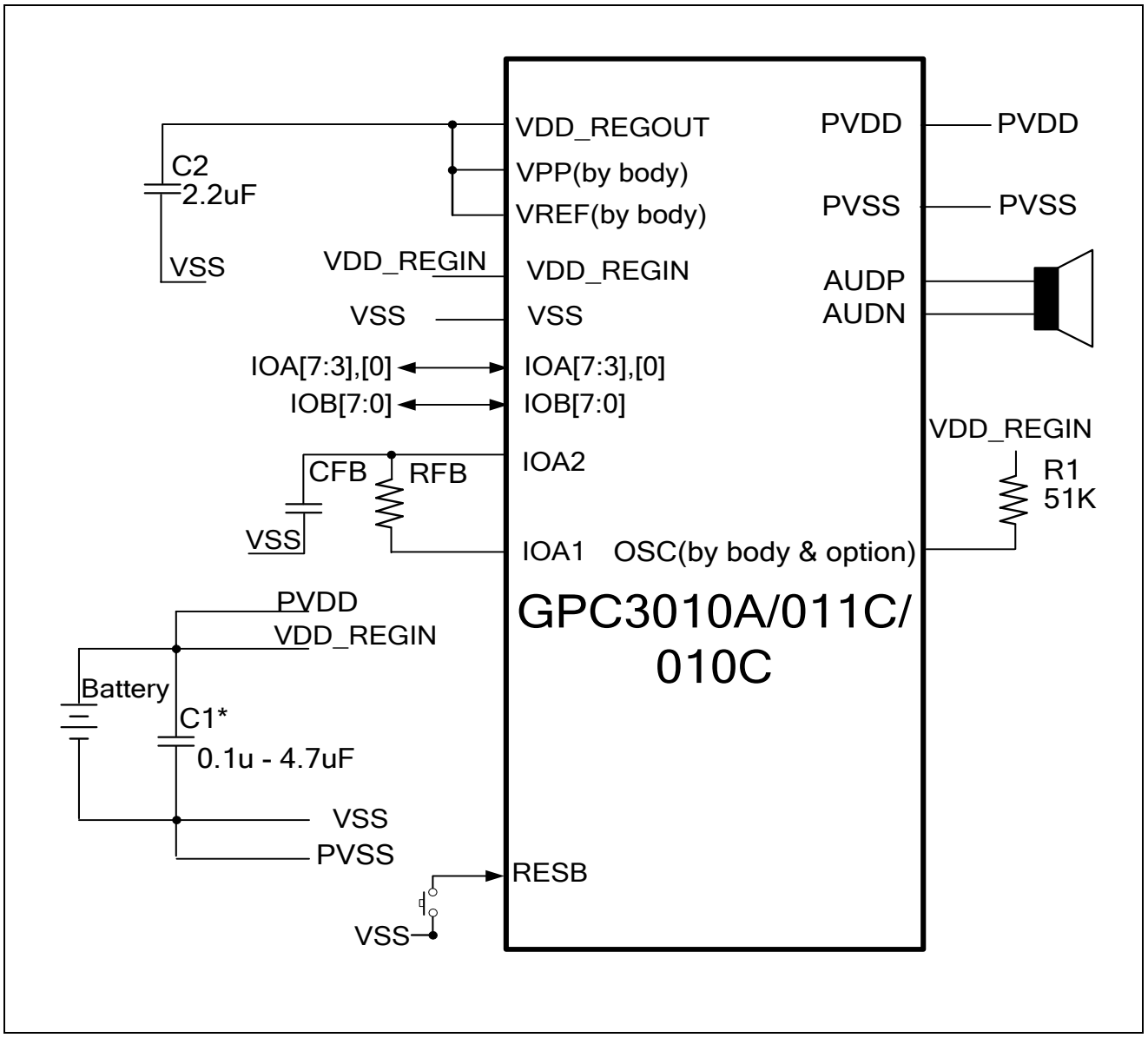
9.6. Application Circuits with Heavy Loading (Such as Motor, High Brightness LED) for GPC3010A/011C/010C



PCB Layout Guidelines:

1. VDD_REGIN and PVDD must be connected to power input port directly rather than the branch of each other.
2. PVDD can be higher than or equal to VDD_REGIN.
3. VSS and PVSS must be connected to ground input directly rather than the branch of each other.
4. The typical value of C2 is 47uF, and should be modified in different loading.

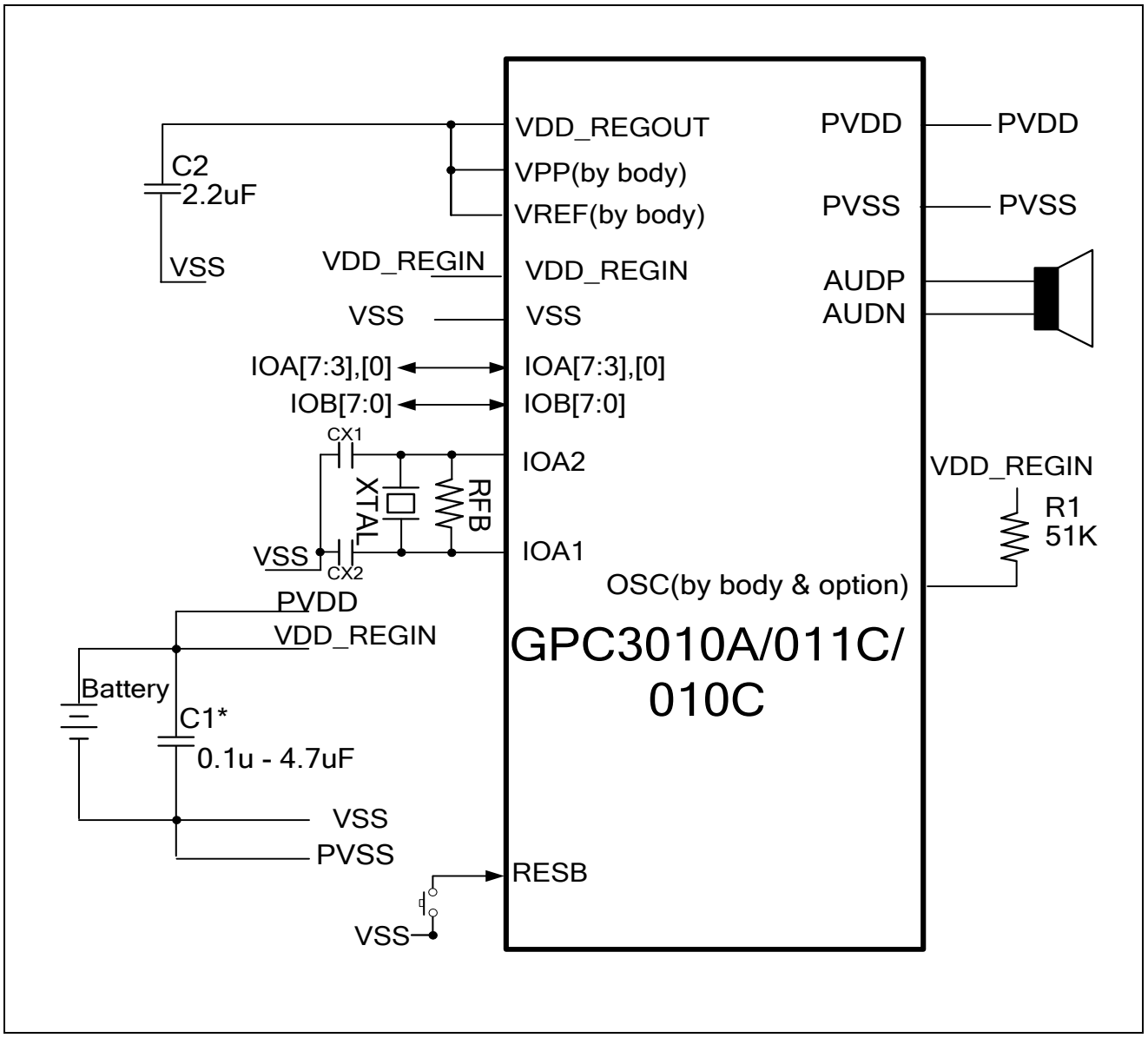
9.7. Application Circuits with Low Loading When Using Feedback RC Mode Enable for GPC3010A/011C/010C



PCB Layout Guidelines:

1. VDD_REGIN and PVDD must be connected to power input port directly rather than the branch of each other.
2. PVDD can be greater than or equal to VDD_REGIN.
3. VSS and PVSS must be connected to ground input directly rather than the branch of each other.
4. C1 is suggested 0.1uF~4.7uF, and should be increased for a high-volume application.

9.8. Application Circuits with Low Loading When Using Feedback XTAL Mode Enable for GPC3010A/011C/010C



PCB Layout Guidelines:

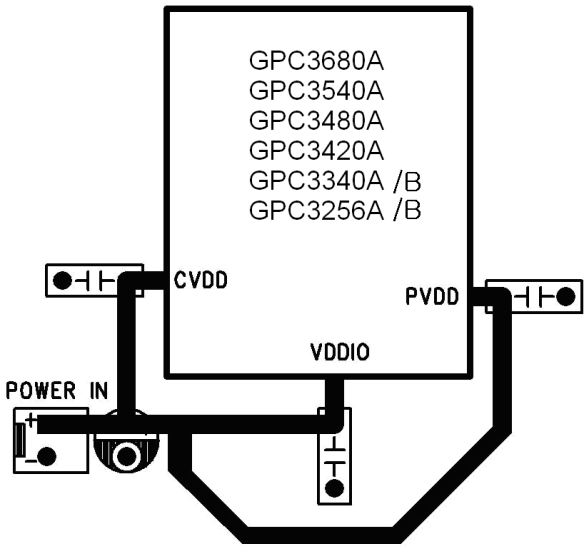
1. VDD_REGIN and PVDD must be connected to power input port directly rather than the branch of each other.
2. PVDD can be greater than or equal to VDD_REGIN.
3. VSS and PVSS must be connected to ground input directly rather than the branch of each other.
4. C1 is suggested 0.1uF~4.7uF, and should be increased for a high-volume application.

10. PCB LAYOUT GUIDE FOR HEAVY LOADING APPLICATION

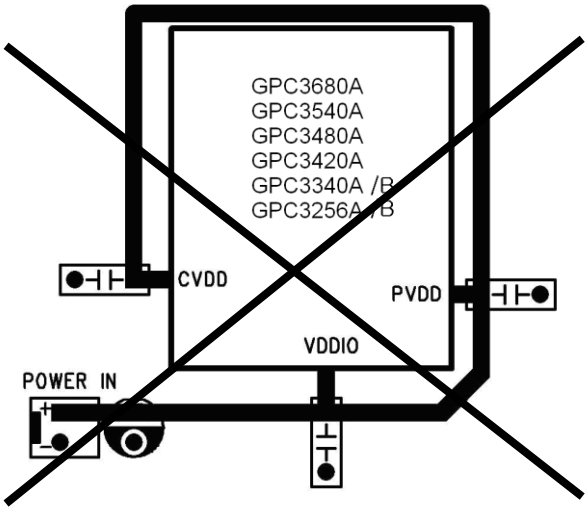
To avoid the unexpected noise, which may end up with incorrect CPU operations, the following cares must be exercised while designing a PCB layout:

1. Bond all VDD and VSS pins out.
2. The 0.1uF capacitor placed between VDD and VSS must be as close as possible to IC itself.
3. Power routes are as independent as possible.

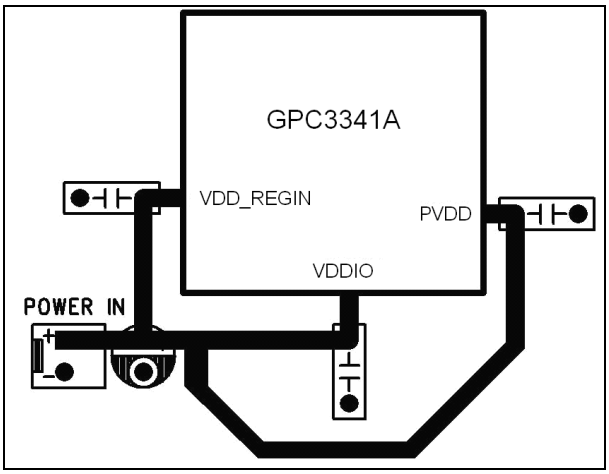
10.1. The PCB layout examples are given as follows (For GPC3680A~ GPC3256A, GPC3340B~ GPC33256B)



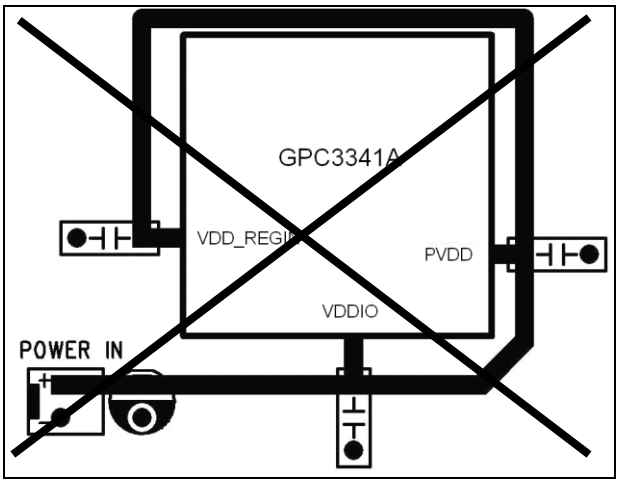
10.2. The PCB layout method (Power line connects in series) as below is *not proposed* (For GPC3680A~ GPC3256A, GPC3340B~ GPC33256B)



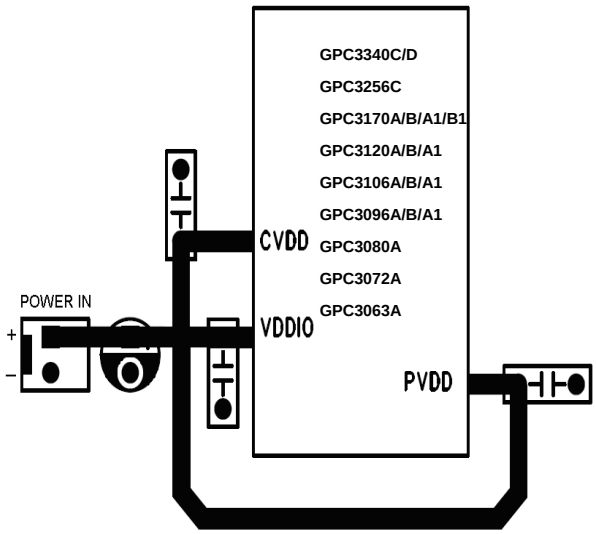
10.3. The PCB layout example is given as follows (For GPC3341A)



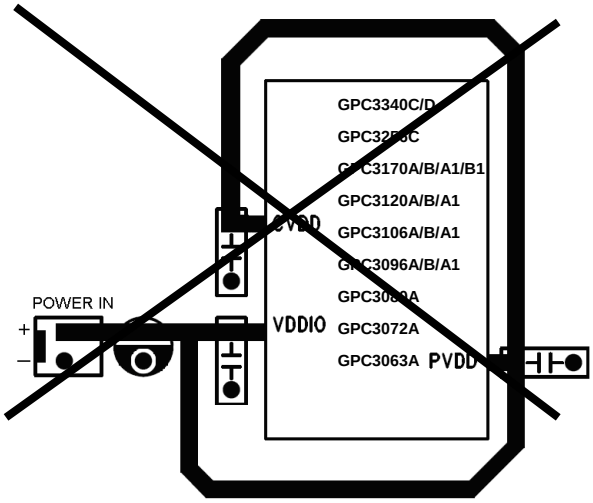
10.4. The PCB layout method (Power line connects in series) as below is *not proposed* (For GPC3341A)



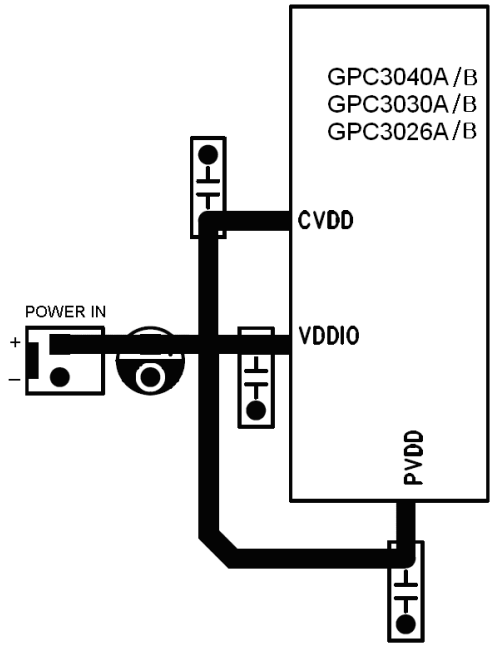
10.5. The PCB layout examples are given as follows (For GPC3170A~ GPC3052A, GPC3170B~ GPC3092B, GPC3340C/D, GPC3256C, GPC3170A1~GPC3096A1, GPC3170B1)



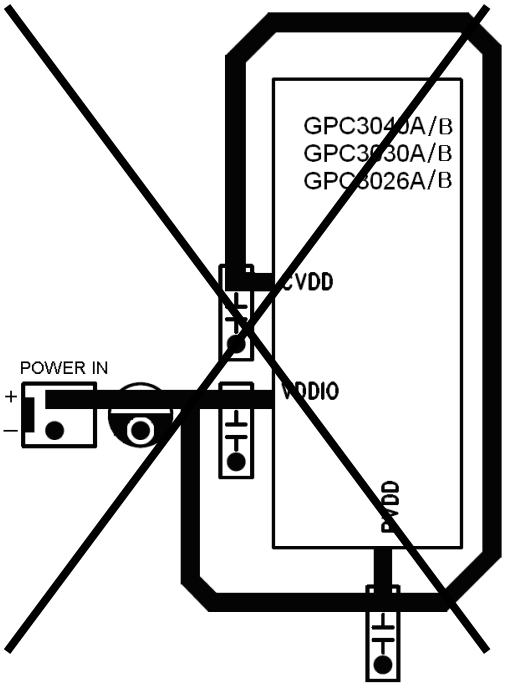
10.6. The PCB layout method (Power line connects in series) as below is *not proposed* (For GPC3170A~ GPC3052A, GPC3170B~ GPC3092B)



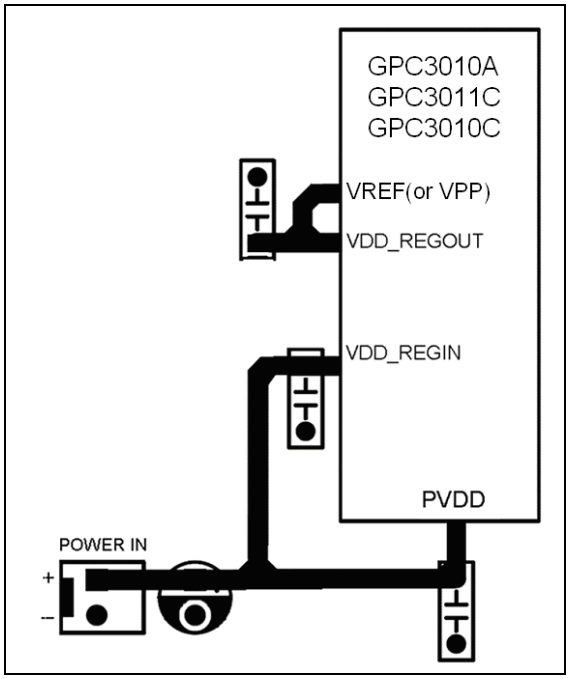
10.7. The PCB layout examples are given as follows (For GPC3040A/B~GPC3026A/B)



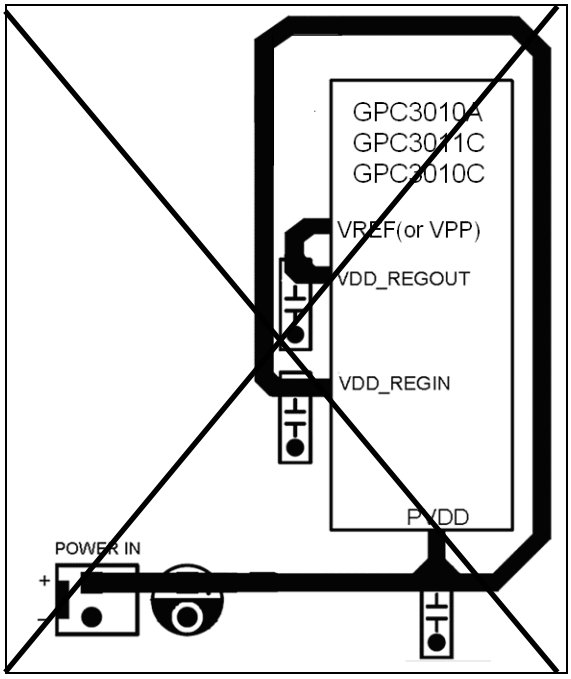
10.8. The PCB layout method (Power line connects in series) as below is *not proposed* (For GPC3040A/B~GPC3026A/B)



10.9. The PCB layout examples are given as follows (For GPC3010A/011C/010C)



10.10. The PCB layout method (Power line connects in series) as below is *not proposed* (For GPC3010A/011C/010C)



11. PACKAGE/PAD LOCATIONS

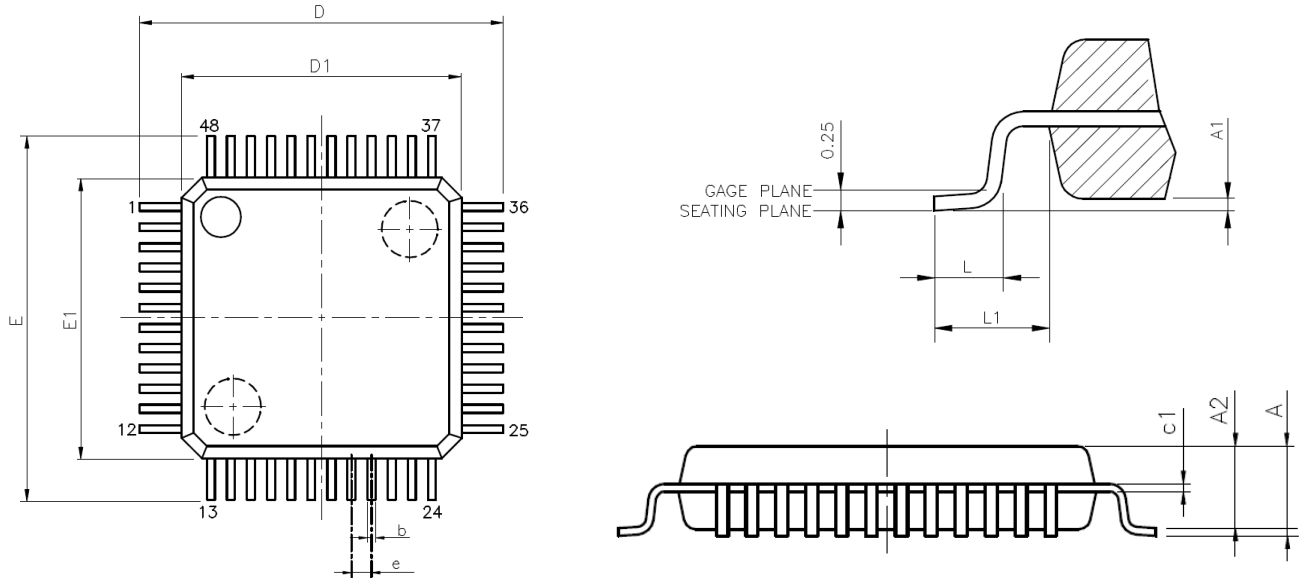
11.1. Ordering Information

Product Number	Package Type
GPC3XXXAx/Bx/Cx/Dx - NnnV - C	Chip form
GPC3XXXAx/Bx/Cx/Dx - NnnV - QL23X	Halogen free LQFP48 package
GPC3XXXAx/Bx/Cx/Dx - NnnV - QL09X	Halogen free LQFP128 package
GPC3XXXAx/Bx/Cx/Dx - NnnV - G08X	Halogen free SSOP20 package

Note1: Code number is assigned for customer.

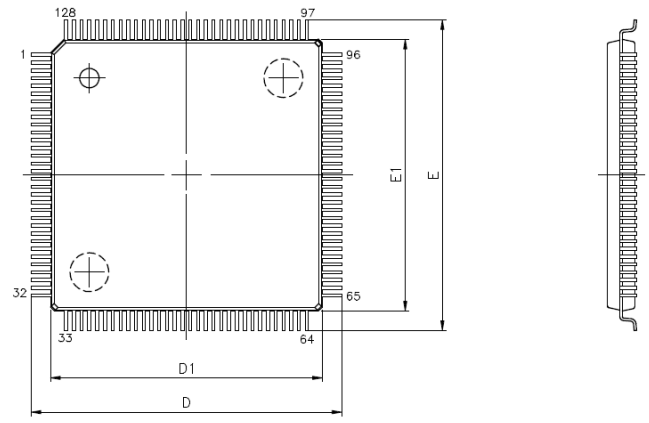
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

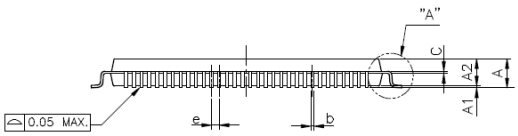
11.2. LQFP48 Information

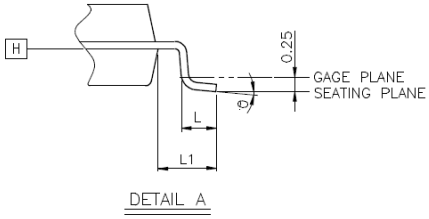


SYMBOLS	Min.	Max.
A	-	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
B	0.17	0.27
L	0.45	0.75
L1	1 REF	

11.3. LQFP128 Information







DETAIL A

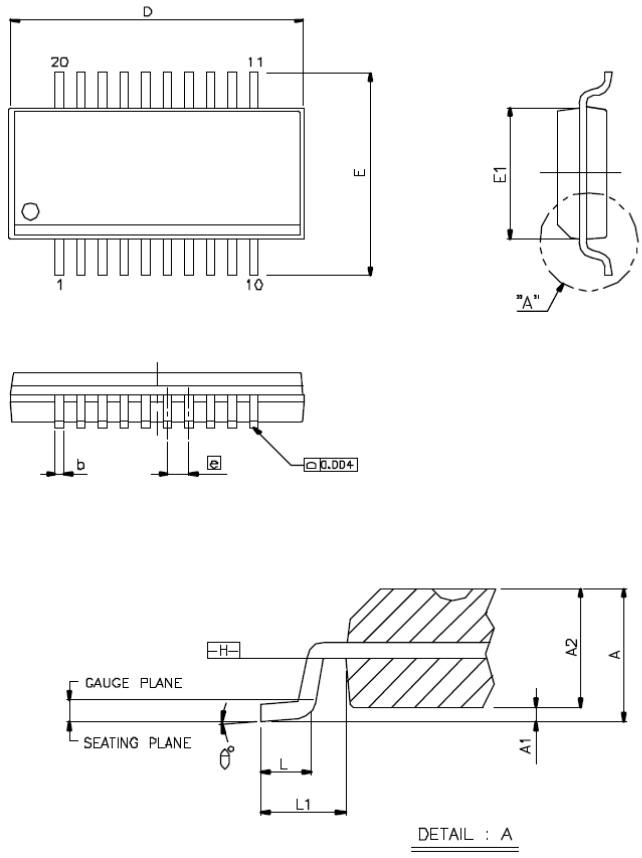
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
c	0.09	--	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:

1. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

11.4. SSOP20 Information



SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	–	–	0.059
b	0.008	–	0.012
C	0.007	–	0.010
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0°	–	8°

UNIT : INCH

NOTES:

1 JEDEC OUTLINE : MO-137 AD

2 DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST

12. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

13. REVISION HISTORY

Date	Revision #	Description	Page
Aug. 28, 2017	2.3	1. Add SSOP20 information. 2. Add LQFP48 information for GPC3010A/C	16-17 11
Jun 02, 2017	2.2	1. Add LQFP48 and LQFP128 information.	11-15,37,38
Apr. 18, 2017	2.1	1. Add GPC3340C/D, GPC3256C, GPC3170A1~GPC3096A1, GPC3170B1 bodies and related information. 2.Modify document title name：GPC3XXXX → GPC3XXXAx/Bx/Cx/Dx.	1-32
Sep. 23, 2014	2.0	1.Add notice pull low R with 1M Ohm only for GPC3340B, GPC3256B, GPC3170B, GPC3120B, GPC3106B, and GPC3092B. 2.Add notice PVDD **can be greater than or equal to** CVDD for GPC3040B, GPC3030B, GPC3026B. 3.Modify GPC3011C/10C IROSC frequency vs VDD dependence	5-7,26-27, 7-10,26-33, 25
Dec. 13, 2011	1.0	Original	32