DATA SHEET

GPC252A

256KB Sound Controller

FEB. 23, 2006

Version 1.0

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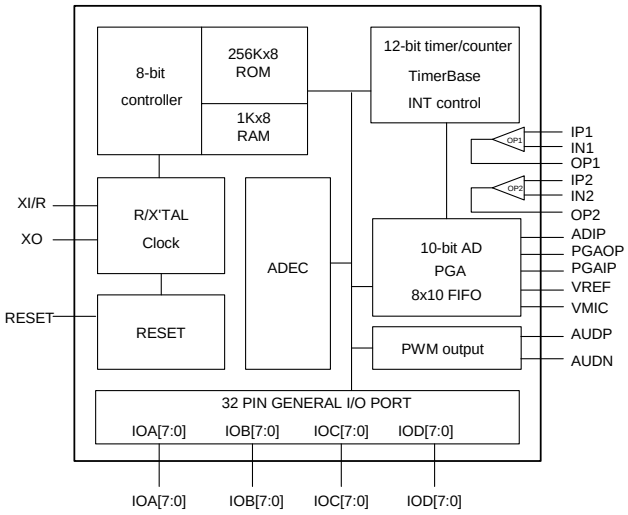
256KB SOUND CONTROLLER

1. GENERAL DESCRIPTION

The GPC252A is a CPU based two-channel speech/melody synthesizer which includes a CMOS 8-bit microprocessor, 256K-byte ROM for speech and melody data (speech compressed by a 4-bit ADPCM with approx. 85 sec speech duration @ 6KHz sampling rate) and 1K-byte working SRAM. In addition, it includes two timer/counters, 10-bit ADC, PGA, 8 x 10 FIFO, two OP Amp., 32 software programmable I/Os, and one PWM audio output. For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V. The Low Voltage Reset function automatically resets CPU whenever the working voltage drops below 2.2V. Moreover, GPC252A has a Clock Stop mode for power savings that saves the RAM contents, but freezes the oscillator. The Clock Stop mode makes all other functions inoperative. The maximum CPU clock frequency is 5.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) - 6 clock cycles (max.). The GPC252A includes, not only the latest technology, but also the full commitment and technical support of Generalplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- Provides 256K-byte ROM for program and audio data
- 1K-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 5.5V @ 5.0MHz
- Supports Crystal Resonator or R_{OSC} (with Mask option)
- Max. CPU clock: 5.0MHz @ 2.4V - 5.5V
- Standby mode (Clock Stop mode) for power savings. Max. 2.0μA @ 5.0V
- 400ns instruction cycle time @ 5.0MHz CPU clock
- Provides 32 general I/Os
- Two 12-bit timer/counters
- 6 INT sources
- Key wake-up function
- 10-bit ADC and PGA
- Two independent OP Amp.
- 8 x 10 FIFOs
- One PWM audio output (single speaker)
- Low Voltage Reset (with mask option)
- Approx. 85 sec speech @ 6.0KHz sampling rate with 4-bit ADPCM

4. APPLICATION FIELD

- Intelligent educational toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- High-end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS*

Mnemonic	PIN No.	Type	Description
VDD	18 38 51	I	VDD for I/O and logic circuit
PVDD	47	I	VDD for audio output
VSS	9 33 60	I	GND for I/O and logic circuit
PVSS	49	I	GND for audio output
AVDD	19	I	VDD for analog circuit
VMIC	20	O	Microphone voltage
VREF	21	O	Reference voltage
IP1	22	I	OP1 non-invert input
IN1	23	I	OP1 invert input
OP1	24	O	OP1 output
VDACT	25	O	DAC output for test mode measure use only
OP2	26	O	OP2 output
IN2	27	I	OP2 invert input
IP2	28	I	OP2 non-invert input
PGAIP	29	I	PGA input
PGAOP	30	O	PGA output
ADIP	31	I	ADC input
AVSS	32	I	Analog ground
XI	34	I	Oscillator crystal input or RESISTOR (Resistor should be connected to VDD)
XO	35	O	Oscillator crystal output
TEST	36	I	Test pin, NC
RESET	37	I	Active low reset for the chip
AUDP AUDN	50 48	O O	Audio output
IOA0 IOA1 IOA2 IOA3 IOA4 IOA5 IOA6 IOA7	1 2 3 4 5 6 7 8	I/O I/O I/O I/O I/O I/O I/O I/O	Port A is an 8-bit bi-directional Input / Output port with Pull-high or Open-drain option. As inputs, Port A can be in either the Pure or Pull-high states. As outputs, Port A3 - 0 can be either Buffer or Open-drain NMOS types (Sink current). Port A7 - 4 can be either Buffer or Open-drain PMOS types (Send current) **See note 1 and 2 below.
IOB0 IOB1 IOB2 IOB3 IOB4 IOB5 IOB6 IOB7	10 11 12 13 14 15 16 17	I/O I/O I/O I/O I/O I/O I/O I/O	Port B is an 8-bit bi-directional Input / Output port with Pull-low or Open-drain option. As inputs, Port B can be in either the Pure or Pull-low states. As outputs, Port B can be either Buffer or Open-drain NMOS types (Sink current). **See note 1 and 2 below.
IOC0 IOC1	59 58	I/O I/O	Port C is an 8-bit bi-directional Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can

Mnemonic	PIN No.	Type	Description
IOC2	57	I/O	be a Buffer type or Open-drain type. Port C3 - 0 are Open-drain NMOS type (Sink
IOC3	56	I/O	current) and Port C7 - 4 are Open-drain PMOS (Send current).
IOC4	55	I/O	IOC0: EXT RC-OSC OUTPUT
IOC5	54	I/O	IOC2: EXT RC-OSC INPUT / EXT COUNT IN
IOC6	53	I/O	
IOC7	52	I/O	**See note 1 and 2 below.
IOD0	46	I/O	Port D is an 8-bit bi-directional Input / Output port with Pull-low or
IOD1	45	I/O	Open-drain option. As inputs, Port D can be either buffer or Open-drain PMOS (Send
IOD2	44	I/O	current). Also, Port D can be software programmed for wake-up I/O pins.
IOD3	43	I/O	(Programmable I/O, Key Change, Wake-up I/O).
IOD4	42	I/O	
IOD5	41	I/O	
IOD6	40	I/O	
IOD7	39	I/O	**See note 1 and 2 below.

* Refer to GPC Programming Guide for more information.

**Note: 1.) Two input states can be specified: Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified: Buffer output, Open Drain PMOS output <send>, Open Drain NMOS output<sink>.

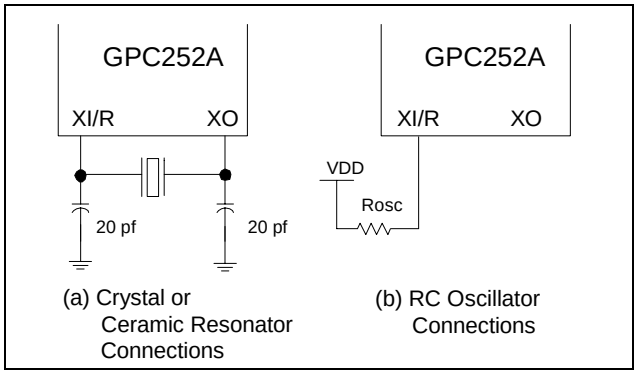
6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The 8-bit microprocessor of GPC252A is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (it is the same as the 6502 instruction structure). GPC252A is able to perform with 5.0MHz (max.) depending on the application specifications.

6.2. Oscillator

The GPC252A supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources by mask option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL / ROSC circuits for most applications:



(a) Crystal or Ceramic Resonator Connections

(b) RC Oscillator Connections

6.3. Mask Option

The GPC252A has the following mask option:

- Supports Crystal Resonator or R_{OSC} with mask option.

6.4. ROM Area

The GPC252A provides a 256K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register; choose bank, and access address to fetch data.

6.5. RAM Area

The total RAM consists of 1K bytes (including Stack) at locations from $80 through $47F.

6.6. Map of Memory and I/Os

*I/O PORT:

- PORT IOA $0002
  IOB $0003
  IOC $0004
  IOD $0005
- I/O CONFIG $0000
  $0001

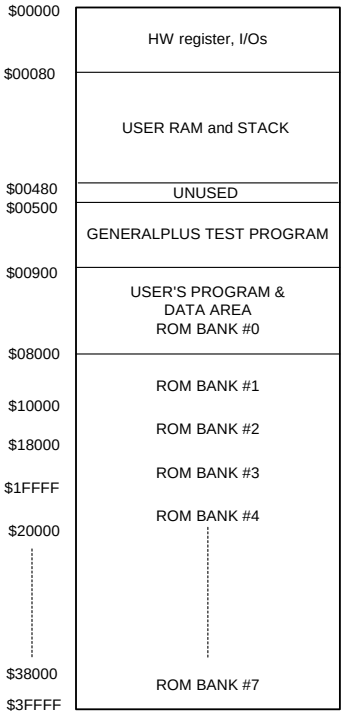
*NMI SOURCE:

- INTA (from TIMER A)

*INT SOURCE:

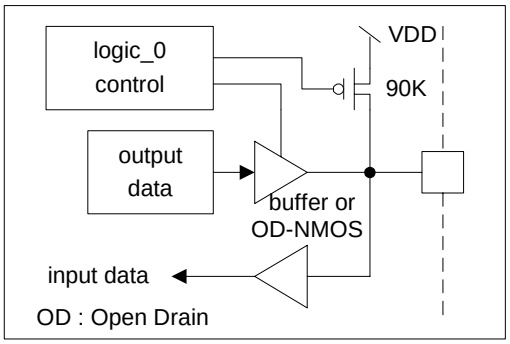
- INTA (from TIMER A)
- INTB (from TIMER B)
- CPU CLK / 1024
- CPU CLK / 8192
- CPU CLK / 65536
- EXT INT

*MEMORY MAP (From ROM view)

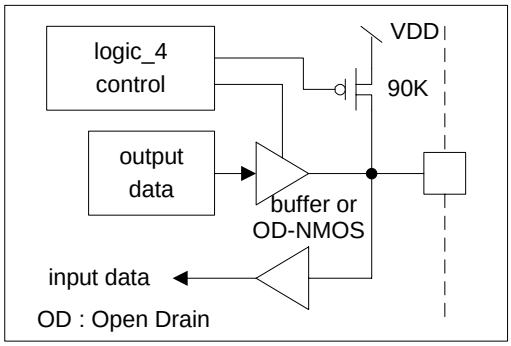


6.7. I/O Port Configuration*

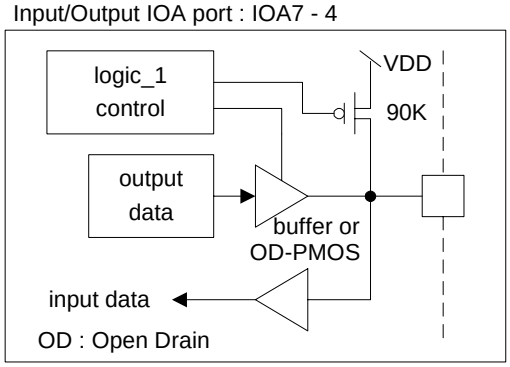
Input/Output IOA port : IOA3 - 0



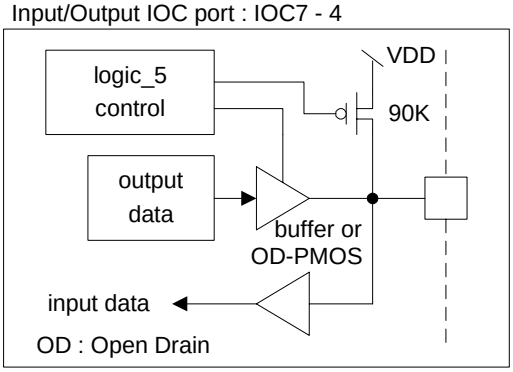
Input/Output IOC port : IOC3 - 0



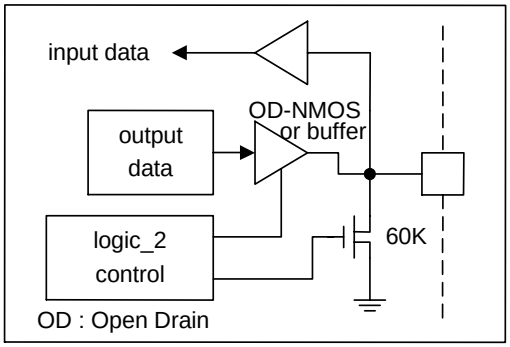
Input/Output IOA port : IOA7 - 4



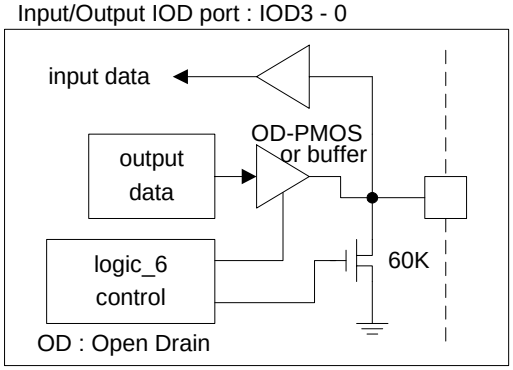
Input/Output IOC port : IOC7 - 4



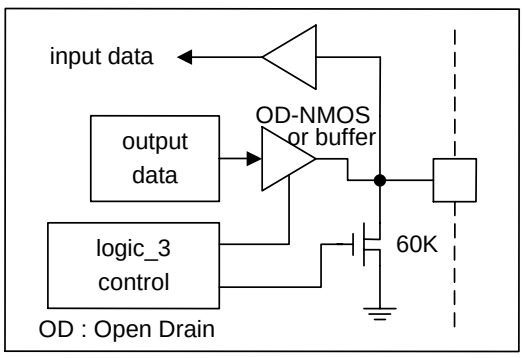
Input/Output IOB port : IOB3 - 0



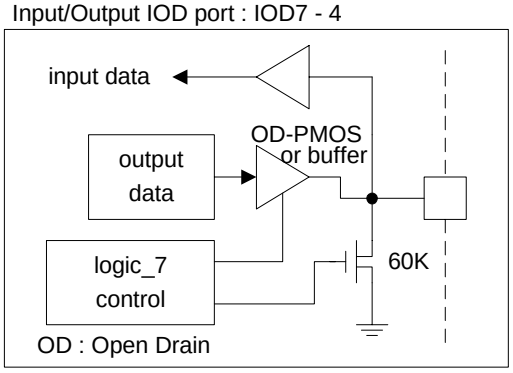
Input/Output IOD port : IOD3 - 0



Input/Output IOB port : IOB7 - 4



Input/Output IOD port : IOD7 - 4



* Figures shown are for VDD = 5.0V test conditions only.

6.8. Timer/Counter

The GPC252A contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal will make the timer automatically reload to the user's pre-set value and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is used as a counter, users can reset it by loading "0" into the counter. After the counter has been activated, the value of the counter can also be read from the counter at the same time.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

6.9. ADC (Analog to Digital Converter)

The way to make AD work is using an ADC (analog-to-digital converter) to send a hypothetical data and compare it with input signal by comparator. GPC252A determines the actual value in two ways, auto mode and manual mode. In auto mode, hardware automatically creates a value for binary search by SAR (successive-approximation register) and will acquire a 10-bit PCM data at the end of search. During converting, system controls sample/hold hardware by its own. The second method is manual mode. Within this mode, users can use their own algorithms such as DM, ADM, PCM, ADPCM, etc. In the auto mode, users are required only to setup the right sample frequency by setting Timer B, and system enters into auto DAC mode. Moreover, users can also use FIFO to reduce interrupt redundancy to improve the performance. In manual mode, users need to send the hypothetical value into DAC register and read the compared result back from hardware to decide whether the hypothetical value is lower or higher than the actual input signal. Within this mode, FIFO is disabled and users need to control sample and hold on their own.

6.10. Power Savings Mode

The GPC252A provides a power savings mode (standby mode) for applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. As a result, the CPU goes to the stand-by mode. In such a mode, RAM and I/Os remain in their previous states until being awoken. Port IOD7 - 0 is the only wake-up source in the GPC252A. After the GPC252A is awoken, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and then continue to execute the program. Wakeup Reset will not influence RAM or I/Os (FIG.1).

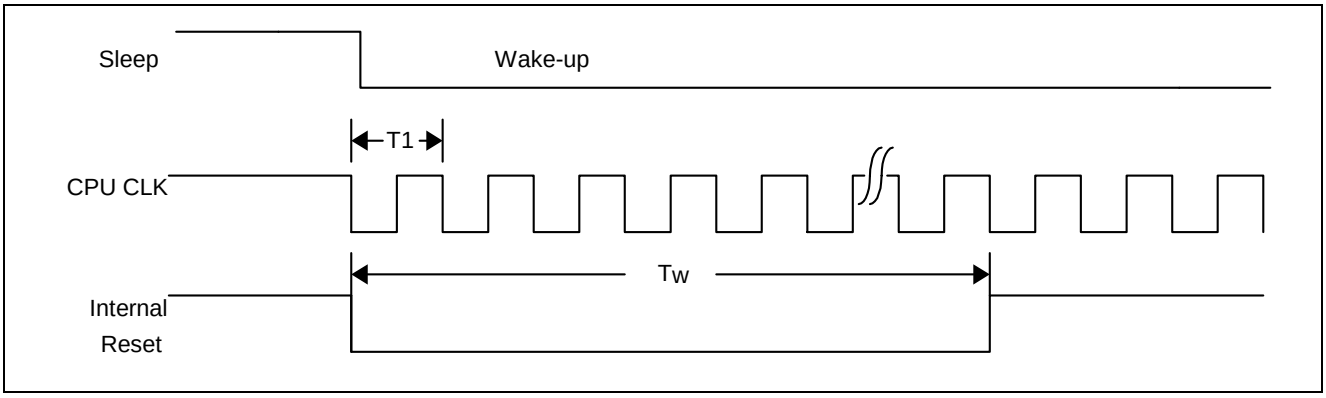
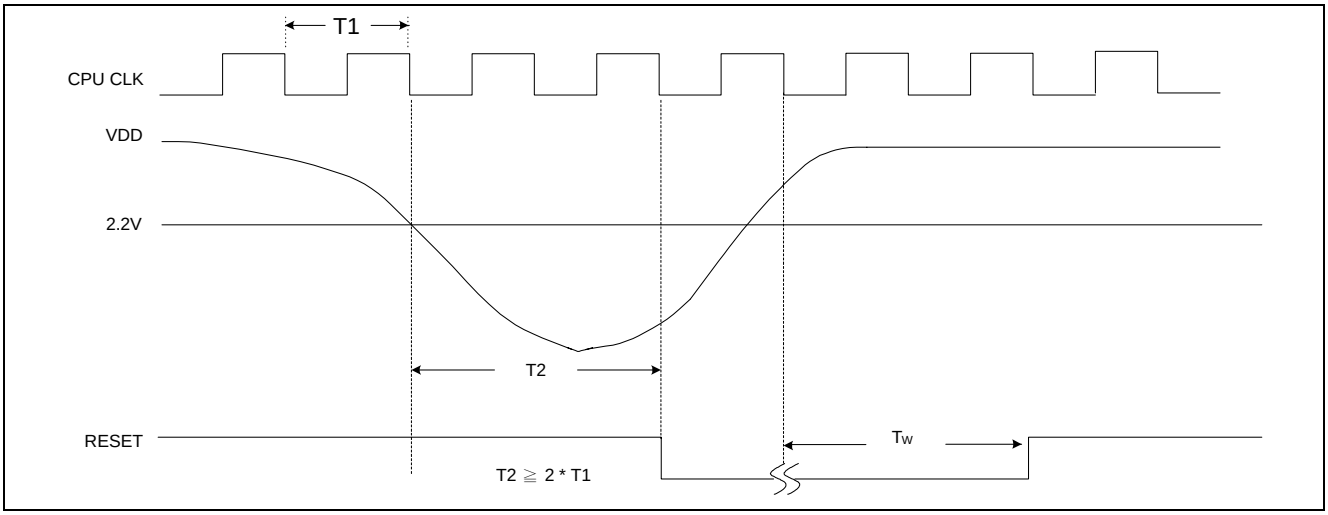


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧ 65536 x T1

6.11. Low Voltage Reset

The GPC252A includes a Low Voltage Reset (LVR) function. Below the minimum power-supply voltage of 2.2V, the CPU system will become unstable and malfunction. Low Voltage Reset will reset all functions into the initial operational (stable) state if the VDD power-supply voltage drops below 2.2V (FIG.2) (with mask option).



(The LVR function is the same as Power ON Reset or External Reset.)

FIG. 2

6.12. FIFOs

GPC252A provides a FIFO with (8+1) (depth) x 10(width). FIFO reduces the time to fetch ADC sample data. It only works when auto mode ADC is enabled. There are two flags users can read, Empty Flag and Full Flag. The Empty Flag indicates the FIFO status when FIFO is empty. The Full Flag represents FIFO status when FIFO is equal or great than FIFO depth samples. For example, suppose users setup FIFO as FIFO depth to 4 samples, once FIFO received 4 samples without any data read by CPU (which means FIFO keeps the amount of samples inside), the Full Flag will active. The FIFO dedicates (8+1) x 10 depth which means the maximum data FIFO can store is 8 samples plus one over-come sample. Once FIFO over-run (means data is still coming while FIFO is keeping 9 samples already), the last coming data will overwrite the 9^{th} data in FIFO regardless the assignment of FIFO depth. FIFO can be re-initialized or cleared by power on reset, writing data to setup FIFO depth, setting to manual mode or turning-off the ADC_EN.

6.13. Speech and Melody

Since the GPC252A provides a large ROM and high CPU operating speeds, it is one of the most suitable devices for speech and melody synthesis. For speech synthesis, the GPC252A can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM. For melody synthesis, the GPC252A provides dual tone mode. Once the GPC252A enters the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to the tone frequency for each channel, and count the envelope of each channel. The hardware will toggle the tone wave automatically without INT.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Bias Current	I_{BIAS}	-	1.0	5.0	μA	-
Input Offset Voltage	V_{OFFSET}	-	10	-	mV	-
Slew Rate		-	0.5	-	V/μs	VDD = 5.0V
Output Voltage Swing		0.2	-	VDD - 0.2	V	-
Input Impedance		-	1.2	-	MΩ	-
ADC Reference Voltage	V_{REF}	1.1	1.3	1.5	V	-
ADC Input Range	V_{IN}	V_{REF} - 1/2V_{REF}	-	V_{REF}+ 1/2V_{REF}	V	-
VMIC Output Current	I_O	-	2.0	-	mA	When VDD = 2.4V, V_o = 2.0V

7.3. DC Characteristics (VDD = 3.0V, T_A = 25℃)

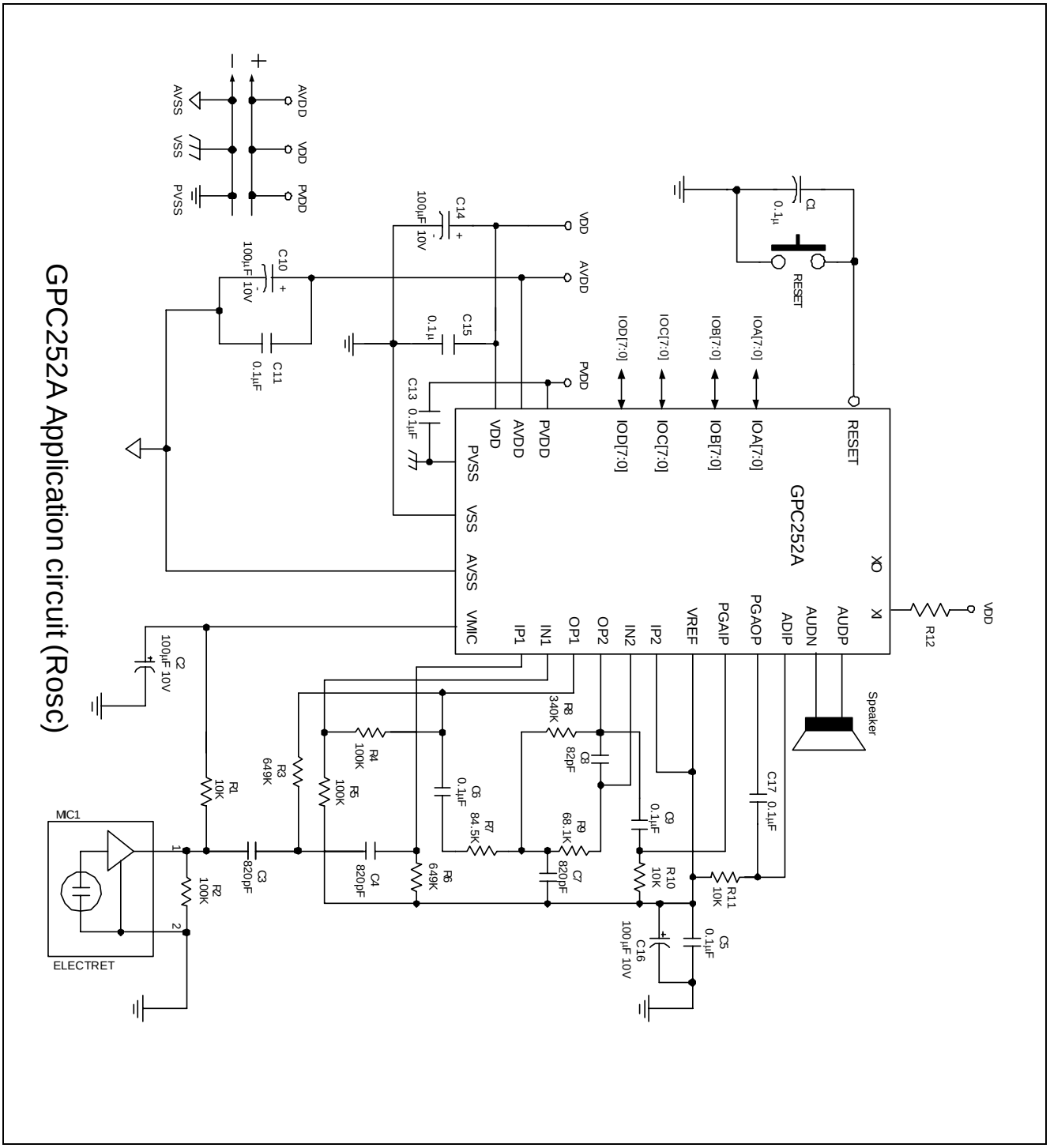
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	6.0	-	mA	F_{CPU} = 3.58MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
PWM Output High I	I_{POH1}	-	-80	-	mA	VDD = 3.0V, V_{OH} = 2.5V For one channel
PWM Output High I	I_{POH2}	-	-140	-	mA	VDD = 3.0V, V_{OH} = 2.0V For one channel
PWM Output Low I	I_{POL1}	-	80	-	mA	VDD = 3.0V, V_{OL} = 0.5V For one channel
PWM Output Low I	I_{POL2}	-	140	-	mA	VDD = 3.0V, V_{OL} = 1.0V For one channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output high I (IOA, IOC, IOD)	I_{OH}	-1.0	-2.0	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output low I (IOA, IOC, IOD)	I_{OL}	3.0	5.0	-	mA	VDD = 3.0V, V_{OL} = 0.8V
Input Resistor (IOA, IOC)	R_{IN}	-	220	-	KΩ	Pull-high, VDD = 3.0V
Input Resistor (IOD)	R_{IN}	-	90	-	KΩ	Pull-low, VDD = 3.0V

7.4. DC Characteristics (VDD = 5.0V, T_A = 25℃)

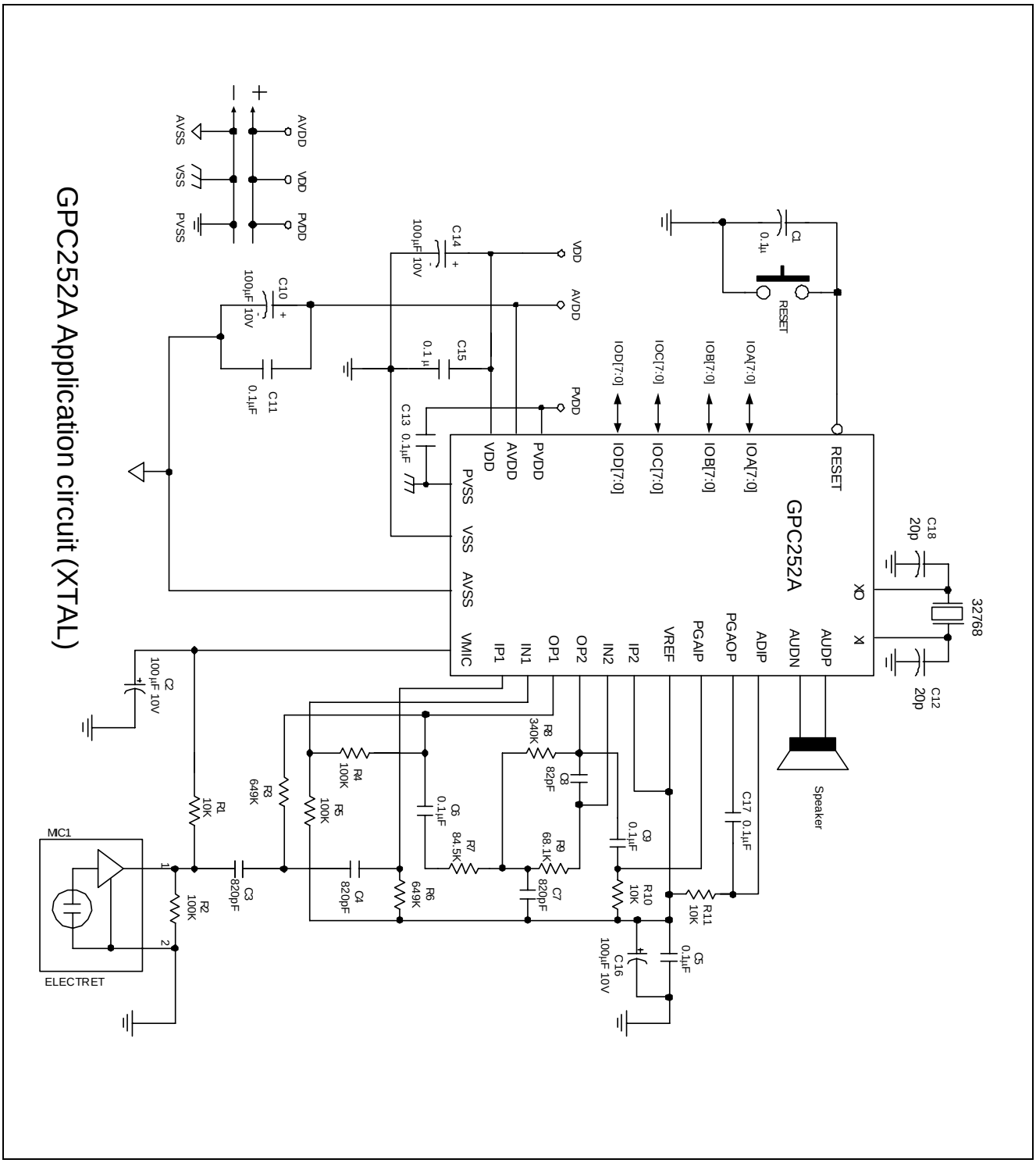
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	9.5	-	mA	F_{CPU} = 4.0MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
PWM Output High I	I_{POH1}	-	-155	-	mA	VDD = 5.0V, V_{OH} = 4.2V For one channel
PWM Output High I	I_{POH2}	-	-300	-	mA	VDD = 5.0V, V_{OH} = 3.3V For one channel
PWM Output Low I	I_{POL1}	-	175	-	mA	VDD = 5.0V, V_{OL} = 0.8V For one channel
PWM Output Low I	I_{POL2}	-	310	-	mA	VDD = 5.0V, V_{OL} = 1.67V For one channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output high I (IOA, IOC, IOD)	I_{OH}	-1.0	-3.5	-	mA	VDD = 5.0V, V_{OH} = 4.2V
Output low I (IOA, IOC, IOD)	I_{OL}	4.0	8.0	-	mA	VDD = 5.0V, V_{OL} = 0.8V
Input Resistor (IOA, IOC)	R_{IN}	-	110	-	KΩ	Pull-high, VDD = 5.0V
Input Resistor (IOD)	R_{IN}	-	50	-	KΩ	Pull-low, VDD = 5.0V

8. APPLICATION CIRCUITS

8.1. Application Circuit - (1)

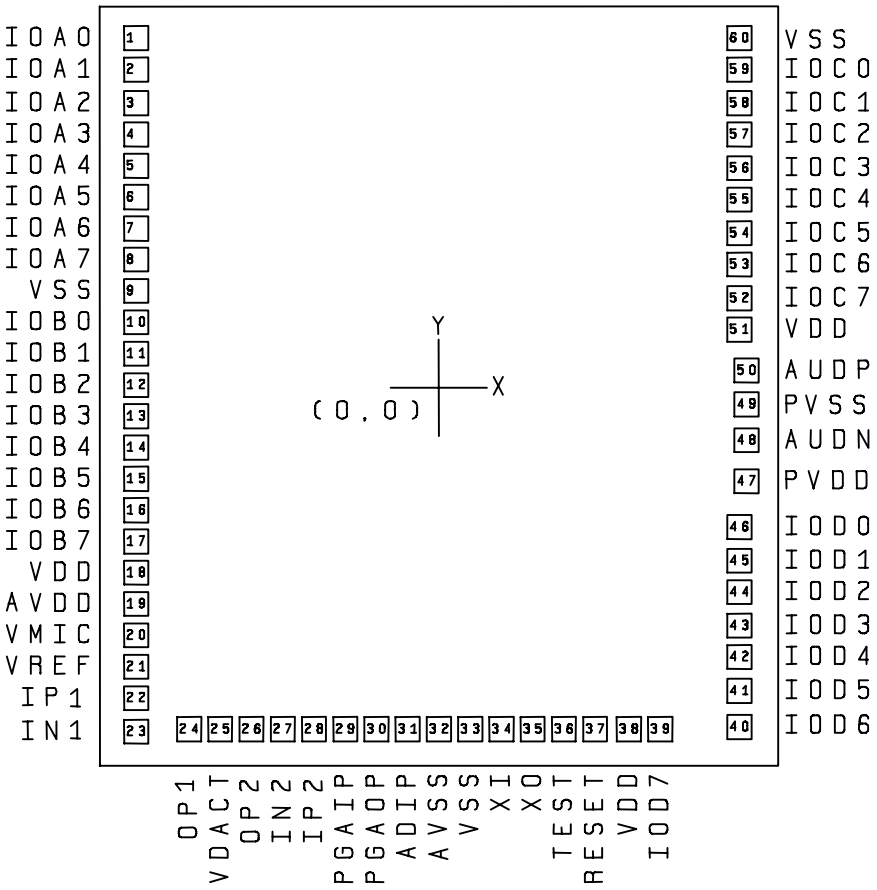


8.2. Application Circuit - (2)



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: To ensure IC function properly, please bond all of the VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
GPC252A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 23, 2006	1.0	Original Note: The GPC252A data sheet v1.0 is a continued version of SPC252A data sheet v0.4.	17