DATA SHEET

GPC11128A2/
GPC11112A2/
GPC11096A2/
GPC11080A2

Sound Controller Series

Sep 02, 2015

Version 1.0

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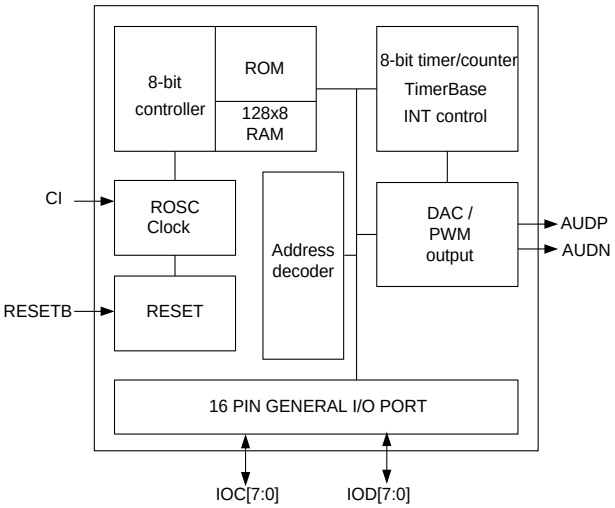
SOUND CONTROLLER SERIES

1. GENERAL DESCRIPTION

This series, a speech/wavetable synthesizer, equips an 8-bit CMOS microprocessor, 128-byte working SRAM, and working ROM memory (ROM size may vary on different series.). Other primary features include two 8-bit timers/counters or one combined 16-bit timer/counter, 16 software selectable I/Os, one 8-bit DAC, and a pair of PWM outputs. It operates at a wide voltage range from 2.1V through 5.5V. In addition, a Clock Stop mode is designed for power savings. The unique power saving mode saves the RAM contents, but it freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) to six clock cycles (max.).

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- Various working ROM memory (refer to the ROM size table)
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.1V* - 5.5V @ 6.0MHz
  3.6V - 5.5V @ 8.0MHz

*Under about 2.1V, the system clock will slow down substantially.

- **Supports ROSC only**
- Max. CPU clock: 6.0MHz @ 3.0V, 8MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2.0μA @ 5.0V
- 16 general I/Os
- Two 8-bit timers/counters or combined to one 16-bit timer/counter
- Six INT sources
- Key wakeup function
- IR function
- External feedback input
- Watchdog function
- **One 8-bit DAC and a pair of PWM outputs**

ROM sizes in different series.

Body	ROM size
GPC11128A2	128KB
GPC11112A2	112KB
GPC11096A2	96KB
GPC11080A2	80KB

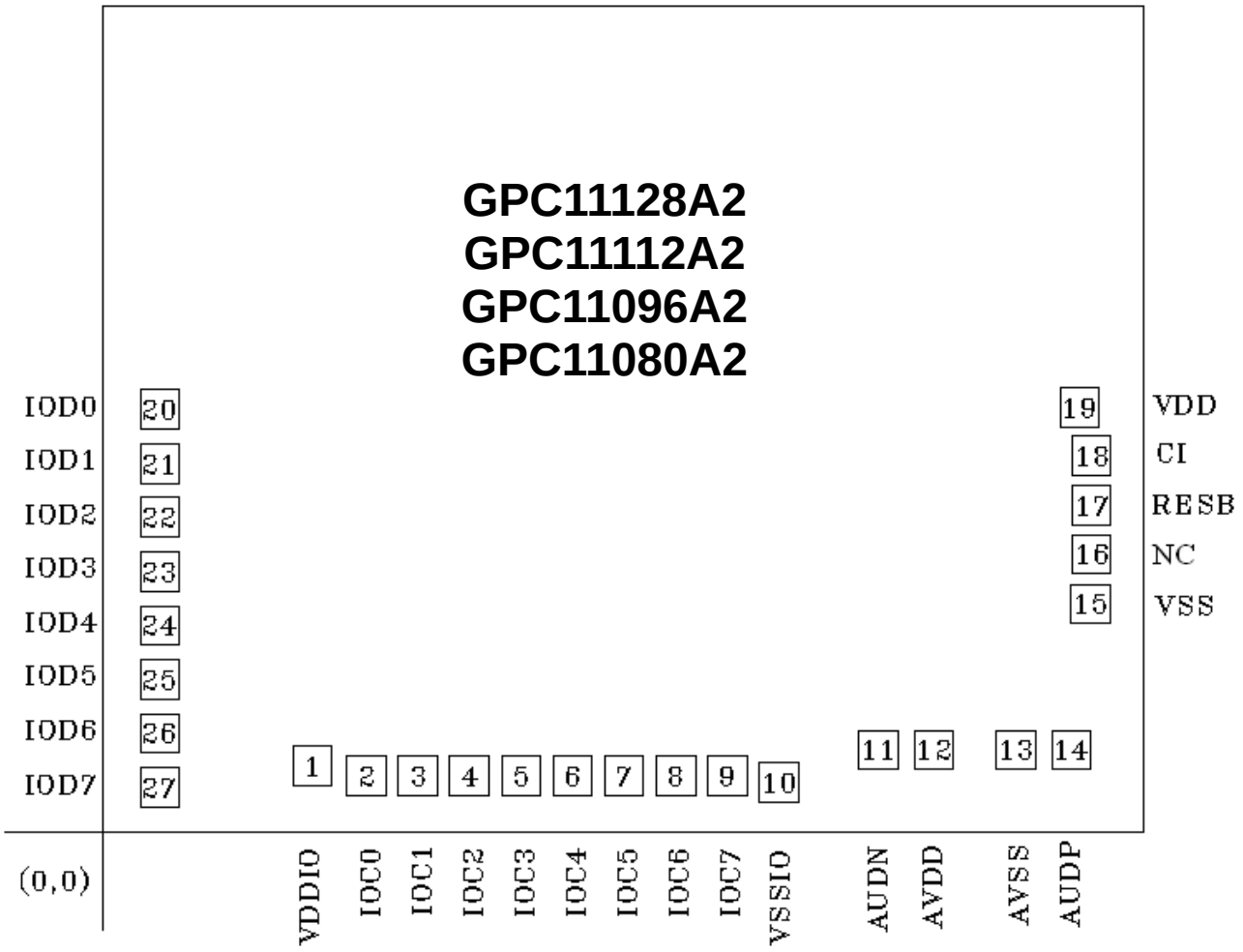
4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No	Type	Description
VDDIO	1	I	lOs PAD Power
VSSIO	10	I	IOs PAD Ground
VDD	19	I	Digital Power
VSS	15	I	Digital Ground
AVDD	12	I	Audio PWM Power Pad
AVSS	13	I	Audio PWM Ground
CI	18	I	ROSC Resistor input (Resistor must be connected to VDD)
RESETB	17	I	RESETB pin, active low to reset the whole system
TEST	16	I	TEST pin, NC
AUDP	14	O	Audio OUTPUT1
AUDN	11	O	Audio OUTPUT2
IOC0	2	I/O	Port C is an 8-bit bi-directional programmable input/output port with pull-low. In input mode, Port C can be either pure or pull-low state. In output mode, Port C can be a buffer.
IOC1	3	I/O	
IOC2	4	I/O	
IOC3	5	I/O	
IOC4	6	I/O	
IOC5	7	I/O	
IOC6	8	I/O	
IOC7	9	I/O	
IOD0	20	I/O	Port D is an 8-bit bi-directional programmable input/output port with pull-low. In input mode, Port D can be either pure or pull-low state. In output mode, Port D can be a buffer. (Key change, wake-up I/O)
IOD1	21	I/O	
IOD2	22	I/O	
IOD3	23	I/O	
IOD4	24	I/O	
IOD5	25	I/O	
IOD6	26	I/O	
IOD7	27	I/O	

5.1. PAD Assignment



The IC substrate should be connected to VSS or floated

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in this series is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you higher fidelity speech and music as well as achieving higher performance.

6.2. RAM Area

The total RAM size is 128-byte (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

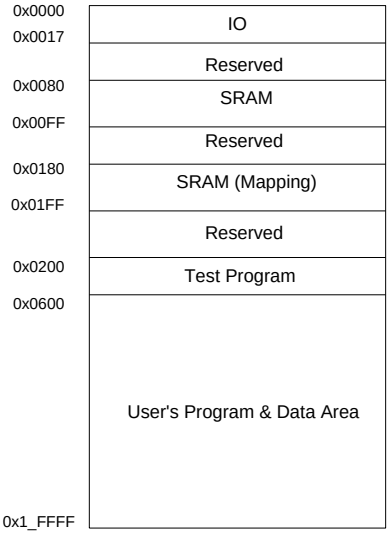
6.3. ROM Area

The ROM size of this series is listed as the table below. The ROM can be defined as program area, audio data area, or both. To access ROM, users should program the BANK SELECT register, choose bank, and access address to fetch data.

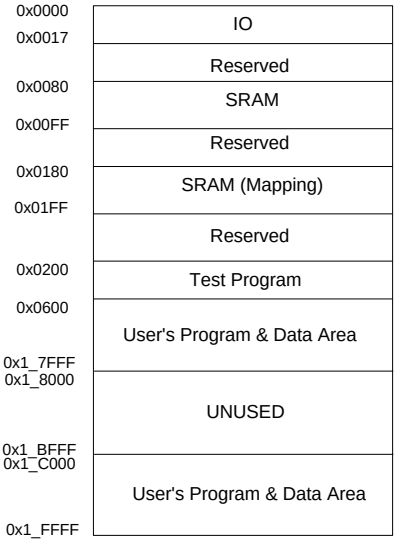
Body	ROM size
GPC11128A2	128KB
GPC11112A2	112KB
GPC11096A2	96KB
GPC11080A2	80KB

6.4. Map of Memory and I/O

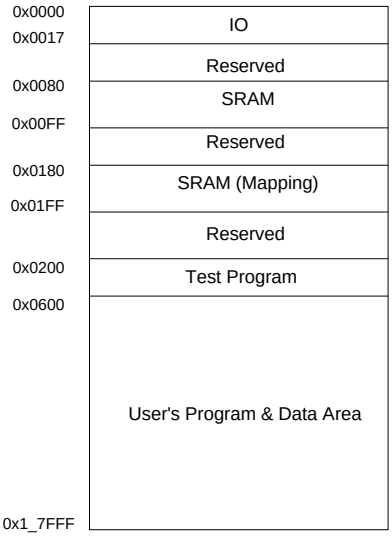
a. GPC11128A2



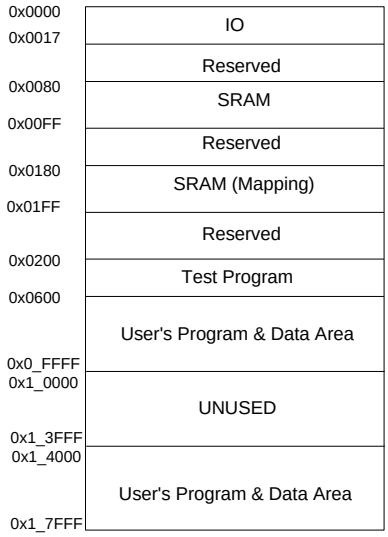
b. GPC11112A2



c. GPC11096A2



d. GPC11080A2

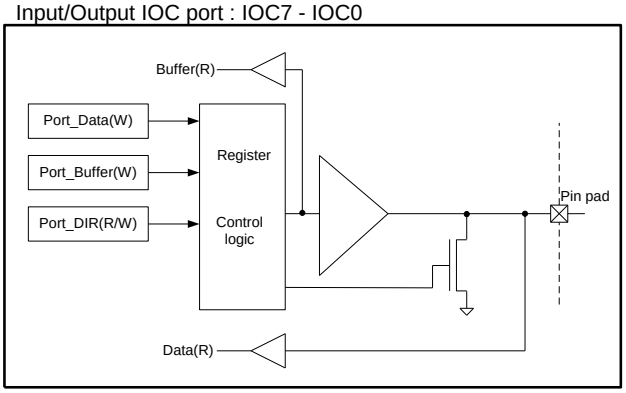


6.5. Speech and Melody

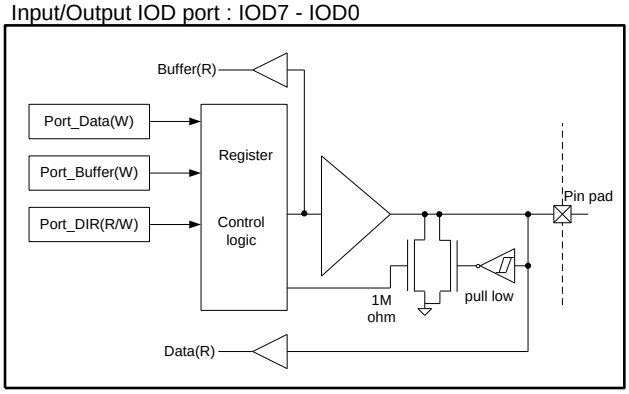
In speech synthesis, this series can use NMI for accurate sampling frequency. User can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, ADPCM and SACM-A3400.

6.6. I/O Port Configuration*

Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



6.7. Power Saving Mode

This series features a Power Saving mode (Standby mode) for those applications requiring very low standby current. To enter Standby mode, the wake-up register must be enabled and stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until wakeup. Port IOD7-0 is the only wake-up source. After it wakes up, the internal CPU will go to the RESET state (Tw $\geqq$ 64 x T1) and continue to execute the program. Wake-up reset will neither affect RAM nor I/Os.

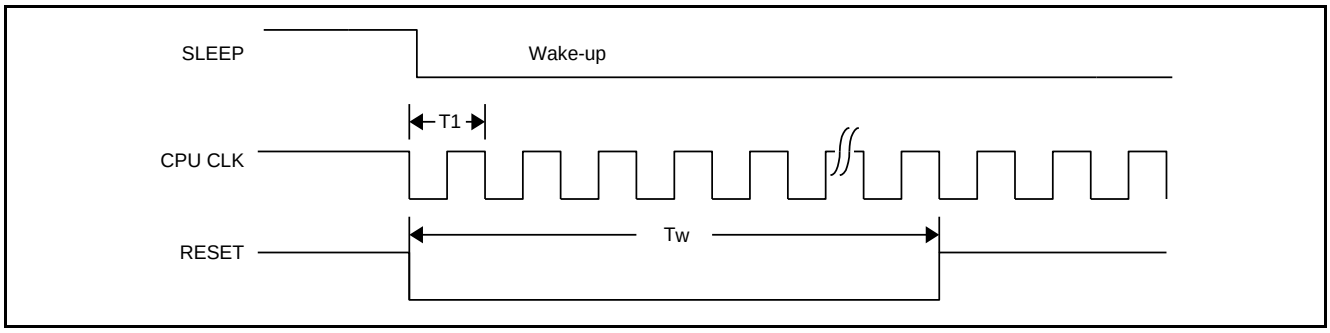
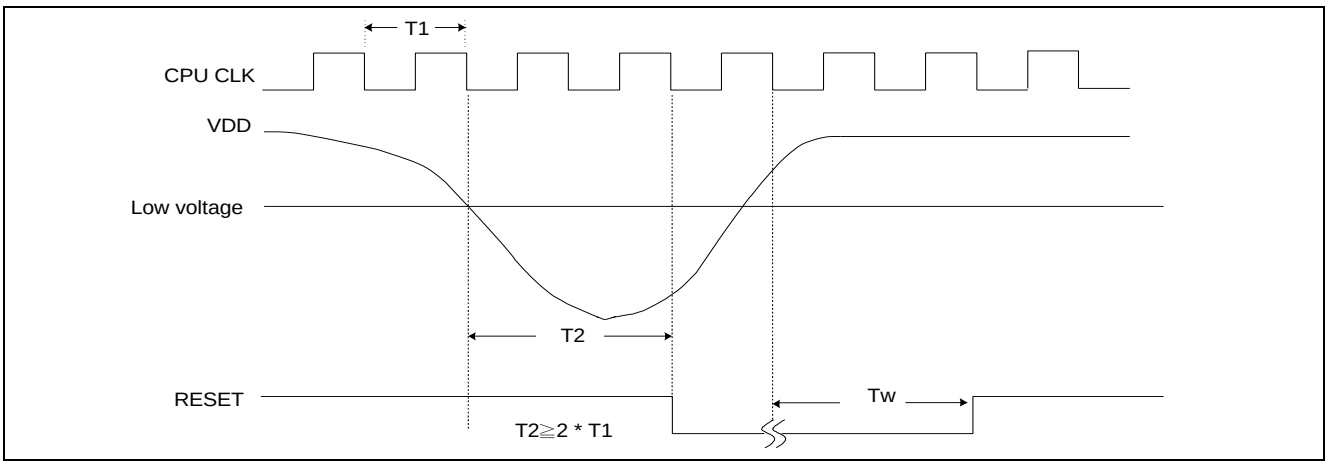


FIG. 1

$T1 = 1 / (F_{CPU})$, Tw ≧64 x T1

6.8. Low Voltage Reset

It has a Low Voltage Reset (LVR) function. In general, CPU becomes unstable and malfunctions when the power voltage drops below certain operating voltage. With the unique design of Low Voltage Reset, it is able to reset all functions to the initial operation (stable) state if the VDD power-supply voltage drops extremely low.



(The LVR function is the same as Power ON Reset or External Reset.)

6.9. Timer/Counter

There are two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are reloaded up-counters. When timer rollovers from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and count up again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will neither affect the value of the counter nor reset it.

Clock source of timer/counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, please see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC2}	-	6	-	MHz	VDD = 2.1V - 3.6V, for 2-battery
		-	8	-	MHz	VDD = 3.6V - 5.5V, for 3-battery

7.3. DC Characteristics (VDD=5.0V, T_A=25℃)

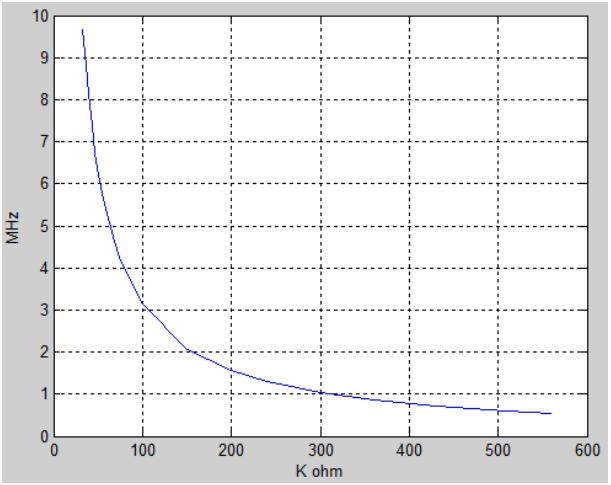
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	-
Operating Current	I_{OP}	-	4	5.2	mA	F_{CPU} = 6.0MHz @ 5.0V
Standby Current	I_{STBY}	-	-	2	μA	VDD = 5.0V
Audio DAC Output Current	I_{AUD}	2.6	3.7	4.8	mA	VDD = 5.0V
Input High Level	V_{IH}	0.7*VDD	-	VDD	V	VDD = 5.0V
Input Low Level	V_{IL}	0	-	0.3*VDD	V	VDD = 5.0V
Output Source Current (IOC, IOD)	I_{OH}	9.5	14	18	mA	VDD = 5.0V, V_{OH} = 3.5V
Output Sink Current (IOC, IOD)	I_{OL}	18.5	27	35	mA	VDD = 5.0V, V_{OL} = 1.5V
Audio PWM Output Current	I_{AUD}	160	230	290	mA	VDD = 5.0V, 8ohm load
Input Resistor (IOC)	R_{IN}	70	105	150	KΩ	VDD = 5.0V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	350	500	650	KΩ	VDD = 5.0V, V_{IN} = VDD

7.4. DC Characteristics(VDD=3.0V, T_A=25℃)

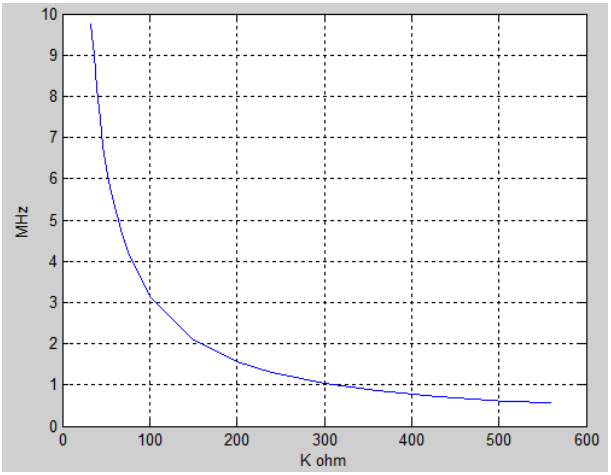
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.1	-	3.6	V	-
Operating Current	I_{OP}	-	1.6	2.1	mA	F_{CPU} = 6.0MHz @ 3.0V
Standby Current	I_{STBY}	-	-	2	μA	VDD = 3.0V
Audio DAC Output Current	I_{AUD}	1.2	1.7	2.2	mA	VDD = 3.0V
Input High Level	V_{IH}	0.7*VDD	-	VDD	V	VDD = 3.0V
Input Low Level	V_{IL}	0	-	0.3*VDD	V	VDD = 3.0V
Output Source Current (IOC, IOD)	I_{OH}	4.0	6	7.5	mA	VDD = 3.0V, V_{OH} = 2.1V
Output Sink Current (IOC, IOD)	I_{OL}	8.0	12	15.5	mA	VDD = 3.0V, V_{OL} = 0.9V
Audio PWM Output Current	I_{AUD}	85	125	160	mA	VDD = 3.0V, 8ohm load
Input Resistor (IOC)	R_{IN}	140	235	260	KΩ	VDD = 3.0V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	700	1160	1300	KΩ	VDD = 3.0V, V_{IN} = VDD

7.5. The Relationship between the R_{OSC} and the F_{CPU}

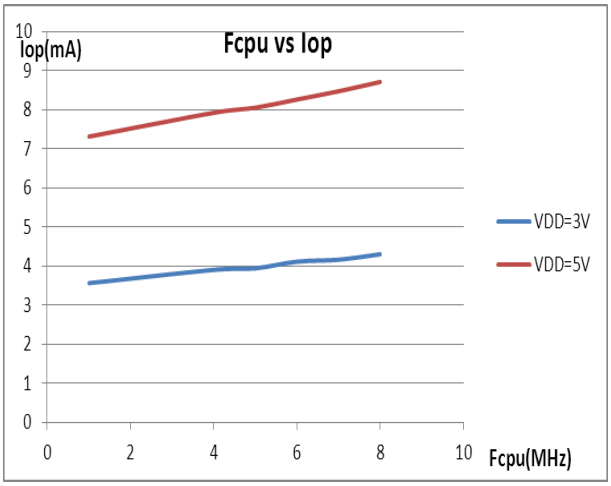
7.5.1. VDD = 3.0V, T_A = 25℃



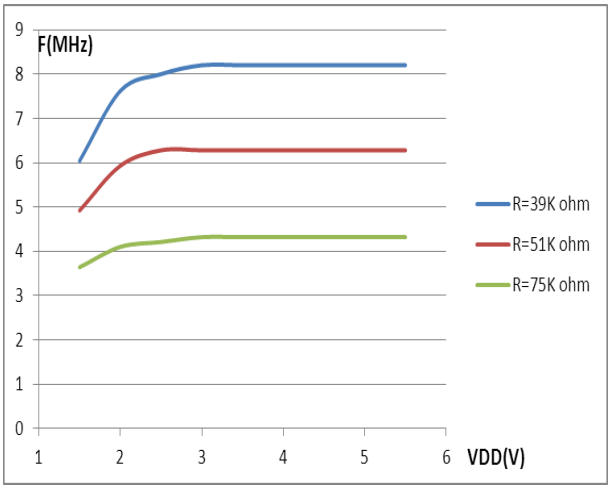
7.5.2. VDD = 5.0V, T_A = 25℃



7.5.3. Operating current vs. frequency vs. VDD

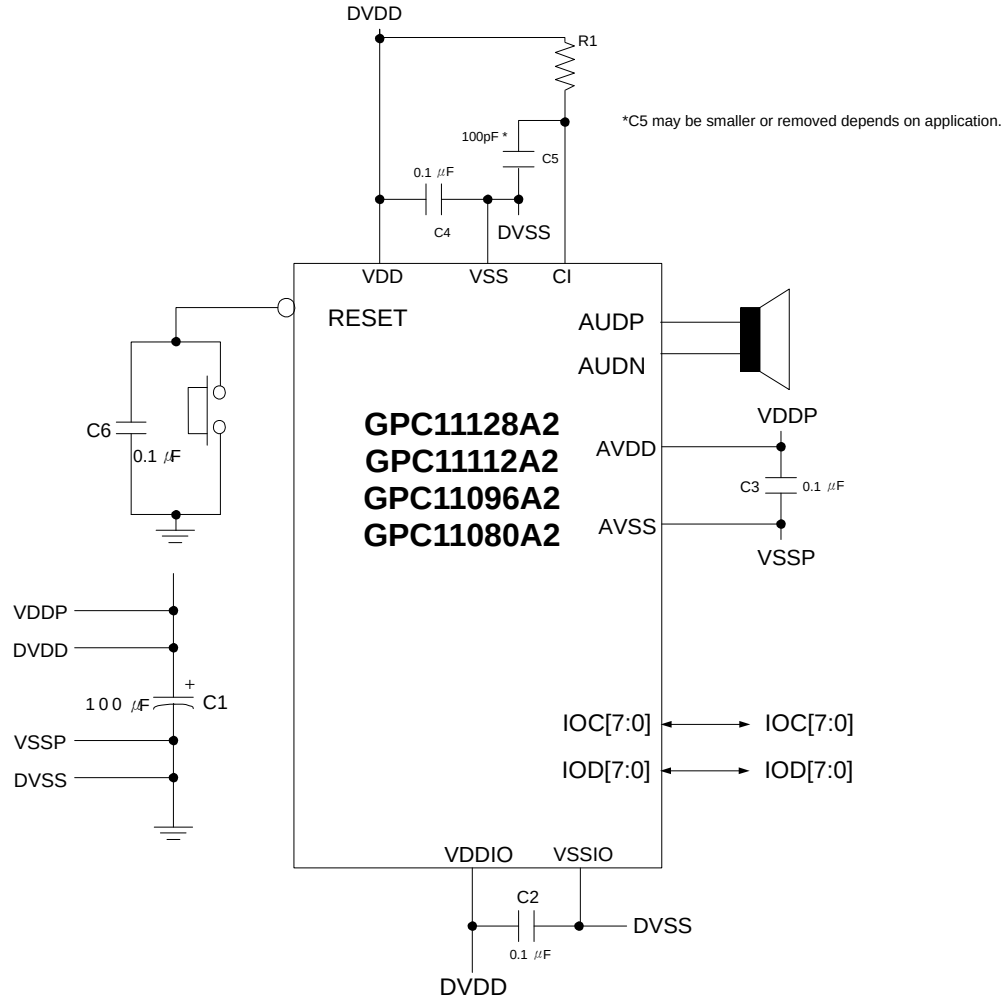


7.5.4. Frequency vs. VDD



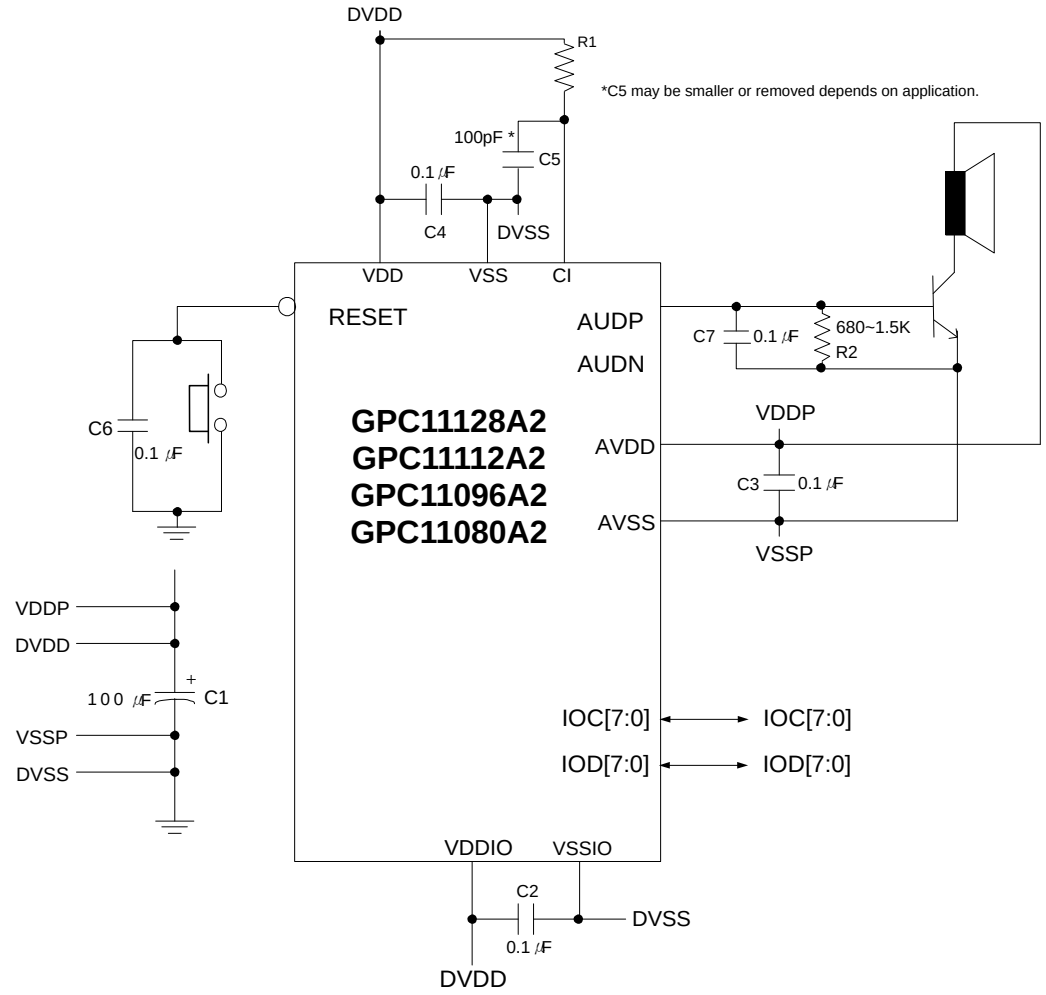
8. APPLICATION CIRCUITS

8.1. Audio: PWM Output



PCB Layout Guidelines:
1.VDDIO, VDD, AVDD must be connected to power input port directly, not to be the branch of each other.
2.VSSIO, VSS, AVSS must be connected to ground input port directly, not to be the branch of each other.
3.R1 and C5 should be as close as possible to CI pin.
4.C2 should be as close as possible to VDDIO/VSSIO pin.
5.C3 should be as close as possible to AVDD/AVSS pin.
6.C4 should be as close as possible to VDD/VSS pin.

8.2. Audio: DAC Output



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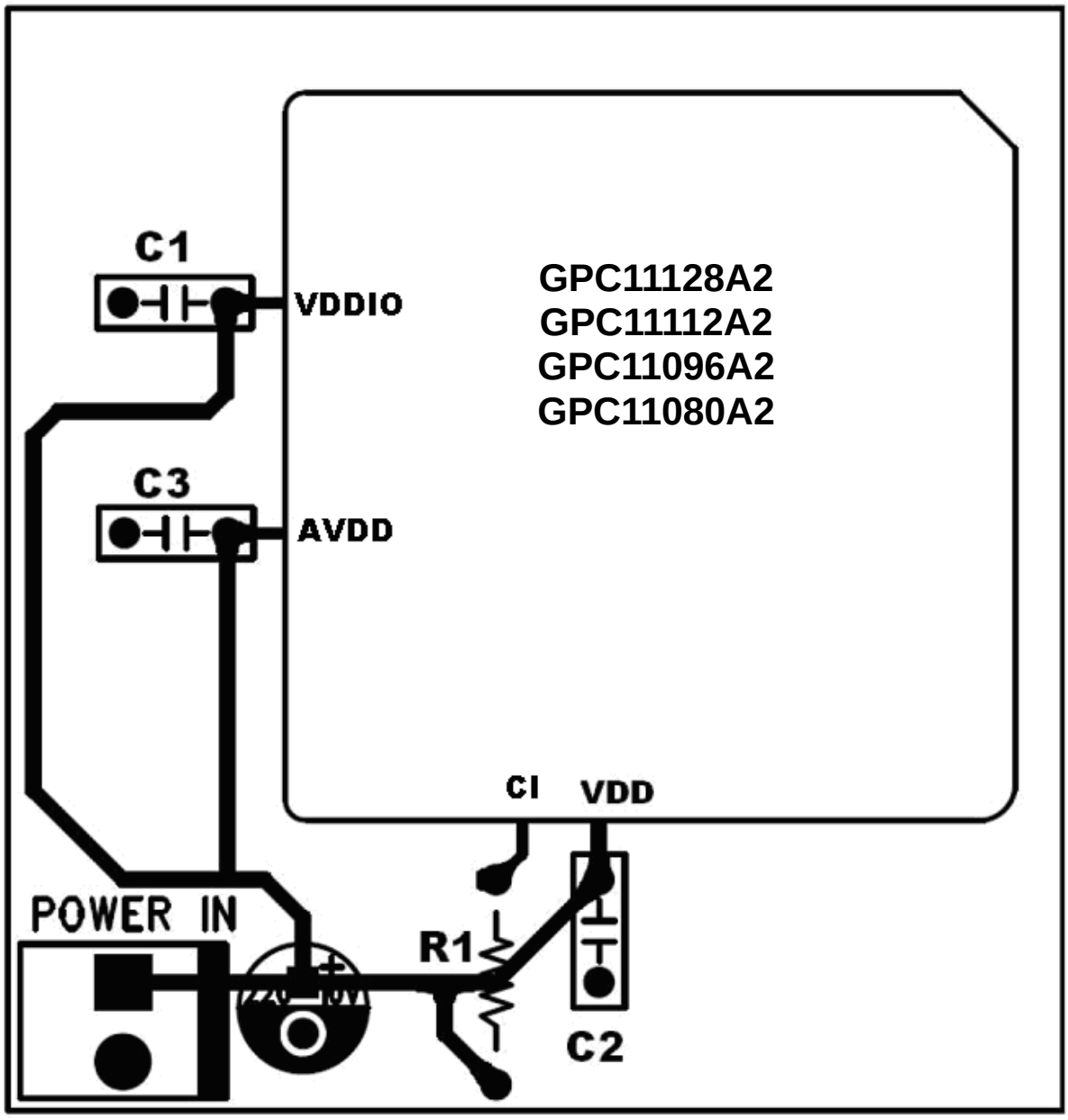
4.C2 should be as close as possible to VDDIO/VSSIO pin.
5.C3 should be as close as possible to AVDD/AVSS pin.
6.C4 should be as close as possible to VDD/VSS pin.

9. PCB LAYOUT GUIDE

To avoid the unexpected noises that may cause abnormal CPU operations, the following cares must be exercised while designing the PCB layout:

1. Bond all VDD and VSS pins out.
2. The 0.1μF capacitor (C1-C3) placed between Power and Ground must be as close as possible to IC itself.
3. The ROSC resistor R1 must be as close as possible to IC itself.

The PCB layout examples are given as follows:



10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPC11128A2-NnnV-C	Chip form
GPC11112A2-NnnV-C	Chip form
GPC11096A2-NnnV-C	Chip form
GPC11080A2-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page
Sep 02, 2015	1.0	Add DC characteristics.	9, 10
May 08, 2015	0.1	Original	15