DATA SHEET

GPC11048A

Sound Controller with 48K-byte ROM

JUL. 19, 2010

Version 1.4

Table of Contents

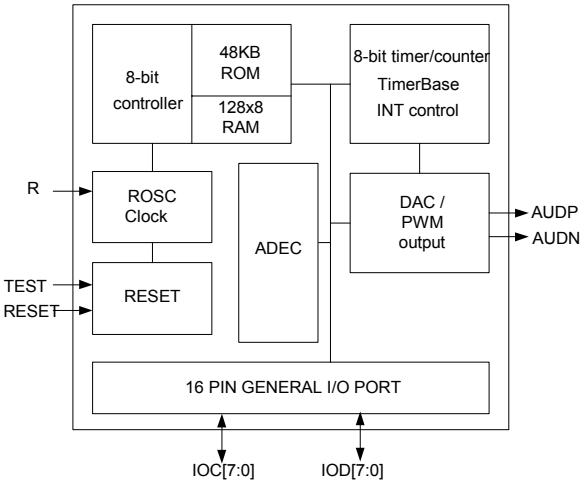
PAGE

SOUND CONTROLLER WITH 48K-BYTE ROM

1. GENERAL DESCRIPTION

The GPC11048A, a speech/wavetable synthesizer, equips an 8-bit CMOS microprocessor, and 48K-byte Working ROM, 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 16 Software Selectable I/Os, One 8-bit DAC and a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The GPC11048A features, not only the latest technology, but also the full commitment and technical support of Generalplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 48K bytes ROM
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 6.0MHz
  3.6V - 5.5V @ 8.0MHz
- **Supports ROSC only**
- Max. CPU clock: 6.0MHz @ 3.0V, 8MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings. Max. 2.0μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- 16 general I/Os
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake -up function
- IR function
- External feedback input
- Watchdog function
- **One DAC and A pair of PWM output**

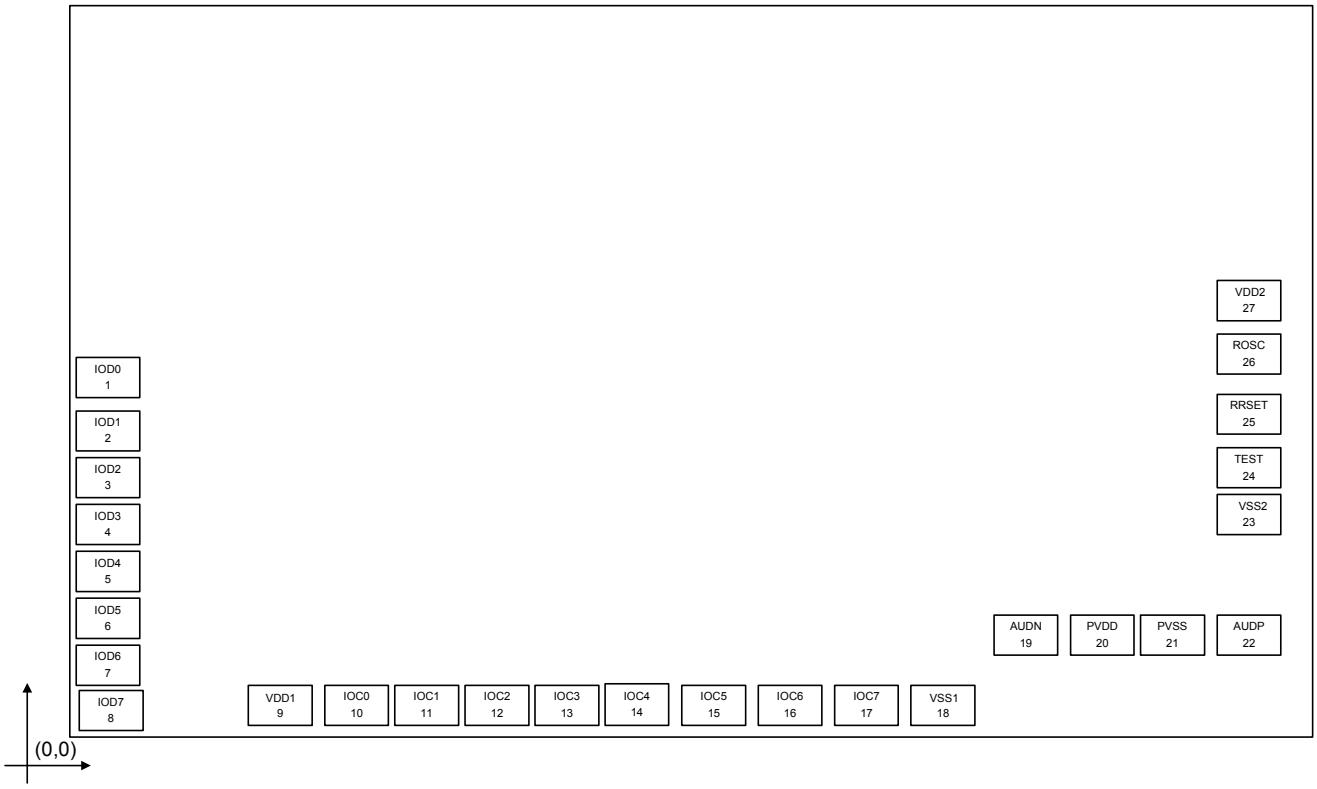
4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No	Type	Description
VDD1	9	I	Digital Power Pad
VSS1	18	I	Digital Ground
VDD2	27	I	Digital Power Pad
VSS2	23	I	Digital Ground
PVDD	20	I	PWM Power Pad
PVSS	21	I	PWM Ground
ROSC	26	I	ROSC Resistor input (Resistor must be connected to VDD)
RESET	25	I	RESET pin, Active low to reset whole system.
TEST	24	I	TEST pin, NC
AUDP	22	O	Audio OUTPUT1
AUDN	19	O	Audio OUTPUT2
IOC0	10	I/O	Port C is an 8-bit bi-directional programmable Input/Output port with Pull-low. In input mode, Port C can be either Pure or Pull-low states. In output mode, Port C can be Buffer.
IOC1	11	I/O	
IOC2	12	I/O	
IOC3	13	I/O	
IOC4	14	I/O	
IOC5	15	I/O	
IOC6	16	I/O	
IOC7	17	I/O	
IOD0	1	I/O	Port D is an 8-bit bi-directional programmable Input/Output port with Pull-low. In input mode, Port D can be either Pure or Pull-low states. In output mode, Port D can be Buffer. (Key change, Wake up I/O)
IOD1	2	I/O	
IOD2	3	I/O	
IOD3	4	I/O	
IOD4	5	I/O	
IOD5	6	I/O	
IOD6	7	I/O	
IOD7	8	I/O	

5.1. PAD Assignment



The IC substrate should be connected to VSS or floated

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in GPC11048A is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

6.2. RAM Area

The total RAM size is 128-byte (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

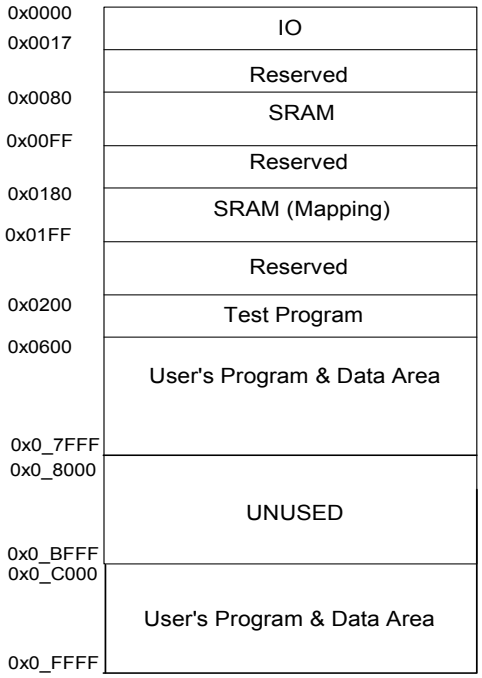
6.3. ROM Area

The GPC11048A provides a 48K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.4. Power Saving Mode

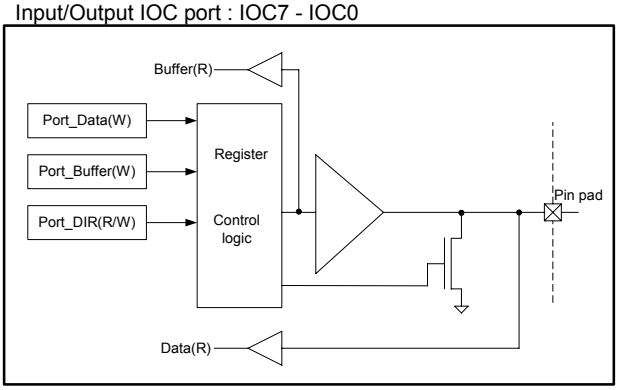
The GPC11048A includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. Port IOD7-0 is the only wake-up source in the GPC11048A. After the GPC11048A is awaken, the internal CPU will go to the RESET State (Tw ≧ 64 x T1) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os.

6.5. Map of Memory and I/Os

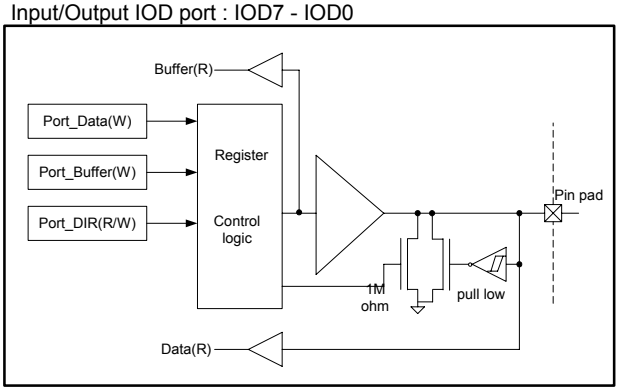


6.6. I/O Port Configuration*

Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



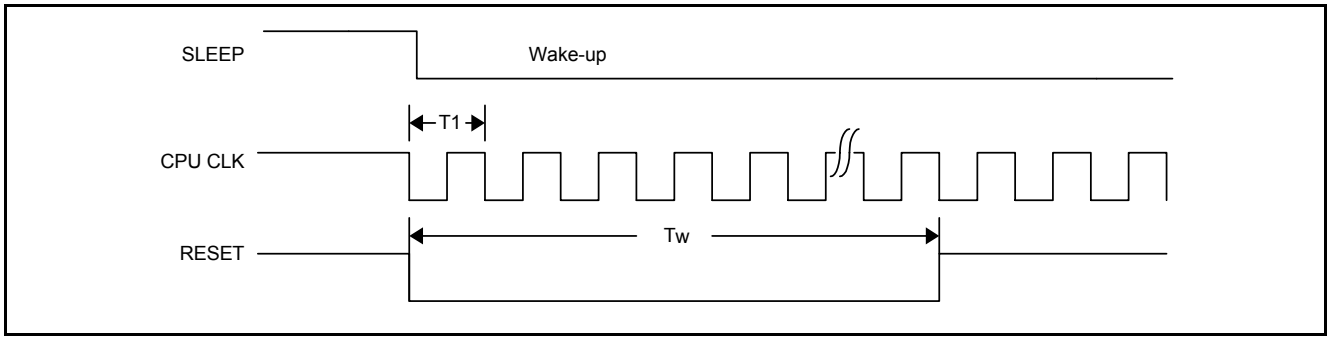
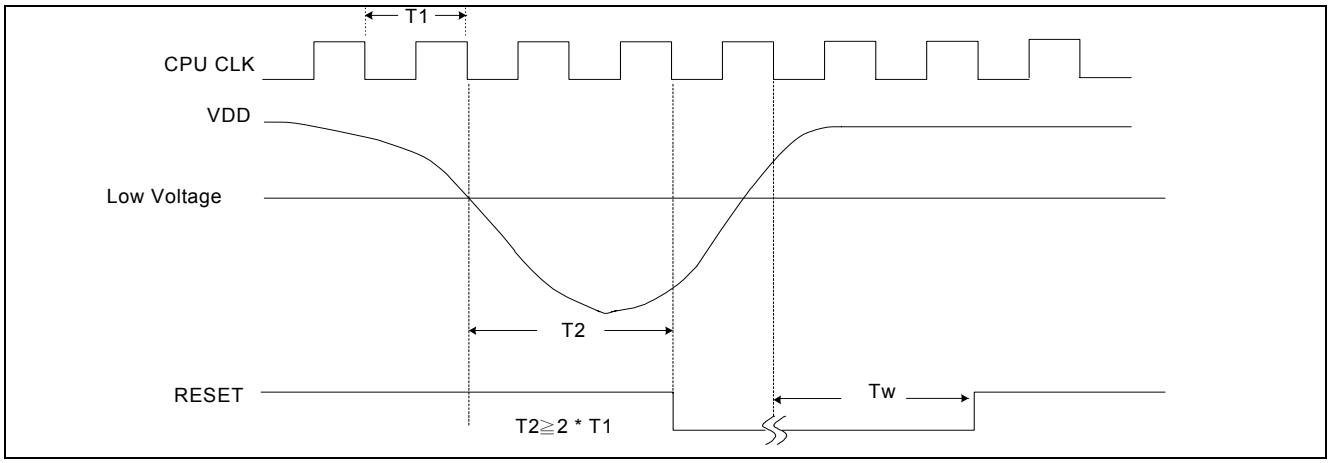


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧64 x T1

6.7. Low Voltage Reset

The GPC11048A has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctions when the power voltage drops below certain operating voltage. With the unique design of Low Voltage Reset in GPC11048A, it is able to reset all functions to the initial operational (stable) state if the VDD power-supply voltage drops too low.



(The LVR function is the same as Power ON Reset or External Reset.)

6.8. Timer/Counter

The GPC11048A has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.9. Speech and Melody

In speech synthesis, the GPC11048A can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, ADPCM and SACM-A3400.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC2}	-	4.0	6.0	MHz	VDD = 2.4V - 3.6V, for 2-battery
		-	6.0	8.0	MHz	VDD = 3.6V - 5.5V, for 3-battery

7.3. DC Characteristics (VDD = 5.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	-
Operating Current	I_{OP}	-	5.0	-	mA	F_{CPU} = 8.0MHz @ 5.0V
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio Output Current	I_{AUD}	-	5	-	mA	VDD = 5.0V
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 5.0V
Output Source Current (IOC, IOD)	I_{OH}	-	-15	-	mA	VDD = 5.0V, V_{OH} = 3.33V
Output Sink Current (IOC, IOD)	I_{OL}	-	21	-	mA	VDD = 5.0V, V_{OL} = 0.8V
Audio PWM Output Current	I_{AUD}	-	295	-	mA	VDD = 5.0V, 8ohm load
Input Resistor (IOC)	R_{IN}	-	85	-	KΩ	VDD = 5.0V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	85	-	KΩ	VDD = 5.0V, V_{IN} = 0V
Input Resistor (IOD)	R_{IN}	-	770	-	KΩ	VDD = 5.0V, V_{IN} = VDD

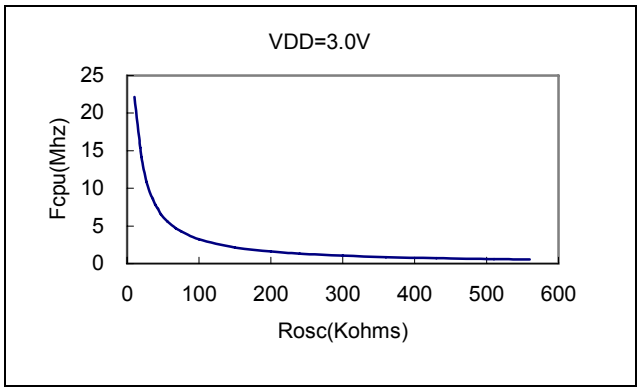
7.4. DC Characteristics (VDD = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	-
Operating Current	I_{OP}	-	2.0	-	mA	F_{CPU} = 6.0MHz @ 3.0V
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio Output Current	I_{AUD}	-	2.5	-	mA	VDD = 3.0V
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD =3.0V
Output Source Current (IOC, IOD)	I_{OH}	-	-7	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink Current (IOC, IOD)	I_{OL}	-	16	-	mA	VDD = 3.0V, V_{OL} = 0.8V
Audio PWM Output Current	I_{AUD}	-	160	-	mA	VDD = 3.0V, 8ohm load
Input Resistor (IOC)	R_{IN}	-	170	-	KΩ	VDD = 3.0V, V_{IN} = VDD

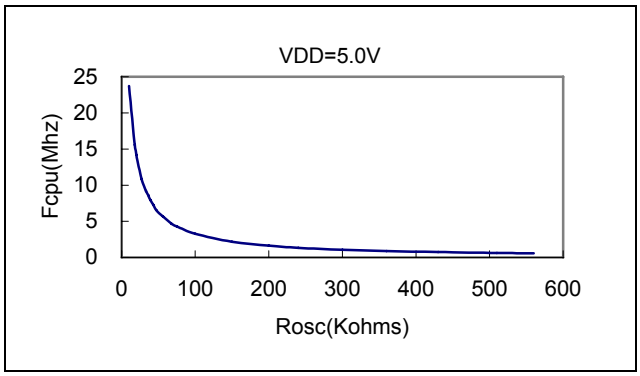
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Input Resistor (IOD)	R_{IN}	-	170	-	KΩ	VDD = 3.0V, V_{IN} = 0V
Input Resistor (IOD)	R_{IN}	-	1000	-	KΩ	VDD = 3.0V, V_{IN} = VDD

7.5. The Relationship between the R_{OSC} and the F_{CPU}

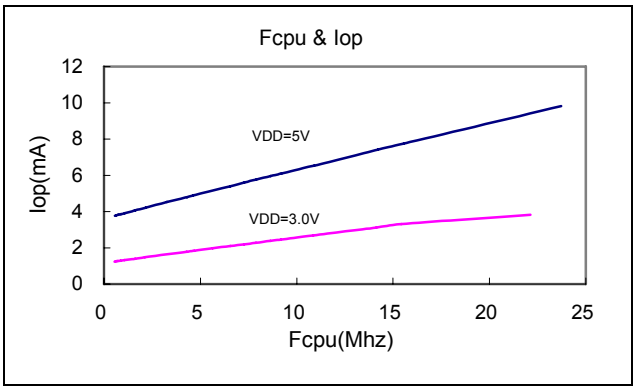
7.5.1. VDD = 3.0V, T_A = 25℃



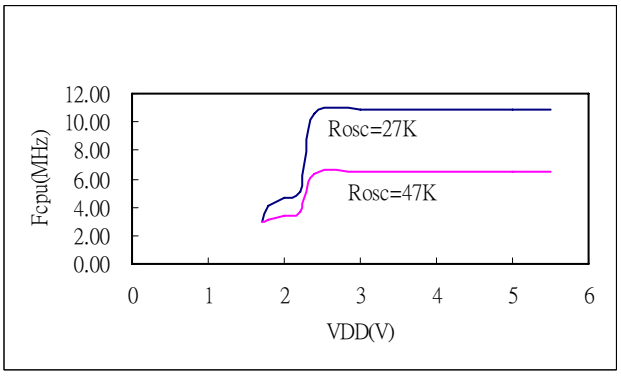
7.5.2. VDD = 5.0V, T_A = 25℃



7.5.3. Operating current vs. frequency vs. VDD

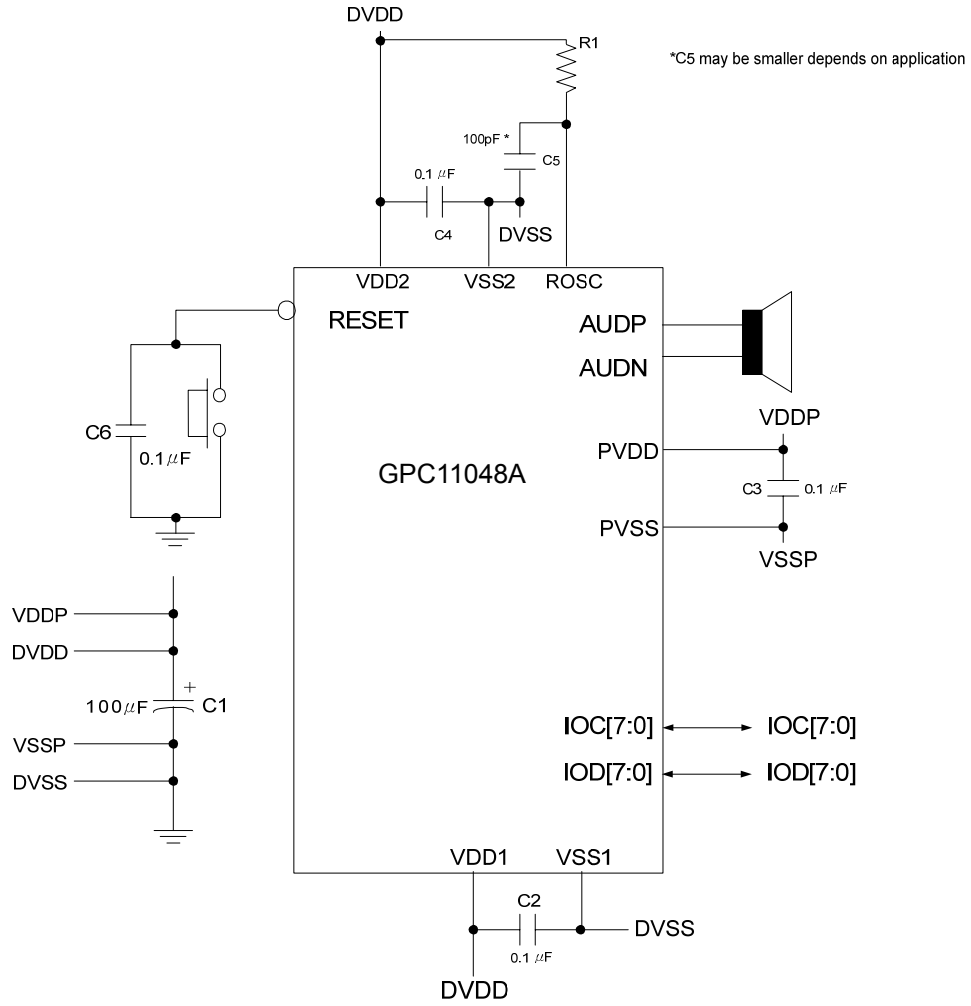


7.5.4. Frequency vs. VDD



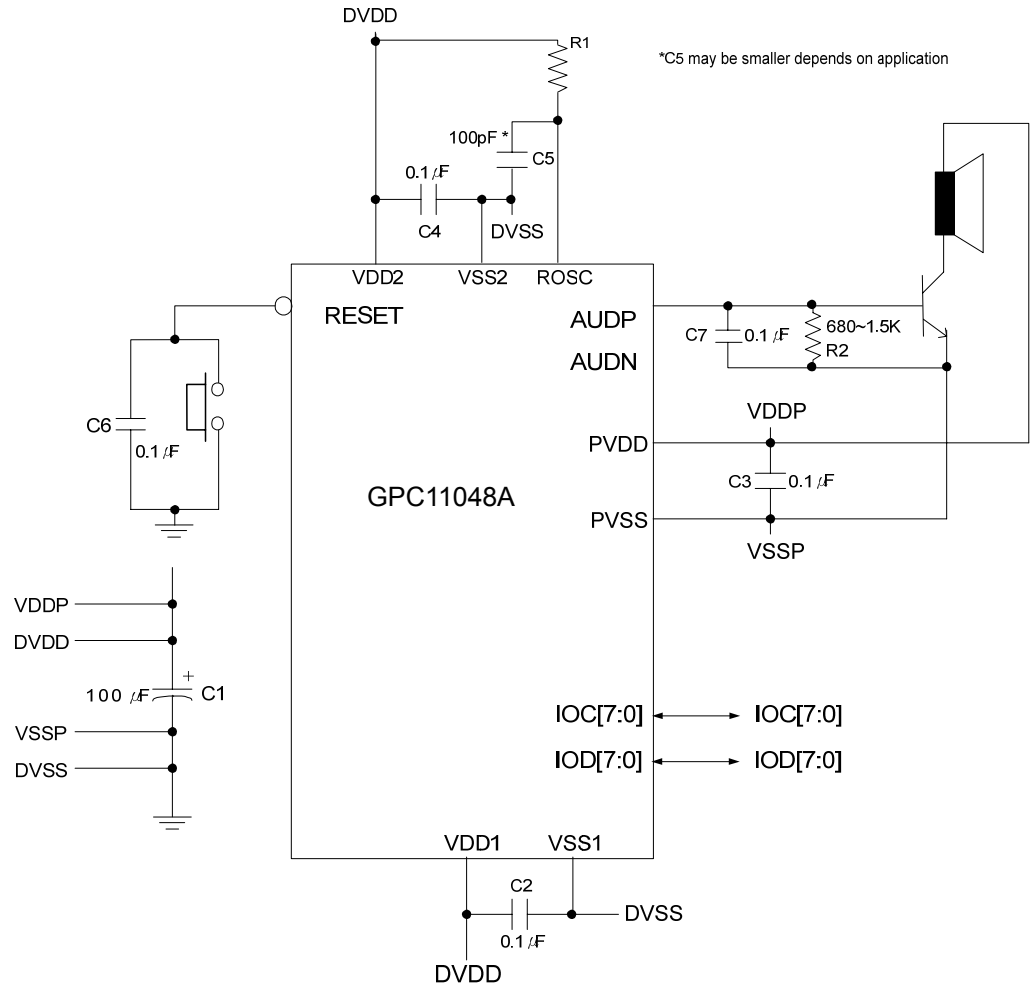
8. APPLICATION CIRCUITS

8.1. Audio: PWM Output



PCB Layout Guidelines:
1.VDD1, VDD2, PVDD must be connected to power input port directly, not to be the branch of each other.
2.VSS1, VSS2, PVSS must be connected to ground input port directly, not to be the branch of each other.
3.R1 and C5 should be as close as possible to ROSC pin.
4.C2 should be as close as possible to VDD1/VSS1 pin.
5.C3 should be as close as possible to PVDD/PVSS pin.
6.C4 should be as close as possible to VDD2/VSS2 pin.

8.2. Audio: DAC Output



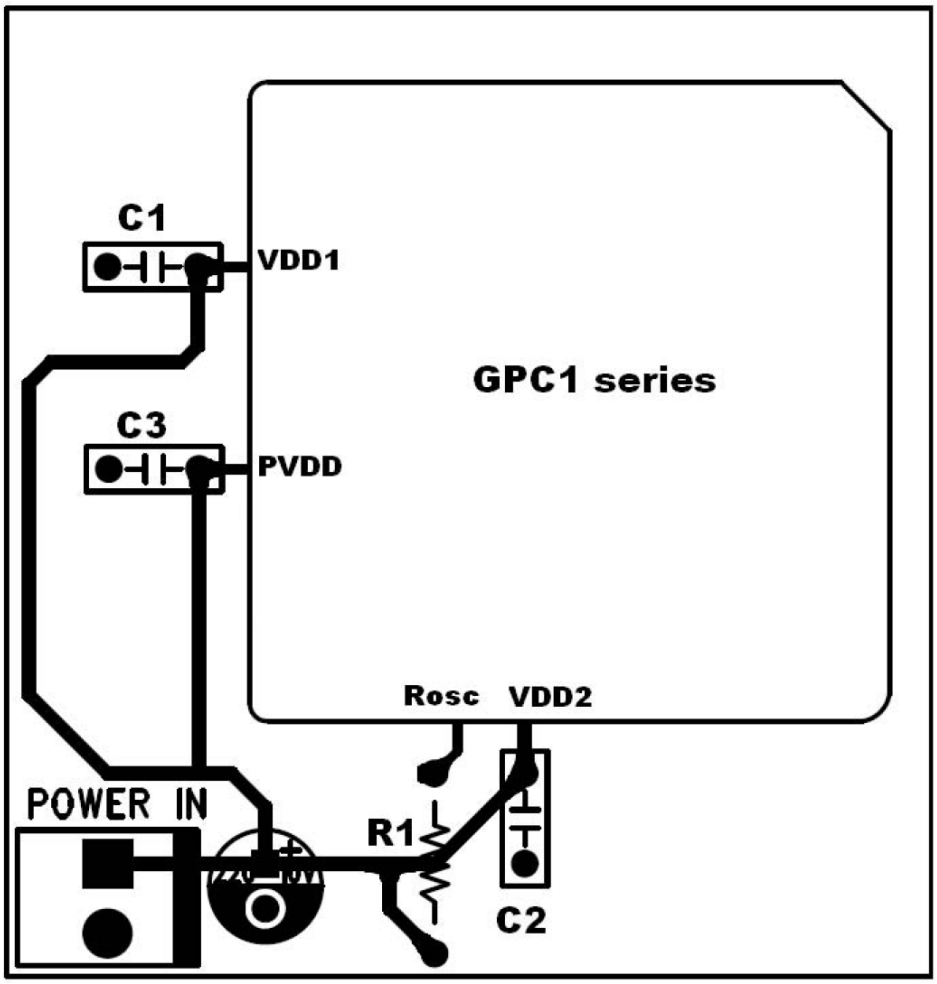
PCB Lay out Guidelines:
1.VDD1 , VDD2, PVDD must connected to power input port directly, not to be the branch of each other.
2.VSS1, VSS2, PVSS must connected to ground input port directly, not to be the branch of each other.
3.R1 and C5 should be as close as possible to ROSC pin.
4.C2 should be as close as possible to VDD1/VSS1 pin.
5.C3 should be as close as possible to PVDD/PVSS pin.
6.C4 should be as close as possible to VDD2/VSS2 pin.

9. PCB LAYOUT GUIDE

To avoid the unexpected noises to end up with abnormal CPU operations, the following cares must be exercised while doing the PCB layout:

1. Bond all VDD and VSS pins out.
2. The 0.1μF capacitor (C1-C3) placed between VDD and VSS must be as closed as possible to IC itself.
3. The ROSC resistor R1 must be as closed as possible to IC itself.

The PCB layout examples are given as follows:



10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPC11048A - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

11. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

12. REVISION HISTORY

Date	Revision #	Description	Page
JUL. 19, 2010	1.4	Modify section 7 to more accurate value.	15
MAY 19, 2008	1.3	Add the “PCB LAYOUT GUIDE” in section 9.	12
FEB. 01, 2008	1.2	Modify the Frequency vs. VDD in section 7.5.4.	9
FEB. 15, 2006	1.1	1. Add the DC Characteristics (VDD = 5.0V, T_A = 25°C) to section 7.3. 2. Modify the DC Characteristics (VDD = 3.0V, T_A = 25°C) in section 7.4.	7 7
OCT. 25, 2005	1.0	Original Note: The GPC11048A data sheet v1.0 is a continued version of SPC11048A data sheet v0.2	13