LG Semicon Co.,Ltd.

GM72V661641DI/DLI

1,048,576 WORD x 16 BIT x 4 BANK
SYNCHRONOUS DYNAMIC RAM

Description

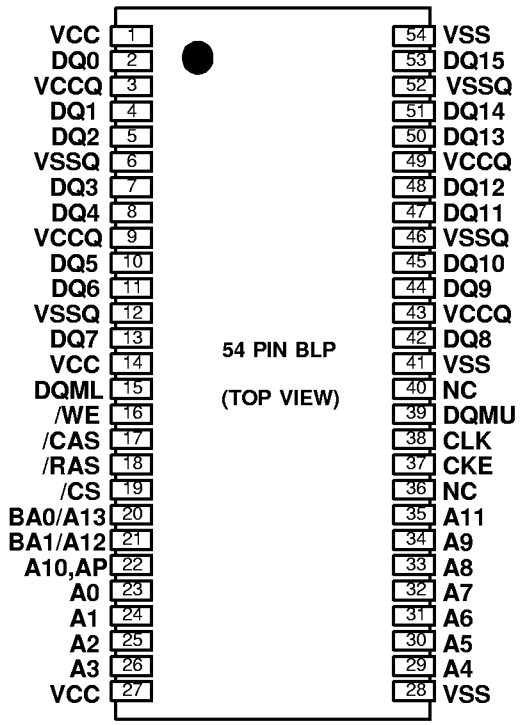
TheGM72V661641DI/DLIis a synchronous dynamic random access memory comprised of 67,108,864 memory cells and logic including input and output circuits operating synchronously by referring to the positive edge of the externally provided clock.

The GM72V661641DI/DLI provides four banks of 1,048,576 word by 16 bit to realize high bandwidth with the clock frequency up to 125 Mhz.

Features

* PC100, PC66 Compatible
  7K(2-2-2), 7J(3-2-2), 10K(PC66)
* 3.3V single power supply
* LVTTL interface
* Max clock frequency
  100/125 MHz
* 4,096 refresh cycle per 64 ms
* Two kind of refresh operation
  Auto refresh/ Self refresh
* Programmable burst access capability ;
  - Sequence:Sequential / Interleave
  - Length :1/2/4/8/FP
* Programmable $\overline{CAS}$ latency : 2/3
* 4 Banks can operate independently or simultaneously
* Burst read/burst write or burst read/single write operation capability
* Byte wide input and output control by DQML and DQMU inputs
* One clock of back to back read or write command interval
* Synchronous power down and clock suspend capability with one clock latency for both entry and exit
* JEDEC Standard 54Pin BLP PKG

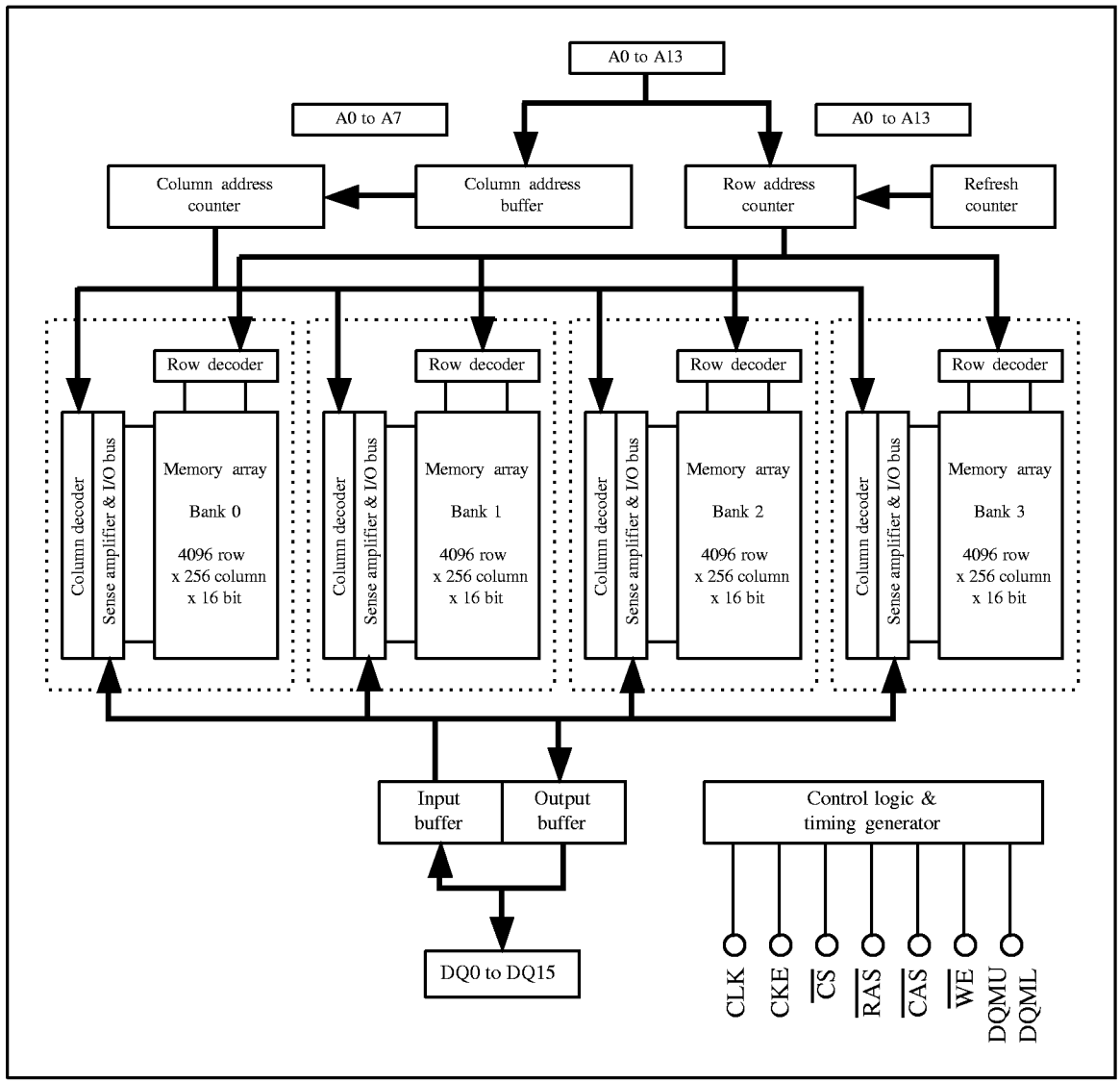
Pin Configuration



Pin Name

CLK	Clock
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A9,A11	Address input
A10 / AP	Address input or Auto Precharge
BA0/A13	Bank select
~BA1/A12	
DQ0~DQ15	Data input / Data output
DQMU/DQML	Data input / output Mask
VCCQ	Vcc for DQ
VSSQ	Vss for DQ
VCC	Power for internal circuit
VSS	Ground for internal circuit
NC	No Connection

Block Diagram



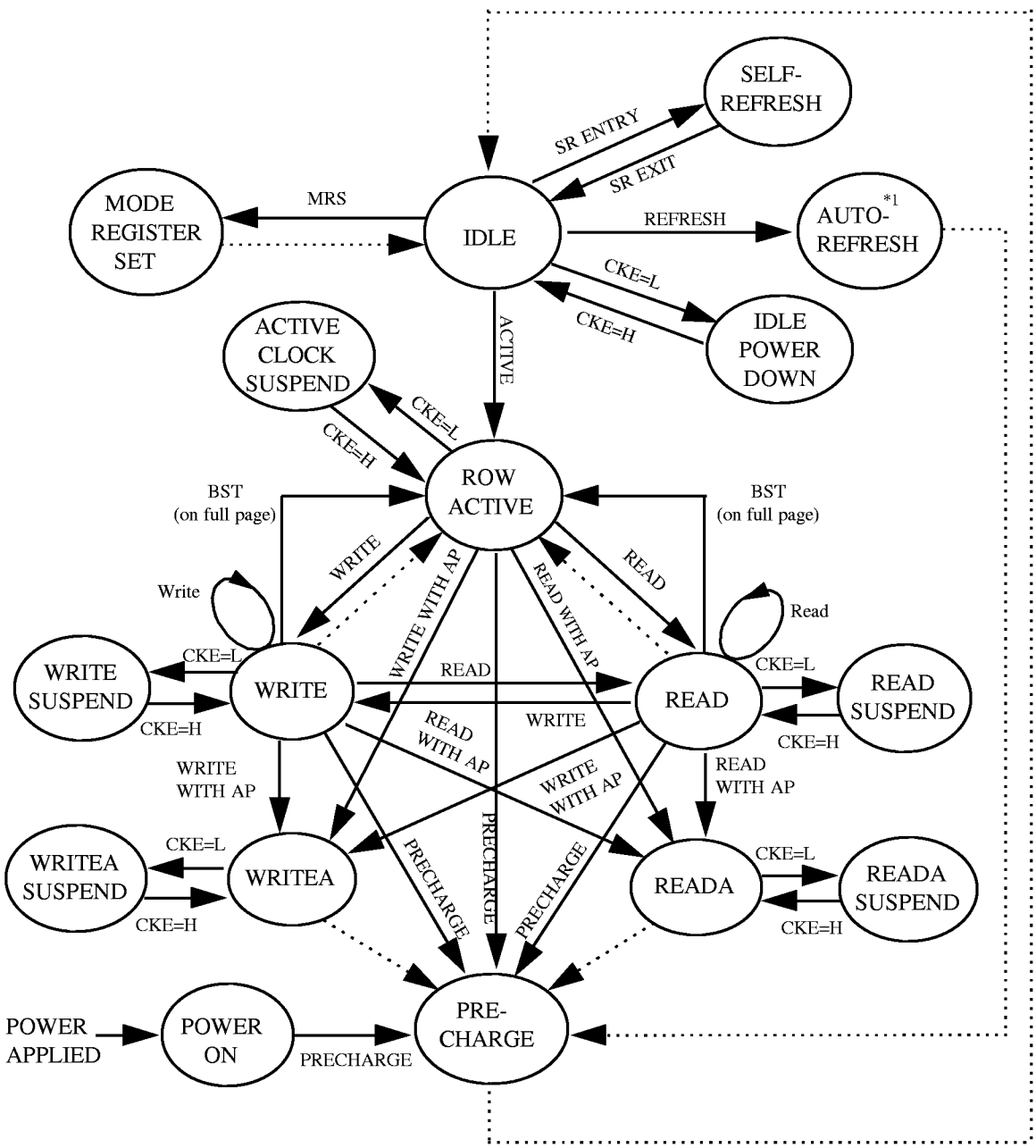
Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. Column address(AY0 to AY7; GM72V661641DI/DLI) is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the Precharge mode. When A10 = High at the Precharge command cycle, all banks are precharged. But when A10 = Low at the Precharge command cycle, only the bank that is selected by A12/A13 (BS) is precharged.
A12/A13 (input pin)	A12/A13 are bank select signal (BS). The memory array of the GM72V661641DI/DLI is divided into bank 0, bank 1, bank2 and bank 3. GM72V661641DI/DLI contain 4096-row x 256-column x 16-bits. contain 4096-row x 1024-column x 4-bits. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.
DQM, DQMU/DQML (input pins)	DQM, DQMU/DQML controls input/output buffers. * Read operation: If DQM, DQMU/DQML is High, The output buffer becomes High-Z. If the DQM, DQMU/DQML is Low, the output buffer becomes Low-Z. * Write operation: If DQM, DQMU/DQML is High, the previous data is held (the new data is not written). If DQM, DQMU/DQML is Low, the data is written.

Pin Description(Continued)

Pin Name	DESCRIPTION
DQ0 ~ DQ15 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAM.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

64M SDRAM Function State Diagram



Note: 1. After the auto-refresh operation, Precharge is performed automatically and enter the IDLE state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-0.5 to Vcc+0.5 (<= 4.6 (max))	V	1
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	C	
Storage temperature	Tstg	-55 to +125	C	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.6V for pulse width <= 3ns

3. V_{IL} (min) = -2.0V for pulse width <= 3ns

DC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3V +/- 0.3V, V_{SS}, V_{SSQ}= 0 V)

Parameter	Symbol	- 7K	- 7J	- 8	- 10K	Unit	Test conditions	Notes
		Max	Max	Max	Max			
Operating current	I_{CC1}	90	90	90	80	mA	Burst length= 1 t_{RC} = min	1, 2, 3
Standby current in power down	I_{CC2P}	2	2	2	2	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)	I_{CC2PS}	2	2	2	2	mA	CKE=V_{IL}, t_{CK}= Infinity	6
		0.4	0.4	0.4	0.4			6,8
Standby current in non power down ($\overline{CAS}$ Latency=2)	I_{CC2N}	15	15	15	15	mA	CKE,CS = V_{IH}, t_{CK} = 12ns	4
		10	10	10	10			4,8
Standby current in non power down (input signal stable)	I_{CC2NS}	5	5	5	5	mA	CKE = V_{IH}, t_{CK} = Infinity	4
Active standby current in power down	I_{CC3P}	6	6	6	6	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
		5	5	5	5			1,2,5,8
Active standby current in power down (input signal stable)	I_{CC3PS}	5	5	5	5	mA	CKE = V_{IL}, t_{CK} = Infinity	2,6
		4	4	4	4			2,6,8
Active standby current in non power down	I_{CC3N}	30	30	30	30	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
		25	25	25	25			1,2,4,8
Active standby current in non power down (input signal stable)	I_{CC3NS}	20	20	20	20	mA	CKE = V_{IH}, t_{CK} = Infinity	2,9
		10	10	10	10			2,8,9
Burst operating current (CL= 2)	I_{CC4}	130	90	110	90	mA	t_{CK} = min BL = 4	1,2,3
Burst operating current (CL= 3)	I_{CC4}	130	130	165	130	mA		
Refresh current	I_{CC5}	110	110	110	90	mA	t_{RC} = min	3
Self refresh current	I_{CC6}	1	1	1	1	mA	V_{IH} >=V_{CC} - 0.2 V_{IL} <=0.2V	7
		0.4	0.4	0.4	0.4			7,8

Parameter	Symbol	- 7K, -7J, -8, -10K		Unit	Test conditions	Notes
		Min	Max			
Input leakage current	I_{LI}	-1	1	uA	0<=Vin <=V_{CC}	
Output leakage current	I_{LO}	-1.5	1.5	uA	0<=Vout <=V_{CC} DQ = disable	
Output high voltage	V_{OH}	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. L-Version.
9. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V)

Parameter	Symbol	Min.	Max.	Unit	Notes
Input capacitance (CLK)	C_{I1}	2.5	4	pF	1, 3, 4
Input capacitance (Signals)	C_{I2}	2.5	5	pF	1, 3, 4
Output capacitance (DQ)	C_O	4.0	6.5	pF	1, 2, 3, 4

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM, DQMU/DQML = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.
4. Measured with 1.4 V bias and 200mV swing at the pin under measurement.

AC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	- 7K		- 7J		- 8		- 10K		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	10	-	15	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	10	-	10	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	6	-	8	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	6	-	8		
Data-out hold time		t_{OH}	3	-	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedance		t_{LZ}	2	-	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedance (CL = 2,3)		t_{HZ}	-	6	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	70	-	72	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	50	120000	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	20	-	24	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	20	-	24	-	30	-	ns	1

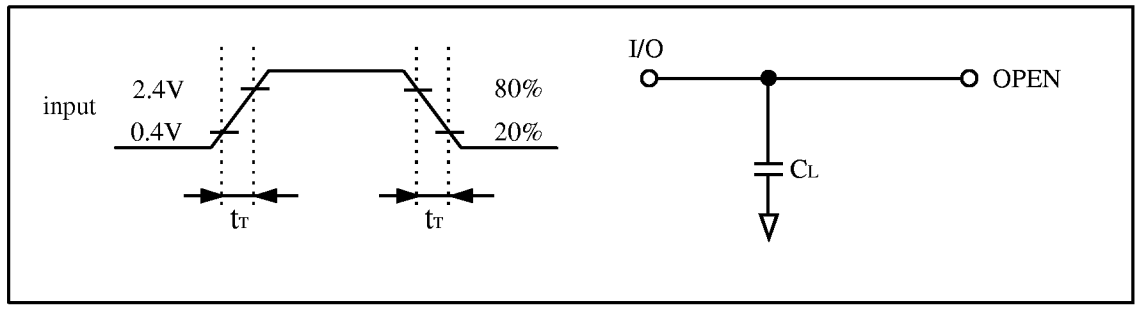
AC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	- 7K		- 7J		- 8		- 10K		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	8	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (min)defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

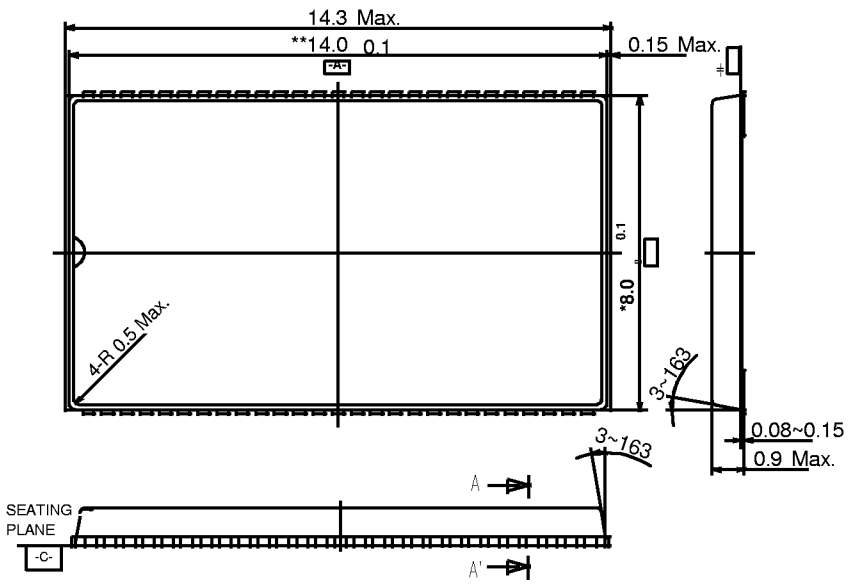
Parameter		Symbol	-7K	-7J		-8		-10K		Notes
frequency(MHz)			100	100	66	125	83	100	66	
t_{CK} (ns)			10	10	15	8	12	10	15	
Active command to column command (same bank)		l_{RCD}	2	2	2	3	2	3	2	1
Active command to active command (same bank)		l_{RC}	7	7	6	9	6	9	6	= [l_{RAS} +l_{RP}], 1
Active command to Precharge command (same bank)		l_{RAS}	5	5	4	6	4	6	4	1
Precharge command to active command (same bank)		l_{RP}	2	2	2	3	2	3	2	1
Write recovery or last data-in to Precharge command (same bank)		l_{RWL}	1	1	1	1	1	1	1	1
Active command to active command (different bank)		l_{RRD}	2	2	2	2	2	2	2	1
Self refresh exit time		l_{SREX}	1	1	1	1	1	1	1	
Last data in to active command (Auto Precharge, same bank)		l_{APW}	3	3	3	4	3	4	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input		l_{SEC}	9	9	6	9	6	9	6	= [l_{RC}]
Precharge command to high impedance	(CL=2)	l_{HZP}	2	-	2	-	2	-	2	
	(CL=3)	l_{HZP}	3	3	3	3	3	3	3	
Last data out to active command (auto Precharge) (same bank)		l_{APR}	1	1	1	1	1	1	1	
Last data out to Precharge (early Precharge)	(CL=2)	l_{EP}	-1	-	-1	-	-1	-	-1	
	(CL=3)	l_{EP}	-2	-2	-2	-2	-2	-2	-2	
Column command to column command		l_{CCD}	1	1	1	1	1	1	1	
Write command to data in latency		l_{WCD}	0	0	0	0	0	0	0	
DQM to data in		l_{DID}	0	0	0	0	0	0	0	
DQM to data out		l_{DOD}	2	2	2	2	2	2	2	
CKE to CLK disable		l_{CLE}	1	1	1	1	1	1	1	
Register set to active command		l_{RSA}	1	1	1	1	1	1	1	
$\overline{CS}$ to command disable		l_{CDD}	0	0	0	0	0	0	0	
Power down exit to command input		l_{PEC}	1	1	1	1	1	1	1	

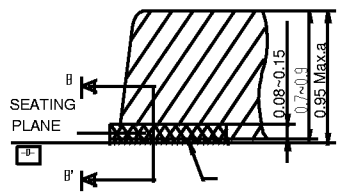
Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7K	-7J		-8		-10K		Notes
frequency(MHz)			100	100	66	125	83	100	66	
t_{CK} (ns)			10	10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	1	-	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	2	
Burst stop to output high impedance	(CL=2)	l_{BSH}	2	-	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	0	

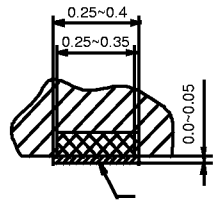
Notes : 1. l_{RCD} to l_{RRD} are recommended value.

Package Dimensions

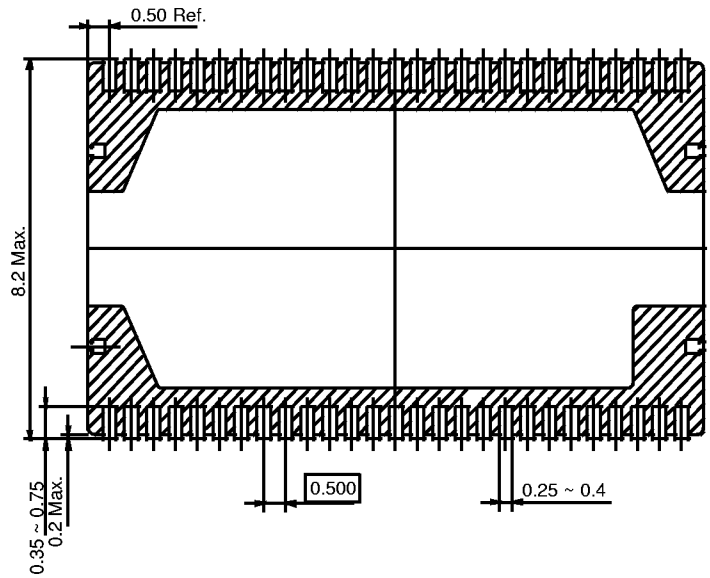




SECTION A-A'



SECTION B-B'

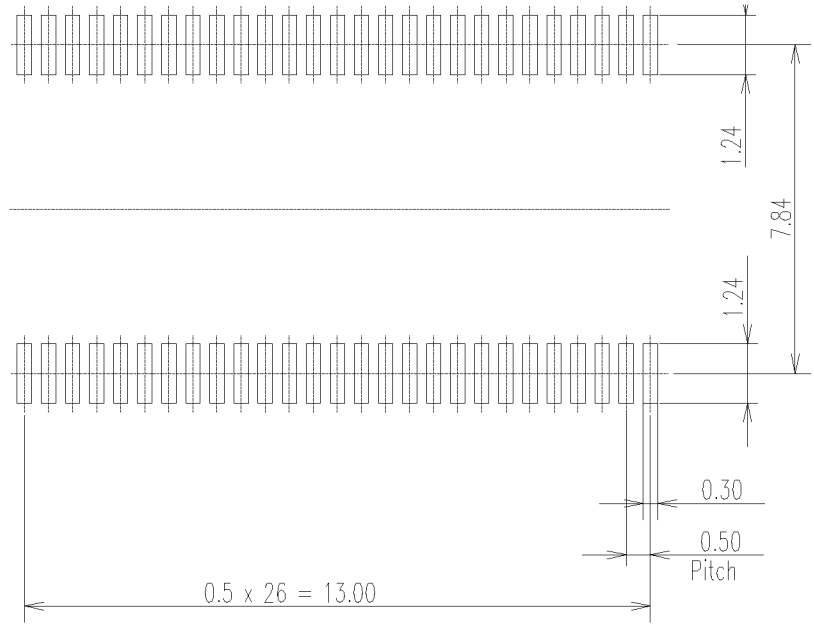


- NOTE -

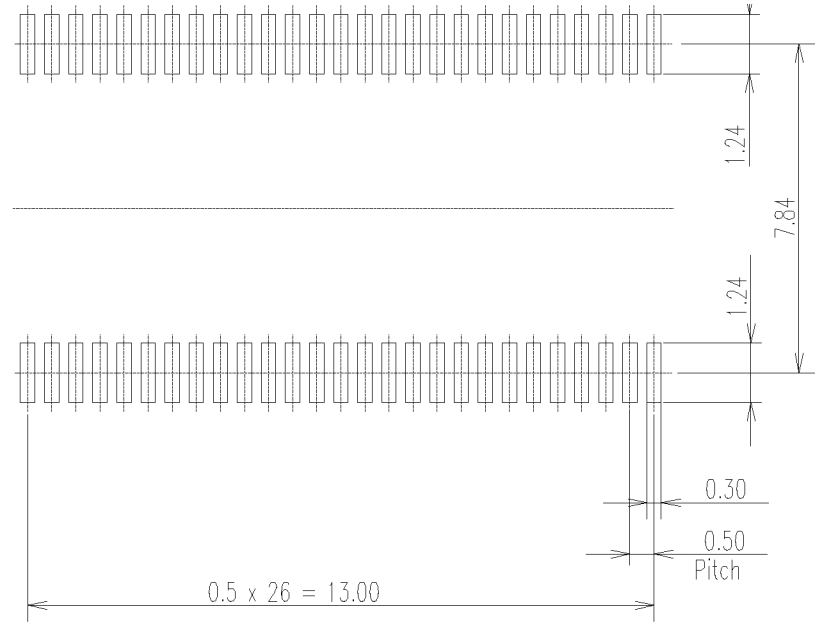
1. DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5M-1982.
2. DATUM -H- COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS BODY.
3. DATUM -A- AND -B- TO BE DETERMINED AT DATUM -H-
4. £¢*£¢& £¢**£¢DIMENSIONS ARE DETERMINED AT DATUM -H-
5. ** MARK DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS AND GATE BURRS.
   MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
6. * MARK DIMENSION DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS.
   INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.15 PER SIDE.
7. LEAD FRAME THICKNESS IS 0.1250.01

DESIGN GUIDELINE FOR 54 pin BLP

LAND DESIGN



METAL MASK DESIGN



Unit : mm
PKG Size: 8 ¡ ¿14, 0.5 pitch