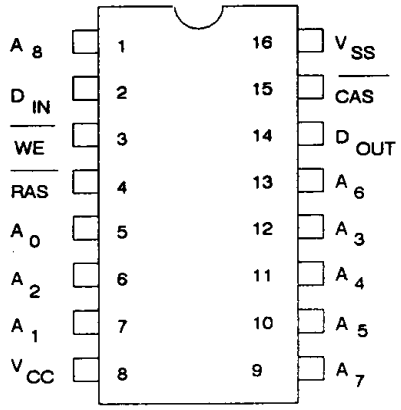
GM71C256
256K X 1 BIT CMOS DYNAMIC RAM

Description

The GM71C256 is a high speed dynamic RAM organized 262,144x1 Bit. The GM71C256 utilizes Goldstar's silicon Gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The GM71C256 offers Fast Page Mode which allows high speed random access memory cells within the same row. Multiplexed address inputs permit the GM71C256 to be packaged in a standard 16 pin DIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The GM71C256 is ideal for high speed, high performance systems such as mainfraim, minicomputer, graphics, PC and high performance μ-processor systems.

Pin Configuration

16 Plastic DIP



Features

- 262,144x1 Bit organization
- Fast access time and cycle time : 80/100/120 ns(Max)
- Single Power Supply of 5V ±10% with a built-in V_{BB} generator
- Performance Range

PARAMETER		GM71C256(ns)		
		-80	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	80	100	120
t_{AA}	Column Address Access Time	40	45	55
t_{CAC}	$\overline{CAS}$ Access Time	20	25	30
t_{RC}	Cycle Time	145	175	205
t_{PC}	Fast Page Mode Cycle Time	55	60	70

- Low Power
- 330mW MAX. Operating (GM71C256-80)
- 247mW MAX. Operating (GM71C256-12)
- 16.5mW MAX. Standby
- Read-Modify-Write, $\overline{RAS}$-only refresh, $\overline{CAS}$ Before $\overline{RAS}$ Refresh and Fast Page Mode Capability
- All input and output TTL compatible
- 256 refresh cycles/4ms
- Industry standard 16 pin Plastic DIP.

Pin Description

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	+5V Supply
V_{SS}	0V Supply

Ordering Information

Type NO.	Access Time	PKG
GM71C256-80 GM71C256-10 GM71C256-12	80 ns 100 ns 120 ns	300 MIL 16 PIN PLASTIC DIP

Recommended Operating Conditions

(T_A = 0°C to 70°C)

V_{CC} Supply Voltage	4.5 ~ 5.5V
V_{IH} Input High Voltage	2.4 ~ 6.5V
V_{IL} Input Low Voltage	-1.0 ~ 0.8V

Absolute Maximum Ratings*

Ambient Temperature Under-Bias	0°C to +70°C
Storage Temperature (plastic)	-55°C to +125°C
Votage on any Pin Except V_{CC} Relative to V_{SS}	-1.0V to 7.0V
Voltage on V_{CC} relative to V_{SS}	-1.0V to +7.0V
Data Output Current	50mA
Power Dissipation	1.0W

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC Electrical Characteristics : (V_{CC} = 5V ±10%, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	–	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN)	80 100 120	- -	60 50 45	mA	3, 4
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		-	3.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN)	80 100 120	- -	60 50 45	mA	3
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN)	80 100 120	- -	40 35 30	mA	3, 4
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		-	3	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current	80 10 12		40 35 30	mA	
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	80 10 12		4 4 4	mA	
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 6.5V, All other Pins Not Under Test = 0V)		-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 6.5V)		-10	10	µA	

Capacitance (V_{CC} = 5V ±10%, f = 1MHz, T_A = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 - A8)	-	4	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	5	pF
C_O	Output Capacitance (D_{OUT})	-	6	pF

* Note : Capacitance is sampled and not 100% tested.

Electrical Characteristics And Recommended AC Operating Conditions

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C256-80		GM71C256-10		GM71C256-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read/Write Cycle Time	145	-	175	-	205	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	175	-	210	-	245	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	60	-	70	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	110	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	-	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	-	30	ns	8, 13
t_{AA}	Access Time from Column Address	-	40	-	45	-	55	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	55	-	65	ns	8, 14
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	25	0	30	ns	9
t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	55	-	65	-	75	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	75000	100	75000	120	75000	ns	
t_{RSH}(R)	$\overline{RAS}$ Hold Time (Read Cycle)	20	-	25	-	30	-	ns	
t_{RSH}(W)	$\overline{RAS}$ Hold Time (Write Cycle)	25	-	30	-	35	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	120	-	ns	
t_{CAS}(R)	$\overline{CAS}$ Pulse width in Read Cycle	20	75000	25	75000	30	75000	ns	
t_{CAS}(W)	$\overline{CAS}$ Pulse Width in Write Cycle	25	-	30	-	35	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	30	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	55	25	65	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	15	-	20	-	25	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	20	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	25	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	45	-	55	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	10
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	5	-	5	-	5	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5	-	5	-	ns	10
t_{AR}	Column Address Hold Time from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{WCR}	Write Commend Hold Time from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	60	-	70	-	80	-	ns	

(V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C) Unit : nS (Note 5, 6, 7)

SYMBOL	PARAMETER	GM71C256-80		GM71C256-10		GM71C256-12		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	15	-	20	-	25	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	15	-	20	-	25	-	ns	11
t_{REF}	Refresh Period (256 cycle)	-	4	-	4	-	4	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to Write Delay Time	20	-	25	-	30	-	ns	12
t_{RWD}	$\overline{RAS}$ to Write Delay Time (RMW)	80	-	100	-	120	-	ns	12
t_{AWD}	Column Address to Write Delay	40	-	45	-	55	-	ns	12
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CSR}	$\overline{CAS}$ Set Up Time $\overline{CBR}$ Refresh	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$ Before $\overline{RAS}$ Refresh	25	-	30	-	40	-	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	-	25	-	30	-	ns	
t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse width	110	-	135	-	160	-	ns	

Notes

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltage are refrenced to VSS
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μS is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5nS.
7. V_{IH} (min) and V_{IL} (max) are referenced levels for measuring timing of input signals. Also transition times are required between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max) and t_{OEZ} (max) defines the time at which the output achieves the open circuit condition and is not refrenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle: If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min) the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither or the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a referenced point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a referenced point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

Timing Waveforms

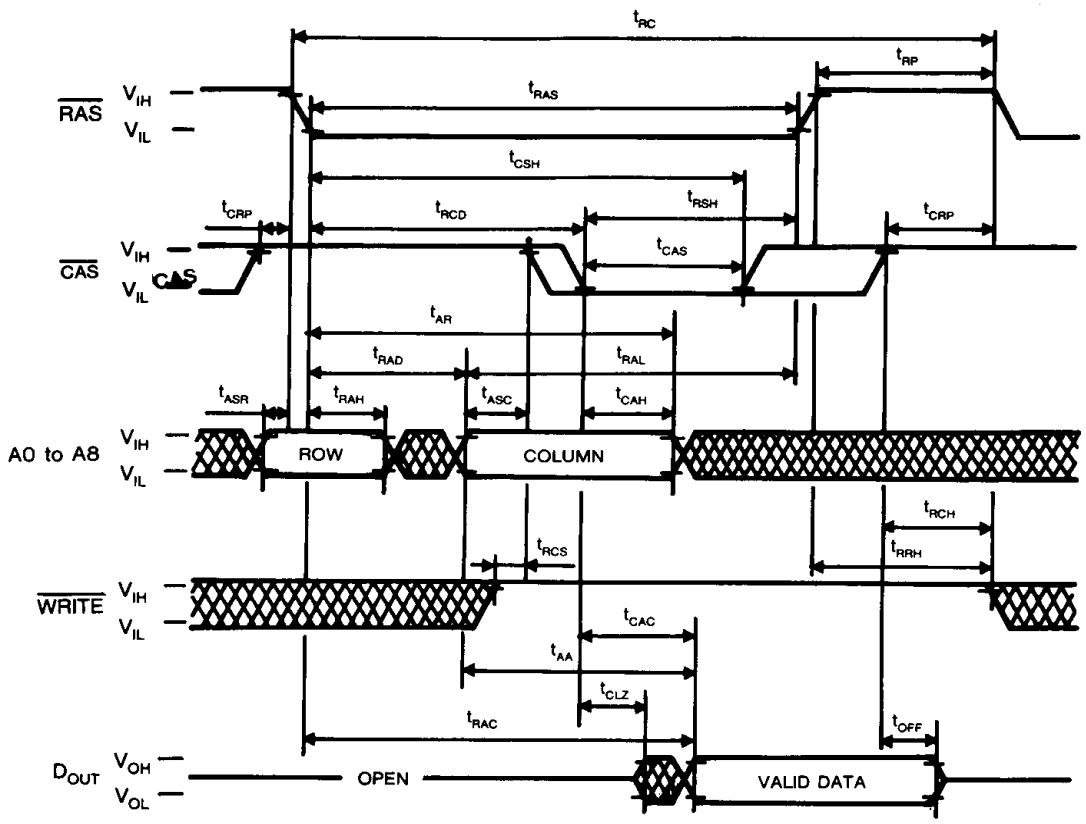


Figure 2 Read Cycle

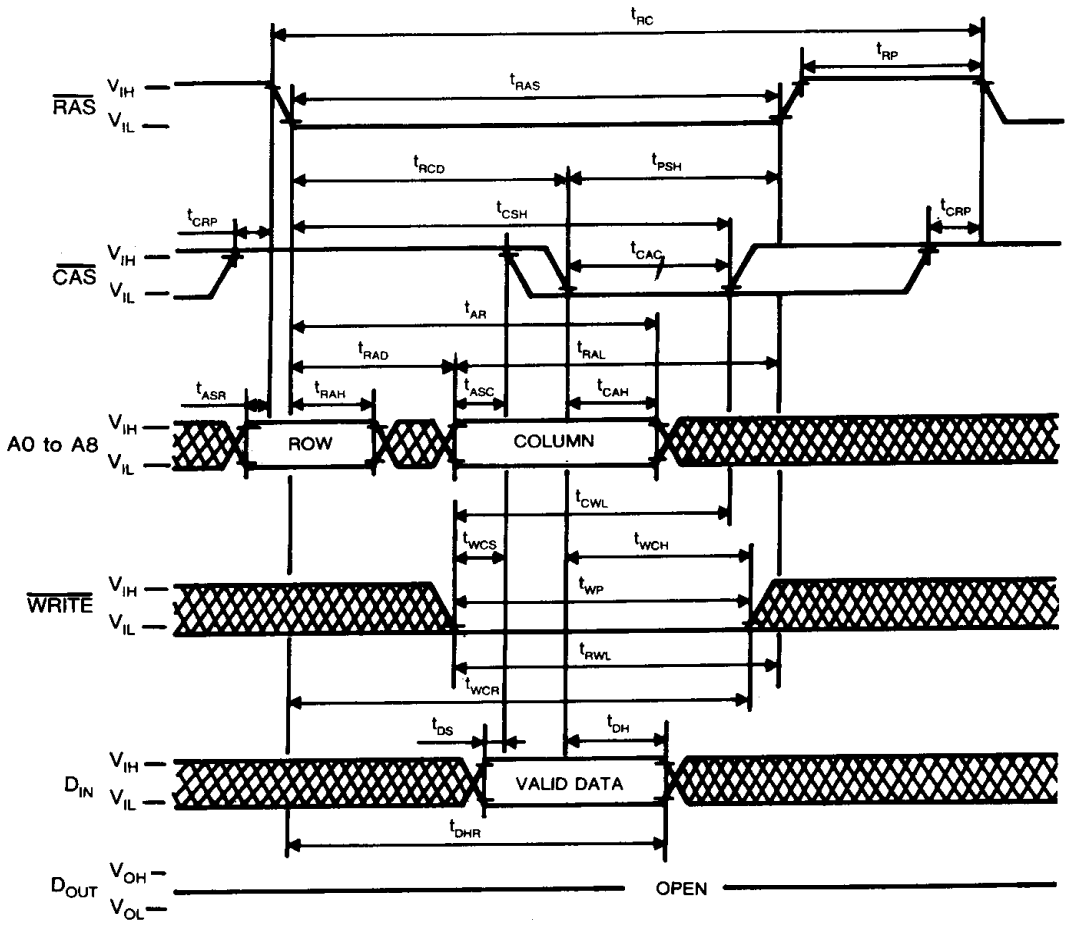


Figure 3 Write Cycle

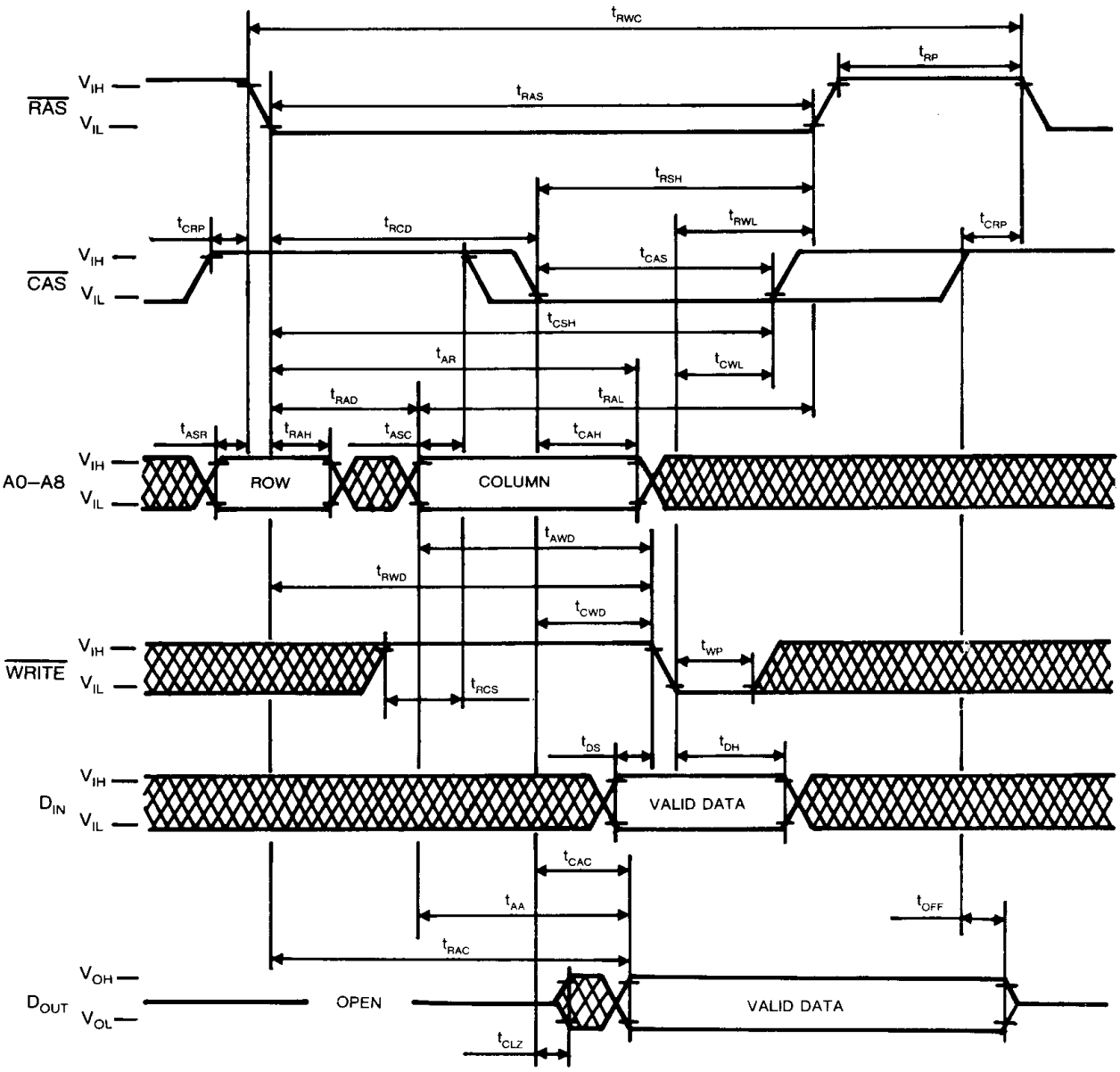


Figure 4. Read-Write Cycle

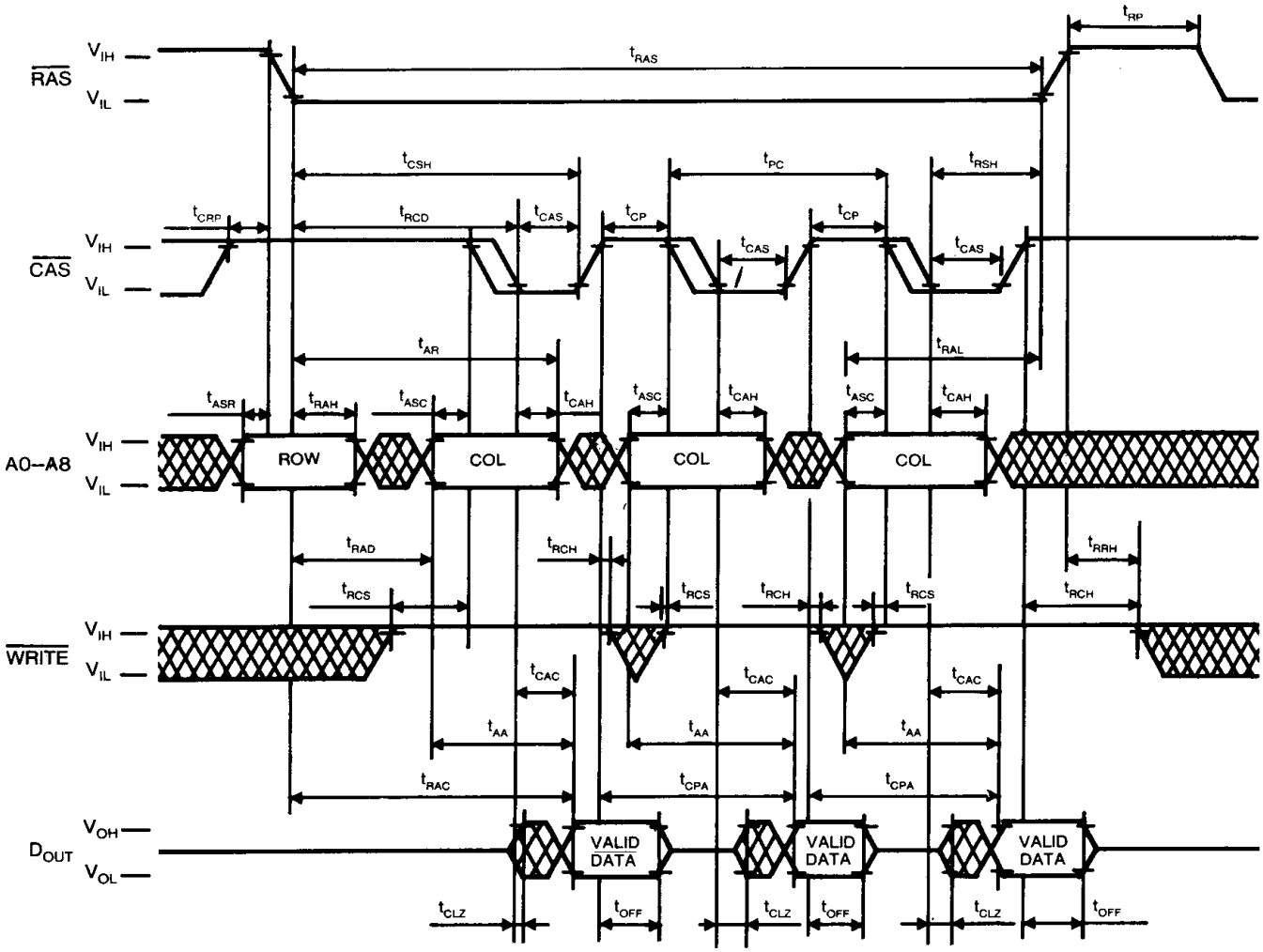


Figure 5. Fast Page Mode Read Cycle

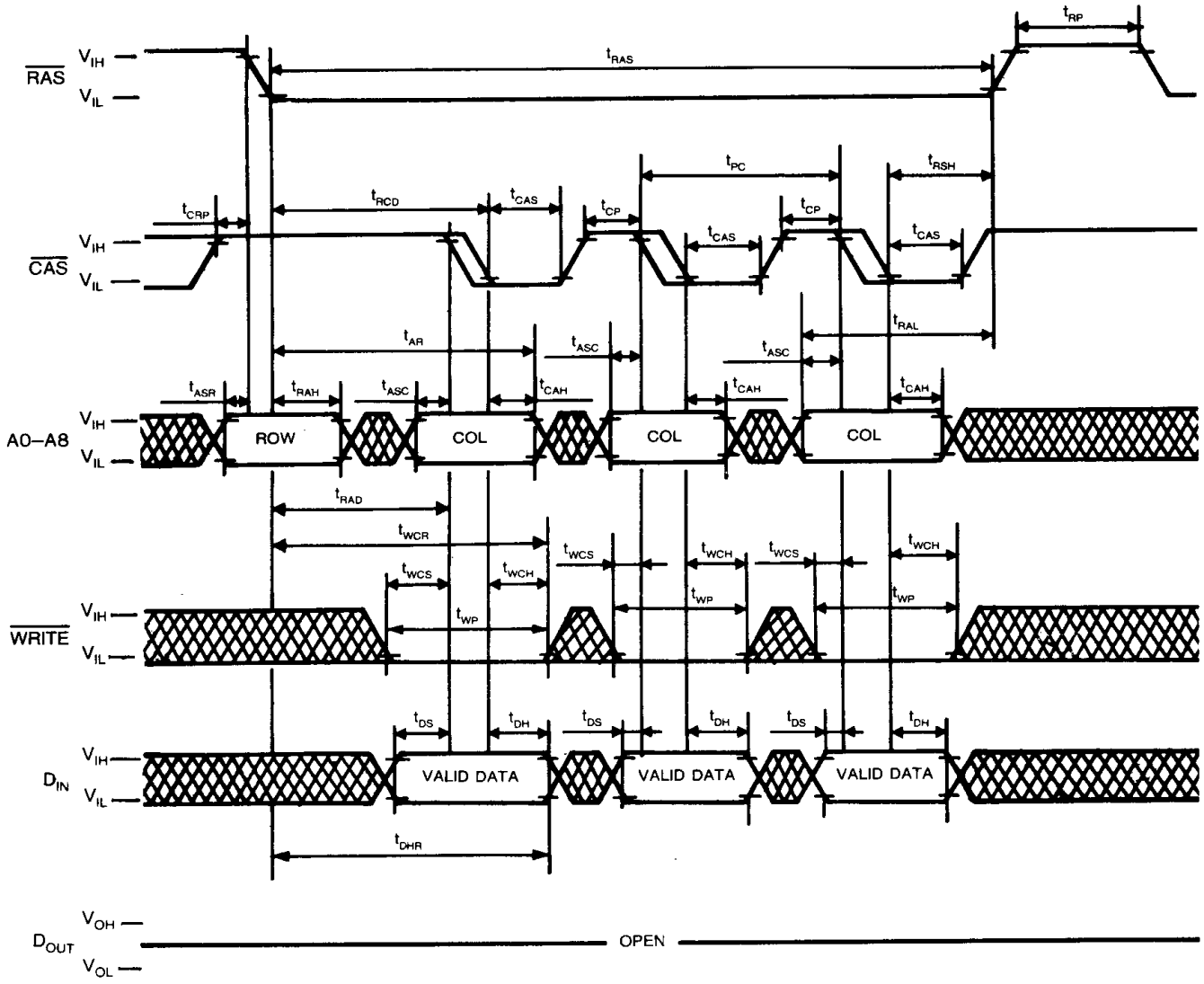


Figure 6. Fast Page Mode Write Cycle (Early Write)

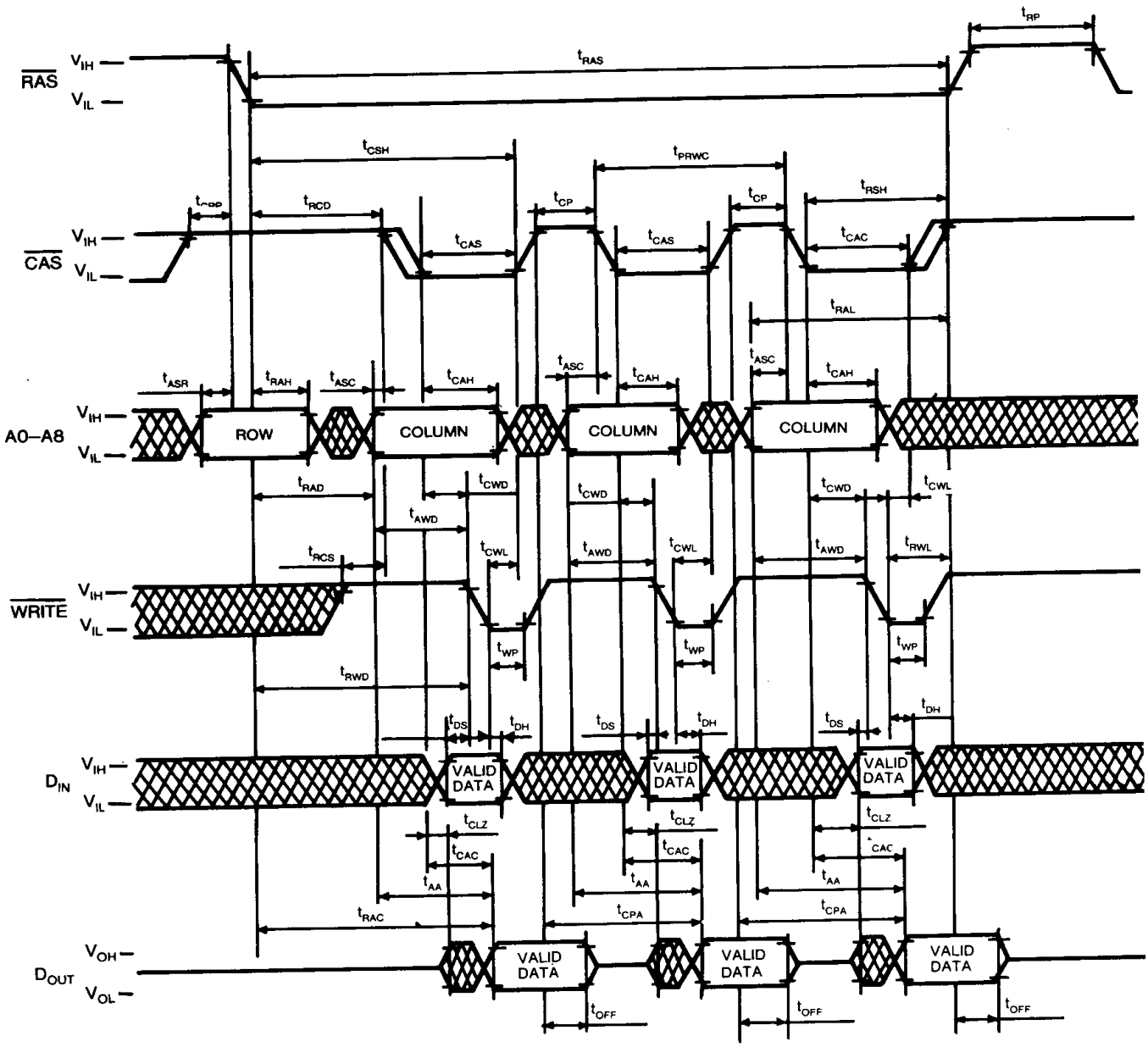


Figure 7. Fast Page Mode Read-Write Cycle

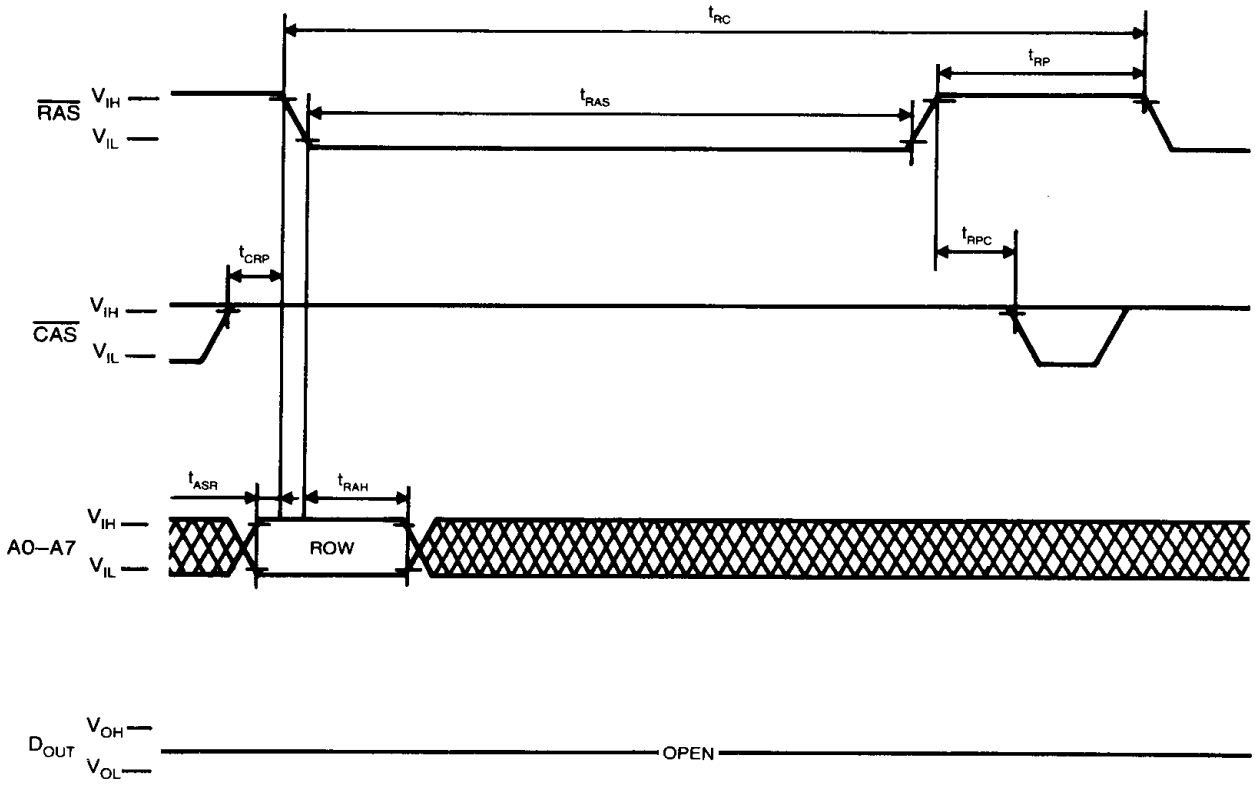


Figure 8. $\overline{RAS}$ Only Refresh Cycle

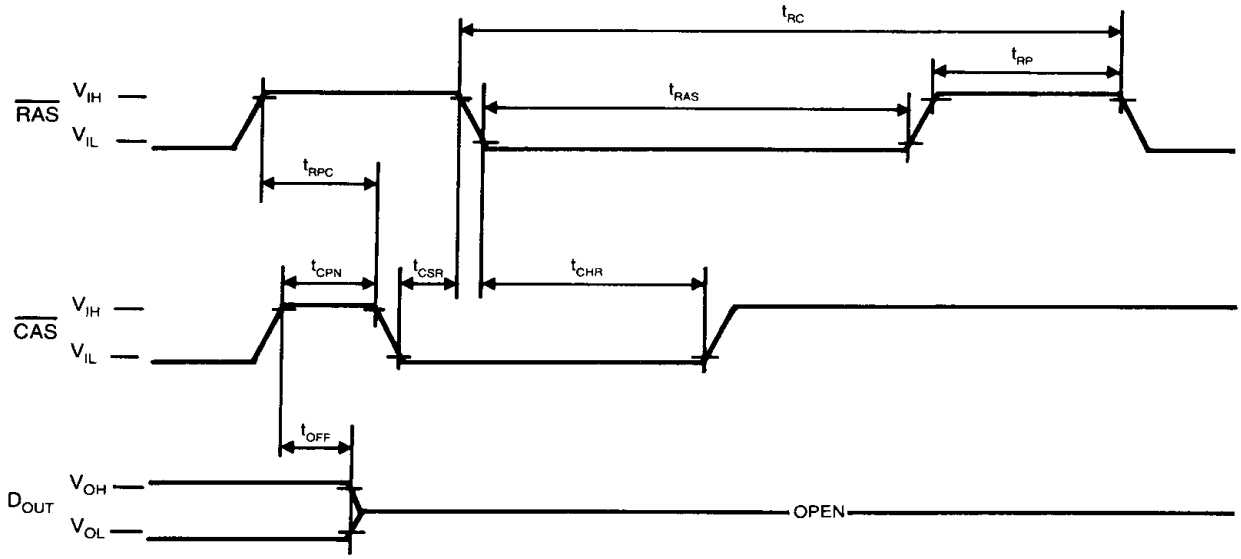


Figure 9. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

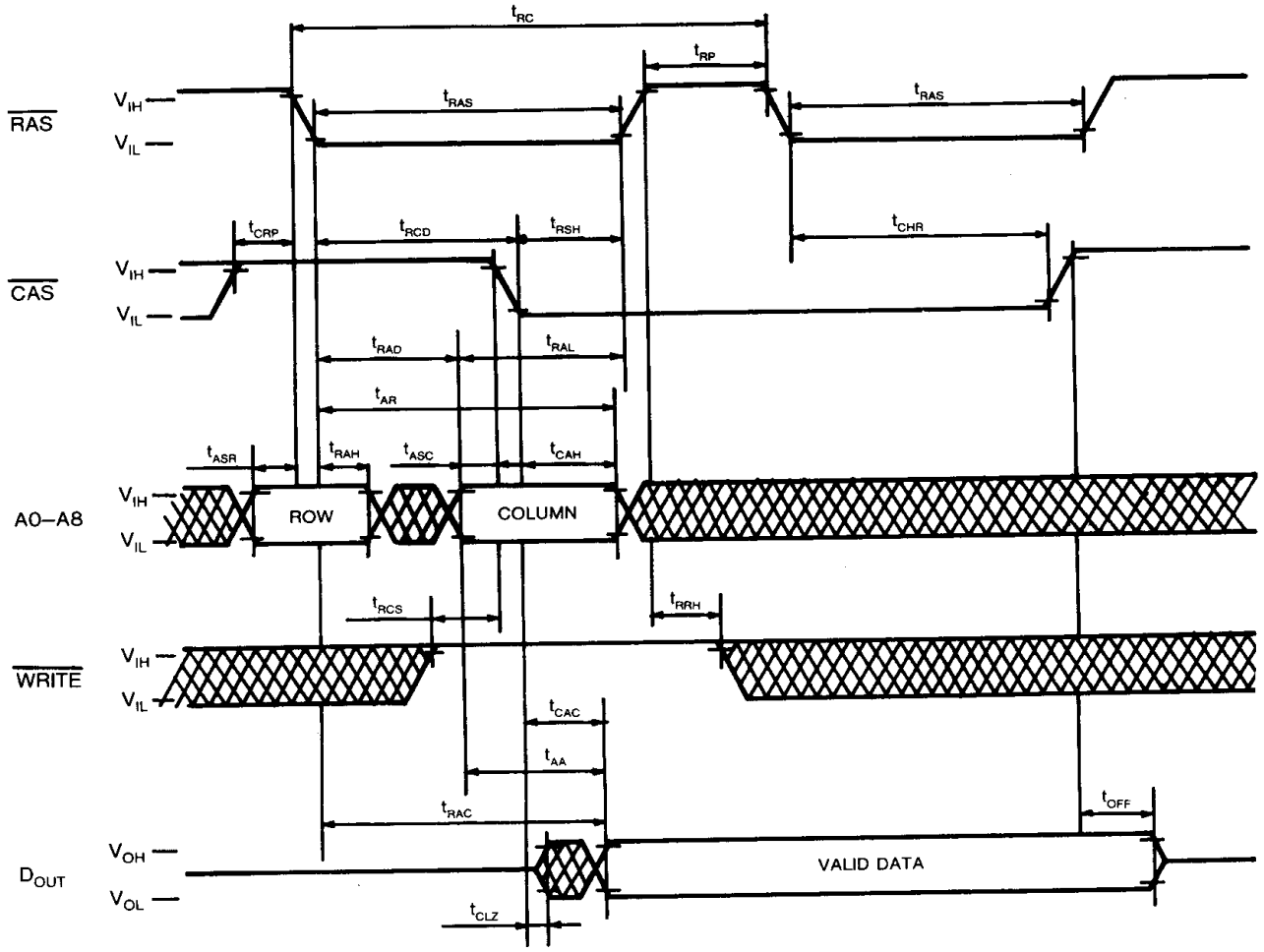


Figure 10. Hidden Refresh Cycle (Read)

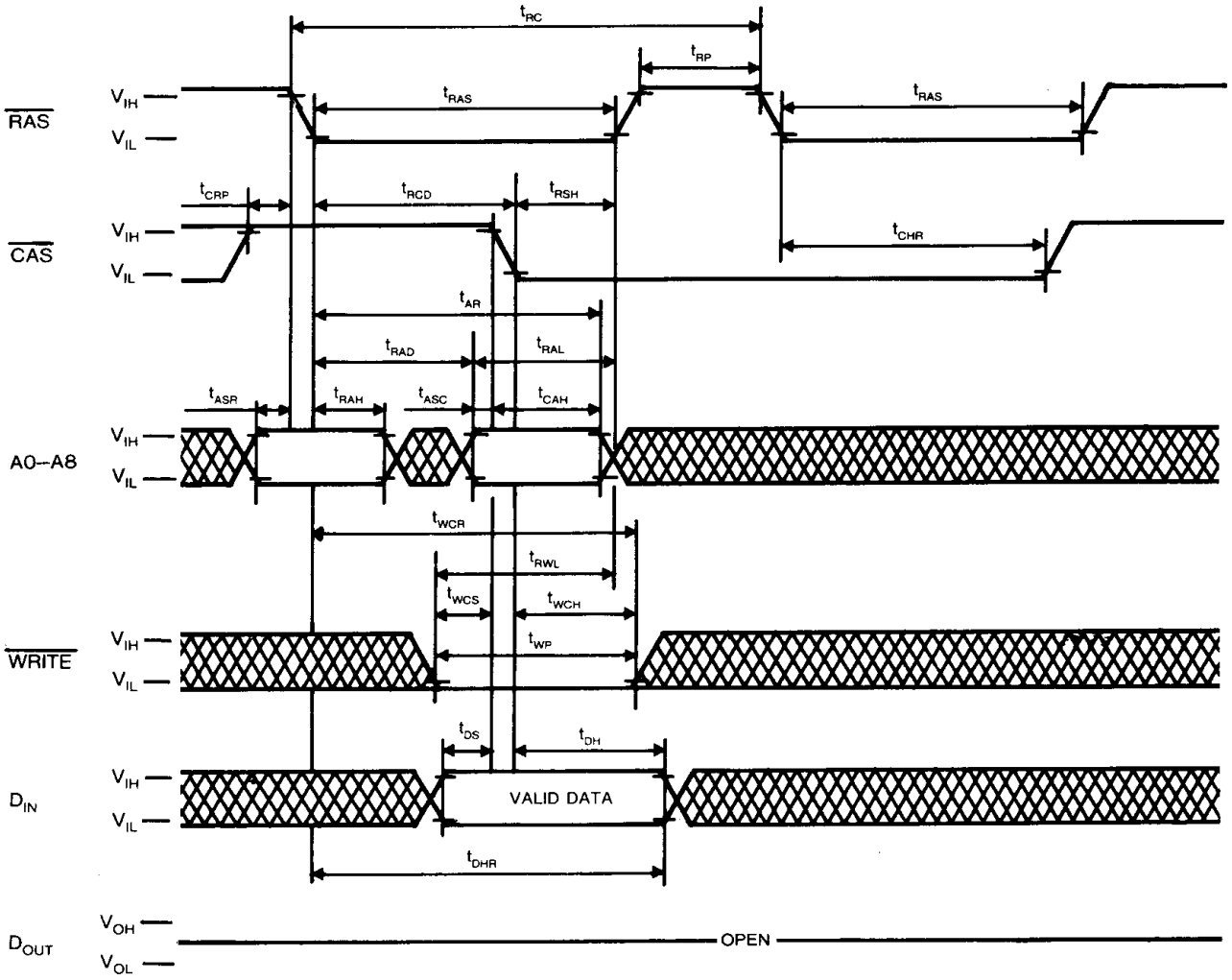


Figure 11. Hidden Refresh Cycle (Write)

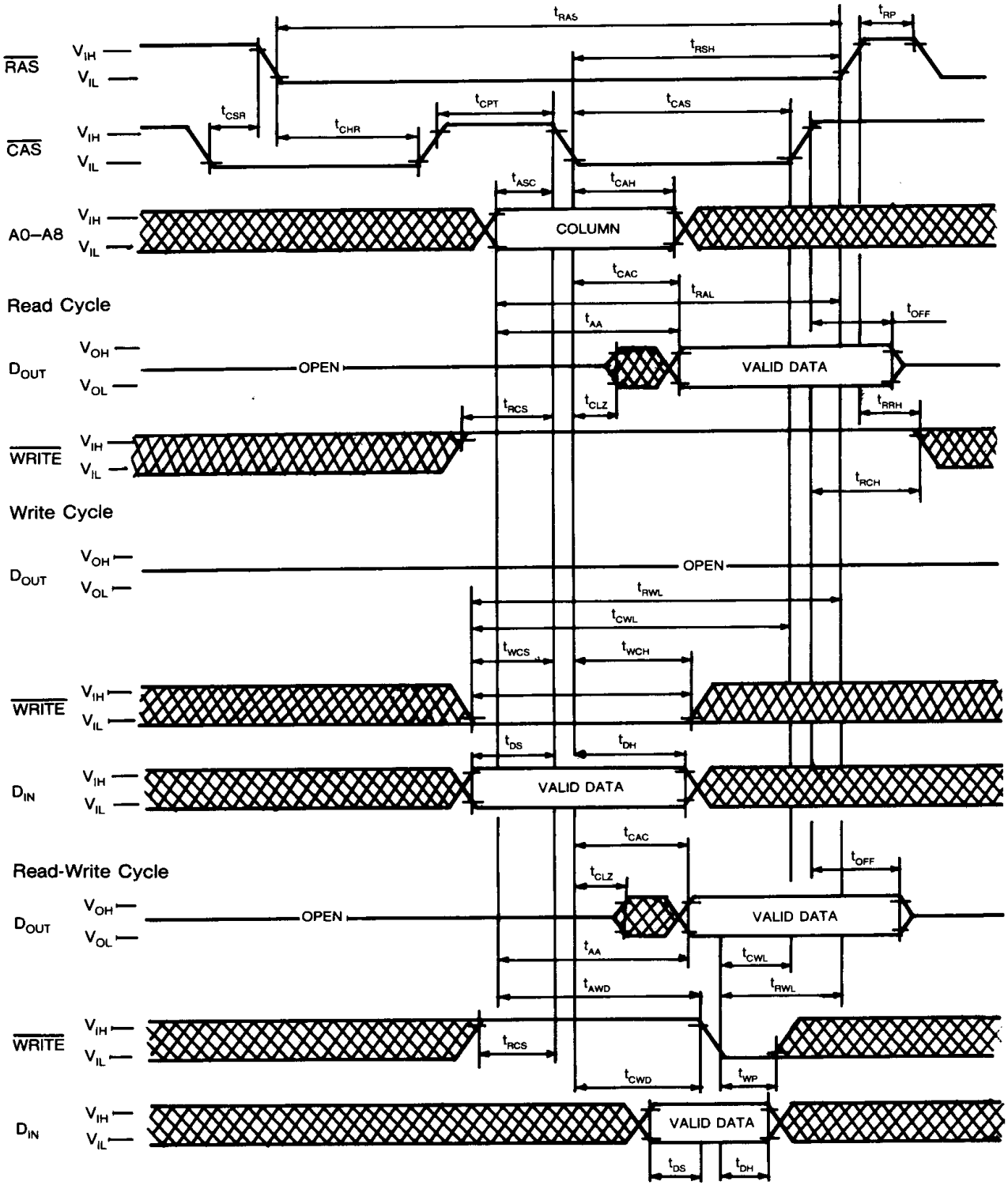


Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle