Genesys Logic, Inc.

GL3590

USB 3.1 Gen 2 Hub Controller

Datasheet

Revision 1.70
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Revision History

Revision	Date	Description
1.00	05/07/2018	Formal Release
1.10	06/20/2018	Modify block diagram and pin descriptions Add Section 4.3.16 Configuration Channel (CC) Characteristics, p.26
1.20	11/12/2018	Remove HID and Billboard information
1.30	01/02/2019	Add GL3590-OV6S1 and GL3590-OV7S1 information Update power consumption, p.43
1.40	02/22/2019	Correct typo Add power range for 1.2V, p.40
1.50	03/28/2019	Correct pin 61 and pin 62 of GL3590-OV7S1 Update package information for BGA289 and BGA144
1.60	05/14/2019	Update GL3590-S functional block, p.27 Update pin description, p.22 and 23
1.70	05/08/2020	Update Section 6.1-6.4

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CHAPTER 1 GENERAL DESCRIPTION

Genesys GL3590 is a low-power, and configurable USB 3.1 Gen 2 hub controller. It is compliant with the USB 3.1 specification. GL3590 integrates Genesys Logic self-developed USB 3.1 Gen 2 Super Speed transmitter/receiver physical layer (PHY) and USB 2.0 High-Speed PHY. It supports Super Speed, Hi-Speed, and Full-Speed USB connections and is fully backward compatible to all USB 2.0 and USB 1.1 hosts. GL3590 also implements multiple TT* (Note1) architecture providing dedicated TT* to each downstream (DS) port, which guarantees Full-Speed(FS) data passing bandwidth when multiple FS devices perform heavy loading operations.

GL3590 features the native fast-charging and complies with USB-IF battery charging specification rev1.2. With different configurations, it could fast-charge Apple devices with up to 2.4A, Samsung Galaxy devices, and any device complaint with BC1.2/1.1. It also allows portable devices to draw up to 1.5A from GL3590 charging downstream ports (CDP[1]) or dedicated charging port (DCP[2]). It can enable systems to fast charge handheld devices even during "Sleep" and "Power-off" modes.

With different part numbers, GL3590 also has USB Type-C function integrated (GL3590-S).

Available packages of GL3590/GL3590-S are listed in the following table.

Product Series	Package Type	Total Ports (UFP+DFP)	Power Mgmt.	GPIOs
GL3590	QFN76	1 USB-A SS+ 4 USB-A SS+	Individual/ Gang	Green/Amber
GL3590-S (USB-C Port Integrated)	QFN88	1 USB-C SS+ 4 USB-A SS+	Individual/ Gang	Green
	QFN88	2 USB-C SS+ 3 USB-A SS+	Individual/ Gang	-
	QFN88	1 USB-C SS+ 4 USB-A SS+ 1 HS non-removable port	Individual/ Gang	Green
	QFN88	1 USB-C SS+ 4 USB-A SS+ 2 HS non-removable ports	Individual/ Gang	Green
	BGA144	3 USB-C SS+ 3 USB-A SS+	Individual/ Gang	Green/Amber
	BGA289	4 USB-C SS+ 2 USB-A SS+ 3 USB-A HS	Individual/ Gang	Green/Amber

GL3590/GL3590-S Available Packages

*Note: TT (transaction translator) implements the control logic defined in Section 11.14 ~ 11.22 of USB specification revision 2.0. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub.

[1] CDP, charging downstream port, the Battery Charging Rev.1.2-compliant USB port that does data communication and charges device up to 1.5A.

[2] DCP, dedicated charging port, the Battery Charging Rev.1.2-compliant USB port that only charges devices up to 1.5A, similar to wall chargers.

CHAPTER 2 FEATURES

- Compliant with USB 3.1 Specification
  - Upstream port supports SuperSpeed+ (10G/SS+), SuperSpeed (5G/SS), HighSpeed (HS) and FullSpeed (FS) traffic
  - Downstream ports support SS+, SS, HS, FS, and LowSpeed (LS) traffic
  - 1 control pipe and 1 interrupt pipe
  - Backward compatible to USB specification Revision 2.0/1.1
- Native USB USB-C/Power delivery support in GL3590-S series
  - Compliant with USB Type-C™ Cable and Connection Specification Revision 1.0
  - Compliant with Power Delivery spec rev. 3.0
  - Support TCPC interface; compliant with Type-C™ Port Controller Interface Spec 1.0
  - Support up to 2-port Power Delivery 3.0
  - Support up to 4-port native USB Type-C ports, no external Mux or CC controller needed
  - USB-C port supporting USB-C current modes , including USB Default, 1.5A@5V, 3A@5V
- On-chip 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - 1 cycle instruction execution (maximum)
  - Performance: 12 MIPS @ 12.5MHz (maximum)
  - With 256-byte RAM, 20K-byte internal ROM, and 64K-byte SRAM
- Multiple Transaction Translator (TT) architecture
  - Providing dedicated TT control logics for each downstream port
  - Superior performance when multiple FS devices operate concurrently
- Integrated USB transceiver
  - Improving output drivers with slew-rate control for EMI reduction
  - Internal power-fail detection for ESD recovery
- Advanced power management and low power consumption
  - Supporting USB 3.1 U0/U1/U2/U3 power management states
  - Supporting USB Link Power Management (LPM) L0/L1/L2
  - Supporting individual/gang mode over-current detection for all downstream ports
  - Supporting both low/high-enabled power switches
  - Patented Smart Power Management
- Configurable settings by firmware
  - Configurable downstream ports, downstream port can be disabled/enabled by each specific port for USB3.1/USB2.0
  - Configurable Upstream and Downstream Ports in GL3590-S
  - Configurable charging port
  - Supporting full in-system programming firmware upgrade by SPI-flash
  - Supporting compound-device (non-removable setting on downstream ports)
  - Supporting customization VID/PID
- Flexible design
  - Supporting Poly-fuse/Power-switch
  - Automatic switching between self-powered and bus-powered modes
  - Supporting electrical tuning for each specific port
  - Supporting programmable breathing LED
  - Supporting register setting by firmware
  - Supporting vendor command and SMBUS
  - Multiple upstream port supported in GL3590-S
  - Host bridge hardware engine implemented in GL3590-S for KM applications

- Featuring fast-charging on all downstream ports and upstream port
  - Compliant with USB Battery Charging Revision v1.2, supporting CDP, DCP, and ACA-Dock
  - Downstream ports can be turned from a Standard Downstream Port (SDP) into Charging Downstream Port (CDP) or Dedicated Charging Port (DCP)
  - Downstream devices can be charged while upstream VBUS is not present, which can be applied on wall charger applications
  - Upstream port is capable of charging and data communicating simultaneously for portable devices supporting ACA-Dock or proprietary charging protocols
  - Supporting Apple 1A/2.1A/2.4A and Samsung Galaxy devices fast-charging
- Low BOM cost
  - Single external 25 MHz crystal / Oscillator clock input
  - Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
- Different package types available for various applications
- Applications
  - Standalone USB hub/Docking station
  - Motherboard
  - Monitor built-in hub, GPIOs can be programmed as I2C interface to easily update scalar firmware through USB interface
  - TV built-in hub
  - KM application
  - Customized applications
    - Dynamically disable/enable ports
    - GPIO signaling of ambient light sensor or rotation/position sensor

CHAPTER 3 PIN ASSIGNMENT

3.1 GL3590 Pin-out Diagram

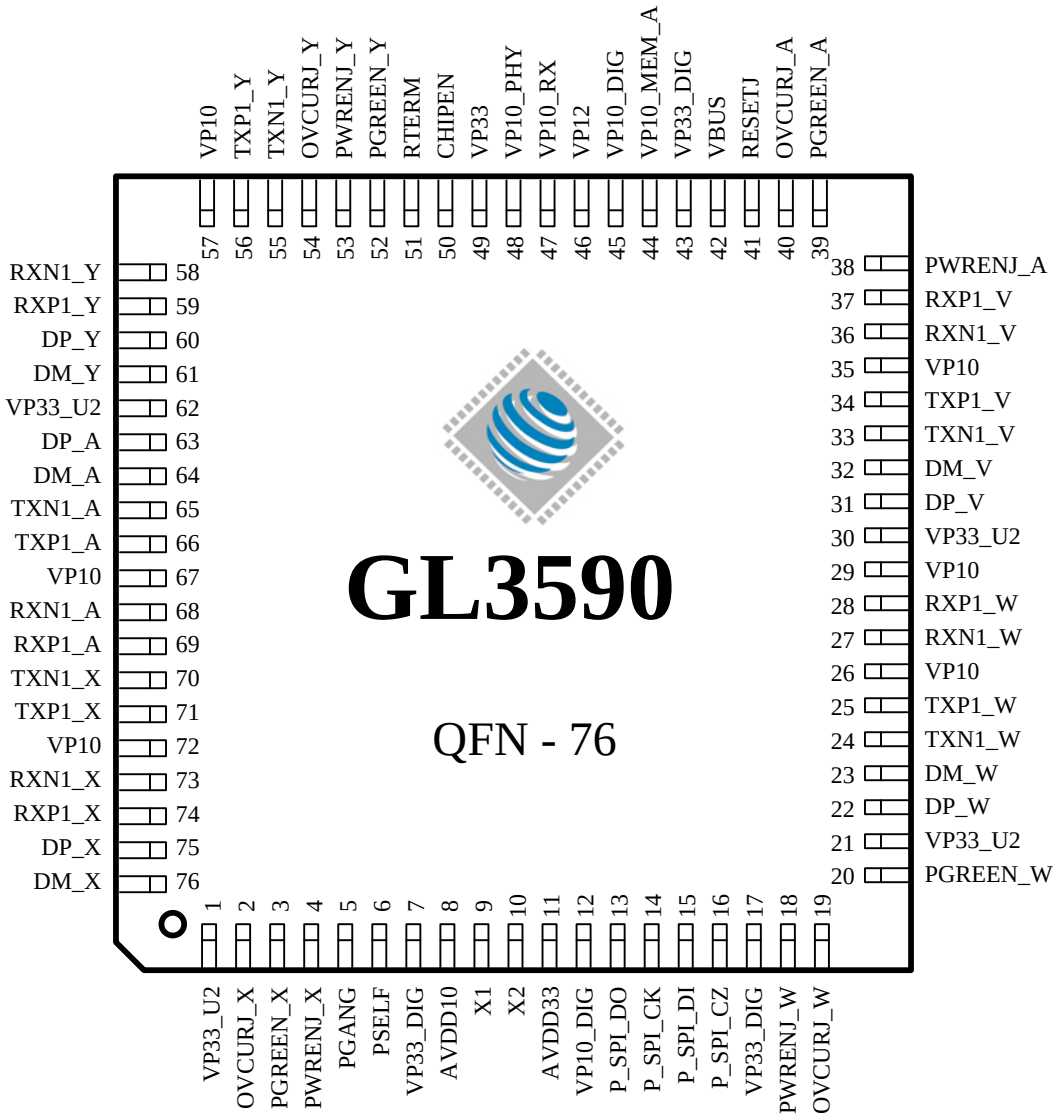


Figure 3.1 - GL3590 QFN 76 (4A DFP) Pin-out Diagram

3.2 GL3590-S Pin-out Diagram

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
OVCURJ_X	DM_Z	TXN2_X	RXN2_X	DP_X	RXP1_X	TXP1_X	PAMBER_Y	RXN1_A	TXP1_A	DP_A	TXN2_Y	RXN2_Y	DP_Y	RXN1_Y	TXN1_Y	GPIO_12	A
PWRENJ_X	DP_Z	TXP2_X	RXP2_X	DM_X	RXN1_X	TXN1_X	PGREEN_Y	RXP1_A	TXN1_A	DM_A	TXP2_Y	RXP2_Y	DM_Y	RXP1_Y	TXP1_Y	GPIO_13	B
PGREEN_X	PAMBER_X	PWRENJ_Z	PAMBER_Z	VP33_U2	VP33_U2	VP33_U2	OVCURJ_Y	PWRENJ_Y	VP33_U2	OVCURJ_C	PWRENJ_C	PAMBER_C	TOD2	VP33_DIG	GPIO_09	GPIO_14	C
VP5_CC_U	OVCURJ_Z	PGREEN_Z	PGANG	VP10	VP10	VP10	VP10	VP10	VP10	VP10	VP10	PGREEN_C	Y_ISENSE	A_ISENSE	GPIO_10	GPIO_15	D
VP5_CC_U	VP33_DIG	VP10	VP10	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_ISENSE	W_ISENSE	GPIO_11	GPIO_16	E
X1	PSELF	TOD1	X_VCDR	GND	GND	GND	GND	GND	GND	GND	GND	GND	A_FBD	W_FBD	VP10_MEM_B	VP33	F
X2	CC1_X	CC2_X	VP10_DIG	GND	GND	GND	GND	GND	GND	GND	GND	GND	RTERM	CHIPEN	VP10_DIG	VP33	G
AVDD33	CC2_Y	CC1_Y	AVDD10	GND	GND	GND	GND	GND	GND	GND	GND	GND	VP33	VP33	VP33	VP33	H
CC1_V	CC2_V	X_ISENSE	Z_ISENSE	GND	GND	GND	GND	GND	GND	GND	GND	GND	NC	NC	NC	NC	J
CC2_W	CC1_W	B_ISENSE	C_ISENSE	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	K
VP5_CC_D	VP10_DIG	VP10_MEM_A	P_SPI_CZ	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VP10_MEM_B	VP10_PHY	VP10_PHY	L
VP5_CC_D	GPIO_06	VP33_DIG	P_SPI_DI	GND	GND	GND	GND	GND	GND	GND	GND	GND	VBUS	VP10_DIG	VP10_PHY	VP10_PHY	M
GPIO_01	GPIO_07	P_SPI_CK	P_SPI_DO	GND	GND	GND	GND	GND	GND	GND	GND	GND	RESETJ	VP10_MEM_A	VP12	VP12	N
GPIO_02	GPIO_08	PWRENJ_B	OVCURJ_W	PWRENJ_W	VP10	VP10	VP10	VP10	VP10	VP10	VP10	VP10	PWRENJ_D	VP33_DIG	VP12	VP12	P
GPIO_03	OVCURJ_B	PGREEN_B	PAMBER_B	PGREEN_W	PAMBER_W	VP33_U2	VP33_U2	VP33_U2	VP33_U2	VP33_U2	VP33_U2	OVCURJ_D	PGREEN_D	PAMBER_D	PAMBER_A	PGREEN_A	R
GPIO_04	DM_C	TXP1_W	RXP1_W	DM_W	RXP2_W	TXP2_W	TXP1_B	RXP1_B	DM_B	TXN1_V	RXN1_V	DP_V	RXP2_V	TXP2_V	DP_D	PWRENJ_A	T
GPIO_05	DP_C	TXN1_W	RXN1_W	DP_W	RXN2_W	TXN2_W	TXN1_B	RXN1_B	DP_B	TXP1_V	RXP1_V	DM_V	RXN2_V	TXN2_V	DM_D	OVCURJ_A	U

Figure 3.2 - GL3590-S BGA 289 Pin-out Diagram

1	2	3	4	5	6	7	8	9	10	11	12	
DP_X	RXN2_X	RXN1_X	TXN1_X	VP10	RXN1_A	TXP1_A	DM_A	DM_Y	TXN2_Y	RXP2_Y	RXP1_Y	A
DM_X	RXP2_X	RXP1_X	TXP1_X	VP10	RXP1_A	TXN1_A	DP_A	DP_Y	TXP2_Y	RXN2_Y	RXN1_Y	B
TXN2_X	VP33_DIG	PWRENJ_X	VP33_U2	OVCURJ_X	OVCURJ_Y	VP10	VP10	VP10	GPIO_12	GPIO_11	TXN1_Y	C
TXP2_X	CC1_X	VP10_DIG	PAMBER_X	PGREEN_X	PWRENJ_Y	VP33_U2	PGREEN_Y	PAMBER_Y	GPIO_14	GPIO_13	TXP1_Y	D
VP5_CC_U	CC2_X	AVDD10	Z_ISENSE	GND	GND	GND	GND	A_FBD	OVCURJ_A	GPIO_15	VP10_DIG	E
X1	CC1_Y	X_ISENSE	C_ISENSE	GND	GND	GND	GND	W_FBD	W_ISENSE	GPIO_16	VP33	F
X2	CC2_Y	B_ISENSE	PGANG	GND	GND	GND	GND	PWRENJ_A	CHIPEN	RTERM	VP10_MEM_B	G
AVDD33	CC2_W	P_SPI_DI	OVCURJ_B	GND	GND	GND	GND	VBUS	PGREEN_A	VP10_PHY	VP10_PHY	H
VP5_CC_D	CC1_W	P_SPI_CK	PGREEN_B	P_SPI_DO	P_SPI_CZ	OVCURJ_W	PGREEN_W	PWRENJ_B	VP12	VP12	VP12	J
VP10_DIG	VP33_DIG	PWRENJ_W	VP33_U2	VP10	VP10	VP33_U2	VP10	VP10	PAMBER_A	RESETJ	VP10_DIG	K
DP_W	TXP1_W	RXN1_W	RXN2_W	TXP2_W	TXP1_B	RXP1_B	DM_B	DM_V	TXP1_V	RXP1_V	VP10_MEM_A	L
DM_W	TXN1_W	RXP1_W	RXP2_W	TXN2_W	TXN1_B	RXN1_B	DP_B	DP_V	TXN1_V	RXN1_V	VP33_DIG	M

Figure 3.3 - GL3590-S BGA 144 (3C3A) Pin-out Diagram

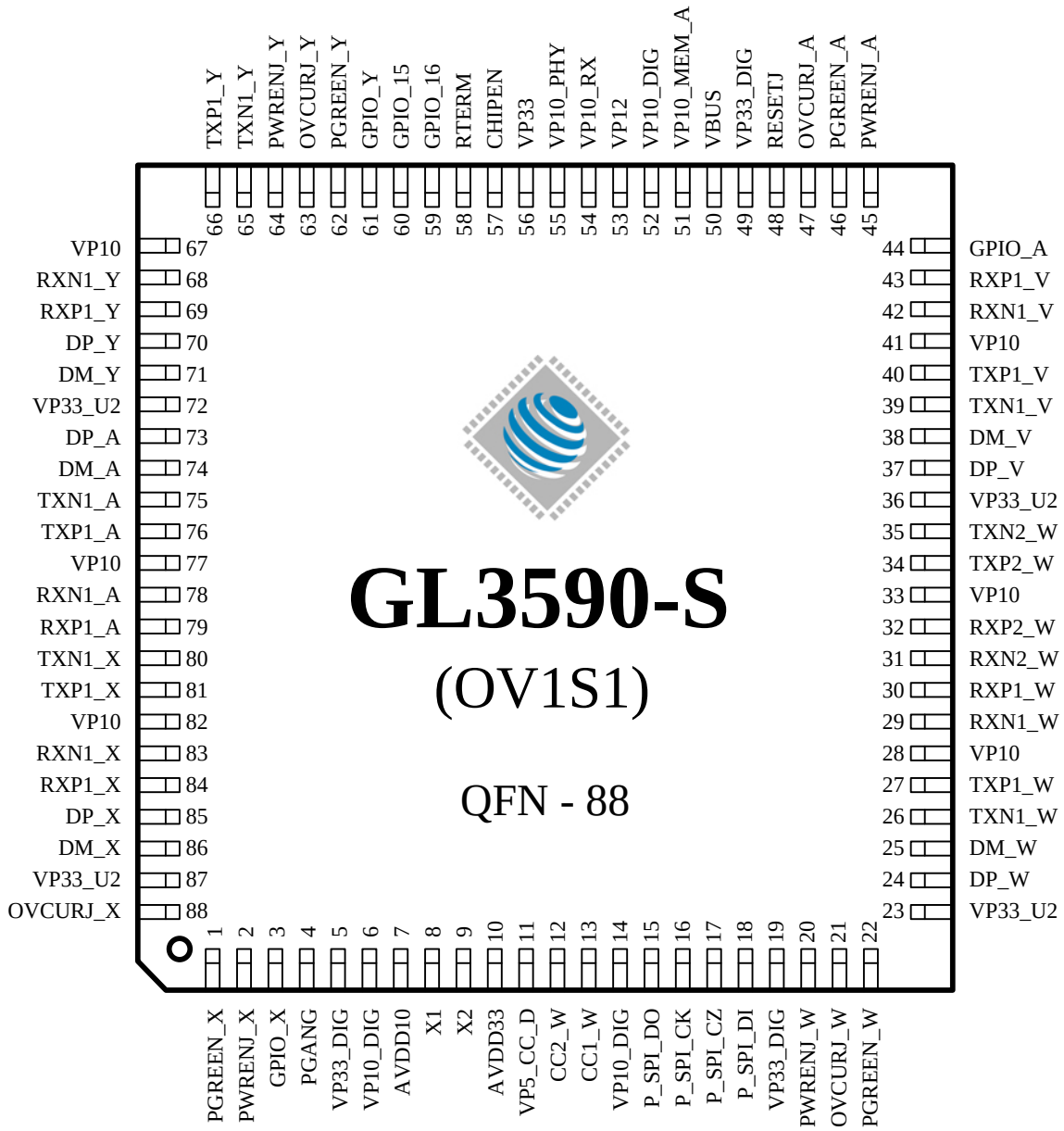


Figure 3.4 - GL3590-S QFN 88 (1C4A) Pin-out Diagram

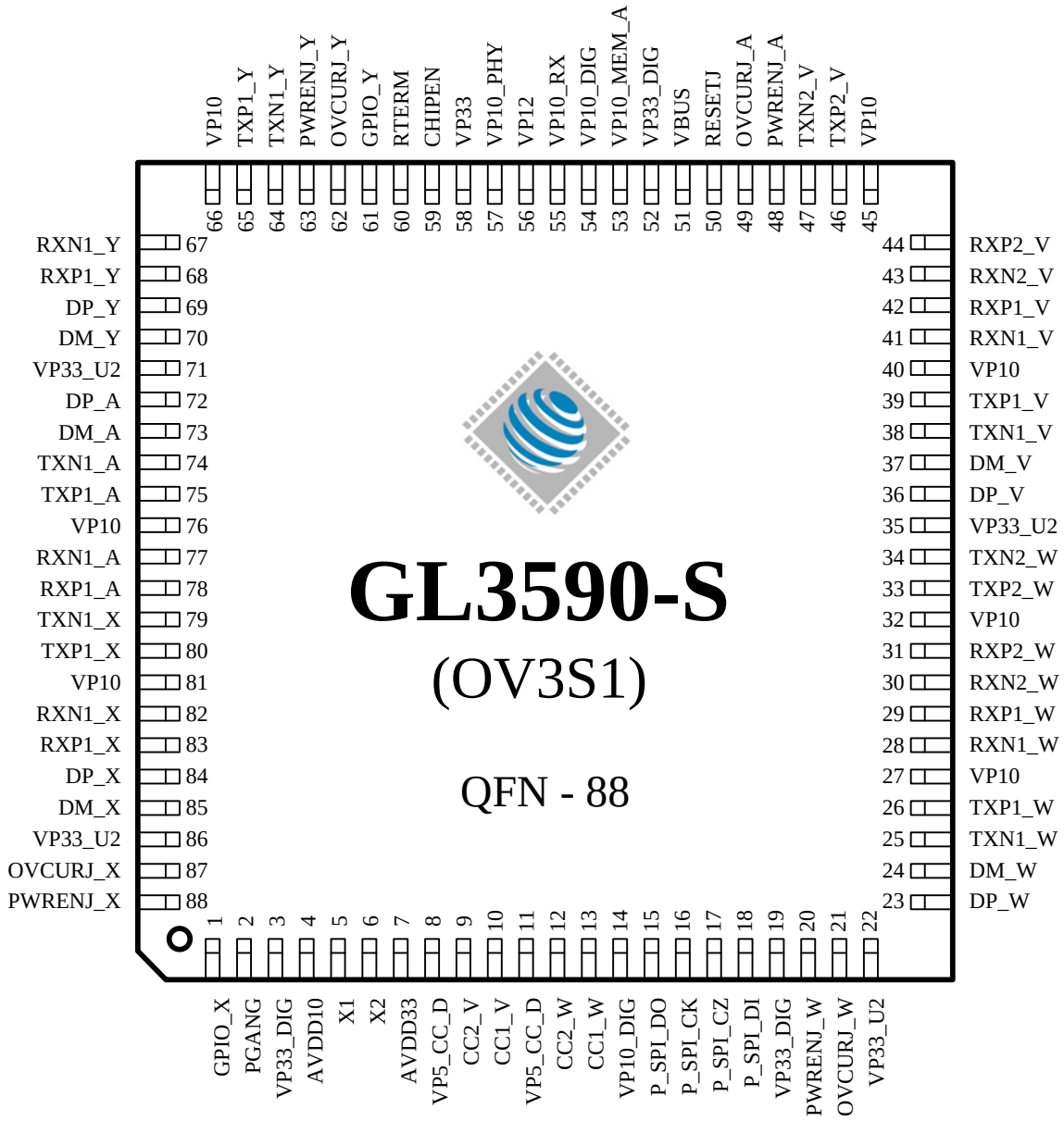


Figure 3.5 - GL3590-S QFN 88 (2C3A) Pin-out Diagram

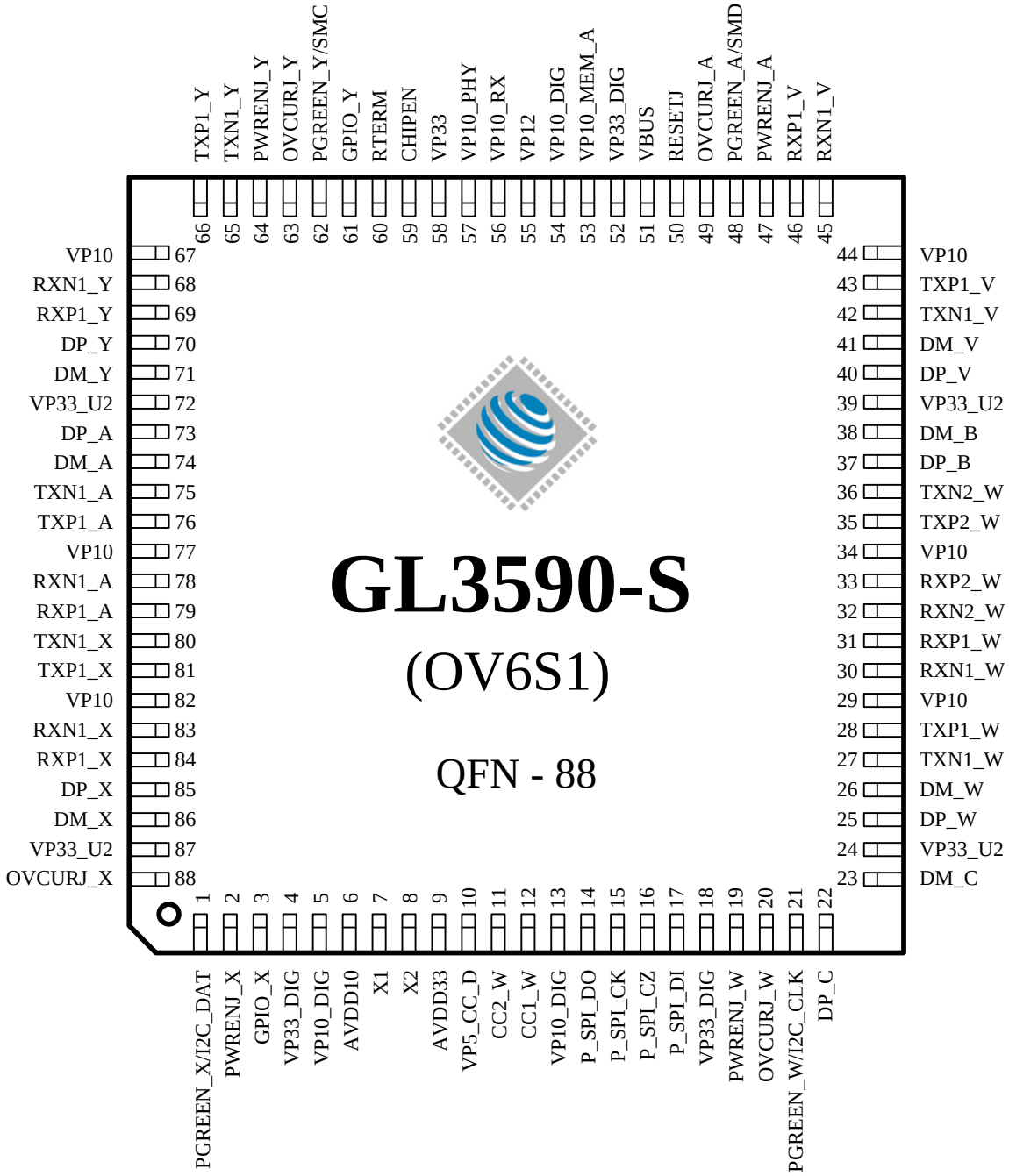


Figure 3.6 - GL3590-S QFN 88 (1C4A2HS) **Pin-out Diagram**

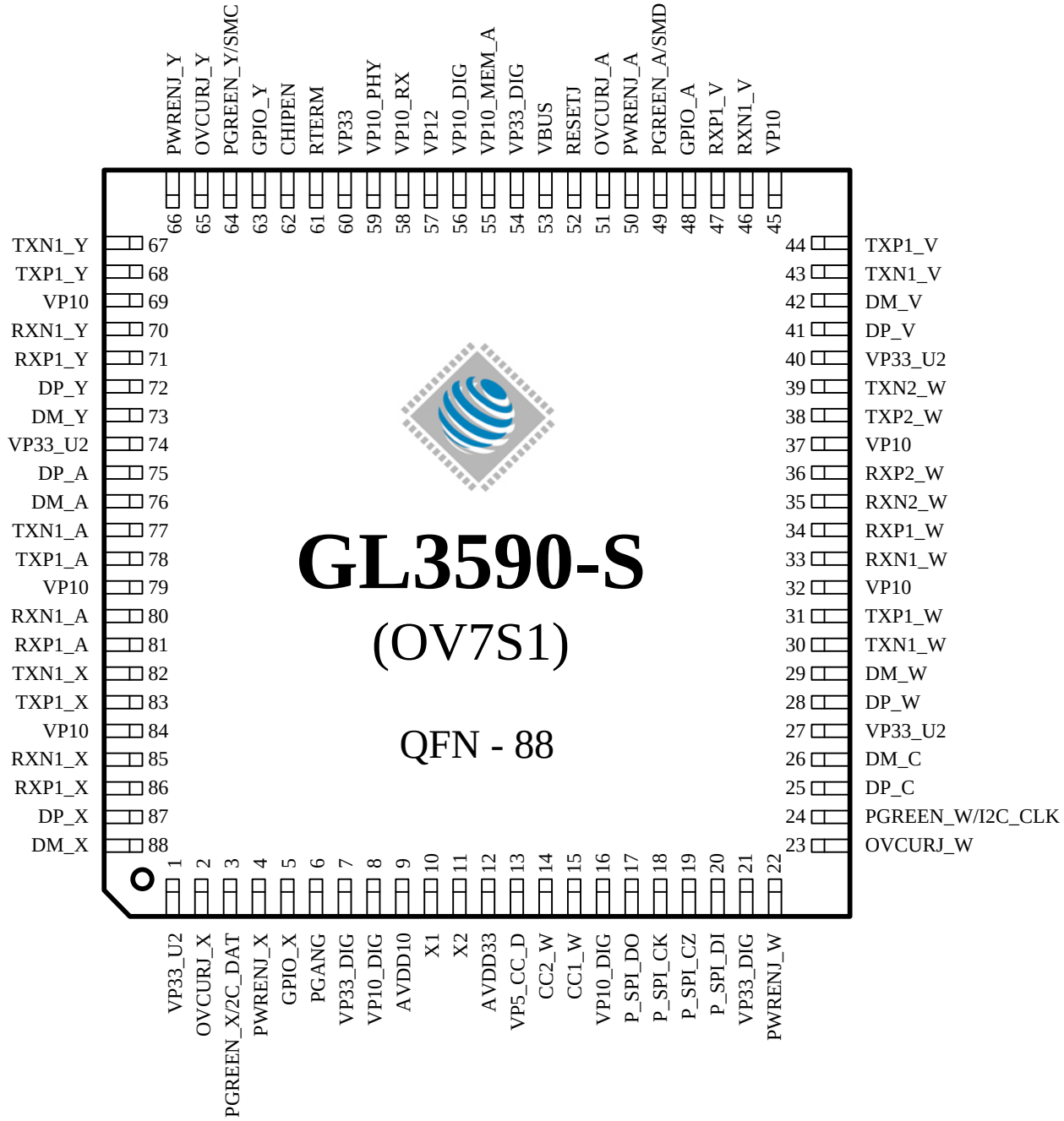


Figure 3.7 - GL3590-S QFN 88 (1C4A1HS) Pin-out Diagram

3.3 GL3590/GL3590-S Port Matrix

Product Series	Package Type	Total Ports (UFP+DFP)	Port Type and Operating Speed
GL3590	QFN76 (GL3590-OTY10)	1 USB-A SS+ 4 USB-A SS+	Port V, W, X, Y, A: USB-A, SS+
GL3590-S (USB-C port Integrated)	QFN88 (GL3590- OV1S1)	1 USB-C SS+ 4 USB-A SS+	Port W: USB-C, SS+ Port V, X, Y, A: USB-A, SS+
	QFN88 (GL3590- OV3S1)	2 USB-C SS+ 3 USB-A SS+	Port V, W: USB-C, SS+ Port X, Y, A: USB-A, SS+
	QFN88 (GL3590-OV6S1)	1 USB-C SS+ 4 USB-A SS+ 2 HS non-removable port	Port W: USB-C, SS+ Port V, X, Y, A: USB-A, SS+ Port B, C: non-removable HS
	QFN88 (GL3590-OV7S1)	1 USB-C SS+ 4 USB-A SS+ 1 HS non-removable port	Port W: USB-C, SS+ Port V, X, Y, A: USB-A, SS+ Port C: non-removable HS
	BGA144 (GL3590-TBYS1)	3 USB-C SS+ 3 USB-A SS+	Port W, X, Y: USB-C, SS+ Port V, A, B: USB-A, SS+
	BGA289 (GL3590-TZYS1)	4 USB-C SS+ 2 USB-A SS+ 3 USB-A HS	Port V, W, X, Y: USB-C, SS+ Port A, B: USB-A, SS+ Port Z, C, D: USB-A, High Speed

3.4 GL3590/GL3590-S Pin Descriptions

USB Interface				
Name	**BGA289**	**BGA144**	**Type**	**Description**
TXN1_V TXP1_V	T11 U11	M10 L10	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_V (default upstream port)
TXN2_V TXP2_V	U15 T15	-	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_V for Type-C (default upstream port)
RXN1_V RXP1_V	T12 U12	M11 L11	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_V (default upstream port)
RXN2_V RXP2_V	U14 T14	-	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_V (default upstream port) for Type-C
TXN1_W TXP1_W	U3 T3	M2 L2	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_W
TXN2_W TXP2_W	U7 T7	M5 L5	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_W for Type-C
RXN1_W RXP1_W	U4 T4	L3 M3	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_W
RXN2_W RXP2_W	U6 T6	L4 M4	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_W for Type-C
TXN1_X TXP1_X	B7 A7	A4 B4	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_X

TXN2_X TXP2_X	A3 B3	C1 D1	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_X for Type-C
RXN1_X RXP1_X	B6 A6	A3 B3	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_X
RXN2_X RXP2_X	A4 B4	A2 B2	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_X for Type-C
TXN1_Y TXP1_Y	A16 B16	C12 D12	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_Y
TXN2_Y TXP2_Y	A12 B12	A10 B10	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_Y for Type-C
RXN1_Y RXP1_Y	A15 B15	B12 A12	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_Y
RXN2_Y RXP2_Y	A13 B13	B11 A11	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_Y for Type-C
TXN1_A TXP1_A	B10 A10	B7 A7	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_A
RXN1_A RXP1_A	A9 B9	A6 B6	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_A
TXN1_B TXP1_B	U8 T8	M6 L6	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_B
RXN1_B RXP1_B	U9 T9	M7 L7	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_B
DM_V DP_V	U13 T13	L9 M9	B	USB 2.0 DM/DP for PORT_V
DM_W DP_W	T5 U5	M1 L1	B	USB 2.0 DM/DP for PORT_W
DM_X DP_X	B5 A5	B1 A1	B	USB 2.0 DM/DP for PORT_X
DM_Y DP_Y	B14 A14	A9 B9	B	USB 2.0 DM/DP for PORT_Y
DM_A DP_A	B11 A11	A8 B8	B	USB 2.0 DM/DP for PORT_A
DM_B DP_B	T10 U10	L8 M8	B	USB 2.0 DM/DP for PORT_B
DM_Z DP_Z	A2 B2	-	B	USB 2.0 DM/DP for PORT_Z
DM_C DP_C	T2 U2	-	B	USB 2.0 DM/DP for PORT_C
DM_D DP_D	U16 T16	-	B	USB 2.0 DM/DP for PORT_D

Name	QFN88 (OV3S1)	QFN88 (OV1S1)	QFN88 (OV6S1)	QFN88 (OV7S1)	QFN 76	Type	Description
TXN1_V TXP1_V	38 39	39 40	42 43	43 44	33 34	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_V (default upstream port)
TXN2_V TXP2_V	47 46	-	-	-	-	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_V for Type-C (default upstream port)
RXN1_V RXP1_V	41 42	42 43	45 46	46 47	36 37	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_V (default upstream port)
RXN2_V RXP2_V	43 44	-	-	-	-	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_V (default upstream port) for Type-C
TXN1_W TXP1_W	25 26	26 27	27 28	30 31	24 25	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_W
TXN2_W TXP2_W	34 33	35 34	36 35	39 38	-	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_W for Type-C
RXN1_W RXP1_W	28 29	29 30	30 31	33 34	27 28	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_W
RXN2_W RXP2_W	30 31	31 32	32 33	35 36	-	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_W for Type-C
TXN1_X TXP1_X	79 80	80 81	80 81	82 83	70 71	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_X
RXN1_X RXP1_X	82 83	83 84	83 84	85 86	73 74	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_X
TXN1_Y TXP1_Y	64 65	65 66	65 66	67 68	55 56	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_Y
RXN1_Y RXP1_Y	67 68	68 69	68 69	70 71	58 59	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_Y
TXN1_A TXP1_A	74 75	75 76	75 76	77 78	65 66	O	USB 3.1 Gen 2 Differential Data Transmitter TX-/TX+ of PORT_A
RXN1_A RXP1_A	77 78	78 79	78 79	80 81	68 69	I	USB 3.1 Gen 2 Differential Data Receiver RX-/RX+ of PORT_A
DM_V DP_V	37 36	38 37	41 40	42 41	32 31	B	USB 2.0 DM/DP for PORT_V
DM_W DP_W	24 23	25 24	26 25	29 28	23 22	B	USB 2.0 DM/DP for PORT_W
DM_X DP_X	85 84	86 85	86 85	88 87	76 75	B	USB 2.0 DM/DP for PORT_X
DM_Y DP_Y	70 69	71 70	71 70	73 72	61 60	B	USB 2.0 DM/DP for PORT_Y
DM_A DP_A	73 72	74 73	74 73	76 75	64 63	B	USB 2.0 DM/DP for PORT_A
DM_B DP_B	-	-	38 37	-	-	B	USB 2.0 DM/DP for PORT_B

DM_C DP_C	-	-	23 22	26 25	-	B	USB 2.0 DM/DP for PORT_C

USB-C Interface				
Name	**BGA289**	**BGA144**	**Type**	**Description**
VP5_CC_U VP5_CC_D	D1,E1 L1,M1	E1 J1	P	5V power input for Type-C function
CC1_V CC2_V	J1 J2	-	I/O	Configuration Channel for PORT_V
CC1_W CC2_W	K2 K1	J2 H2	I/O	Configuration Channel for PORT_W
CC1_X CC2_X	G2 G3	D2 E2	I/O	Configuration Channel for PORT_X
CC1_Y CC2_Y	H3 H2	F2 G2	I/O	Configuration Channel for PORT_Y

USB-C Interface						
Name	**QFN88 (OV3S1)**	**QFN88 (OV1S1)**	**QFN88 (OV6S1)**	**QFN88 (OV7S1)**	**Type**	**Description**
VP5_CC_U VP5_CC_D	- 8,11	- 11	10	13	P	5V power input for Type-C function
CC1_V CC2_V	10 9	-	-	-	I/O	Configuration Channel for PORT_V
CC1_W CC2_W	13 12	13 12	12 11	15 14	I/O	Configuration Channel for PORT_W

Hub Interface				
Name	**BGA289**	**BGA144**	**Type**	**Description**
PGREEN_W PGREEN_X PGREEN_Y PGREEN_A	R5 C1 B8 R17	J8 D5 D8 H10	B	Green LED indicator for PORT_W~A ▪ In reset state : PGREEN_Y will be SMC, PGREEN_A will be SMD ▪ SMBUS function is only available in BGA289
PGREEN_B PGREEN_Z PGREEN_C PGREEN_D	R3 D3 D13 R14	J4 - - -	B	Green LED indicator for PORT_B~D
PAMBER_W PAMBER_X PAMBER_Y PAMBER_A	R6 C2 A8 R16	- D4 D9 K10	B	Amber LED indicator for PORT_W~A
PAMBER_B PAMBER_Z PAMBER_C PAMBER_D	R4 C4 C13 R15	-	B	Amber LED indicator for PORT_B~D

PWRENJ_W PWRENJ_X PWRENJ_Y PWRENJ_A	P5 B1 C9 T17	K3 C3 D6 G9	B	Active low. Power enable output for PORTW~A PWRENJ_W is the only power-enable output for GANG mode.
PWRENJ_B PWRENJ_Z PWRENJ_C PWRENJ_D	P3 C3 C12 P14	J9 - - -	B	Active low. Power enable output for PORT_B~D
OVCURJ_W OVCURJ_X OVCURJ_Y OVCURJ_A	P4 A1 C8 U17	J7 C5 C6 E10	I (pd)	Active low. Over current indicator for PORT_W~A OVCURJ_W is the only over current flag for GANG mode.
OVCURJ_B OVCURJ_Z OVCURJ_C OVCURJ_D	R2 D2 C11 R13	H4 - - -	I (pd)	Active low. Over current indicator for PORT_B~D
PGANG	D4	G4	I	It's input mode by default after power-on reset. Individual/gang mode is strapped during this period.
PSELF	F2	-	I	0: GL3590 is bus-powered. 1: GL3590 is self-powered.

Hub Interface							
Name	**QFN88 (OV3S1)**	**QFN88 (OV1S1)**	**QFN88 (OV6S1)**	**QFN88 (OV7S1)**	**QFN76**	**Type**	**Description**
PGREEN_W PGREEN_X PGREEN_Y PGREEN_A	-	22 1 62 46	21 1 62 48	24 3 64 49	20 3 52 39	B	Green LED indicator for PORT_W~A ▪ In reset state : PGREEN_Y will be SMC, PGREEN_A will be SMD ▪ SMBUS function is only available in BGA289
PWRENJ_W PWRENJ_X PWRENJ_Y PWRENJ_A	20 88 63 48	20 2 64 45	19 2 64 47	22 4 66 50	18 4 53 38	B	Active low. Power enable output for PORTW~A PWRENJ_W is the only power-enable output for GANG mode.
OVCURJ_W OVCURJ_X OVCURJ_Y OVCURJ_A	21 87 62 49	21 88 63 47	20 88 63 49	23 2 65 51	19 2 54 40	I (pd)	Active low. Over current indicator for PORT_W~A OVCURJ_W is the only over current flag for GANG mode.
PGANG	2	4	-	6	5	I	It's input mode by default after power-on reset. Individual/gang mode is strapped during this period.
PSELF	-	-	-	-	6	I	0: GL3590 is bus-powered. 1: GL3590 is self-powered.

Clock and Reset Interface				
Name	**BGA289**	**BGA144**	**Type**	**Description**
X1	F1	F1	I	Crystal / OSC clock input
X2	G1	G1	O	Crystal clock output.
RESETJ	N14	K11	I	Active low. External reset input. When RESET# = low, whole chip is reset to the initial state.
CHIPEN	G15	G10	I (pu)	0: Chip disabled 1: Normal operating

Clock and Reset Interface							
Name	**QFN88 (OV3S1)**	**QFN88 (OV1S1)**	**QFN88 (OV6S1)**	**QFN88 (OV7S1)**	**QFN 76**	**Type**	**Description**
X1	5	8	7	10	9	I	Crystal / OSC clock input
X2	6	9	8	11	10	O	Crystal clock output.
RESETJ	50	48	50	52	41	I	Active low. External reset input. When RESET# = low, whole chip is reset to the initial state.
CHIPEN	59	57	59	62	50	I (pu)	0: Chip disabled 1: Normal operating

SPI Interface				
Name	**BGA289**	**BGA144**	**Type**	**Description**
P_SPI_CK	N3	J3	B	For SPI data clock
P_SPI_CZ	L4	J6	B	For SPI data chip enable
P_SPI_DO	N4	J5	B	For SPI data Input
P_SPI_DI	M4	H3	B	For SPI data Output

SPI Interface							
Name	**QFN88 (OV3S1)**	**QFN88 (OV1S1)**	**QFN88 (OV6S1)**	**QFN88 (OV7S1)**	**QFN76**	**Type**	**Description**
P_SPI_CK	16	16	15	18	14	B	For SPI data clock
P_SPI_CZ	17	17	16	19	16	B	For SPI data chip enable
P_SPI_DO	15	15	14	17	13	B	For SPI data Input
P_SPI_DI	18	18	17	20	15	B	For SPI data Output

Power/Ground Interface				
Name	**BGA289**	**BGA144**	**Type**	**Description**
VP12	N16, N17, P16, P17	J10~J12	P	1.2V power source for LDO 1.2V to 1.0V
VP10	E3, E4, D5~D12, P6~P13	A5, B5, K5, K6, K8, K9, C7~C9	P	1.0V power for analog circuits
AVDD10	H4	E3	P	1.0V power for analog PLL circuits
VP10_DIG	L2, M15, G4, G16	K1, D3, E12, K12	P	1.0V power pins for digital circuits
VP10_PHY	L16, L17, M16, M17	H11, H12	P	1.0V power pins for analog circuits
VP10_ MEM_A	L3, N15	L12	P	1.0V internal memory group 1 power pins
VP10_ MEM_B	F16, L15	G12	P	1.0V internal memory group 2 power pins
VP33_DIG	E2, M3, C15, P15	C2, K2, M12	P	3.3V power for digital circuits
AVDD33	H1	H1	P	3.3V power for analog PLL circuits
VP33_U2	C5~C7, C10, R7~R12	C4, K4, D7, K7	P	Analog 3.3V power pins
GND	E5~E13, F5~F13, G5~G13, H5~H13, J5~J13, K5~K17 L5~L14, M5~M13 N5~N13	E5~E8, F5~F8, G5~G8 H5~H8	P	Digital/Analog ground
VBUS	M14	H9	I	VBUS valid detection pin
VP33	F17,G17 H14~ H17	F12	P	3.3V power input

Power/Ground Interface							
Name	**QFN88 (OV3S1)**	**QFN88 (OV1S1)**	**QFN88 (OV6S1)**	**QFN88 (OV7S1)**	**QFN 76**	**Type**	**Description**
VP12	56	53	55	57	46	P	1.2V power source for LDO 1.2V to 1.0V
VP10	27, 32, 40, 45, 66, 76, 81	28, 33, 41, 67, 77, 82	29,34,44 67,77,82	32,37, 45.69, 79,84	26, 29, 35, 57, 67, 72	P	1.0V power for analog circuits

AVDD10	4	7	6	9	8	P	1.0V power for analog PLL circuits
VP10_DIG	14, 54	6, 14, 52	5,13,54	8,16, 56	12, 45	P	1.0V power pins for digital circuits
VP10_PHY	57	55	57	59	48	P	1.0V power pins for analog circuits
VP10_RX	55	54	56	58	47	P	1.0V power pins for digital circuits
VP10_ MEM_A	53	51	53	55	44	P	1.0V internal memory group 1 power pins
VP33_DIG	3,19, 52	5, 19, 49	4,18,52	7,21, 54	7, 17, 43	P	3.3V power pins for digital circuits
AVDD33	7	10	9	12	11	P	3.3V power for analog PLL circuits
VP33_U2	22, 35, 71, 86	23, 36, 72, 87	24,39,72, 87	1,27, 40,74	1, 21, 30, 62	P	Analog 3.3V power pins
VBUS	51	50	51	53	42	I	VBUS valid detection pin
VP33	58	56	58	60	49	P	3.3V power input

I2C Interface				
Name	**BGA289**	**BGA144**	**Type**	**Description**
I2C_CLK	R5	J8	B	I2C clock for Hub as master or slave
I2C_DAT	C1	D5	B	I2C data for Hub as master or slave
I2C_CLK_MST	D17	E11	B	I2C clock for Hub as master
I2C_DAT_MST	E17	F11	B	I2C data for Hub as master
SMC	B8	D8	B	SMBus clock
SMD	R17	H10	B	SMBus data

I2C Interface							
Name	**QFN88 (OV3S1)**	**QFN88 (OV1S1)**	**QFN88 (OV6S1)**	**QFN88 (OV7S1)**	**QFN 76**	**Type**	**Description**
I2C_CLK	-	22	21	24	20	B	I2C clock for Hub as master or slave
I2C_DAT	-	1	1	3	3	B	I2C data for Hub as master or slave
I2C_CLK _MST	-	-	-	-	-	B	I2C clock for Hub as master
I2C_DAT _MST	-	-	-	-	-	B	I2C data for Hub as master
SMC	-	62	62	64	52	B	SMBus clock
SMD	-	46	48	49	39	B	SMBus data

Charger and Power Related				
Name	**BGA289**	**BGA144**	**Type**	**Description**
A_FBD W_FBD	F14 F15	E9 F9	A	Feedback pin; it's connected to reference input of external power supply to set output voltage.
V_ISENSE W_ISENSE X_ISENSE Y_ISENSE Z_ISENSE A_ISENSE B_ISENSE C_ISENSE	E14 E15 J3 D14 J4 D15 K3 K4	- F10 F3 - E4 - G3 F4	A	Voltage detector input Note: Maximum input voltage = 3.3v

Miscellaneous				
Name	**BGA289**	**BGA144**	**Type**	**Description**
RTERM	G14	G11	A	A 20Kohm resister must be connected between RTERM and Ground
GPIO_01~08	N1, P1, R1, T1, U1, M2, N2, P2	-	B	General Purpose I/O
GPIO_09~16	C16, D16, E16, A17, B17, C17, D17, E17,	-,-, C11,C10,D11,D10,E11,F11	B	General Purpose I/O
TOD1 TOD2 X_VCDR	F3 C14 F4	-	B	Reserved. Please leave as not connected.
NC	J14~J17	-	-	Not Connected

Miscellaneous							
Name	**QFN88 (OV3S1)**	**QFN88 (OV1S1)**	**QFN88 (OV6S1)**	**QFN88 (OV7S1)**	**QFN 76**	**Type**	**Description**
RTERM	60	58	60	61	51	A	A 20Kohm resister must be connected between RTERM and Ground
GPIO_09~16	-	- - - 60, 59	-	-	-	B	General Purpose I/O
GPIO_X	1	3	3	5	-	B	General Purpose I/O
GPIO_Y	61	61	61	63	-	B	General Purpose I/O
GPIO_A	-	44		48	-	B	General Purpose I/O

Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must take care the power routing and the ground plane. For detailed information, please refer to **USB 3.1 Hub Design Guide**.

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	P	Power / Ground
	A	Analog
	pu	Internal pull up
	pd	Internal pull down

CHAPTER 4 FUNCTION DESCRIPTION

4.1 GL3590 Functional Block

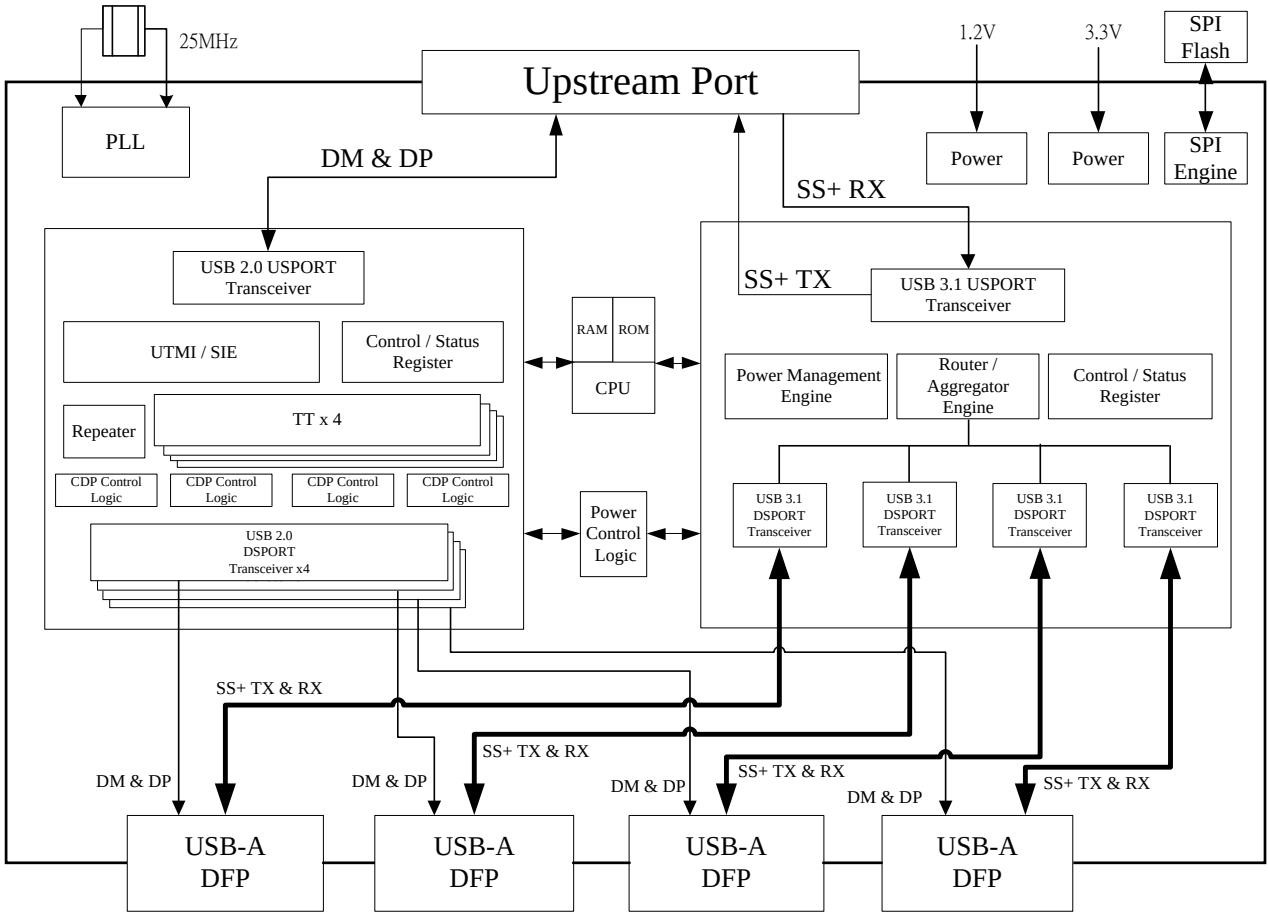


Figure 4.1 – GL3590 Architecture Diagram

4.2 GL3590-S Functional Block

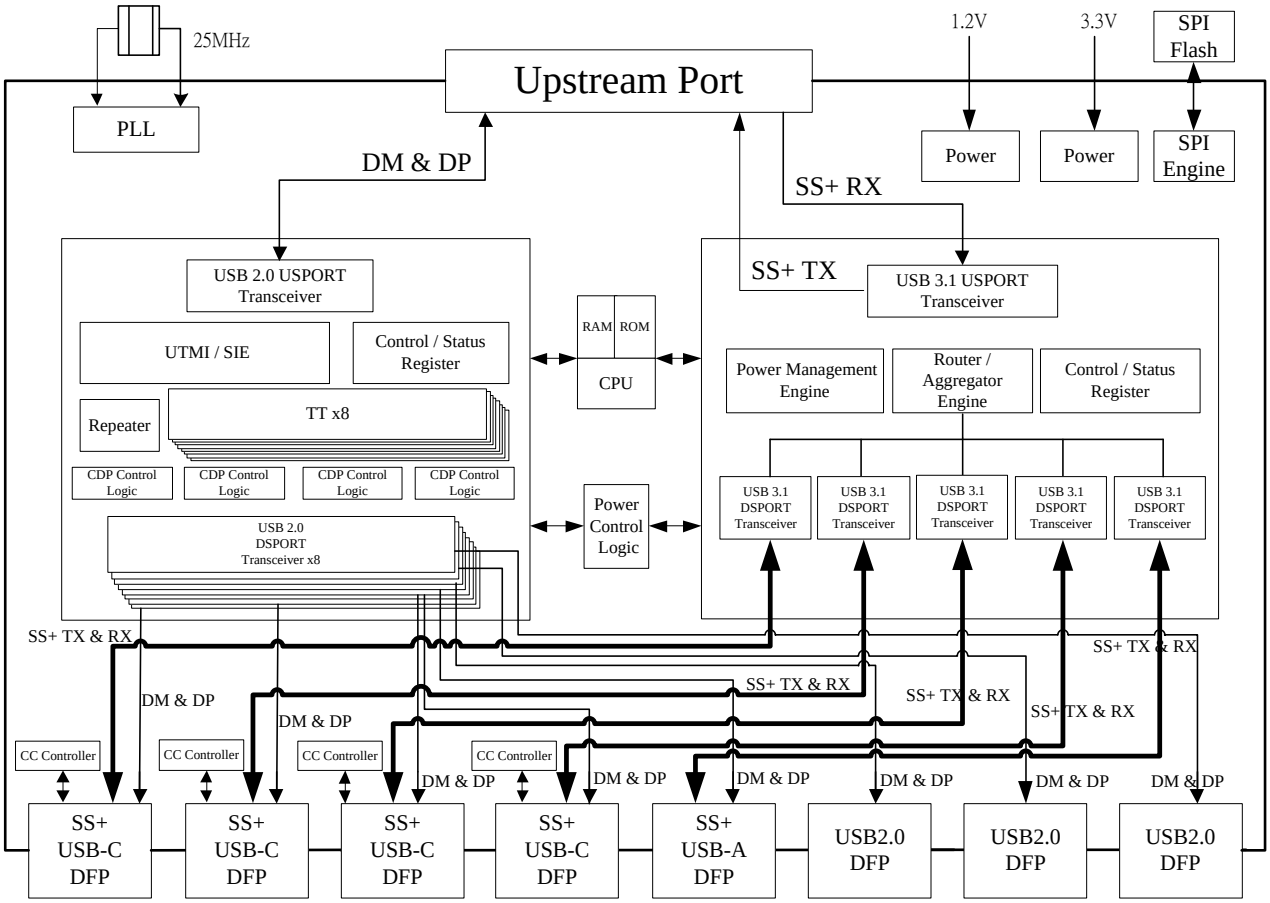


Figure 4.2 – GL3590-S Architecture Diagram

4.3 General Description

4.3.1 USB 2.0 USPORT Transceiver

USB 2.0 USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in Chapter 7 of USB specification revision 2.0. USPORT transceiver will operate in full-speed electrical signaling when GL3590 is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL3590 is plugged into a 2.0 host/hub.

4.3.2 USB 3.1 Gen 2 USPORT Transceiver

USB3.1 Gen 2 USPORT (upstream port) transceiver is the analog circuit that has elastic buffer and supports receiver detection, data serialization and de-serialization. Besides, it has PIPE interface with SuperSpeed Link Layer

4.3.3 PLL (Phase Lock Loop)

PLL generates the clock sources for the whole chip. The generated clocks are proven quite accurate that help in generating high speed signal without jitter.

4.3.4 SPI Engine

SPI engine is to move code from external flash to the internal RAM.

4.3.5 RAM/ROM/CPU

The micro-processor unit of GL3590 is an 8-bit RISC processor with 20K-byte ROM and 256-bytes RAM. It operates at 12MIPS of 12.5 MHz clock(maximum) to decode the USB command issued from host and then prepares the data to respond to the host.

4.3.6 UTMI (USB 2.0 Transceiver Microcell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

4.3.7 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in Chapter 8 of USB specification revision 2.0. It co-works with μC to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

4.3.8 Control/Status Register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipelines. Through the firmware based architecture, GL3590 possesses higher flexibility to control the USB protocol easily and correctly.

4.3.9 Power Management Engine

The power management of GL3590 is compliant with USB3.1 Gen 2 specification. When operating in SuperSpeed mode, GL3590 supports U0, U1, U2, and U3 power states. U0 is the functional state. U1 and U2 are lower power states compared to U0. U1 is a low power state with fast exit to U0; U2 is a low power state which saves more power than U1 with slower exit to U0. U3 is suspend state, which is the most power-saving state, with tens of milliseconds exit to U0. Unlike USB 2.0, SuperSpeed packet traffic is unicast rather than broadcast. Packet only travels the direct path in-between host and the target device. SuperSpeed traffic will not reach an unrelated device. When enabled for U1/U2 entry, and there is no pending traffic within comparable exit latency, GL3590 will initiate U1/U2 entry to save the power. On the

other hand, the link partner of GL3590 may also initiate U1/U2 entry. In this case, GL3590 will accept or reject low power state entry according to its internal condition.

4.3.10 Router/Aggregator Engine

Router/Aggregator Engine implements the control logic defined in Chapter10 of USB 3.1 specification. Router/Aggregator Engine uses smart method for route packet to device or aggregate packet to host.

4.3.11 REPEATER

Repeater logic implements the control logic defined in Section 11.4 and Section 11.7 of USB specification revision 2.0. REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

4.3.12 TT

TT (Transaction Translator) implements the control logic defined in Section 11.14 ~ 11.22 of USB specification revision 2.0. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL3590 adopts multiple TT architecture to provide the most performance effective solution. Multiple TT provides control logics for each downstream port respectively.

4.3.12.1 Connected to 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

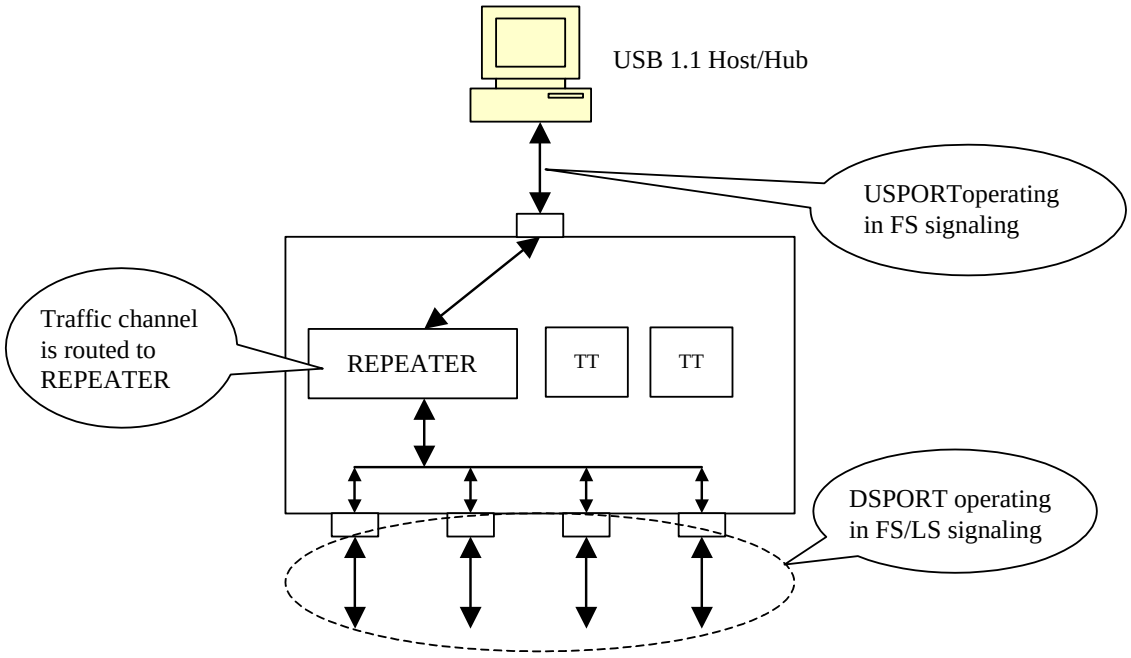


Figure 4.3 - Operating in USB 1.1 Schemes

4.3.12.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

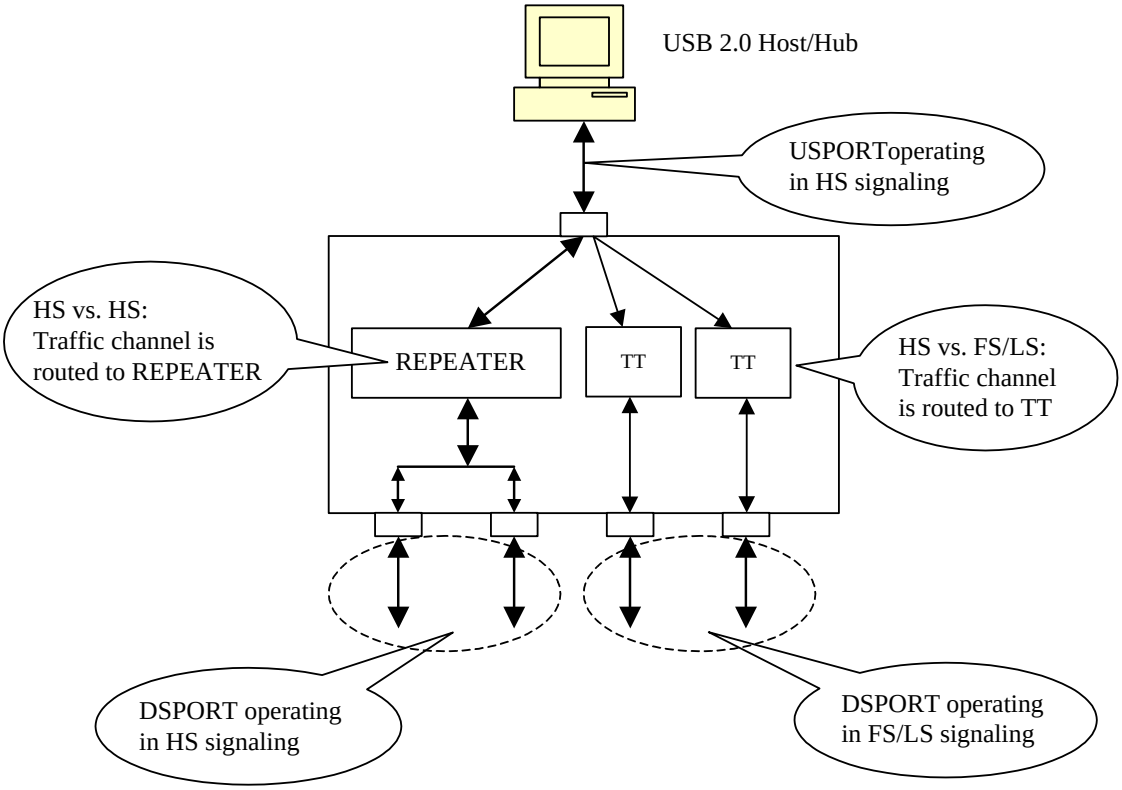


Figure 4.4 - Operating in USB 2.0 Schemes

4.3.13 USB 3.1 Gen 2/USB 2.0 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics. In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

4.3.14 CDP Control Logic

CDP (charging downstream port) control logic implements the logic defined in USB Battery charging specification revision 1.2. The major function of it is to control DSPORT Transceiver to make handshake with a portable device which is compliant with USB Battery charging spec rev1.2 as well. After recognizing charging detection each other, portable device will draw up to 1.5A from VBUS to fast charge its battery.

4.3.15 Analog Digital Converter (ADC)

GL3590 integrates eight 8-bit general purpose ADC used to detect voltage, current, and temperature, etc. physical value. V/W/X/Y/Z/A/B/C_ISENSE are input pins of ADC. Maximum input voltage is 3.3v.

4.3.16 Configuration Channel (CC) Characteristics

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
VP5_CC_D/U	CC 5V input range (VP5_CC_D/U has to be supplied with 5V power to use CC function)	-	4.5	5	5.5	V
CC_{load}	CC pin output loading	-	-	-	10	uF
I_{P-80u}	CC Termination (Current Source) for Default USB Power	Rd=5.1k	-8%	80	+8%	uA
I_{P-180u}	CC Termination (Current Source) for 1.5A @ 5V	Rd=5.1k	-8%	180	+8%	uA
I_{P-330u}	CC Termination (Current Source) for 3.0A @ 5V	Rd=5.1k	-8%	330	+8%	uA
Rd	Device resistance to GND	-	-10%	5.1k	+10%	ohm
Ron-vconn	Ron of Vconn Source	-	-	1	1.25	ohm
OCP level	OCP level	-	-	400	-	mA

4.3.17 Power Delivery and TCPM

GL3590-S series of Hubs have dedicated MCU responsible for Power Delivery protocol. With integrating Type-C Port Manager (TCPM), GL3590-S is able to communicate and mange external Power Delivery PHY.

The following figure shows the interconnection between the TCPM and two USB Type-C Port Controllers (TCPCs). One TCPM may be used to drive multiple TCPCs subject to the timing constraints defined in the USB PD Specification.
The connection between the TCPM and the TCPC is defined as the USB Type-C Port Controller Interface, TCPCI.

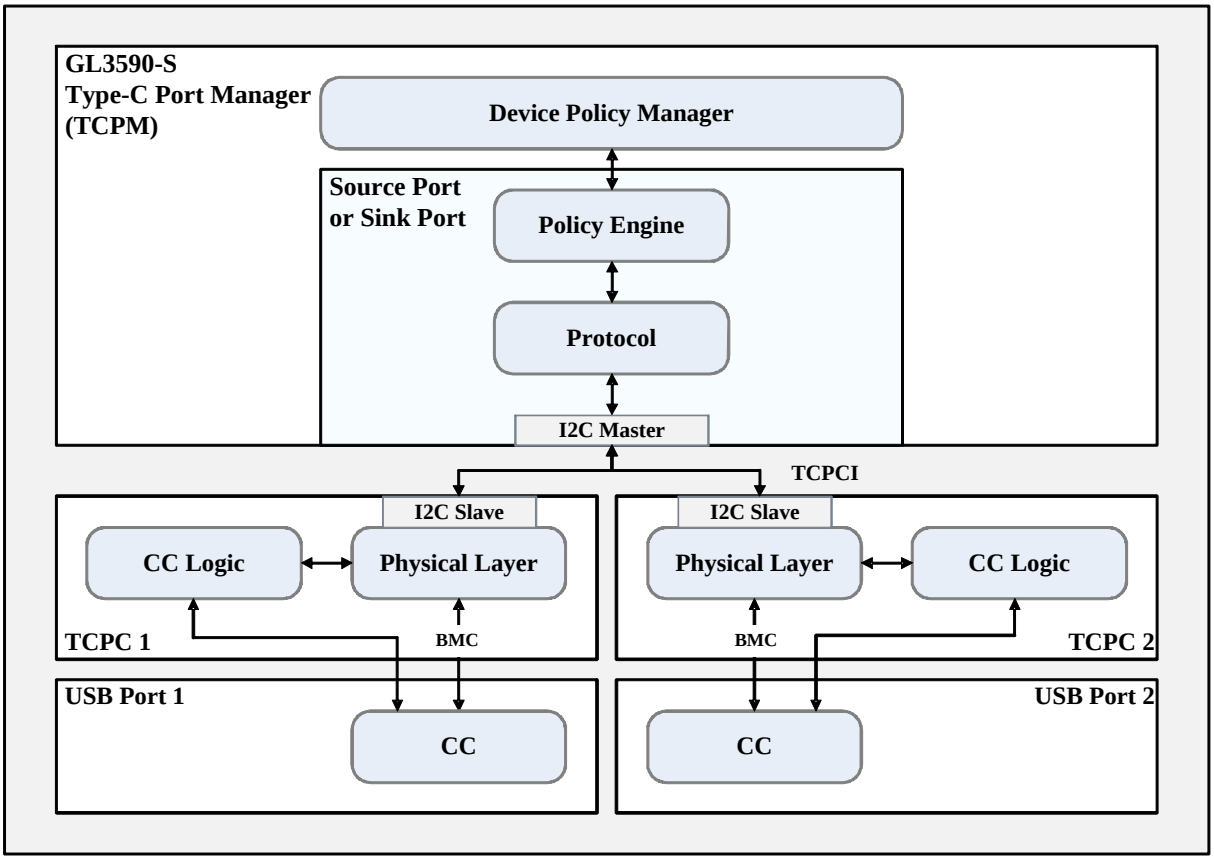


Figure 4.5 – Type-C Port Manager (TCPM) Diagram

4.4 Configuration and I/O Settings

4.4.1 RESET Setting

GL3590's power on reset can be triggered by external reset circuit. The reset trigger voltage can be set by adjusting the value of resistor R1 and R2 (Please refer to schematics for suggested value). GL3590's internal reset is designed to monitor silicon's internal core power (1.2V) and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 500μS after power good.

To fully control the reset process of GL3590, we suggest the reset time applied in the external reset circuit should be longer than that of the internal reset circuit. Timing of Power-on-Reset is illustrated as below figure.

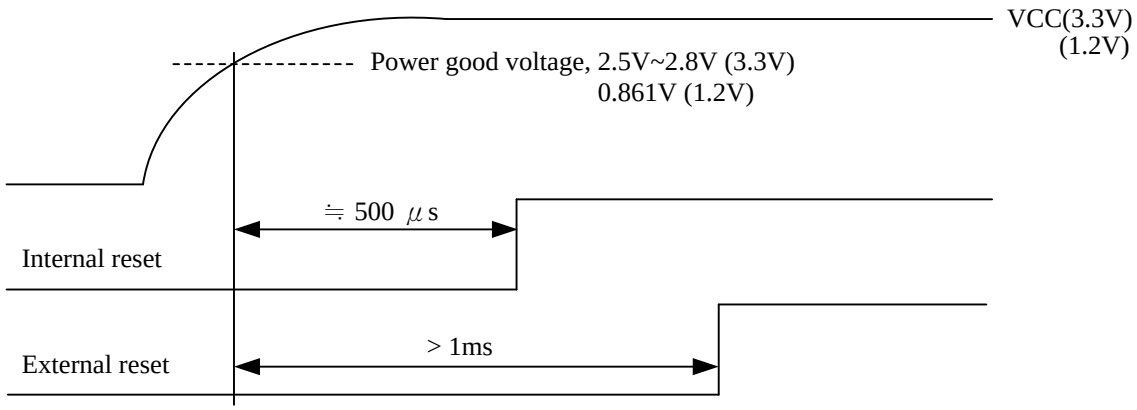


Figure 4.6 - Power on Sequence of GL3590

4.4.2 PGANG Setting

To save pin count, GL3590 uses the same pin to decide individual/gang mode as well as to output the suspend flag. The individual/gang mode is decided within 21us after power on reset. Then, about 50ms later, this pin is changed to output mode. GL3590 outputs the suspend flag once it is globally suspended. For individual mode, a pull low resister greater than 100KΩ should be placed. For gang mode, a greater than 100KΩ pull high resister should be placed. In figure 4.7, we also depict the suspend LED indicator schematics. It should be noticed that the polarity of LED must be followed, otherwise the suspend current will be over spec limitation (2.5mA).

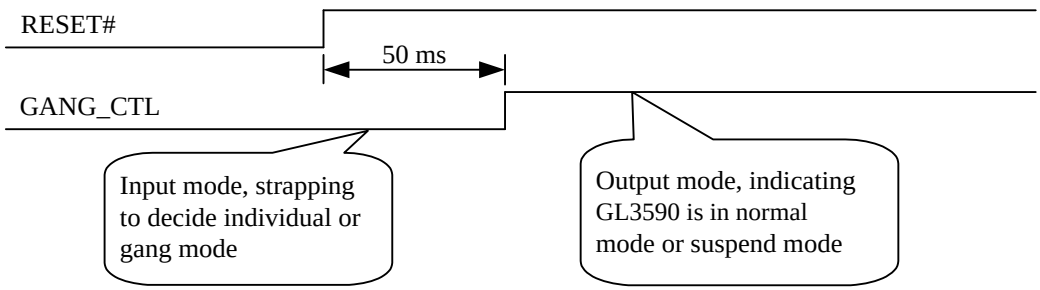


Figure 4.7 - Timing of PGANG Strapping

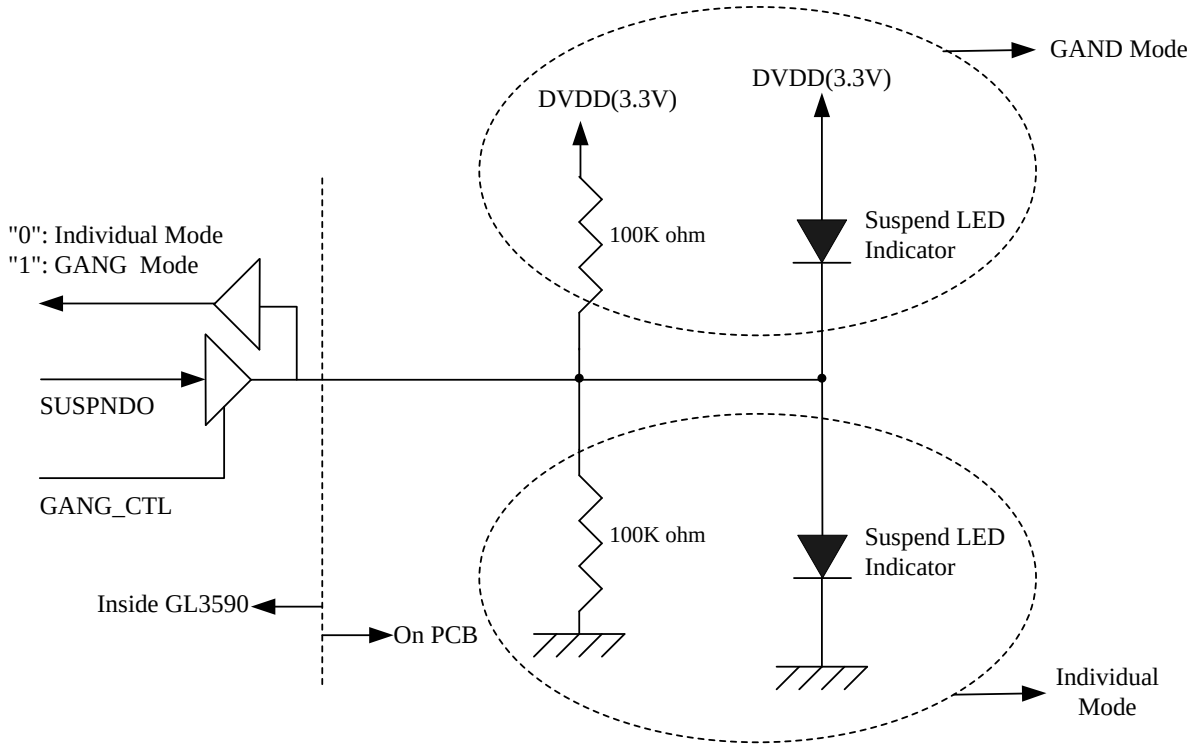


Figure 4.8 - GANG Mode Setting

4.4.3 SELF/BUS Power Setting

By setting PSELF, GL3590 can be configured as a bus-powered or a self-powered hub.

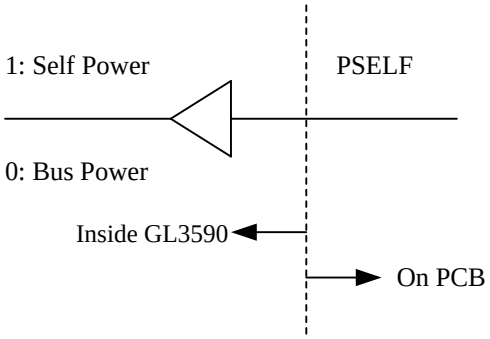


Figure 4.9 - SELF/BUS Power Setting

4.4.4 LED Connections

GL3590 controls the LED lighting according to the flow defined in Section 11.5.3 of Universal Serial Bus Specification Revision2.0. Both manual mode and Automatic mode are supported in GL3590. When GL3590 is globally suspended, GL3590 will turn off the LED to save power.

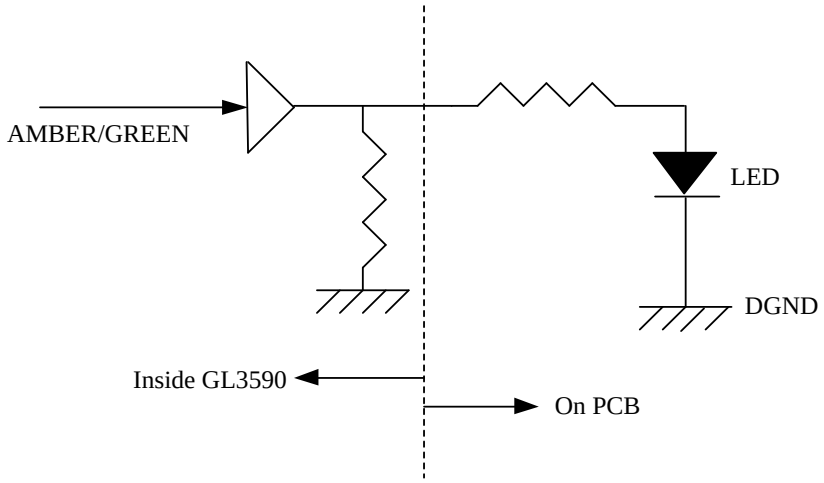


Figure 4.10 - LED Connection

4.4.5 Power Switch Enable Polarity

Both low/high-active power switches are supported by firmware configuration.

4.4.6 Port Configuration

Each specific downstream port can be disabled individually by firmware, SMBus or vendor command, which extends the flexibility for PCB design and fits more applications.
In GL3590-S series of Hub, multiple upstream ports are also allowed for special applications. For further usage information, please contact Genesys FAE or sales team.

4.4.7 Non-removable Port Setting

For compound applications or embedded systems, downstream ports that always connect inside the system can be set as non-removable by firmware configuration, EEPROM, and pin strapping. Please refer to **Genesys USB3.1 Hub FW ISP Tool User Guide** for the detailed setting information.

4.4.8 SMBUS Mode (SMBUS Slave Address=0x25)

GL3590 enters SMBUS mode since Power-On occurs, and RESET# pin is asserted as well. After that, GL3590 will define OVCUR3J as SMC and OVCUR4J as SMD. GL3590 will exit the SMBUS mode since the RESET# pin is de-asserted. The more complicated settings such as PID, VID, power saving, port number, port non/removable, and downstream port electrical tuning can be configured by SMBUS.

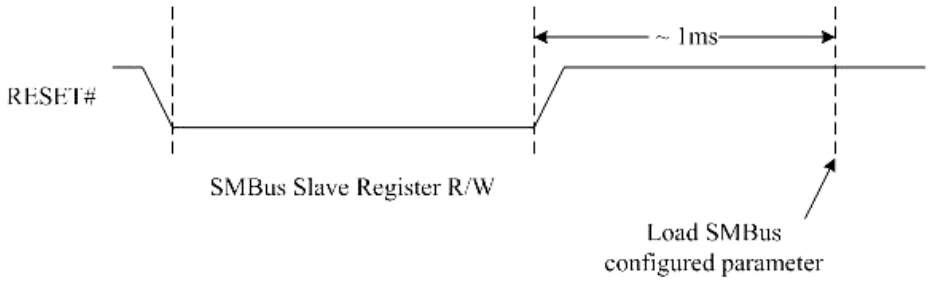


Figure 4.11 - SMBus Timing Diagram

CHAPTER 5 FAST CHARGING SUPPORT

5.1 Charging Mode

GL3590 supports different kinds of charging mechanisms which will be introduced in this section.

5.1.1 Battery Charging Specification Rev.1.2

The USB ports on personal computers are convenient places for portable devices to draw current for charging their batteries. This convenience has led to the creation of dedicated chargers that simply expose a USB standard-A receptacle. This allows portable devices to use the same USB cable to charge from either a PC or from a dedicated charger.

If a portable device is attached to a USB host or hub, then the USB 2.0 specification requires that after connecting, a portable device must draw less than:

- 2.5 mA average if the bus is suspended
- 100 mA maximum if bus is not suspended and not configured
- 500 mA maximum if bus is not suspended and configured for 500 mA

If a portable device is attached to a charging host or hub, it is allowed to draw a current up to 1.5A, regardless of suspend. In order for a portable device to determine how much current it is allowed to draw from an upstream USB port, the USB-IF Battery Charging specification defines the mechanisms that allow the portable device to distinguish between a USB standard host, hub or a USB charging host. Since portable devices can be attached to USB charging ports from various manufactures, it is important that all USB charging ports behave the same way. This specification also defines the requirements for a USB chargers and charging downstream ports.

5.1.1.1 Standard Downstream Port (SDP)

GL3590 complies with Battery Charging Specification rev1.2, which defines three charging ports: SDP, CDP and DCP. The SDP is a standard USB port which can transfer data and provide maximum 500mA current.

5.1.1.2 Charging Downstream Port (CDP)

GL3590 supports battery charging detection, turning its downstream port from a standard downstream port (SDP) into charging downstream port (CDP). GL3590 will make physical layer handshaking when a portable device that complies with BC rev1.2 attaches to its downstream port. After physical layer handshaking, a portable device is allowed to draw more current up to 1.5A.

Once the charging downstream port of GL3590 is enabled, it will monitor the VDP_SRC on D+ line anytime. When a portable device, which is compliant with BC rev1.2, is attached to the downstream port, it will drive VDP_SRC on D+ line to initiate the handshake with charging downstream port. GL3590 will response on its D- line by VDM_SRC and keep in a certain period of time and voltage level. The portable device will accept this handshaking on its D- line in correct timing period and voltage level, and then turns off its VDP_SRC on D+ line. GL3590 will recognize that charging negotiation is finished by counting time between the portable device turning on and off its VDP_SRC. After that, the portable device can start to draw more current from VBUS to charge its battery more rapidly. It can draw current up to 1.5A.

If there is no response from D- line, the portable device will recognize that it is attached to a standard downstream port, not a charging port.

5.1.1.3 Dedicated Charging Port (DCP)

GL3590 also supports dedicated charging port, which is a downstream port on a device that outputs power through a USB connector, but it is not capable of enumerating a downstream device. With the adequate system circuit design, GL3590 will turn its downstream port from a standard downstream port (SDP) into dedicated charging port (DCP), i.e short the D+ line to the D- line, to let the portable device draws current up to 1.5A. Please refer to the **USB3.1 Hub Design Guide** document for the detailed information.

5.1.2 ACA-Dock (Upstream port only)

An ACA-Dock is a docking station that has one upstream port, and zero or more downstream ports. The upstream port can be attached to a portable device (PD), and is capable of sourcing ICDP to the PD, which means that the upstream port can charge and have data communication with the PD at the same time. Please refer to Battery Charging Spec v1.2 for more details.

5.1.3 Apple and Samsung Devices

GL3590 Hub not only supports BC1.2, but also supports fast-charging for Apple 1A/2.1A/2.4A and Samsung Galaxy devices.

5.1.4 Auto mode

In Auto mode, GL3590 will automatically detect the connected device and switch to appropriate configuration.

5.2 Charging Port Configuration

Fast-charging capability can be disabled/enabled by each specific downstream port. Please refer to the **Genesys USB3.1 Hub FW ISP Tool User Guide** document for the detailed setting information.

5.3 Functional Description

5.3.1 Feedback control

GL3590 changes output voltage by adjusting the current of feedback loop through internal current source (IFBD(SRC)) and current sink (IFBD(SNK)). With default output voltage 5V, both internal current source and sink are off. To meet the output voltage requirement, the mandatory value for the upper resistor (R1) in the feedback loop divider is 102KΩ(±1%). Please refer to Figure 5.1 for details.

For a regulator using 1.27V as reference voltage for instance, the lower resistor (R2) in the feedback loop is set to 34KΩ (±1%) to set the default output voltage to USB default 5V.

GL3590 can also support power supply which reference voltage of feedback is lower than 1.27v by adding additional resistor R3 as shown in Figure 5.2.

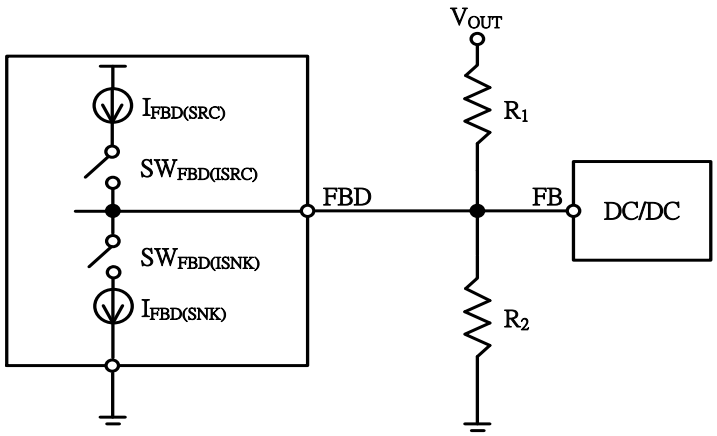


Figure 5.1 - Feedback loop design when reference voltage of FB is 1.27V

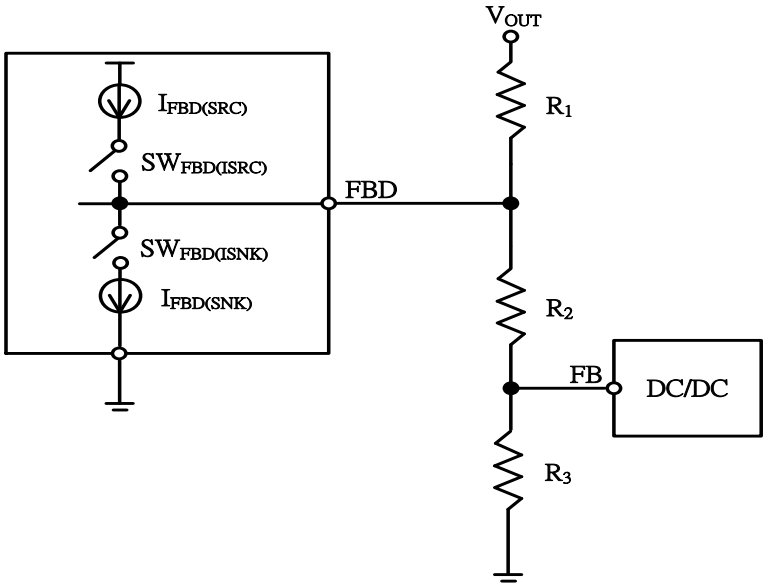


Figure 5.2 - Feedback loop design when reference voltage of FB < 1.27V

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1- Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_5	5V Power Supply	-0.5	+6.0	V
V_{DD}	3.3V Power Supply	-0.3	+3.6	V
V_{12}	1.2V Power Supply	-0.2	+1.32	V
VDDcore	1.0VPower Supply	-0.2	+1.1	V
V_{IN}	3.3V Input Voltage for digital I/O(EE_DO) pins*	-0.3	+5	V
T_S	Storage Temperature under bias	-20	+80	^oC
F_{OSC}	Frequency	25 MHz ± 0.03%		

*Please refer to the reference design schematic.

6.2 Operating Ranges

Table 6.2- Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_5	5V Power Supply	4.75	5.0	5.25	V
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V
V_{12}	1.2V Power Supply	1.15	1.2	1.32	V
VDDcore	1.0V Power Supply	0.95	1.0	1.05	V
V_{IND}	Input Voltage for digital I/O pins	-0.3	3.3	4.0	V
T_A	Ambient Temperature	0	-	70	^oC
T_J	Absolute maximum junction temperature	0	-	125	^oC

6.3 DC Characteristics

6.3.1 DC Characteristics except USB Signals

Table 6.3- DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	3	3.3	3.6	V
V_{IL}	LOW level input voltage	-0.3	-	0.8	V
V_{IH}	HIGH level input voltage	2	-	5.5	V
V_{TLH}	Schmitt trigger PAD*-LOW to HIGH threshold voltage	1.61	1.69	1.77	V
V_{THL}	Schmitt trigger PAD*- HIGH to LOW threshold voltage	1.18	1.27	1.35	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-	-	30	μA
R_{DN}	Pad internal pull down resister	232	378	647	KΩ
R_{UP}	Pad internal pull up resister	276	435	718	KΩ

* Schmitt trigger pads are VBUS, RESET

6.3.2 USB 2.0 Interface DC Characteristics

GL3590 conforms to DC characteristics for Universal Serial Bus specification rev. 2.0. Please refer to the specification for more information.

6.3.3 USB 3.1 Interface DC Characteristics

GL3590 conforms to DC characteristics for Universal Serial Bus 3.1 specification. Please refer to the specification for more information.

6.4 Power Consumption

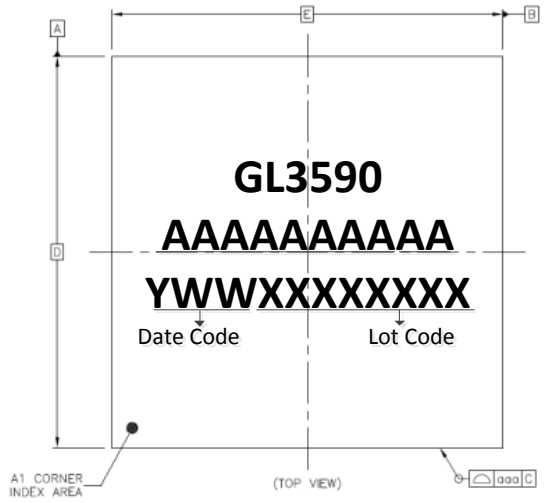
Number of Active USB 3.1 Gen 2 DFPs	1.2V		3.3V		Unit
	Config.	Read/ Write	Config.	Read/ Write	
Chip Disabled	7		0		uA
Reset	18		1.2		mA
Suspend	18		1.2		mA
Upstream	70	-	33	33	mA
1	321	325	33	33	mA
2	422	422	33	33	mA
3	511	523	33	33	mA
4	605	613	33	33	mA
5	698	709	33	33	mA

Number of Active USB 2.0 DFPs	1.2V		3.3V		Unit
	Config.	Read/ Write	Config.	Read/ Write	
Chip Disabled	7		0		uA
Reset	18		1.2		mA
Suspend	18		1.2		mA
Upstream	70	-	32	-	mA
1	71	75	36	37	mA
2	71	85	40	42	mA
3	72	87	44	47	mA
4	73	90	49	51	mA
5	74	119	53	57	mA
6	75	131	57	64	mA
7	76	152	61	68	mA
8	77	175	65	76	mA

6.5 External Clock

XOUT: 25MHz crystal oscillator output. It should be left open if an external clock source is used.
XIN: 25MHz crystal oscillator input. If an external 3.3V clock source is used, its frequency has to be 25MHz +/-300ppm with a peak-to-peak jitter less than 50ps.

CHAPTER 7 PACKAGEDIMENSION



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.3
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		12	BSC
	E		12	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.65	BSC
BALL COUNT	n		289	
EDGE BALL CENTER TO CENTER	D1		10.4	BSC
	E1		10.4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

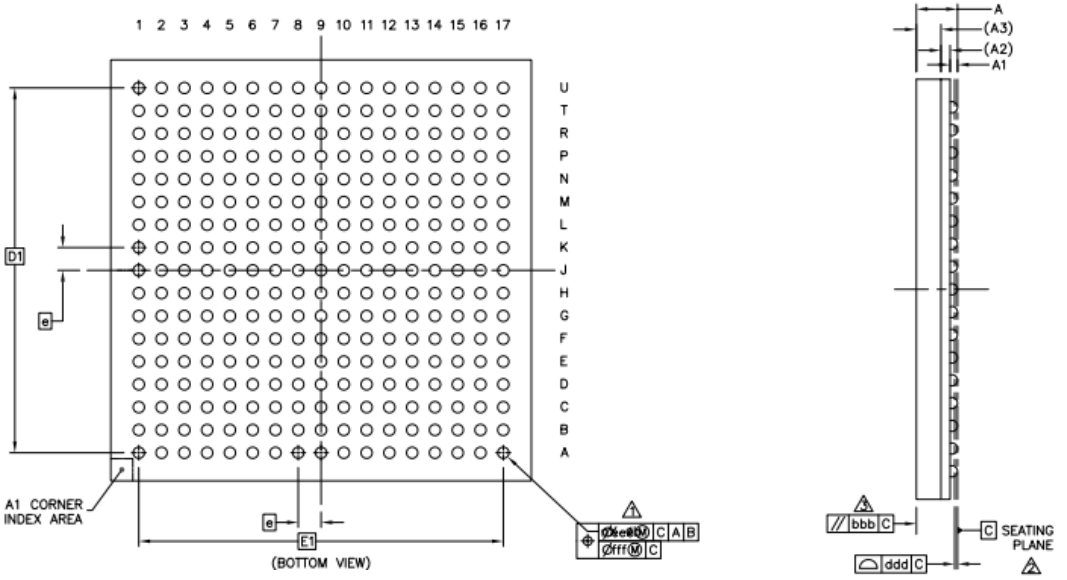
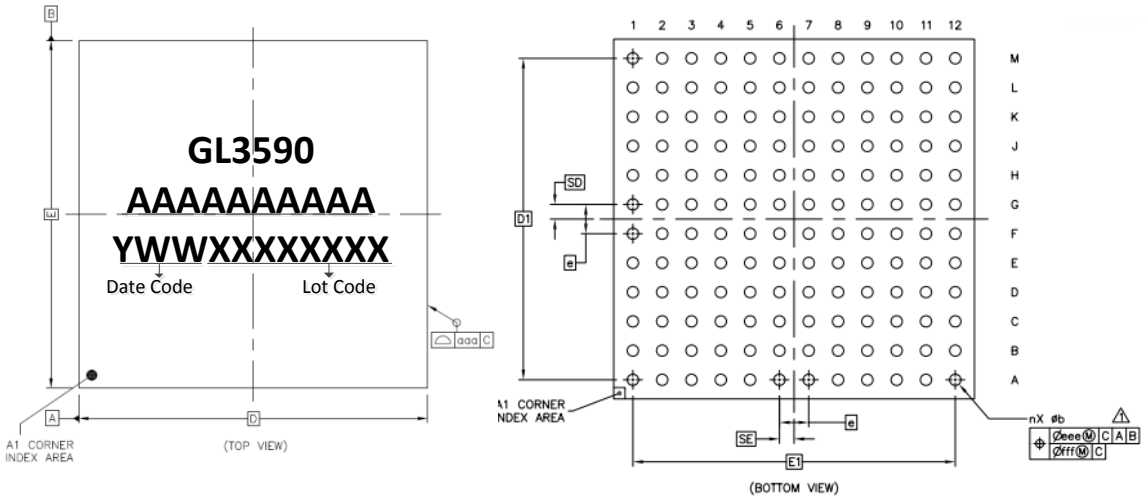
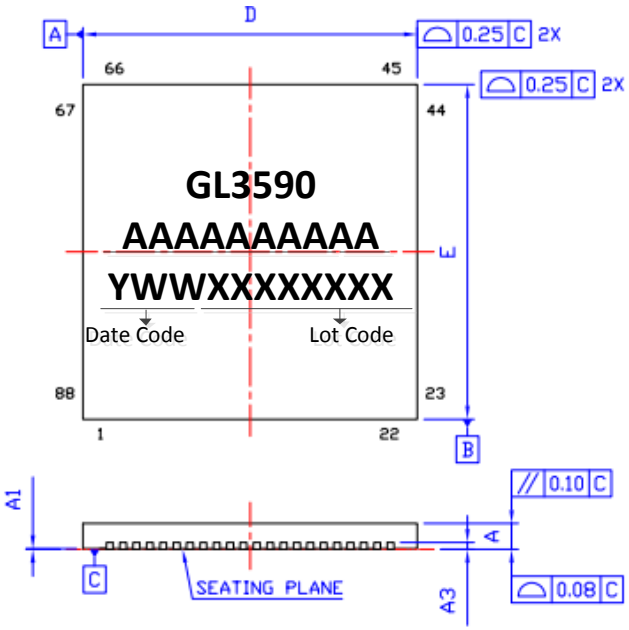


Figure 7.1- GL3590 BGA289 Package



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.3
STAND OFF	A1	0.11	---	0.21
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		8	BSC
	E		8	BSC
BALL DIAMETER			0.25	
BALL OPENING			0.25	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.65	BSC
BALL COUNT	n		144	
EDGE BALL CENTER TO CENTER	D1		7.15	BSC
	E1		7.15	BSC
BODY CENTER TO CONTACT BALL	SD		0.325	BSC
	SE		0.325	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

Figure 7.2- GL3590 BGA144 Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
D	10.00 (393.7) BSC		
D2	5.45 (214.5)	5.60 (220.5)	5.75 (226.4)
E	10.00 (393.7) BSC		
E2	5.45 (214.5)	5.60 (220.5)	5.75 (226.4)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

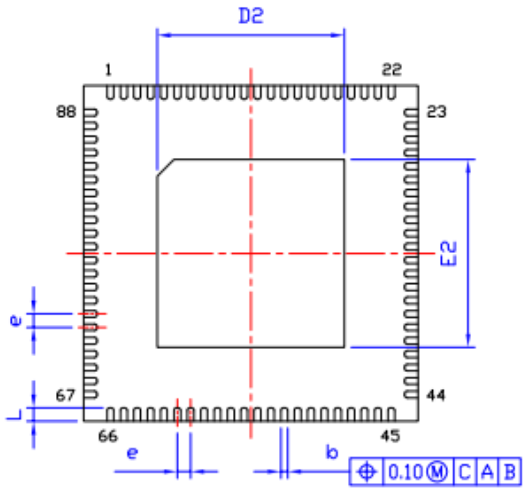
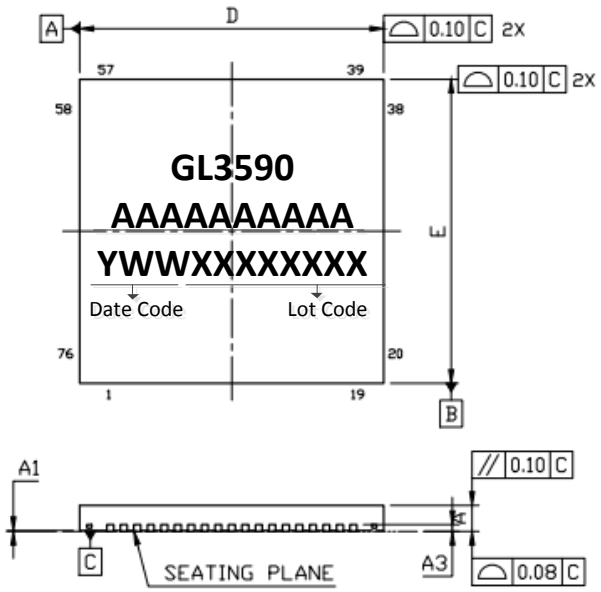


Figure 7.3- GL3590 QFN88 Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.80 (31.5)	0.90 (35.4)
A1	0.00 (0.00)	0.035 (1.4)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.15 (5.9)	0.2 (7.9)	0.25 (9.8)
D	9.00 (354.3) BSC		
D2	5.10 (200.8)	5.75 (226.4)	6.40 (252)
E	9.00 (354.3) BSC		
E2	5.10 (200.8)	5.75 (226.4)	6.40 (252)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)
R	0.075 (3.0)	-	-

Note: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

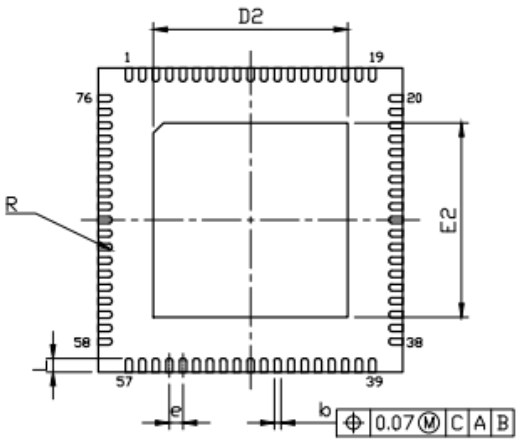


Figure 7.4- GL3590 QFN76 Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Material	Version	Status
GL3590-OTY10	QFN76	Green Package	10	Available
GL3590-TZYS1	LFBGA289	Green Package	S1	Available
GL3590-TBYS1	LFBGA144	Green Package	S1	Available
GL3590-OV3S1	QFN88 (2C3A)	Green Package	S1	Available
GL3590-OV1S1	QFN88 (1C4A)	Green Package	S1	Available
GL3590-OV6S1	QFN88 (1C4A2HS)	Green Package	S1	Available
GL3590-OV7S1	QFN88 (1C4A1HS)	Green Package	S1	Available