Genesys Logic, Inc.

GL3520-22

USB 3.0 Hub Controller

Datasheet

Revision 1.07
Apr. 21, 2016

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Revision History

Revision	Date	Description
1.00	01/07/2014	Formal release
1.01	01/15/2014	Updated CH2 Features, p. 8
1.02	02/18/2014	Updated CH7 Package Dimension, p. 31
1.03	04/23/2014	Updated CH8 Ordering Information, p. 32
1.04	06/04/2014	Updated CH2 Features, p.8, 9 Added CH5.8 ACA-Dock, p.25
1.05	08/07/2014	Updated QFN64 Package Information.
1.06	09/24/2014	Updated CH3.2 Pin Descriptions, p.14
1.07	04/21/2016	Updated Power Switch Information, Section 4.3.5

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CHAPTER 1 GENERAL DESCRIPTION

Genesys GL3520-22 is a 4-port, low-power, and configurable hub controller. It is compliant with the USB3.0 specification. GL3520-22 integrates Genesys Logic self-developed USB 3.0 Super Speed transmitter/receiver physical layer (PHY) and USB 2.0 High-Speed PHY. It supports Super Speed, Hi-Speed, and Full-Speed USB connections and is fully backward compatible to all USB 2.0 and USB 1.1 hosts. GL3520-22 also implements multiple TT* (Note1) architecture providing dedicated TT* to each downstream (DS) port, which guarantees Full-Speed(FS) data passing bandwidth when multiple FS devices perform heavy loading operations. Furthermore, GL3520-22 has built-in 5V to 3.3V regulator, which saves customers' BOM cost, and eases for PCB design.

GL3520-22 features the native fast-charging and complies with USB-IF battery charging specification rev1.2, it could fast-charge Apple, Samsung Galaxy devices, and any device complaint with BC1.2/1.1. It also allows portable devices to draw up to 1.5A from GL3520-22 charging downstream ports (CDP[1]) or dedicated charging port (DCP[2]). It can enable systems to fast charge handheld devices even during "Sleep" and "Power-off" modes.

Available package: QFN88 (10x10 mm), QFN64 (8x8 mm). Summarize as below table

Package Type	# of DS Ports	Power Mgmt.	LED Support	Firmware Upgrade
QFN 88	4	Individual/Gang	Green/Amber	SPI Flash
QFN 64 (OS8)	4	Individual/Gang	N/A	SPI Flash
QFN 64 (OS3)	4	Gang	N/A	SPI Flash

GL3520-22 Package – Feature Summary

*Note: TT (transaction translator) implements the control logic defined in section 11.14 ~ 11.22 of USB specification revision 2.0. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub.

[1] CDP, charging downstream port, the Battery Charging Rev.1.2-compliant USB port that does data communication and charges device up to 1.5A.

[2] DCP, dedicated charging port, the Battery Charging Rev.1.2-compliant USB port that only charges devices up to 1.5A, similar to wall chargers.

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CHAPTER 2 FEATURES

- Compliant with USB Specification Revision 3.0
  - Upstream port supports super speed(SS) high speed(HS) and full speed(FS) traffic
  - Downstream ports support SS, HS, FS, and low speed(LS) traffic
  - 1 control pipe and 1 interrupt pipe
  - Backward compatible to USB specification Revision 2.0/1.1
- Featuring fast-charging on all downstream ports and upstream port
  - Compliant with USB Battery Charging Revision v1.2, supporting CDP, DCP, and ACA-Dock
  - Downstream ports can be turned from a Standard Downstream Port (SDP) into Charging Downstream Port (CDP) or Dedicated Charging Port (DCP)
  - Downstream devices can be charged while upstream VBUS is not present, which can be applied on wall charger applications
  - Upstream port is capable of charging and data communicating simultaneously for portable devices supporting ACA-Dock or proprietary charging protocols, such as Sony Z1 and ZL
  - Supporting Apple 2.4A and Samsung Galaxy devices fast-charging
- On-chip 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - 1 cycle instruction execution (maximum)
  - Performance: 12 MIPS @ 12MHz (maximum)
  - With 256-byte RAM, 20K-byte internal ROM, and 20K-byte SRAM
- Multiple Transaction Translator(TT) architecture
  - Providing dedicated TT control logics for each downstream port
  - Superior performance when multiple FS devices operate concurrently
- Integrated USB transceiver
  - Improving output drivers with slew-rate control for EMI reduction
  - Internal power-fail detection for ESD recovery
- Advanced power management and low power consumption
  - Supporting USB3.0 U0/U1/U2/U3 power management states
  - Supporting USB Link Power Management (LPM) L0/L1/L2
  - Supporting individual/gang mode over-current detection for all downstream ports
  - Supporting low active power switch
  - Patented Smart Power Management
- Configurable settings by SPI-flash/EEPROM/pin strapping
  - Configurable charging port
  - Configurable 4/3/2 downstream ports
  - Configurable Poly-fuse/Power-switch
  - Supporting full in-system programming firmware upgrade by SPI-flash and EEPROM
  - Supporting compound-device (non-removable setting on downstream ports)
  - Supporting customization VID/PID
- Flexible design
  - Automatic switching between self-powered and bus-powered modes
  - Supporting PHY tuning
  - Supporting register setting by firmware
  - Supporting vendor command and SMBUS
  - Allow downstream ports to connect up to 8 devices, 4 x USB3.0 non-removable devices with 4 x USB2.0 non-removable devices or exposed ports
- Low BOM cost
  - Single external 25 MHz crystal / Oscillator clock input
  - Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
  - Built-in 5 to 3.3V regulator

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- Available package type
  - QFN 88 (10x10mm)
  - QFN 64 (8x 8 mm)
- Applications
  - Standalone USB hub/Docking station
  - Tablet/Ultrabook/NB
  - Motherboard
  - Monitor built-in hub, GL3520-22 GPIOs can be programmed as I2C interface to easily update scalar firmware through USB interface
  - TV built-in hub
  - Compound device, such as hub-reader application
  - USB wall charger
  - Other consumer electronics
  - Customized applications
    - Dynamically disable/enable ports
    - GPIO signaling of ambient light sensor or rotation/position sensor

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CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

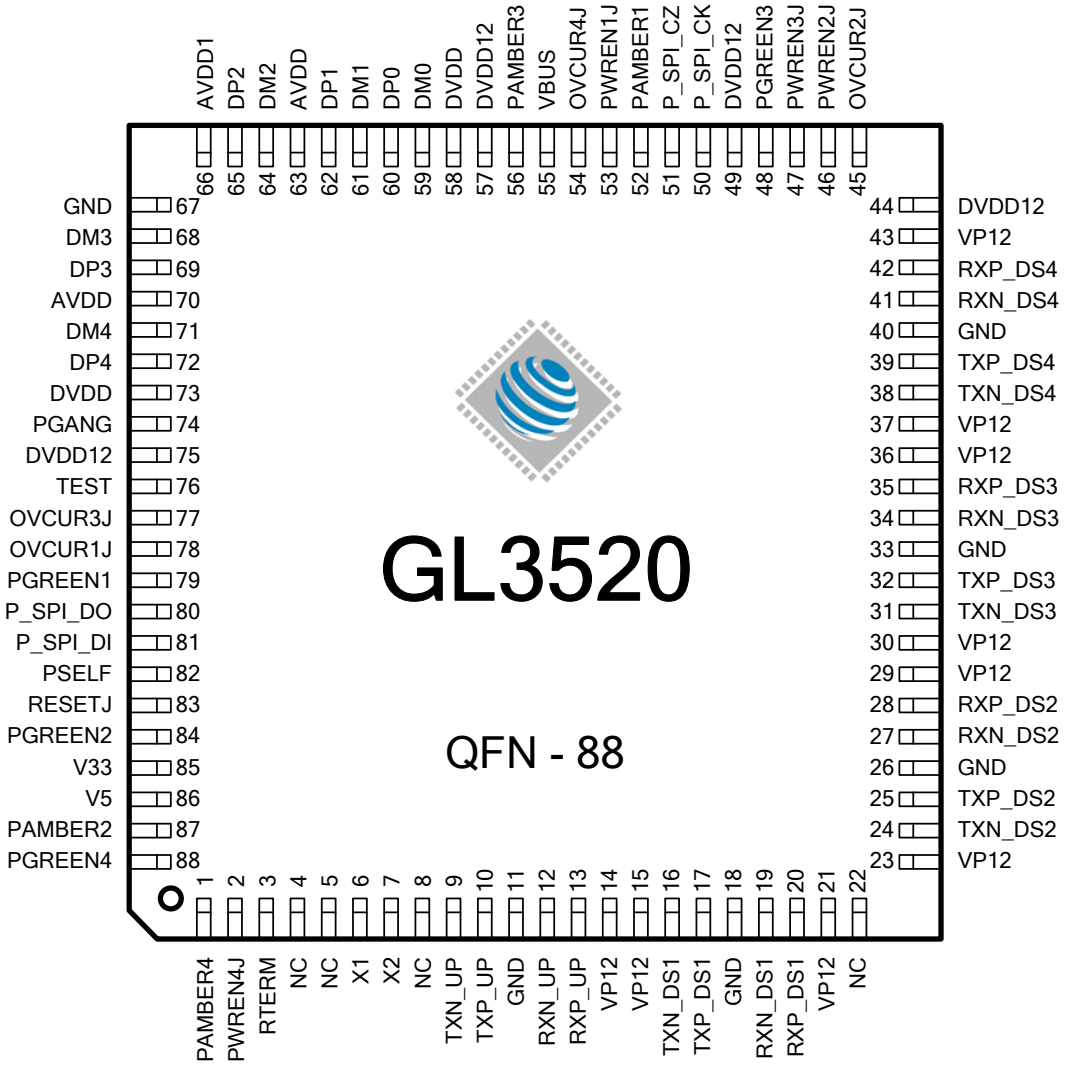

Figure 3.1 - GL3520-22 QFN 88 Pin out Diagram

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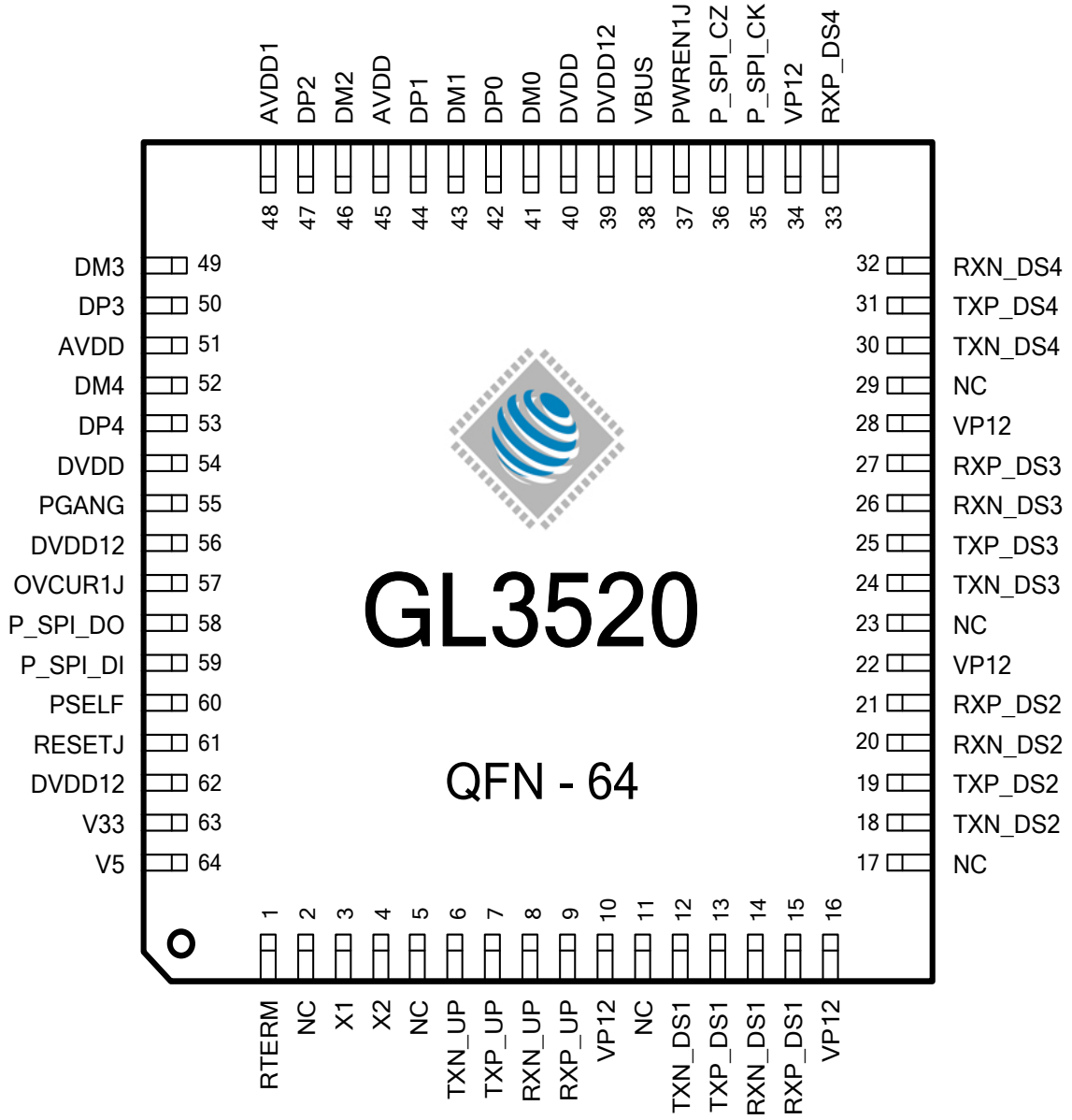

Figure 3.2 - GL3520-22 QFN64 (OS3) Pin out Diagram (Gang)

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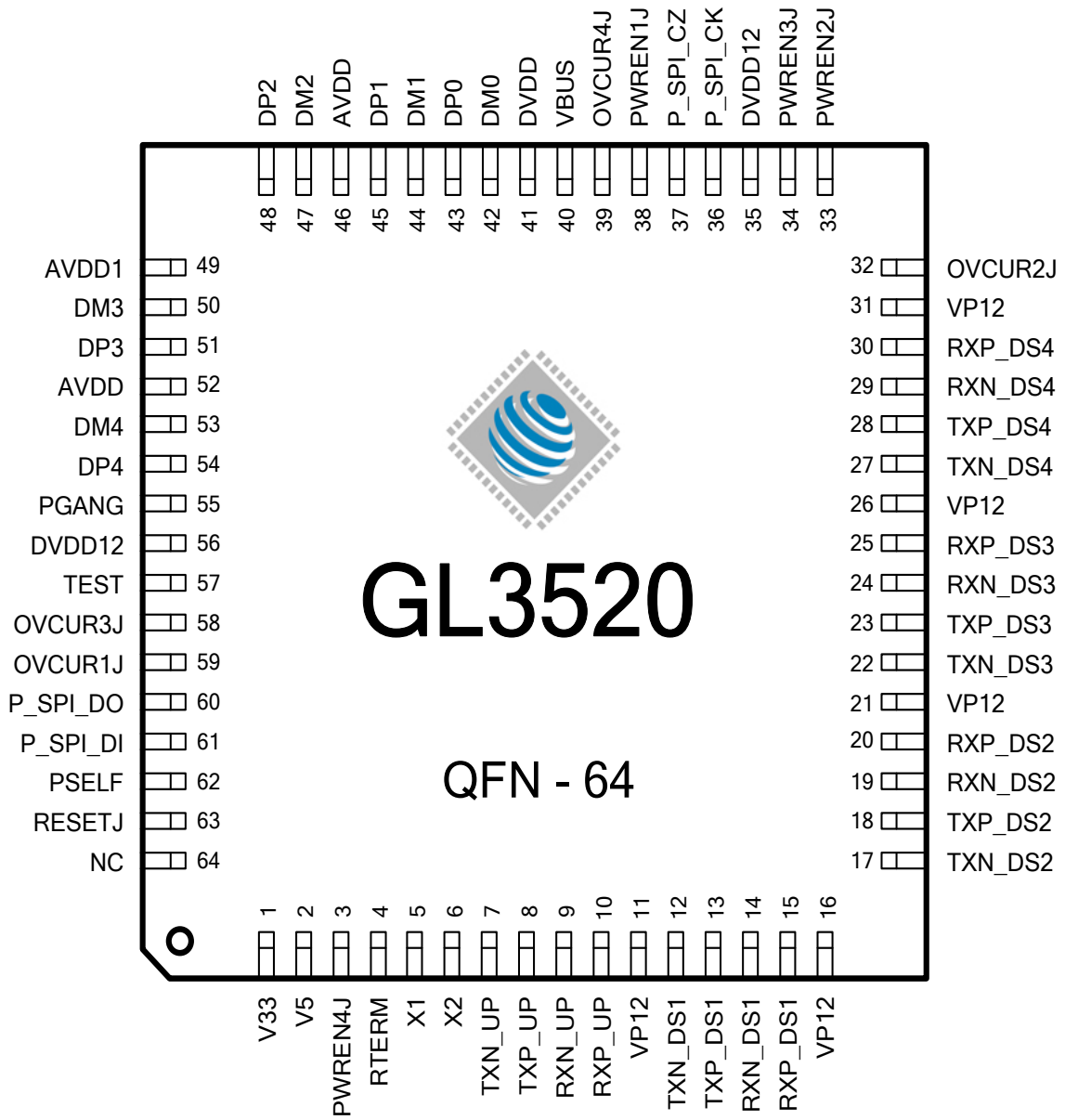

Figure 3.3 - GL3520-22 QFN64 (OS8) Pin out Diagram (Individual)

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3.2 Pin Descriptions

USB Interface					
Pin Name	**QFN 88**	**QFN 64** (OS3)	**QFN 64** (OS8)	**Type**	**Description**
TXN_UP TXP_UP	9 10	6 7	7 8	O	USB 3.0 Differential Data Transmitter TX-/TX+ of USPORT
RXN_UP RXP_UP	12 13	8 9	9 10	I	USB 3.0 Differential Data Receiver RX-/RX+ of USPORT
TXN_DS1 TXP_DS1	16 17	12 13	12 13	O	USB 3.0 Differential Data Transmitter TX-/TX+ of DSPORT1
RXN_DS1 RXP_DS1	19 20	14 15	14 15	I	USB 3.0 Differential Data Receiver RX-/RX+ of DSPORT1
TXN_DS2 TXP_DS2	24 25	18 19	17 18	O	USB 3.0 Differential Data Transmitter TX-/TX+ of DSPORT2
RXN_DS2 RXP_DS2	27 28	20 21	19 20	I	USB 3.0 Differential Data Receiver RX-/RX+ of DSPORT2
TXN_DS3 TXP_DS3	31 32	24 25	22 23	O	USB 3.0 Differential Data Transmitter TX-/TX+ of DSPORT3
RXN_DS3 RXP_DS3	34 35	26 27	24 25	I	USB 3.0 Differential Data Receiver RX-/RX+ of DSPORT3
TXN_DS4 TXP_DS4	38 39	30 31	27 28	O	USB 3.0 Differential Data Transmitter TX-/TX+ of DSPORT4
RXN_DS4 RXP_DS4	41 42	32 33	29 30	I	USB 3.0 Differential Data Receiver RX-/RX+ of DSPORT4
DM0,DP0	59 60	41 42	42 43	B	USB 2.0 DM/DP for USPORT
DM1, DP1	61 62	43 44	44 45	B	USB 2.0 DM/DP for DSPORT1
DM2, DP2	64 65	46 47	47 48	B	USB 2.0 DM/DP for DSPORT2
DM3, DP3	68 69	49 50	50 51	B	USB 2.0 DM/DP for DSPORT3
DM4, DP4	71 72	52 53	53 54	B	USB 2.0 DM/DP for DSPORT4

Hub Interface					
Pin Name	**QFN 88**	**QFN 64** (OS3)	**QFN 64** (OS8)	**Type**	**Description**
PGREEN1~4	79,84,48,88	-	-	B (pd)	Green LED indicator for DSPORT1~4
PAMBER1~4	52,87,56,1	-	-	B (pd)	Amber LED indicator for DSPORT1~4
PWREN1~4J	53,46,47,2	37	38,33,34,3	B	Active low. Power enable output for DSPORT1~4 PWREN1# is the only power-enable output for GANG mode.

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OVCUR1~4J	78,45,77,54	57	59,32,58,39	I (pd)	Active low. Over current indicator for DSPORT1~4 OVCUR1# is the only over current flag for GANG mode.
PGANG	74	55	55	I	Default put in input mode after power-on reset. Individual/gang mode is strapped during this period.
PSELF	82	60	62	I	0: GL3520 is bus-powered. 1: GL3520 is self-powered.

Clock and Reset Interface					
Pin Name	**QFN 88**	**QFN 64** (OS3)	**QFN 64** (OS8)	**Type**	**Description**
X1	6	3	5	I	Crystal / OSC clock input
X2	7	4	6	O	Crystal clock output.
RESETJ	83	61	63	I (pd)	Active low. External reset input, default pull high 10KΩ. When RESET# = low, whole chip is reset to the initial state.

SPI Interface					
Pin Name	**QFN 88**	**QFN 64** (OS3)	**QFN 64** (OS8)	**Type**	**Description**
P_SPI_CK	50	35	36	B	For SPI data clock
P_SPI_CZ	51	36	37	B	For SPI data chip enable
P_SPI_DO	80	58	60	B	For SPI data Input
P_SPI_DI	81	59	61	B	For SPI data Output

Power/Ground Interface					
Pin Name	**QFN 88**	**QFN 64** (OS3)	**QFN 64** (OS8)	**Type**	**Description**
VP12	14,15,21, 23,29,30, 36,37,43	10,16,22, 28,34	11,16,21, 26,31	P	Analog 1.2V power input for Analog circuit
DVDD12	44,49,57,75	39,56,62	35,56	P	1.2V digital power input for digital circuits
DVDD	58,73	40,54	41	P	3.3V digital power input for digital circuits
AVDD	63,66,70	45,48,51	46,49,52	P	Analog 3.3V power input
GND	11,18,26, 33,40,67	-	-	P	Digital/Analog ground
VBUS	55	38	40	I	VBUS valid input
V33	85	63	1	P	5V-to-3.3V regulator Vout & 3.3 input
V5	86	64	2	P	5V Power input. It need be NC if using external regulator

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Miscellaneous Interface					
Pin Name	**QFN 88**	**QFN 64** (OS3)	**QFN 64** (OS8)	**Type**	**Description**
RTERM	3	1	4	A	A 680ohm resister must be connected between RTERM and Ground
TEST	76	-	57	B (pd)	TEST: 0: Normal operation. 1: Chip will be put in test mode.

Unspecified					
Pin Name	**QFN 88**	**QFN 64** (OS3)	**QFN 64** (OS8)	**Type**	**Description**
NC	4,5,8,22	2,5,11, 17,23,29	64	-	Not connected

Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must take care the power routing and the ground plane. For detailed information, please refer to **USB 3.0 Hub Design Guide**.

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	P	Power / Ground
	A	Analog
	pu	Internal pull up
	pd	Internal pull down

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CHAPTER 4 FUNCTION DESCRIPTION

4.1 Block Diagram

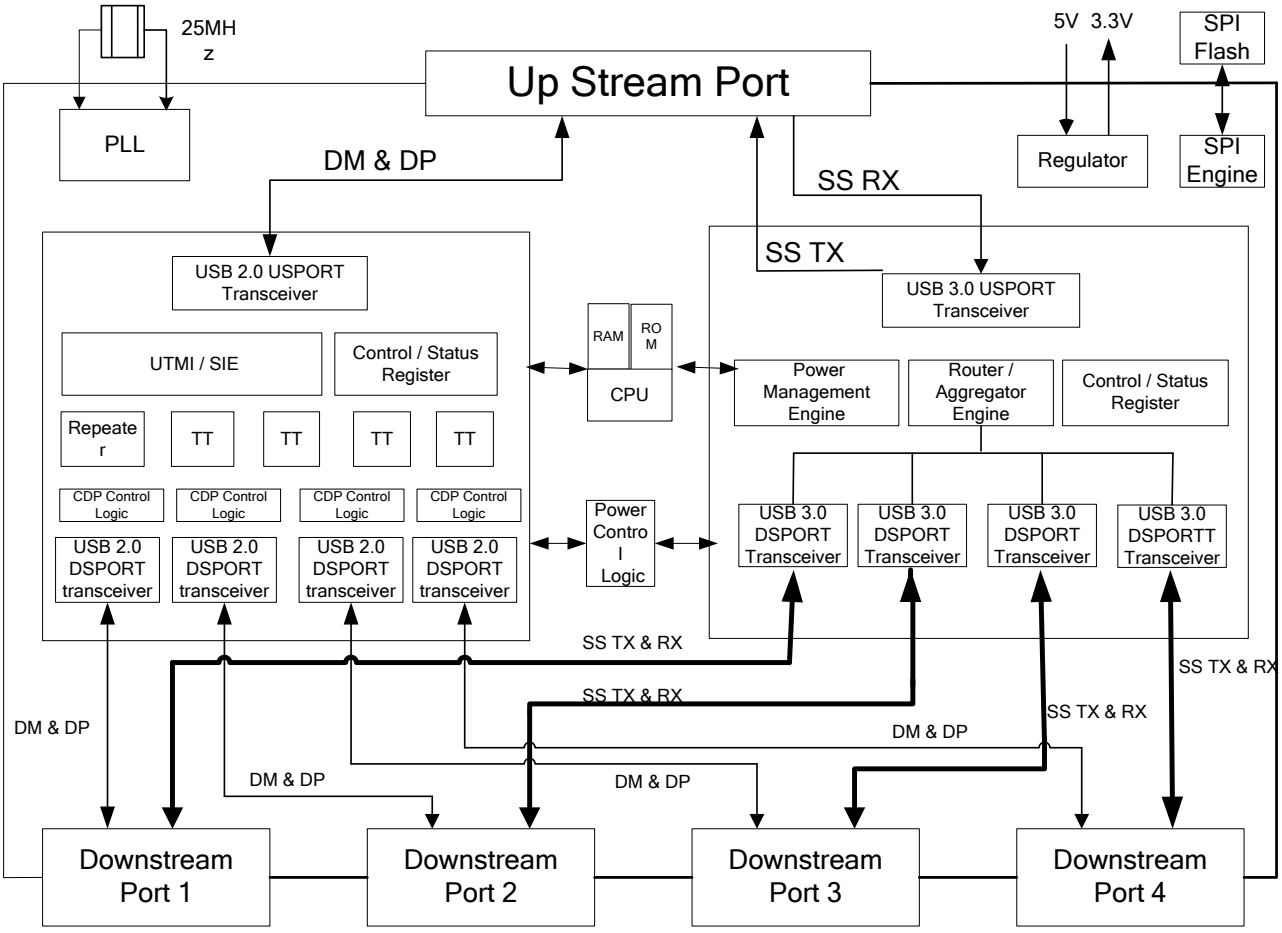

Figure 4.1 - Block Diagram

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4.2 General Description

4.2.1 USB 2.0 USPORT Transceiver

USB 2.0 USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in chapter 7 of USB specification revision 2.0. USPORT transceiver will operate in full-speed electrical signaling when GL3520-22 is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL3520-22 is plugged into a 2.0 host/hub.

4.2.2 USB 3.0 USPORT Transceiver

USB 3.0 USPORT (upstream port) transceiver is the analog circuit that has elastic buffer and supports receiver detection, data serialization and de-serialization. Besides, it has PIPE interface with SuperSpeed Link Layer

4.2.3 PLL (Phase Lock Loop)

PLL generates the clock sources for the whole chip. The generated clocks are proven quite accurate that help in generating high speed signal without jitter.

4.2.4 Regulator

GL3520-22 build in internal regulator converts 5V input to 3.3V output.

4.2.5 SPI Engine

SPI engine is to move code from external flash to the internal RAM.

4.2.6 RAM/ROM/CPU

The micro-processor unit of GL3520-22 is an 8-bit RISC processor with 16K-byte ROM and 256-bytes RAM. It operates at 12MIPS of 12 MHz clock(maximum) to decode the USB command issued from host and then prepares the data to respond to the host.

4.2.7 UTMI (USB 2.0 Transceiver Microcell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

4.2.8 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in chapter 8 of USB specification revision 2.0. It co-works with μC to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

4.2.9 Control/Status Register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipelines. Through the firmware based architecture, GL3520-22 possesses higher flexibility to control the USB protocol easily and correctly.

4.2.10 Power Management Engine

The power management of GL3520-22 is compliant with USB 3.0 specification. When operates in SuperSpeed mode, GL3520-22 supports U0, U1, U2 and U3 power states. U0 is the functional state. U1 and U2 are lower power states compared to U0. U1 is a low power state with fast exit to U0; U2 is a low power state which saves more power than U1, with slower exit to U0. U3 is suspend state, which is the most power-saving state, with tens of milliseconds exit to U0. Unlike USB 2.0, SuperSpeed packet traffic is unicast rather than broadcast. Packet only travels the direct path in-between host and the target device.

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SuperSpeed traffic will not reach an unrelated device. When enabled for U1/U2 entry, and there is no pending traffic within comparable exit latency, GL3520-22 will initiate U1/U2 entry to save the power. On the other hand, the link partner of GL3520-22 may also initiate U1/U2 entry. In this case, GL3520-22 will accept or reject low power state entry according to its internal condition.

4.2.11 Router/Aggregator Engine

Router/Aggregator Engine implements the control logic defined in Ch10 of USB3.0 specification. Router/Aggregator Engine use smart method for route packet to device or aggregate packet to host.

4.2.12 REPEATER

Repeater logic implements the control logic defined in section 11.4 and section 11.7 of USB specification revision 2.0. REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

4.2.13 TT

TT(Transaction Translator) implements the control logic defined in section 11.14 ~ 11.22 of USB specification revision 2.0. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL3520-22 adopts multiple TT architecture to provide the most performance effective solution. Multiple TT provides control logics for each downstream port respectively.

4.2.13.1 Connected to 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

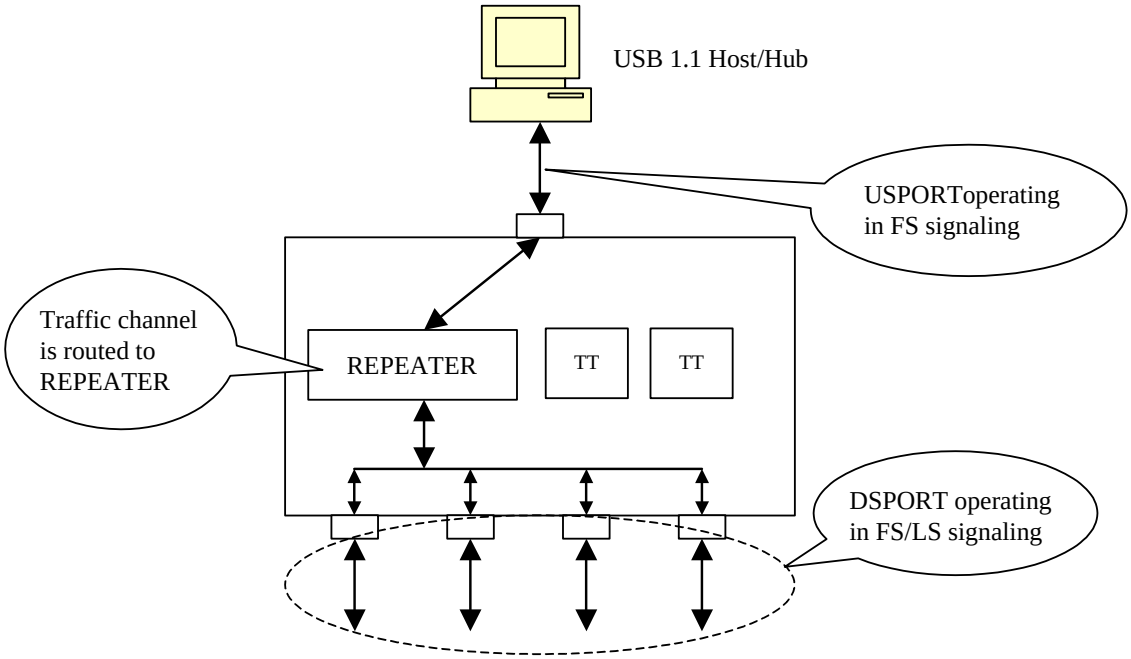

Figure 4.2 - Operating in USB 1.1 Schemes

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4.2.13.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

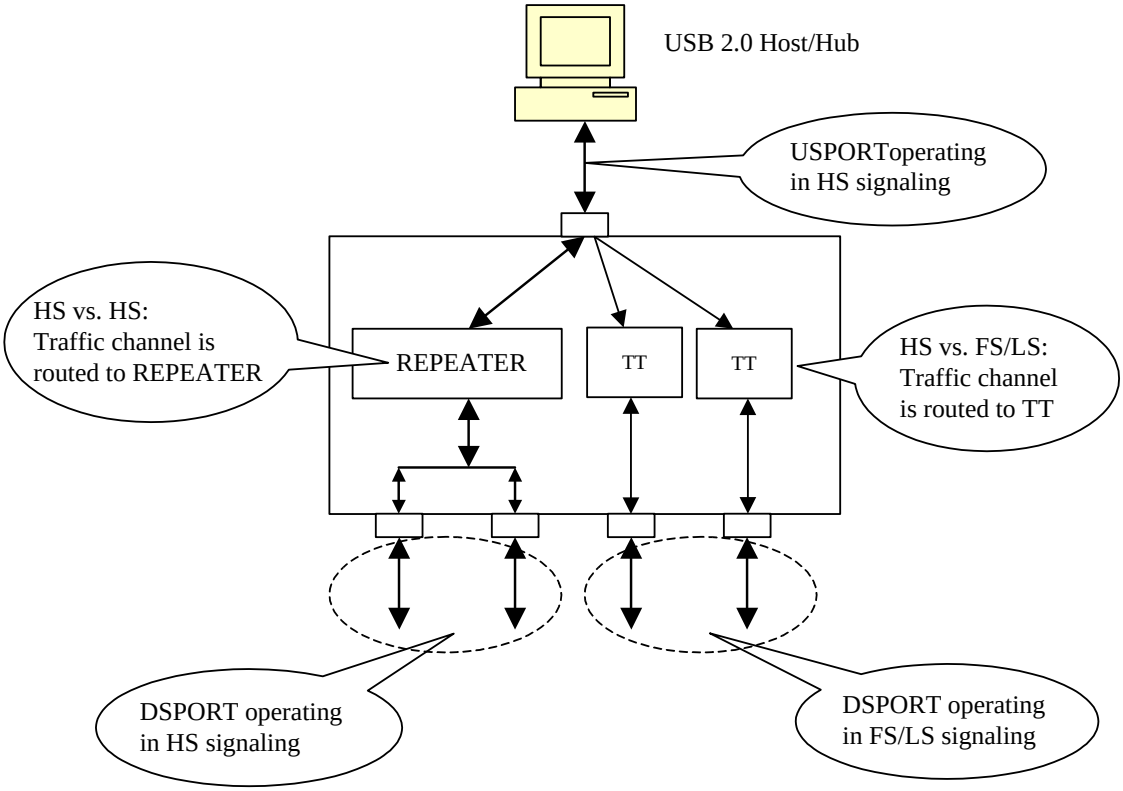

Figure 4.3 - Operating in USB 2.0 Schemes

4.2.14 CDP Control Logic

CDP (charging downstream port) control logic implements the logic defined in USB Battery charging specification revision 1.2. The major function of it is to control DSPORT Transceiver to make handshake with a portable device which is compliant with USB Battery charging spec rev1.2 as well. After recognizing charging detection each other, portable device will draw up to 1.5A from VBUS to fast charge its battery.

4.2.15 USB 3.0/USB 2.0 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics. In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

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4.3 Configuration and I/O Settings

4.3.1 RESET Setting

GL3520-22's power on reset can either be triggered by external reset or internal power good reset circuit. The external reset pin, RESETJ, is connected to upstream port Vbus (5V) to sense the USB plug / unplug or 5V voltage drop. The reset trigger voltage can be set by adjusting the value of resistor R1 and R2 (Suggested value refers to schematics) GL3520-22's internal reset is designed to monitor silicon's internal core power (1.2V) and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 40 μS after power good. GL3520-22's reset circuit as depicted in the picture.

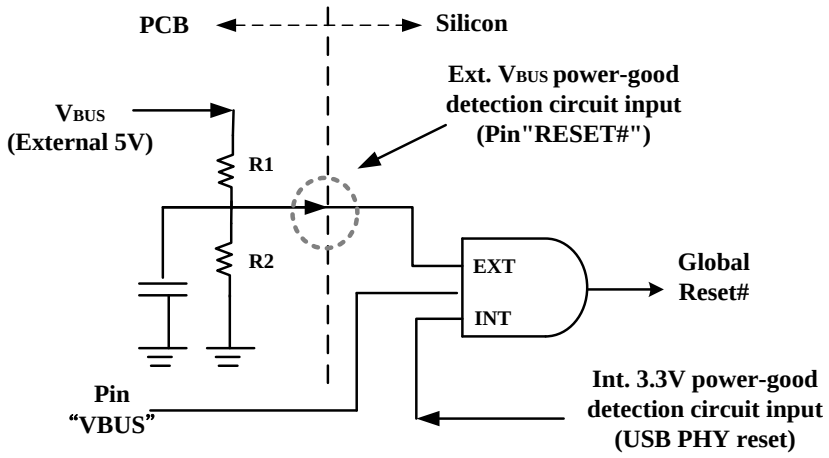

Figure 4.4 - Power on Reset Diagram

To fully control the reset process of GL3520-22, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit. Timing of POR is illustrated as below figure.

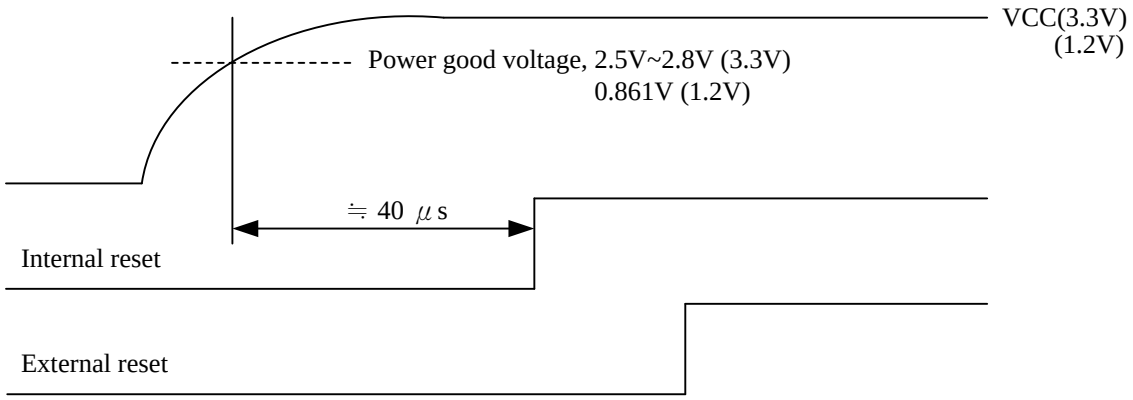

Figure 4.5 - Power on Sequence of GL3520-22

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4.3.2 PGANG Setting

To save pin count, GL3520-22 uses the same pin to decide individual/gang mode as well as to output the suspend flag. The individual/gang mode is decided within 21us after power on reset. Then, about 50ms later, this pin is changed to output mode. GL3520-22 outputs the suspend flag once it is globally suspended. For individual mode, a pull low resister greater than 100KΩ should be placed. For gang mode, a greater than 100KΩ pull high resister should be placed. In figure 4.7, we also depict the suspend LED indicator schematics. It should be noticed that the polarity of LED must be followed, otherwise the suspend current will be over spec limitation (2.5mA).

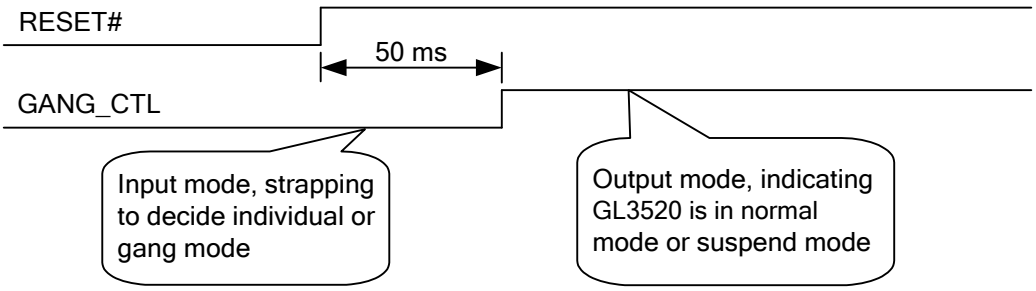

Figure 4.6 - Timing of PGANG Strapping

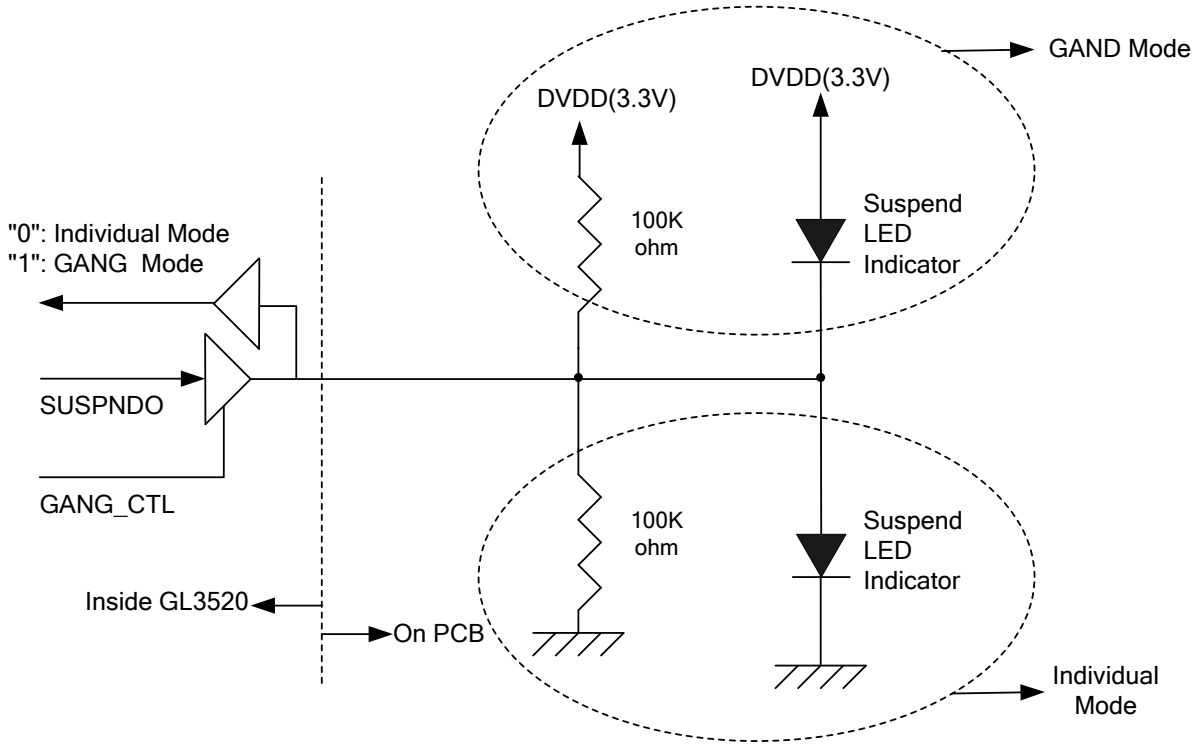

Figure 4.7 - GANG Mode Setting

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4.3.3 SELF/BUS Power Setting

By setting PSELF, GL3520-22 can be configured as a bus-power or a self-power hub.

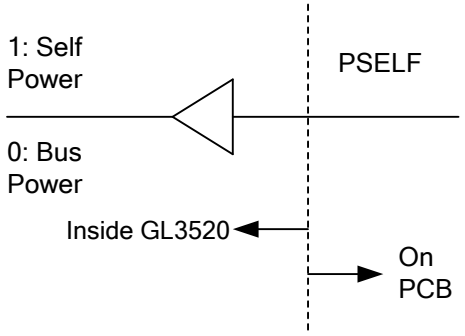

Figure 4.8 - SELF/BUS Power Setting

4.3.4 LED Connections

GL3520-22 controls the LED lighting according to the flow defined in section 11.5.3 of Universal Serial Bus Specification Revision2.0. Both manual mode and Automatic mode are supported in GL3520-22. When GL3520-22 is globally suspended, GL3520-22 will turn off the LED to save power.

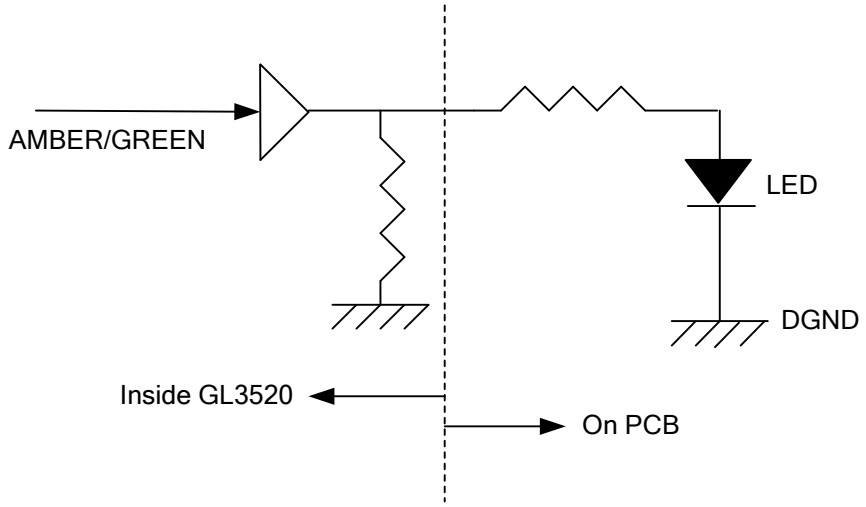

Figure 4.9 - LED Connection

4.3.5 Power Switch

GL3520 supports low active power switch. Please refer to the reference schematic for power switch control.

4.3.6 Port Number Configuration

Number of downstream port can be configured as 4/3/2 ports by firmware configuration, EEPROM, and pin strapping. Please refer to **Genesys USB 3.0 Hub FW ISP Tool User Guide** for the detailed setting information.

4.3.7 Non-removable Port Configuration

For compound application or embedded system, downstream ports that always connect inside the system can be set as non-removable by firmware configuration, EEPROM, and pin strapping. Please refer to **Genesys USB 3.0 Hub FW ISP Tool User Guide** for the detailed setting information.

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CHAPTER 5 BATTERY CHARGING SPECIFICATION REV.1.2 SUPPORT

5.1 Background

The USB ports on personal computers are convenient places for portable devices to draw current for charging their batteries. This convenience has led to the creation of dedicated chargers that simply expose a USB standard-A receptacle. This allows portable devices to use the same USB cable to charge from either a PC or from a dedicated charger.

If a portable device is attached to a USB host or hub, then the USB 2.0 specification requires that after connecting, a portable device must draw less than:

- 2.5 mA average if the bus is suspended
- 100 mA maximum if bus is not suspended and not configured
- 500 mA maximum if bus is not suspended and configured for 500 mA

If a portable device is attached to a charging host or hub, it is allowed to draw a current up to 1.5A, regardless of suspend. In order for a portable device to determine how much current it is allowed to draw from an upstream USB port, the USB-IF Battery Charging specification defines the mechanisms that allow the portable device to distinguish between a USB standard host, hub or a USB charging host. Since portable devices can be attached to USB charging ports from various manufactures, it is important that all USB charging ports behave the same way. This specification also defines the requirements for a USB chargers and charging downstream ports.

5.2 Standard Downstream Port (SDP)

GL3520-22 complies with Battery Charging Specification rev1.2, which defines three charging ports: SDP, CDP and DCP. The SDP is a standard USB port which can transfer data and provide maximum 500mA current.

5.3 Charging Downstream Port (CDP)

GL3520-22 supports battery charging detection, turning its downstream port from a standard downstream port (SDP) into charging downstream port (CDP). GL3520-22 will make physical layer handshaking when a portable device that complies with BC rev1.2 attaches to its downstream port. After physical layer handshaking, a portable device is allowed to draw more current up to 1.5A.

Once the charging downstream port of GL3520-22 is enabled, it will monitor the V_{DP_SRC} on D+ line anytime. When a portable device, which is compliant with BC rev1.2, is attached to the downstream port, it will drive V_{DP_SRC} on D+ line to initiate the handshake with charging downstream port. GL3520-22 will response on its D- line by V_{DM_SRC} and keep in a certain period of time and voltage level. The portable device will accept this handshaking on its D- line in correct timing period and voltage level, and then turns off its V_{DP_SRC} on D+ line. GL3520-22 will recognize that charging negotiation is finished by counting time between the portable device turning on and off its V_{DP_SRC}. After that, the portable device can start to draw more current from VBUS to charge its battery more rapidly. It can draw current up to 1.5A.

If there is no response from D- line, the portable device will recognize that it is attached to a standard downstream port, not a charging port.

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5.4 Dedicated Charging Port (DCP)

GL3520-22 also supports dedicated charging port, which is a downstream port on a device that outputs power through a USB connector, but it is not capable of enumerating a downstream device. With the adequate system circuit design, GL3520-22 will turn its downstream port from a standard downstream port (SDP) into dedicated charging port (DCP), i.e short the D+ line to the D- line, to let the portable device draws current up to 1.5A. Please refer to the **USB 3.0 Hub Design Guide** document for the detailed information.

5.5 ACA-Dock

An ACA-Dock is a docking station that has one upstream port, and zero or more downstream ports. The upstream port can be attached to a portable device (PD), and is capable of sourcing ICDP to the PD, which means that the upstream port can charge and have data communication with the PD at the same time. Please refer to Battery Charging Spec v1.2 for more details.

5.6 Apple and Samsung Devices

Except BC rev1.2-complied portable devices, GL3520-22 also supports the fast charging of Apple and Samsung devices.

- Apple: iPhone, iPad series.
- Samsung: Galaxy Tab series, Galaxy Mobile Phones series.

5.7 Port Numbers of Charging Downstream Port Configuration

Number of charging downstream port can be configured as 1/2/3/4 ports by firmware configuration. Please refer to the **Genesys USB 3.0 Hub FW ISP Tool User Guide** document for the detailed setting information.

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CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_5	5V Power Supply	-0.5	+6.0	V
V_{DD}	3.3V Power Supply	-0.5	+3.6	V
VDDcore	1.2VPower Supply	-0.5	+1.32	V
V_{IN}	3.3V Input Voltage for digital I/O(EE_DO) pins*	-0.5	+5	V
Vincore	1.2V	-0.5	+1.32	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
T_S	Storage Temperature under bias	-60	+100	^oC
F_{OSC}	Frequency	25 MHz ± 0.03%		

*Please refer to the reference design schematic.

6.2 Operating Ranges

Table 6.2 - Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_5	5V Power Supply	4.75	5.0	5.25	V
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V
VDDcore	1.2V Power Supply	1.15	1.2	1.32	V
V_{IND}	Input Voltage for digital I/O pins	-0.5	3.3	3.6	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5	3.3	3.6	V
T_A	Ambient Temperature	0	-	70	^oC
T_J	Absolute maximum junction temperature	0	-	125	^oC

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6.3 DC Characteristics

6.3.1 DC Characteristics except USB Signals

Table 6.3 - DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	3	3.3	3.6	V
V_{IL}	LOW level input voltage	-	-	1	V
V_{IH}	HIGH level input voltage	1.4	-	-	V
V_{TLH}	Schmitt trigger PAD*-LOW to HIGH threshold voltage	1.7	-	-	V
V_{THL}	Schmitt trigger PAD*- HIGH to LOW threshold voltage	-	-	0.7	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-	-	30	μA
R_{DN}	Pad internal pull down resister	232	378	647	KΩ
R_{UP}	Pad internal pull up resister	276	435	718	KΩ

* Schmitt trigger pads are VBUS, RESET

6.3.2 USB 2.0 Interface DC Characteristics

The GL3520-22 conforms to DC characteristics for Universal Serial Bus specification rev. 2.0. Please refer to this specification for more information.

6.3.3 USB 3.0 Interface DC Characteristics

The GL3520-22 conforms to DC characteristics for Universal Serial Bus specification rev.3.0. Please refer to this specification for more information.

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6.4 Power Consumption

Number of Active USB 3.0 Ports	5V		1.2V		3.3V		Unit
	Config.	Read/ Write	Config.	Read/ Write	Config.	Read/ Write	
Suspend	17		9		4		mW
1	210	462	36	271	108	108	mW
2	210	612	36	397	108	108	mW
3	210	771	36	519	108	108	mW
4	210	945	36	644	108	108	mW

Number of Active USB 2.0 Ports	5V		1.2V		3.3V		Unit
	Config.	Read/ Write	Config.	Read/ Write	Config.	Read/ Write	
Suspend	17		9		4		mW
1	217	233	18	18	128	138	mW
2	248	315	18	18	149	193	mW
3	280	360	18	18	170	222	mW
4	312	394	18	18	191	244	mW

Note:

Test result represents silicon level operating current, without considering additional power consumption contributed by external over-current protection circuit such as power switch or polyfuse. The power consumption measured by 5V is based on Genesys' evaluation board. It may be diverse with regulator power transfer efficiency and firmware configurations.

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6.5 On-Chip Power Regulator

GL3520-22 requires 3.3V source power for normal operation of internal core logic and USB physical layer (PHY). The integrated low-drop power regulator converts 5V power input from USB cable (Vbus) to 3.3V voltage for silicon power source. The 3.3V power output is guaranteed by an internal voltage reference circuit to prevent unstable 5V power compromise USB data integrity. The regulator's maximum current loading is 250mA, which provides enough tolerance for normal GL3520-22 operation (below 100mA).

On-chip Power Regulator Features:

- 5V to 3.3V low-drop power regulator
- 250mA maximum output driving capability
- Provide stable 3.3V output when Vin = 3.4V~5.5V
- 125uA maximum quiescent current (typical 80uA).

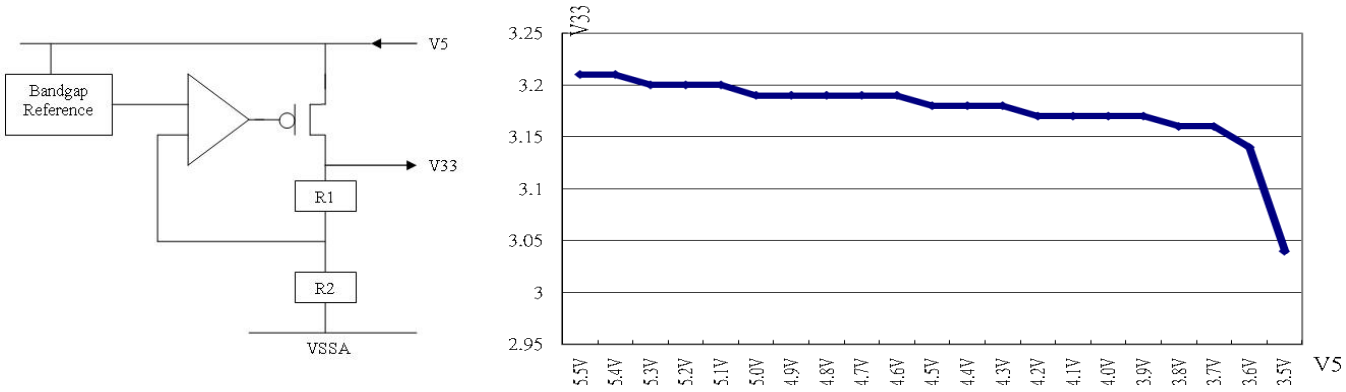

Figure 6.1 - Vin(V5) vs Vout(V33)*

*Note: Measured environment: Ambient temperature = 25℃ / Current Loading = 250mA

6.6 External Clock

XOUT: 25MHz crystal oscillator output. It should be left open if an external clock source is used.
XIN: 25MHz crystal oscillator input. If an external 3.3V clock source is used, its frequency has to be 25MHz +/-300ppm with a peak-to-peak jitter less than 50ps.

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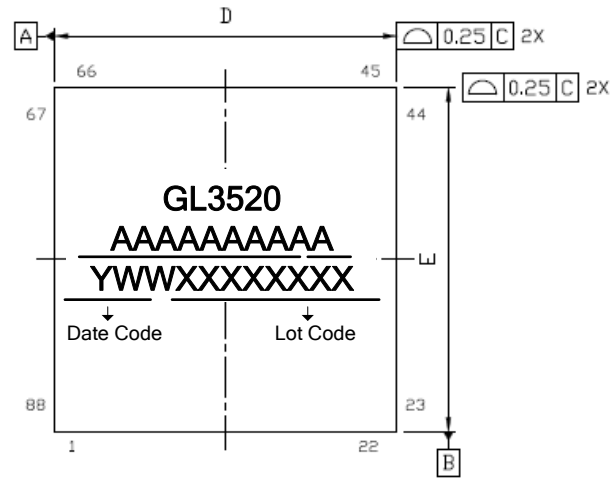
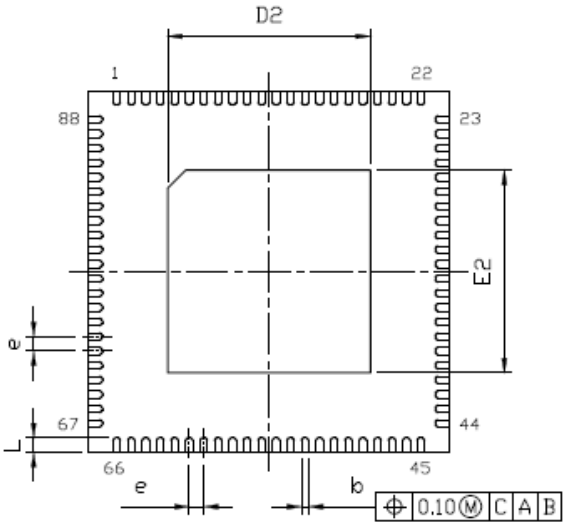
CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
D	10.00 (393.7) BSC		
D2	5.45 (214.5)	5.60 (220.5)	5.75 (226.4)
E	10.00 (393.7) BSC		
E2	5.45 (214.5)	5.60 (220.5)	5.75 (226.4)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.



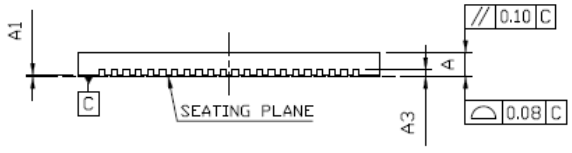


Figure 7.1 – GL3520-22 88 Pin QFN Package

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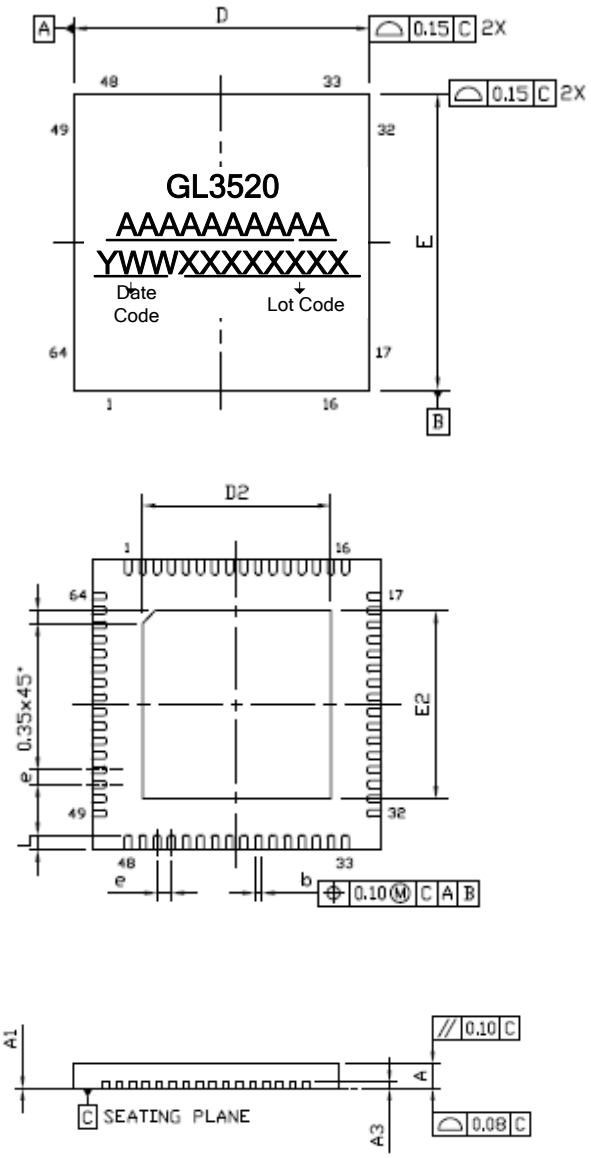

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
D	8.00 (315.0) BSC		
D2	4.10 (161.4)	5.35 (210.6)	6.60 (259.8)
E	8.00 (315.0) BSC		
E2	4.10 (161.4)	5.35 (210.6)	6.60 (259.8)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.2 – GL3520-22 64 Pin QFN Package

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CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Material	Version	Status
GL3520-OVY22	QFN 88	Green Package	22	Available
GL3520-OS322	QFN 64 (Gang)	Green Package	22	Available
GL3520-OS822	QFN 64 (Individual/Gang)	Green Package	22	Available

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