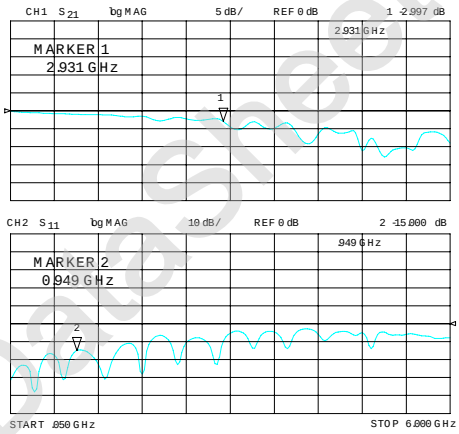
Thin Film Technology Corp.

Delay Line Data Book



thin Film
On board
tm

Thin Film Technology. Delay Lines.
Because *Timing is Everything.*™

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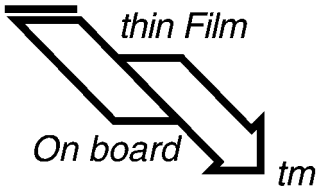


The component needs for future systems design will be met with higher technology. Thin Film Technology.

High speed system design needs full wave regime implementation in order to maintain signal fidelity. Harmonics not considered at slower speeds must be accounted for when fast rise times and high bandwidths are to be used. When edge rates and circuit speeds enter the sub-nanosecond regime, all components used in a system design must obey high speed design rules, whether they be packages, devices, integrated circuits, interconnects, or printed circuit boards.

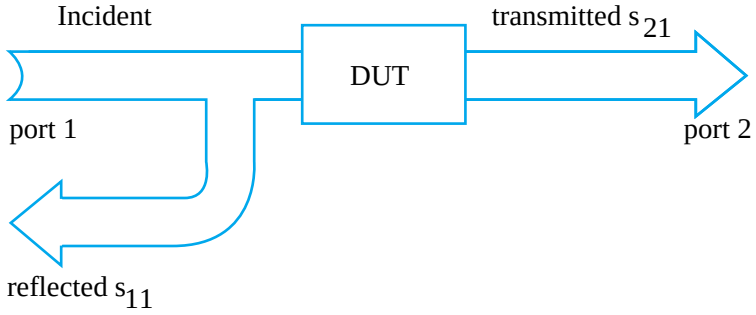
Thin film component design is uniquely appropriate for high frequency design: the precision of pattern features, purity of film, stability of substrate materials, and advanced assembly technologies offer solutions for high speed design. Wave propagation through correctly designed thin film elements provide for precise impedance control, a reduction in capacitive and inductive parasitics, and elimination of ground bounce. Shielded designs protect for electro-magnetic and radio-frequency interference.

Thin Film Technology Corporation manufactures high speed delay lines based on microstrip, stripline, and multi-conductor transmission lines. Available in leaded, surface mount, and chip configuration, these products have performance to 5 gigahertz. New designs and materials are under continuous development to extend this range. It is our philosophy that higher technology components can improve your system performance and lower your costs, both now and in the future.

High frequency measurement is essential to assure correct device characterization. Attention to field patterns is necessary when representing transmission lines in order to understand reflections, mismatches, and skin effects. Test design layout should replicate the field patterns that will actually occur with the real package, so that accurate device characteristics represented by scattering parameters can be made. Proper calibration standards used at the device under test are sine qua non.

DEFINITIONS

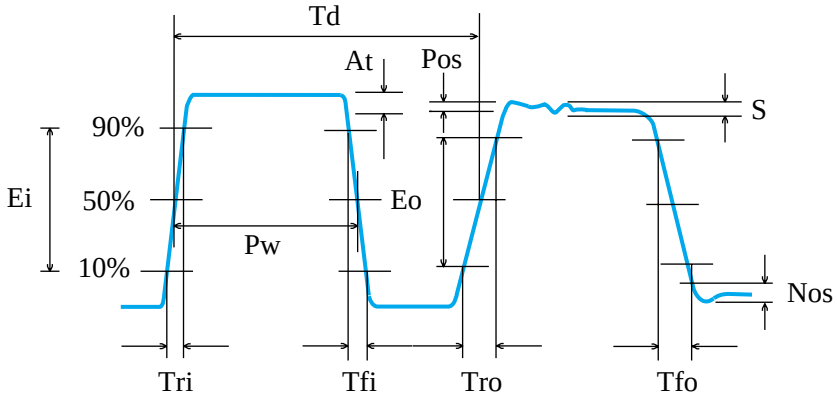
Scattering Parameters (S-parameters): a two port numbering convention used commonly at high frequencies relating to network measurements. The first number represents the port where the energy is emerging from the device and the second number is the port where the energy is entering the device.



Parameter s21: The forward transmission coefficient indicating the ratio of energy emerging from port 2 to the energy incident to port 1.
Parameter s11: The reflected transmission coefficient indicating the ratio of energy emerging from port 1 to the energy incident to port 1.
Time Delay (Td): The elapsed time from the 50% on the leading edge of the input pulse to the 50% point on the leading edge of the delayed pulse.
Network Risetime and Fall time(Tr): The true measure of delayed pulse risetime performance expressed by the following:

$$Tr = \sqrt{(T_r \text{ output})^2 - (T_r \text{ input})^2}$$

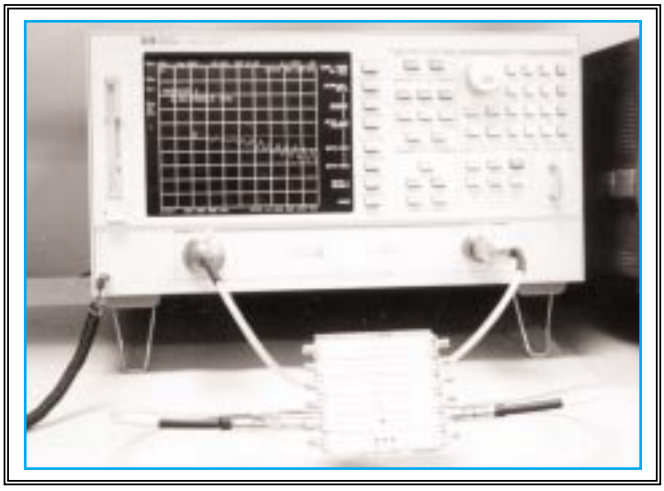
Input Risetime and Falltime (Tri and Tfi): The time between the 10% and 90% of the input voltage.
Output Risetime and Falltime (Tro and Tfo): The time between the 10% and 90% of the output voltage.
Input and Output Voltage (Ei and Eo): The amplitude of the input and output voltages, respectively.
Attenuation (At): The difference in amplitude between input and output pulses. Attenuation is caused primarily by the Direct Current (DC) resistance of the delay line.



Pulsewidth (Pw): The time difference between the 50% point of the leading edge and the 50% point of the trailing edge of the pulse.
Pulse Distortion (S): The maximum spurious % change, either positive or negative, relative to the pulse amplitude.
Pulse Edge Over/Undershoot: (Pos, Nos): Peak amplitudes occurring at either the top or bottom of the output pulse.

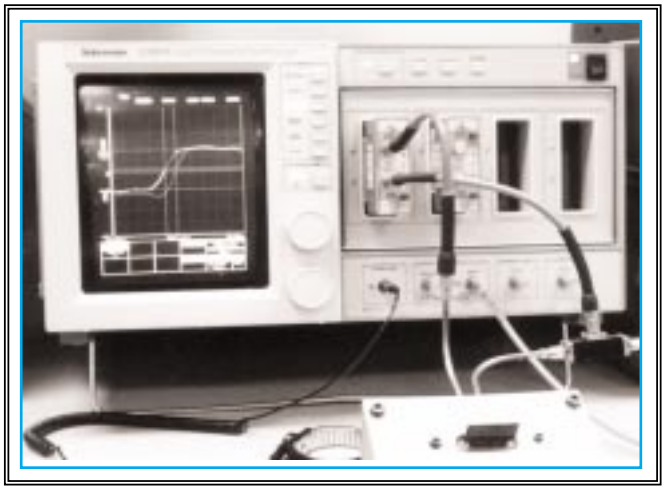
DELAY LINE TEST METHODS

Frequency Domain Measurement



Network analysis may be used to measure insertion loss, return loss, phase and group delay, with signal stimulus both forward and reverse to the device. For our passive delay lines, performance is indicated as loss in the frequency domain.

The graphed information presented in this databook is labeled according to traditional Scattering parameters (S-parameters). S_{21} and S_{11} on the following pages indicates insertion loss (energy incident but lost through the device) and return loss (energy incident but reflected away from the device). The data is presented in summary form, but frequency performance data may be requested for specific part numbers.



Time Domain Measurement

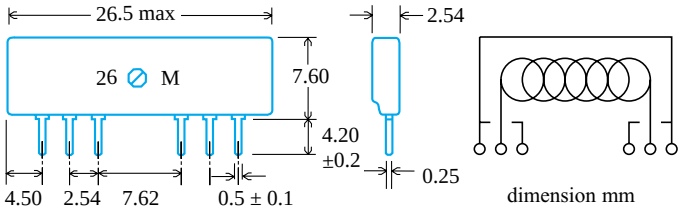
High speed (Rise Time <55 ps) digital signals are used to stimulate the device for Rise time (Tro) and Fall time (Tfo) performance. Data is presented in the time domain, and is another measure indicating frequency performance. Sampling measurements can be used to demonstrate signal fidelity and can be processed by a variety of techniques.

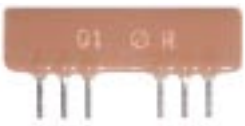
Additionally, Time Domain Reflectometry (TDR) measurements may be made to provide time delay performance as well as detailed impedance mapping of the device transmission structure. TDR measurements can be performed either in a single end driven mode, or in a dual end (differential) driven mode, which is necessary for the GL2L Series Differential Delay Line product.

DL SERIES DELAY LINES

DL1L5 ** *** S

U.S. Patent 4,641,113





Application note: for precise high speed digital timing deskew, socket the delay line for custom timing adjustments against lot to lot propagation delay variations in IC devices.

DL1L5 SERIES 50 ohm

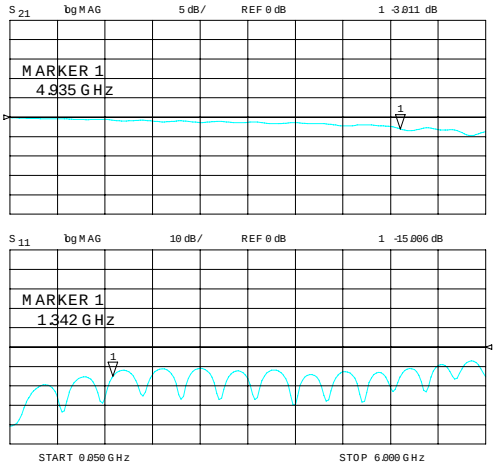
P/N	Td (ns)	Insertion Loss (-3 dB)	Return Loss (15 dB)	Tro	Tfo	DCRV
DL1L5WK010S	0.10	>4.5 GHz	>0.9 GHz	<200 ps	<200 ps	<0.2 ohm
DL1L5WK020S	0.20					
DL1L5WK030S	0.30					
DL1L5WK040S	0.40					
DL1L5WK050S	0.50					<0.4 ohm
DL1L5XK060S	0.60					
DL1L5XK070S	0.70					
DL1L5XK080S	0.80			<250 ps	<250 ps	
DL1L5XK090S	0.90					
DL1L5XK100S	1.00					
DL1L5XK110S	1.10					
DL1L5XK120S	1.20					
DL1L5XK130S	1.30					
DL1L5XK140S	1.40					
DL1L5XK150S	1.50			<300 ps	<300 ps	<0.6 ohm
DL1L5XK160S	1.60	>2.5 GHz				
DL1L5XK170S	1.70					
DL1L5XK180S	1.80					
DL1L5XK190S	1.90					
DL1L5XK200S	2.00					
DL1L5XK210S	2.10					
DL1L5XK220S	2.20			<350 ps	<350 ps	
DL1L5XK230S	2.30	>2.0 GHz				<1.0 ohm
DL1L5XK240S	2.40					
DL1L5XK250S	2.50					
DL1L5XK260S	2.60					
DL1L5YK270S	2.70			<400 ps	<400 ps	
DL1L5YK280S	2.80					
DL1L5YK290S	2.90					
DL1L5YK300S	3.00					<1.2 ohm
DL1L5YK310S	3.10					
DL1L5YK320S	3.20					
DL1L5YK330S	3.30			<450 ps	<450 ps	
DL1L5YK340S	3.40					
DL1L5YK350S	3.50					
DL1L5ZK360S	3.60					<1.4 ohm
DL1L5ZK370S	3.70					
DL1L5ZK380S	3.80					
DL1L5ZK390S	3.90					
DL1L5ZK400S	4.00	>1.5 GHz		<500 ps	<500 ps	
DL1L5ZK410S	4.10					
DL1L5ZK420S	4.20					<1.6 ohm
DL1L5ZK430S	4.30					
DL1L5ZK440S	4.40					
DL1L5ZK450S	4.50					
DL1L5ZK460S	4.60					
DL1L5ZK470S	4.70					
DL1L5ZK480S	4.80	>1.0 GHz		<550 ps	<550 ps	<2.0 ohm
DL1L5ZK490S	4.90					
DL1L5ZK500S	5.00					
DL1L5ZK510S	5.10					

DL SERIES DELAY LINES

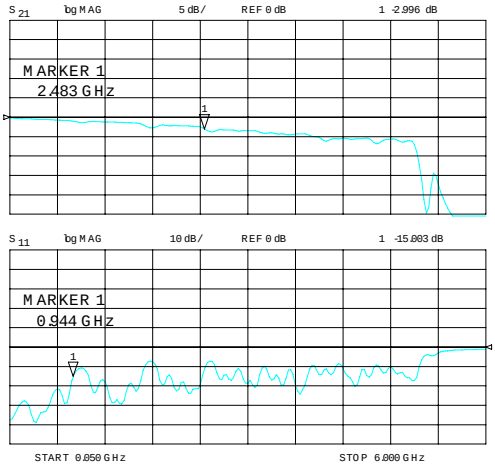
DL1L5 ** *** S

U.S. Patent 4,641,113

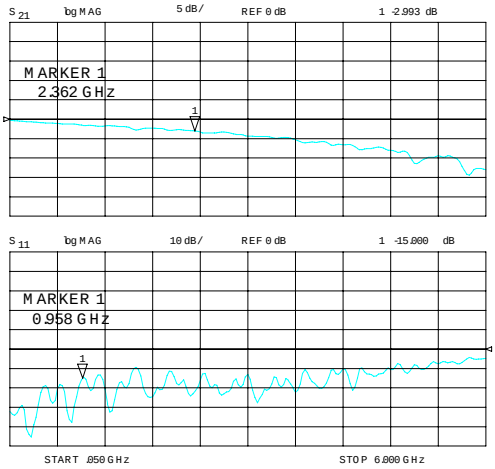
DL1L5XK100S *1 NS*



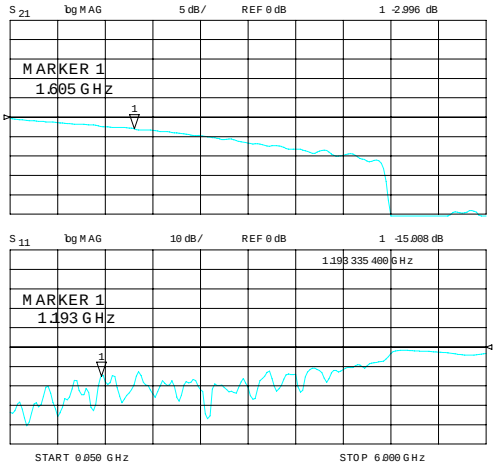
DL1L5XK200S *2 NS*



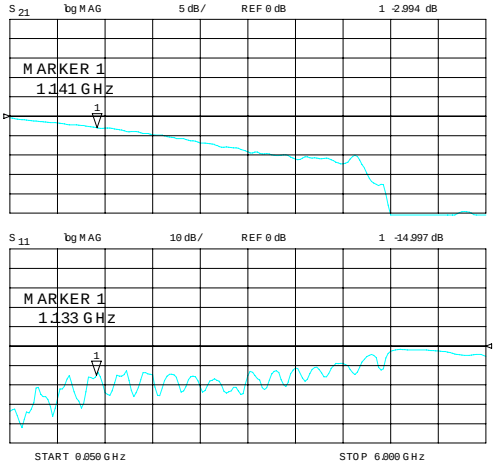
DL1L5YK300S *3 NS*



DL1L5ZK400S *4 NS*



DL1L5ZK500S *5 NS*



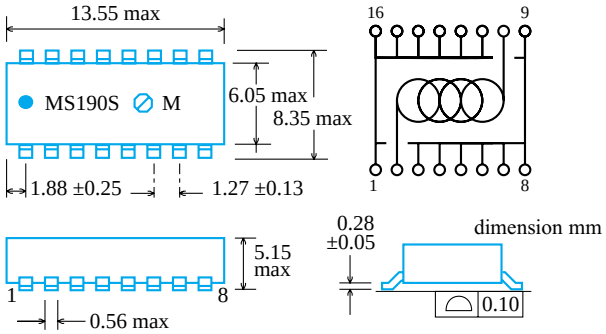
Characterization data is typical for this series of delay lines.

thin Film On board tm

GL1 SERIES DELAY LINES

GL1L5 ** *** S

U.S. Patent 5,365,203



Application note: save time with board layout and maintain flexibility with your clock distribution network. Design in a SMT delay line and avoid timely and costly board revisions.

GL1L5 SERIES 50 ohm

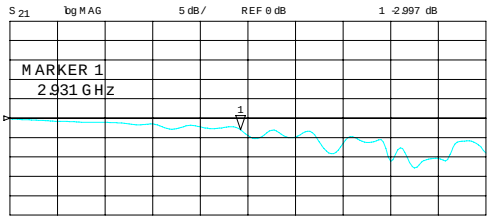
P/N	Td (ns)	Insertion Loss (-3 dB)	Return Loss (15 dB)	Tro	Tfo	DCRV
GL1L5LS010S	0.10	>2.50 GHz	>0.60 GHz	<200 ps	<200 ps	<1.0 ohm
GL1L5LS020S	0.20					
GL1L5LS030S	0.30					
GL1L5LS040S	0.40					
GL1L5LS050S	0.50					
GL1L5LS060S	0.60					
GL1L5LS070S	0.70					
GL1L5LS080S	0.80					
GL1L5LS090S	0.90	>2.00 GHz		<400 ps	<400 ps	<2.0 ohm
GL1L5LS100S	1.00					
GL1L5MS110S	1.10					
GL1L5MS120S	1.20					
GL1L5MS130S	1.30					
GL1L5MS140S	1.40					
GL1L5MS150S	1.50					
GL1L5MS160S	1.60	>1.50 GHz				
GL1L5MS170S	1.70					
GL1L5MS180S	1.80					
GL1L5MS190S	1.90					
GL1L5MS200S	2.00					
GL1L5MS210s	2.10					<3.0 ohm
GL1L5MS220S	2.20					
GL1L5MS230S	2.30					
GL1L5MS240S	2.40					
GL1L5MS250S	2.50	>1.00 GHz		<600 ps	<600 ps	
GL1L5MS260S	2.60					
GL1L5MS270S	2.70					
GL1L5MS280S	2.80					
GL1L5MS290S	2.90					
GL1L5MS300S	3.00					
GL1L5MS310S	3.10					<4.0 ohm
GL1L5MS320S	3.20					
GL1L5MS330S	3.30					
GL1L5MS340S	3.40					
GL1L5MS350S	3.50					
GL1L5MS360S	3.60					
GL1L5MS370S	3.70					
GL1L5MS380S	3.80	>0.75 GHz				
GL1L5MS390S	3.90					
GL1L5MS400S	4.00					
GL1L5MS410S	4.10					
GL1L5MS420S	4.20					
GL1L5MS430S	4.30					
GL1L5MS440S	4.40					<5.0 ohm
GL1L5MS450S	4.50					
GL1L5MS460S	4.60	>0.50 GHz				
GL1L5MS470S	4.70					
GL1L5MS480S	4.80					
GL1L5MS490S	4.90					
GL1L5MS500S	5.00					

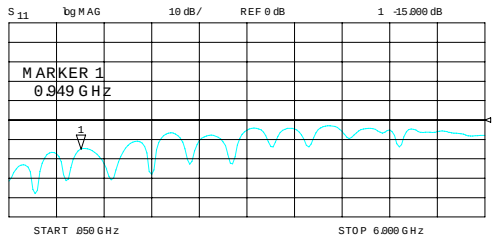
GL1 SERIES DELAY LINES

GL1L5 ** *** S

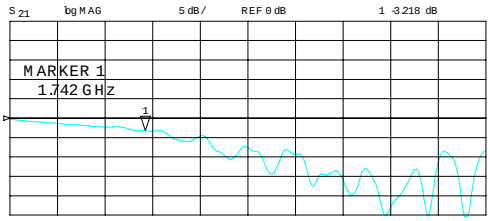
U.S. Patent 5,365,203

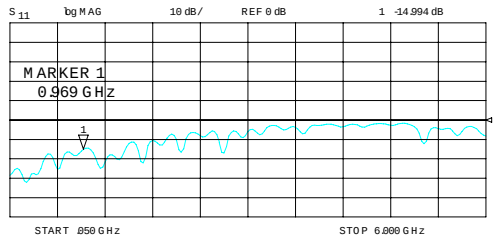
GL1L5LS100S *1 NS*



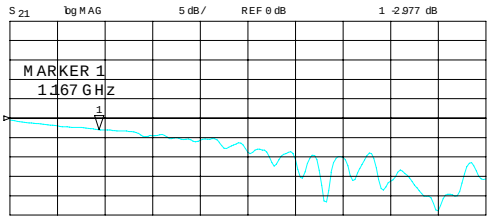


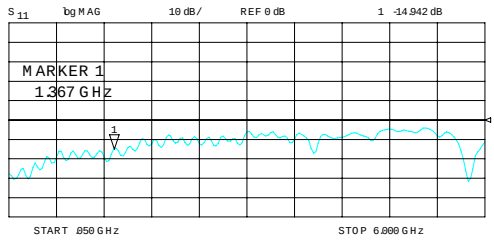
GL1L5MS200S *2 NS*



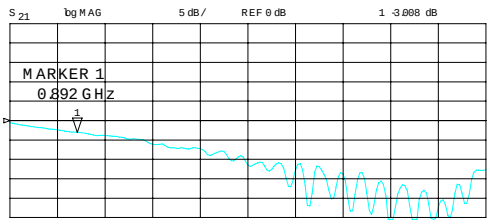


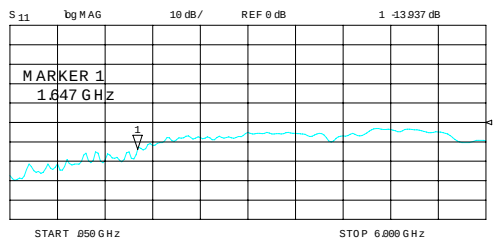
GL1L5MS300S *3 NS*



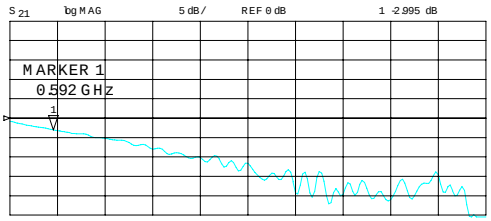


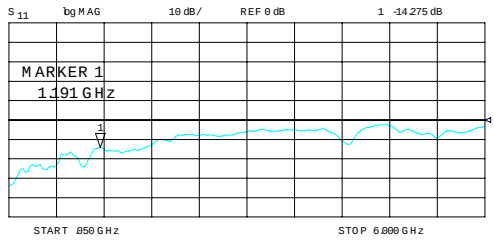
GL1L5MS400S *4 NS*





GL1L5MS500S *5 NS*





Characterization data is typical for this series of delay lines.

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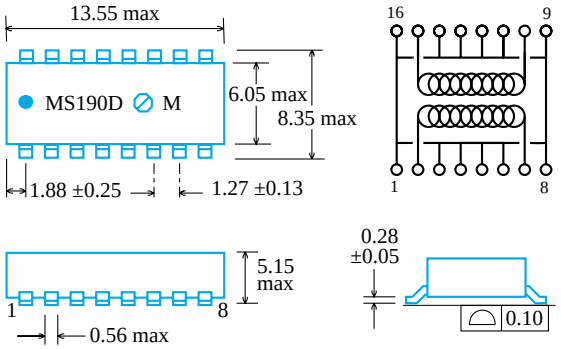
GL2 SERIES DELAY LINES

GL2L5 ** ***D

U.S. Patent 5,815,050



dimension mm

Application note: apply to Positive Emitter Coupled Logic (PECL) or other differentially driven circuits to produce a precisely cotrolled clock distribution network (see page 17).

GL2L5 SERIES 50 ohm

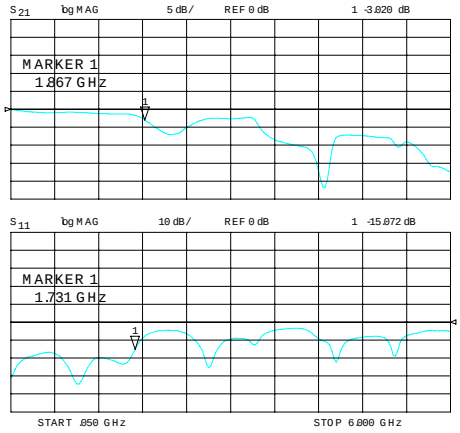
P/N	Td (ns)	Insertion Loss (-3 dB)	Return Loss (15 dB)	Tro	Tfo	DCRV
GL2L5LS050D	0.50	>1.80 GHz	>0.60 GHz	<400 ps	<400 ps	<1.0 ohm
GL2L5LS100D	1.00					
GL2L5MS150D	1.50	>0.80 GHz				<2.0 ohm
GL2L5MS200D	2.00					
GL2L5MS250D	2.50	>0.45 GHz				<3.0 ohm
GL2L5MS300D	3.00			<800 ps	<800 ps	
GL2L5MS350D	3.50					<4.0 ohm
GL2L5MS400D	4.00	>0.25 GHz				
GL2L5MS450D	4.50					<5.0 ohm

GL2 SERIES DELAY LINES

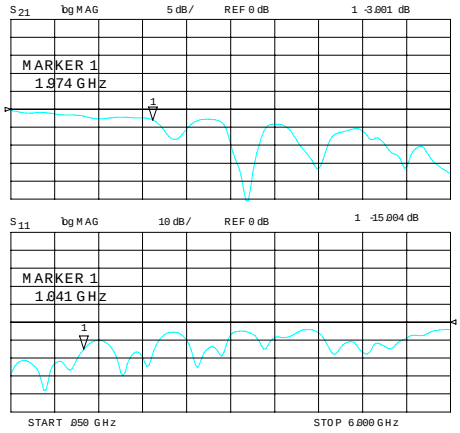
GL2L5 ** ***D

U.S. Patent 5,815,050

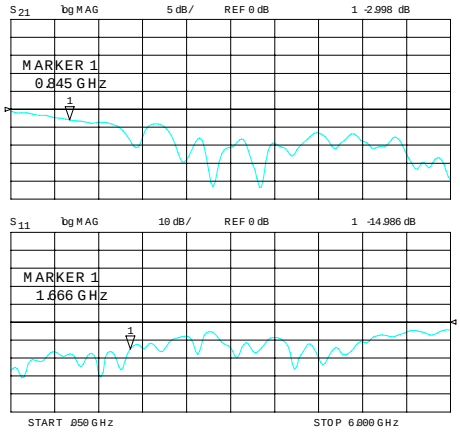
GL2L5LS050D *0.5 NS*



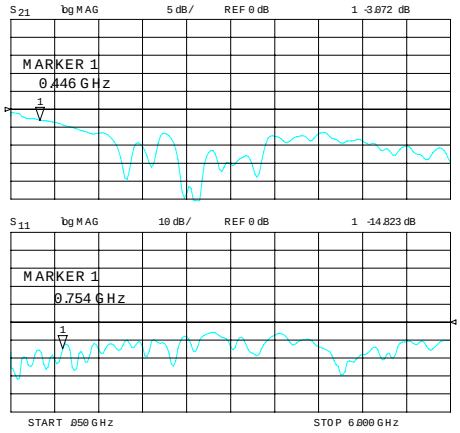
GL2L5LS100D *1 NS*



GL2L5MS200D 2 *NS*



GL2L5MS300D *3 NS*



Characterization data is typical for this series of delay lines.

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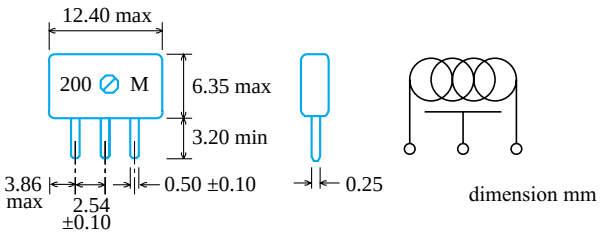
DS SERIES DELAY LINES

DS1L5 ** *** S

U.S. Patent 4,641,113



Application note: Use the DS delay lines in series with the GL2 delay line during board prototype to define the required timing delay.

DS1L5 SERIES 50 ohm

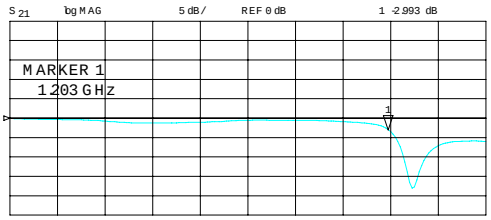
P/N	Td (ns)	Insertion Loss GHz (-3 dB)	Return Loss GHz (15 dB)	Tro (ns)	Tfo (ns)	DCRV (ohm)
DS1L5DJ010S	0.10	>1.000	>1.000			<0.10
DS1L5DJ020S	0.20	0.900	0.750			0.20
DS1L5DJ030S	0.30	0.700	0.650			0.30
DS1L5DJ040S	0.40	0.650	0.475	<0.50	<0.50	0.40
DS1L5DJ050S	0.50	0.600	0.450			0.50
DS1L5DJ060S	0.60	0.550	0.375			0.60
DS1L5DJ070S	0.70	0.500	0.350			0.70
DS1L5DJ080S	0.80	0.500	0.300			0.80
DS1L5DJ090S	0.90	1.200		0.50	0.50	
DS1L5DJ100S	1.00	1.100	0.300	0.55	0.55	0.25
DS1L5DJ110S	1.10	1.000		0.60	0.60	
DS1L5DJ120S	1.20	1.000		0.65	0.65	
DS1L5DJ130S	1.30	0.950	0.275	0.70	0.70	0.30
DS1L5DJ140S	1.40	0.900		0.75	0.75	
DS1L5DJ150S	1.50	0.850		0.80	0.80	
DS1L5DJ160S	1.60	0.800		0.85	0.85	0.50
DS1L5DJ170S	1.70	0.750	0.250	0.90	0.90	
DS1L5DJ180S	1.80	0.700		0.95	0.95	
DS1L5DJ190S	1.90	0.650		1.00	1.00	0.70
DS1L5DJ200S	2.00	0.600	0.550	1.05	1.05	
DS1L5DJ225S	2.25	0.550	0.500	1.10	1.10	
DS1L5DJ250S	2.50	0.500	0.450	1.25	1.25	
DS1L5DJ275S	2.75	0.450	0.400	1.35	1.35	1.00
DS1L5DJ300S	3.00	0.400	0.300	1.45	1.45	
DS1L5DJ325S	3.25	0.550				1.10
DS1L5DJ350S	3.50			1.00	1.00	1.20
DS1L5DJ375S	3.75	0.450	0.250			1.30
DS1L5DJ400S	4.00					1.40
DS1L5DJ425S	4.25	0.425				1.50
DS1L5DJ450S	4.50			1.10	1.10	1.60
DS1L5DJ475S	4.75	0.400				1.70
DS1L5DJ500S	5.00		0.225			1.80
DS1L5VJ550S	5.50	0.375				2.00
DS1L5VJ600S	6.00	0.350		1.15	1.15	2.20

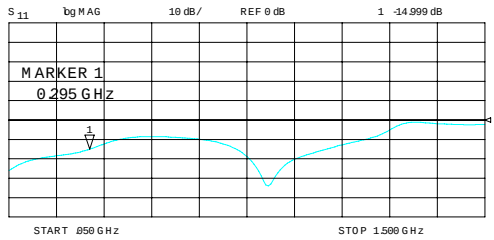
DS SERIES DELAY LINES

DS1L5 ** *** S

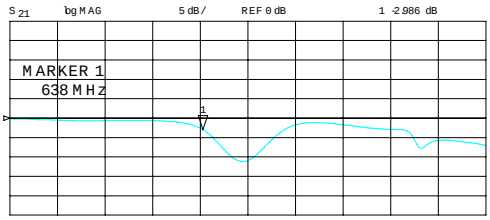
U.S. Patent 4,641,113

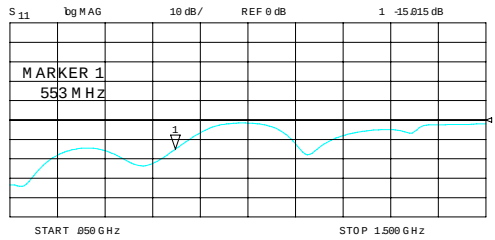
DS1L5DJ100S *1 NS*



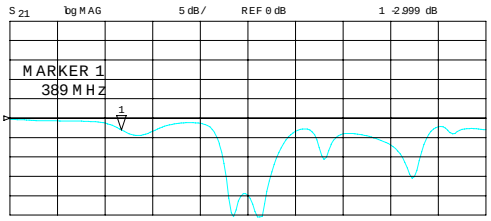


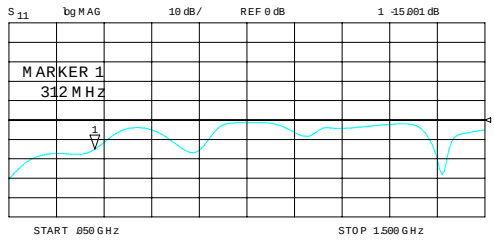
DS1L5DJ200S *2 NS*



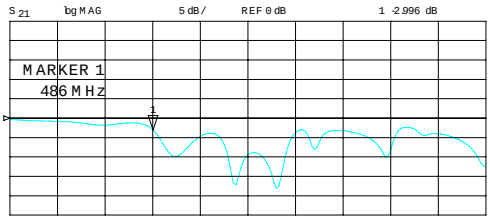


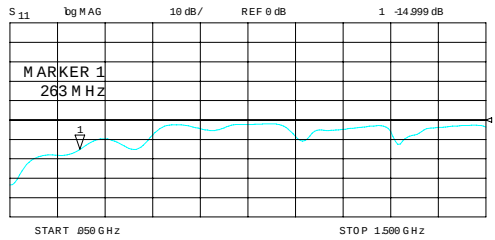
DS1L5DJ300S *3 NS*



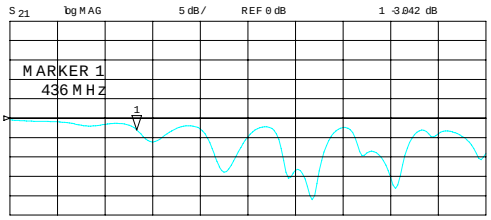


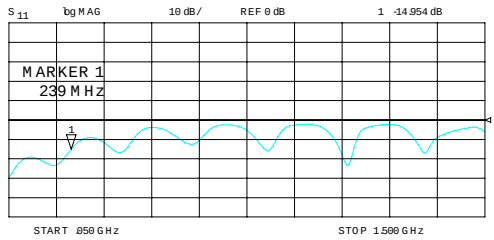
DS1L5DJ400S *4 NS*





DS1L5DJ500S *5 NS*





Characterization data is typical for this series of delay lines.

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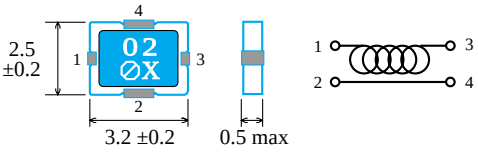
CL SERIES DELAY LINES

CL1L52H*** S

U.S. Patent 5,808,241

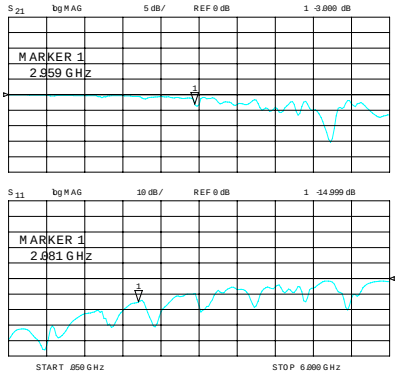


Application note: Use for ultra-precise delay adjustments where circuit trace is nearly adequate on the smallest of boards. Use for phase-locked loop timing schemes.

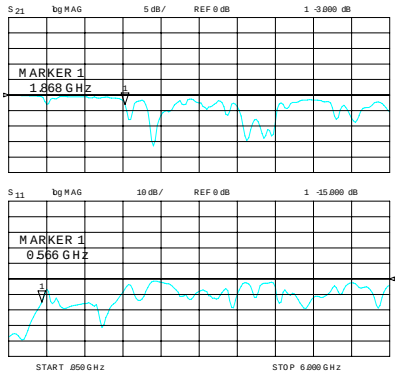
CL1L5 SERIES 50 ohm

P/N	Td (ps)	Insertion Loss GHz(-3 dB)	Return Loss GHz(15 dB)	Tro (ps)	Tfo (ps)	DCRV (ohm)
CL1L52H002S	20	2.4	0.600	<10	<10	<0.30
CL1L52H004S	40	2.3				
CL1L52H006S	60	2.2				
CL1L52H008S	80	2.1				
CL1L52H010S	100	2.0				
CL1L52H012S	120	1.9		20	20	0.60
CL1L52H014S	140	1.8				
CL1L52H016S	160	1.7				
CL1L52H018S	180	1.6				
CL1L52H020S	200	1.5				

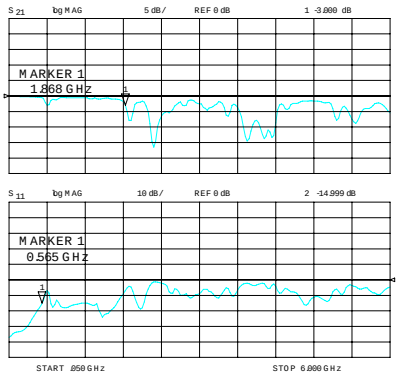
CL1L52H002S *0.02 NS*



CL1L52H016S *0.16 NS*



CL1L52H020S *0.20 NS*



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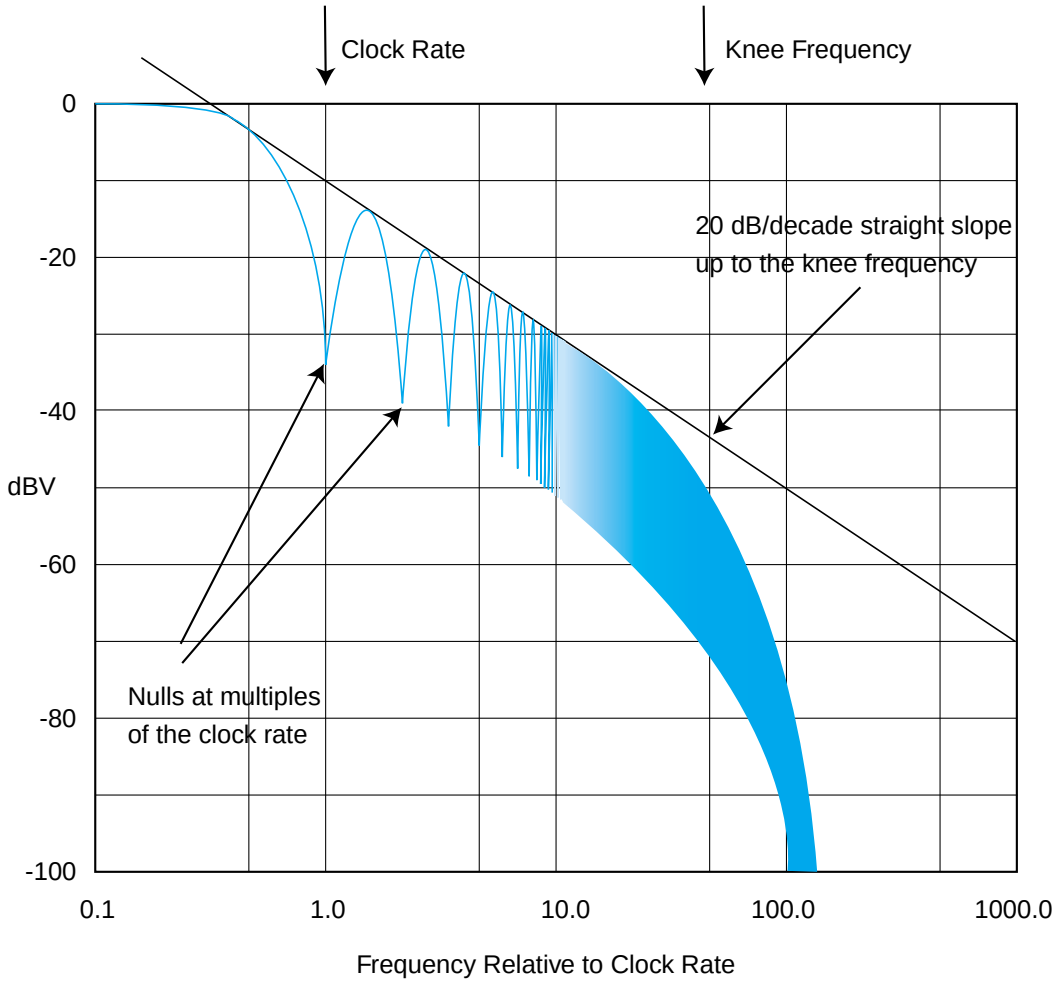
BANDWIDTH CONSIDERATIONS

High frequency signals with fast rise and fall times can push circuit elements to their limit in high speed digital design. Below illustrates what happens in the relationship between a random digital pulse train and the important part of the frequency spectrum when an output is flip-flop clocked at a rate of F_{clock} with a risetime T_r that is 1% of the clock period.



The plotted spectral power density displays nulls at multiples of the clock rate and an overall -20dB/decade slope from F_{clock} up to F_{knee}, where the roll off is faster. The knee frequency for a digital signal is related to the rise and fall times, not the clock rate:

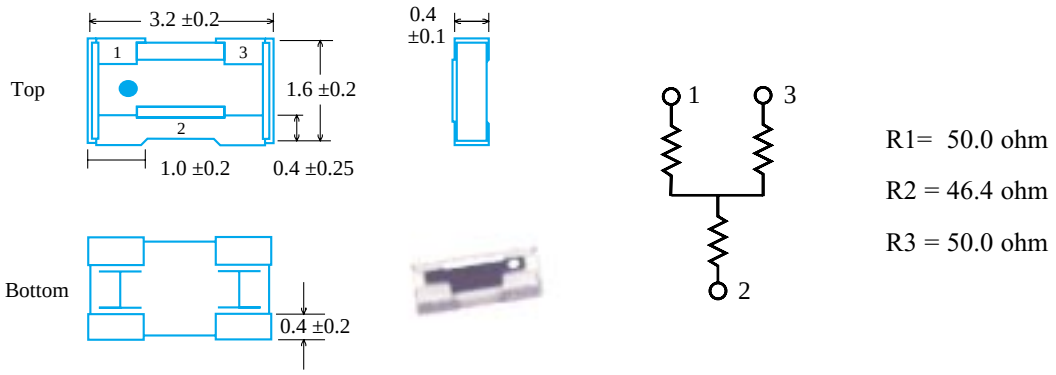
$$F_{knee} = \frac{0.5}{Tr},$$

F_{knee} = the frequency which most energy in digital pulses concentrates

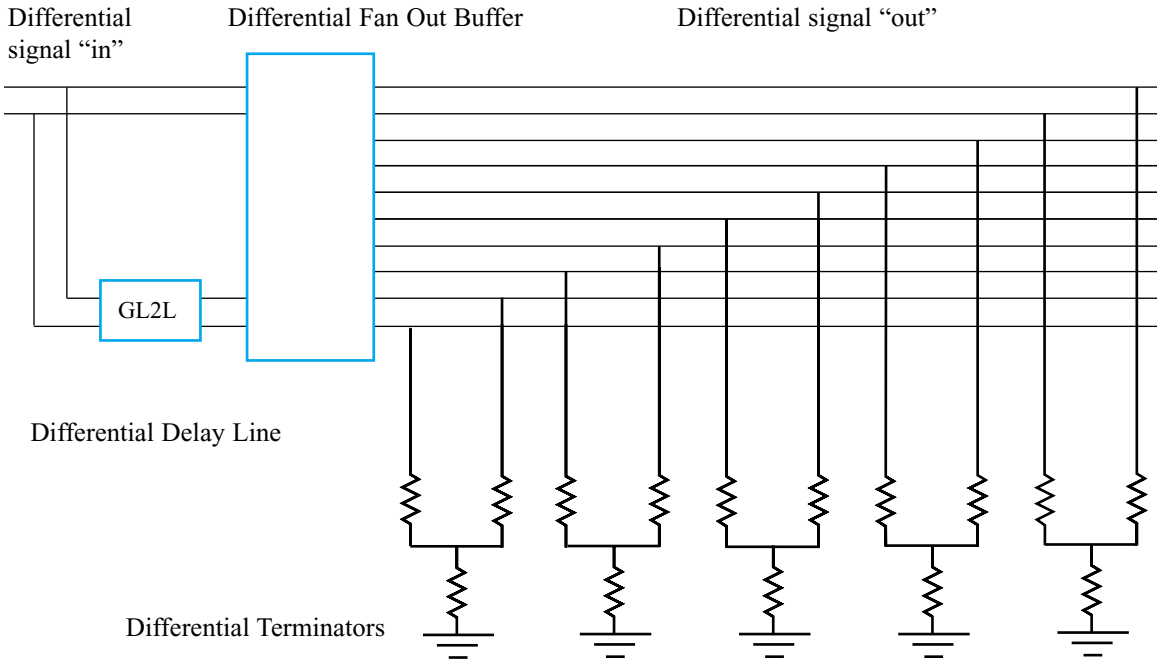
T_r = pulse rise time

COMPLIMENTARY PRODUCT Differential Terminator

RN1632N1DNC



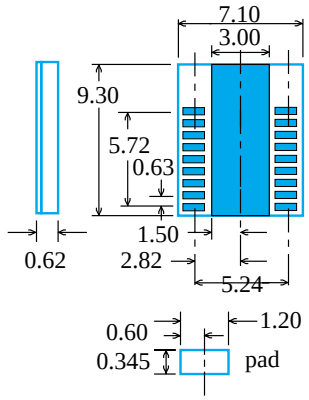
This standard 1206 size chip resistor network is popular for Positive Emitter Coupled Logic (PECL) applications as a terminator. Because this single chip contains three resistors, it reduces pick and place actions from three to one.



Clock Distribution Network Example Using GL2L Delay Line and RN1632 Terminators

COMPLIMENTARY PRODUCTS

SLOT sets
PSKT***N*



Typical high frequency calibration routines call for a series of nulling procedures that use electrical shorts, opens, loads, and throughs that are connected to the cable ends that feed the test instrument. These will effectively null out undesired matching, loading, frequency response, etc., of the test system to the cable ends. However, the Device Under Test (DUT) requires a socket or fixture to mate with the cable connector. The actual measurement taken includes both the DUT *and* the test fixture.

The PSKT***N* series calibration standards are for de-embedding the test fixture effects in these high speed measurements, because the calibration routine is performed at the test fixture. Essentially a custom set of products containing an electrical short, open, load, and through, specifically designed for the targeted schematic, these are used during the calibration routine with a network analyzer or other high speed test equipment. The end result is that the device under test performance is more accurate.

Available in SIP and DIP form factors, these calibration standards have gold finished electrodes and are intended for surface mount applications.

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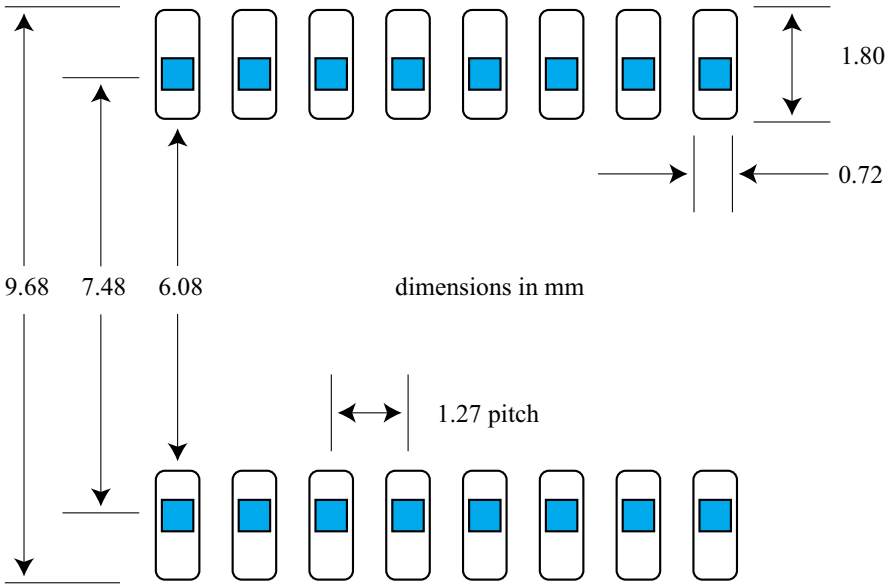
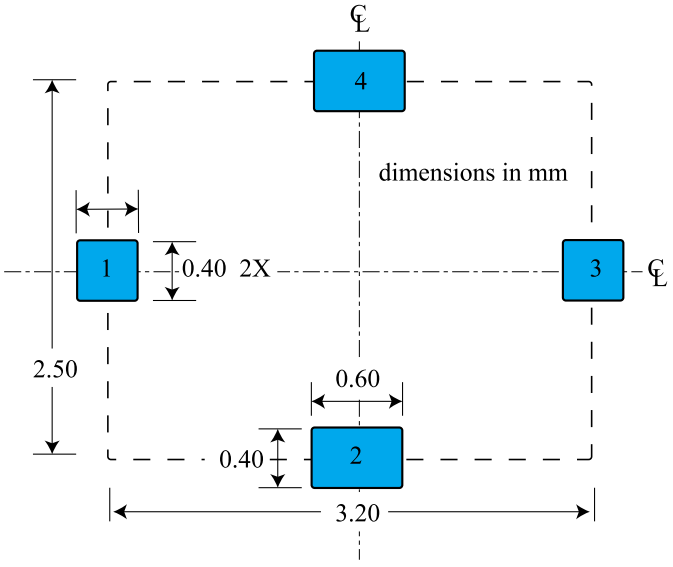
FOOTPRINT LAYOUTS

GL1L and GL2L SERIES



CL1L SERIES



The above land dimensions are suggested for the surface mount products GL1L/GL2L and CL1L series delay lines. Optimized geometries will vary depending on assembly process parameters. Since each assembly engineer is familiar with character unique to their process, these dimensions are a starting point, not to be recognized as a definitive solution.

Thin Film Technology Corp.

Because *Timing is Everything.*[tm]

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