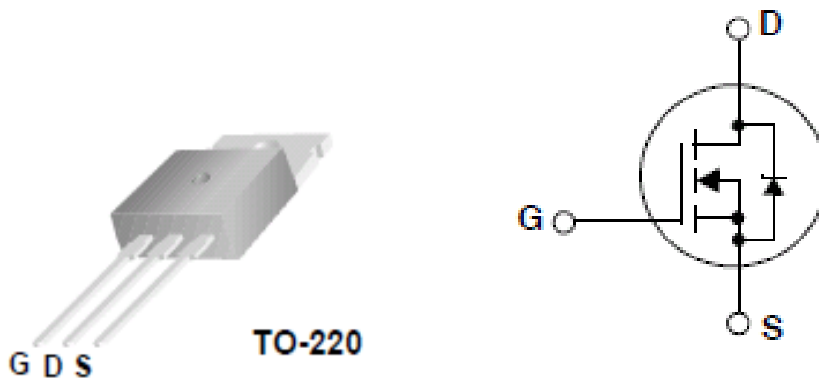


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	GFP 75N08

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General description

- These N-channel enhancement mode power field effect Transistors are produced using planar stripe DMOS technology.
- This advanced technology has been especially tailored to minimize on-state resistance and gate charge. It is well suited for high-frequency isolated DC-DC converters for telecom and computer applications. It is also intended for any applications with low gate drive requirements



Absolute maximum ratings $T=25^{\circ}\text{C}$ unless otherwise noted

Characteristics	Symbol	Value	Units
Drain-Source Voltage	BV_{DSS}	75	V
Drain Current	I_D	75	A
Gate-Source Voltage	V_{GS}	± 20	V
Single Pulsed Avalanche Energy	E_{AS}	680	mJ
Power Dissipation	P_D	300	W
Operating and Storage Temperature Range	T_{STG}	-55 –150	$^{\circ}\text{C}$
Thermal Resistance ,Junction-to Case	$R_{\theta JC}$	1.67	$^{\circ}\text{C}/\text{W}$
Drain-source Diode Forward Voltage	V_{SD}	1.4	V

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Parameter	Symbol	Min	Typ.	Max	Units	Test conditions
Gate threshold voltage	$V_{GS(th)}$	2.0	-	4.0	V	$V_{DS}=V_{GS}$ $I_D=250\mu A$
Gate-Body leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V$, $V_{DS}=0V$
Zero Gate voltage Drain current	I_{DSS}	-	-	10	μA	$V_{DS}=75V$, $V_{GS}=0V$
Static drain-source on-resistance	$R_{DS(on)}$	-	10	13	Ω	$V_{GS}=10V$, $I_D=37.5A$
Input capacitance	C_{iss}	-	3900	-	pF	$V_{GS}=0V$, $V_{DS}=25V$, $F=1.0MHz$
Output capacitance	C_{oss}	-	660	-		
Reverse transfer capacitance	C_{rss}	-	210	-		
Turn-on delay time	$t_d(on)$	-	27	-	ns	$V_{DD}=40V$, $I_D=37.5A$, $R_G=4.7\Omega$ $V_{GS}=10V$
Turn-on rise time	t_r	-	100	-		
Turn-off delay time	$t_d(off)$	-	75	-		
Turn-off fall time	t_f	-	25	-		
Total Gate charge	Q_g	-	110	130	nC	$V_{DS}=60V$, $V_{GS}=10V$, $I_D=75A$,
Gate-source charge	Q_{gs}	-	24	-		
Gate-drain charge	Q_{gd}	-	42	-		