

GD54/74LS155

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

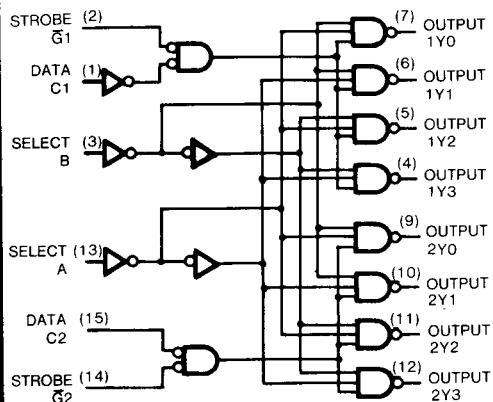
Features

- Applications:
 - Dual 2-to-4-line decoder
 - Dual 1-to-4-line demultiplexer
 - 3-to-8-line decoder
 - 1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design

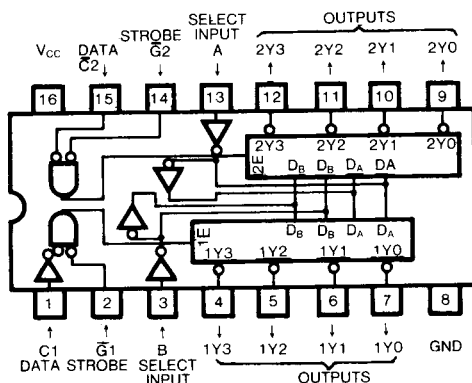
Description

These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at $\overline{C2}$ is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexers, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Functional Block Diagram



Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package

Function Tables

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Select		Inputs		Outputs			
B	A	Strobe G1	Data C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	L	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Select		Inputs		Outputs			
B	A	Strobe G2	Data C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	L	L	H	H
H	L	L	L	L	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Select		Inputs		Outputs							
C*	B A	Strobe Or Data G**		(0) 2Y0	(1) 2Y1	(2) 2Y2	(3) 2Y3	(4) 1Y0	(5) 1Y1	(6) 1Y2	(7) 1Y3
X	X X	H	H	H	H	H	H	H	H	H	H
L	L L	L	L	L	H	H	H	H	H	H	H
L	L H	L	L	L	L	H	H	H	H	H	H
L	H L	L	L	L	H	L	H	H	H	H	H
L	H H	L	L	L	H	H	L	H	H	H	H
H	L L	L	L	H	H	L	H	L	H	H	H
H	L H	L	L	H	H	H	L	L	H	H	H
H	H L	L	L	H	H	H	H	L	L	H	H
H	H H	L	L	H	H	H	H	H	L	L	H

C* = inputs C1 and C2 connected together
 G** = inputs G1 and G2 connected together
 H = high level L = low level X = don't care

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Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS -55°C to 125°C
74LS 0°C to 70°C
- Storage temperature range -65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5		5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54, 74			-400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	-55		125	$^{\circ}\text{C}$
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.7	V
			74			0.8	
V_{IK}	Input clamp voltage	$V_{CC} = \text{Min}$, $I_I = -18\text{mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$, $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	$V_{CC} = \text{Min}$, $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	$I_{OL} = 4\text{mA}$	54, 74	0.25	0.4	V
			$I_{OL} = 8\text{mA}$	74	0.35	0.5	
I_I	Input current at maximum input voltage	$V_{CC} = \text{Max}$, $V_I = 7\text{V}$				0.1	mA
I_{IH}	High-level input current	$V_{CC} = \text{Max}$, $V_I = 2.7\text{V}$				20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{Max}$, $V_I = 0.4\text{V}$				-0.4	mA
I_{OS}	Short-circuit output current	$V_{CC} = \text{Max}$ (Note 2)	54	-20		-100	mA
			74	-20		-100	
I_{CC}	Supply current	$V_{CC} = \text{Max}$ (Note 3)			6.1	10	mA

Note 1: All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and $\overline{C}2$, $\overline{G}1$, and $\overline{G}2$ inputs grounded.

Switching Characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	54LS155 74LS155			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, $\bar{C}2$ $\bar{G}1$ or $\bar{G}2$	Y	2	$C_L = 15pF$, $R_L = 2k\Omega$, See Note 4	10	15		ns
t_{PHL}	A, B, $\bar{C}2$ $\bar{G}1$ or $\bar{G}2$	Y	2		19	30		ns
t_{PLH}	A or B	Y	3		17	26		ns
t_{PHL}	A or B	Y	3		19	30		ns
t_{PLH}	C1	Y	3		18	27		ns
t_{PHL}	C1	Y	3		18	27		ns

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

Application Example**4-PHASE CLOCK PULSE GENERATOR**