

# GD3160

## Advanced IGBT/SiC gate driver

Rev. 13 — 6 May 2024

Product data sheet

### 1 General description

---

The GD3160 is an advanced, single-channel gate driver for IGBTs and SiC power devices. Integrated Galvanic isolation and low on-resistance drive transistors provide high charging and discharging current, low dynamic saturation voltage and rail-to-rail gate voltage control.

Current and temperature sense minimizes IGBT/SiC stress during faults. Accurate and configurable undervoltage lockout (UVLO) provides protection while ensuring sufficient gate-drive voltage headroom.

The GD3160 autonomously manages severe faults and reports faults and status via INTB and/or INTA pins and an SPI interface. It is capable of directly driving gates of most IGBTs and SiC MOSFETs. Self test, control, and protection functions are included for design of high-reliability systems (ASIL C/D). The GD3160 meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.



## 2 Features and benefits

This section summarizes the key features, safety features, and regulatory approvals for the GD3160.

### 2.1 Key features

- Integrated Galvanic signal isolation (up to 8 kV)
- High gate current integrated: 15 A source/sink capable
- SPI interface for safety monitoring, configuration, and diagnostic reporting
- Supports high switching frequencies: PWM up to 100 kHz
- Fail-safe state management from LV and HV domain for user-selectable safe state
- Programmable gate voltage regulator
- Temperature sense compatible with diode-based temperature sensors, NTC and PTC thermistors
- Configurable desaturation and current sense optimized for protecting SiC and IGBTs
- Integrated soft shutdown, two-level turn-off, optimized for unique gate drive requirements of SiC
- Real-time VCE and VGE reporting via INTA pin
- Integrated ADC for monitoring parameters from HV domain
- CMTI > 100 V/ns
- Compatible with 200 to 1700 V IGBT/SiC, power range > 125 kW
- Operating temperature range -40 to 125 °C
- Available in 5.0 or 3.3 V logic interface variants
- Small package footprint (10 mm x 11 mm) 32-pin SOIC

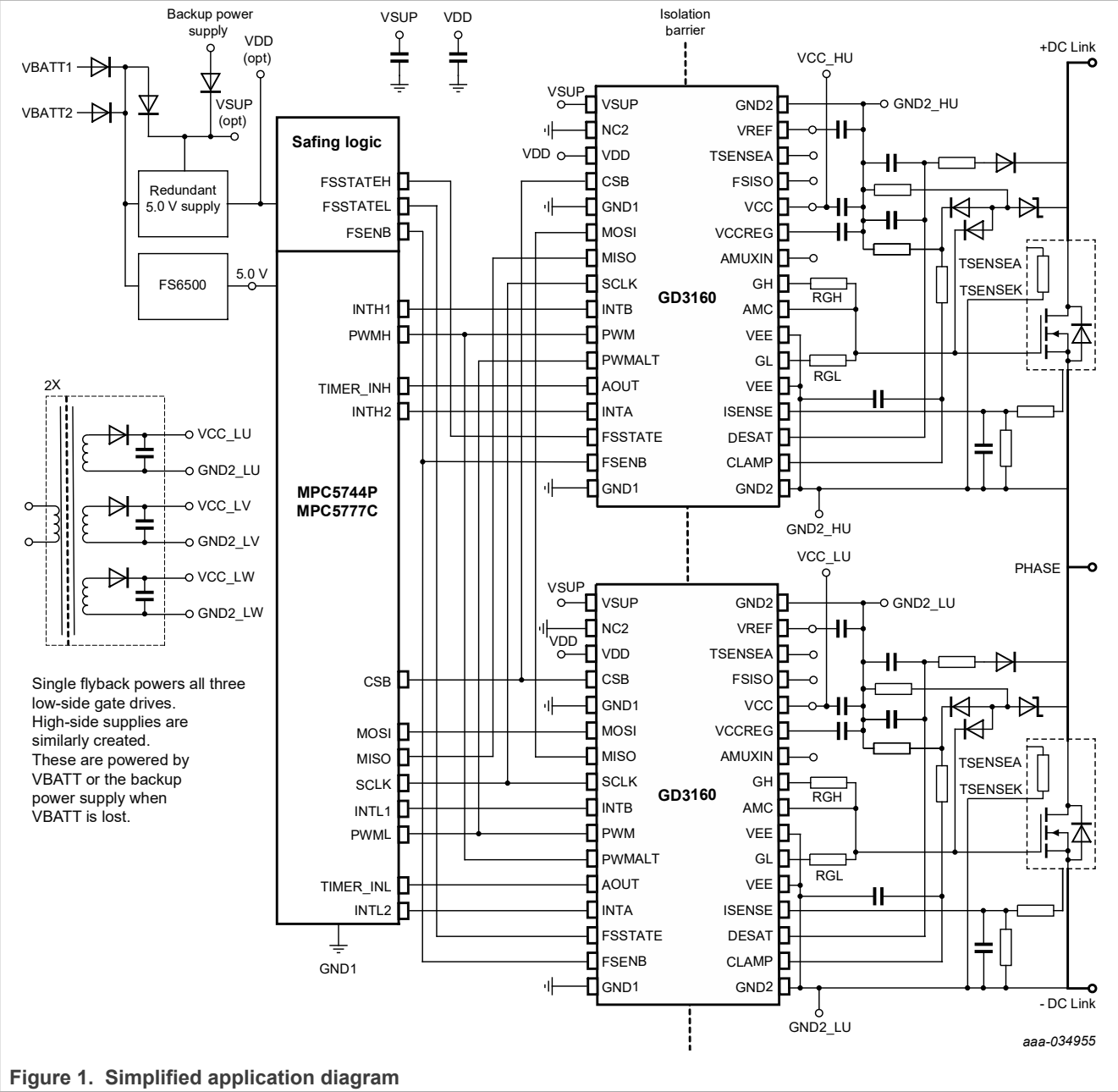
### 2.2 Safety features

- Certified compliant with ISO 26262, supporting ASIL D level functional safety
- Error checking of SPI and configuration data with 8-bit CRC
- Autonomously manages severe faults and reports status via configurable INTB and/or INTA pins, and SPI interface
- Current, DESAT, and temperature sense inputs and ADC reporting for IGBT/SiC monitoring and protection
- Interrupt pins (INTA and INTB) for fast response to faults
- Built-in self-check of all analog and digital circuits
- Continuous watchdog of communications across isolation barrier
- Deadtime enforcement
- Over- and undervoltage supervision of all power supplies on both low- and high-voltage sides
- Dedicated fail-safe state management pins on both low- and high-voltage sides
- VGE real-time cycle-by-cycle monitoring

### 2.3 Safety and regulatory approvals

- Reinforced isolation per DIN V VDE V 0884-10
- Withstand 5000 V rms (1 minute) isolation per UL 1577
- AEC-Q100 grade 1 automotive qualified

3 Simplified application diagram



## 4 Applications

---

- SiC gate driver
- IGBT gate driver
- DC/DC power converter
- Automotive traction inverter

5 Ordering information

Table 1. Orderable part variations

| Part number <sup>[1]</sup> | VDD   | External clearance and creepage distance <sup>[2]</sup> | Material (isolation) group <sup>[3]</sup> | FSISO option (Gate state when FSISO is activated) | Temperature (T <sub>J</sub> ) | Package                              |
|----------------------------|-------|---|---|---|-------------------------------|--------------------------------------|
| MGD3160AM515EK             | 5.0 V | > 7.72 mm   | II  | Gate ON   | -40 °C to 150 °C              | 32-pin wide body SOIC, 0.65 mm pitch |
| MGD3160AM518EK             | 5.0 V | > 8.0 mm  | I   | Gate ON   |                               |                                      |
| MGD3160AM535EK             | 5.0 V | > 7.72 mm   | II  | Gate 3-STATE                                      |                               |                                      |
| MGD3160AM538EK             | 5.0 V | > 8.0 mm  | I   | Gate 3-STATE                                      |                               |                                      |
| MGD3160AM315EK             | 3.3 V | > 7.72 mm   | II  | Gate ON   |                               |                                      |
| MGD3160AM318EK             | 3.3V  | > 8.0 mm  | I   | Gate ON   |                               |                                      |
| MGD3160AM335EK             | 3.3 V | > 7.72 mm   | II  | Gate 3-STATE                                      |                               |                                      |
| MGD3160AM338EK             | 3.3 V | > 8.0 mm  | I   | Gate 3-STATE                                      |                               |                                      |

[1] To order parts in tape and reel, add the R2 suffix to the part number. To order parts in tray packing, add the T suffix to the part number.  
[2] per IEC 60950-1 Tables 2K and 2N  
[3] per IEC 60664-1

6 Internal block diagram

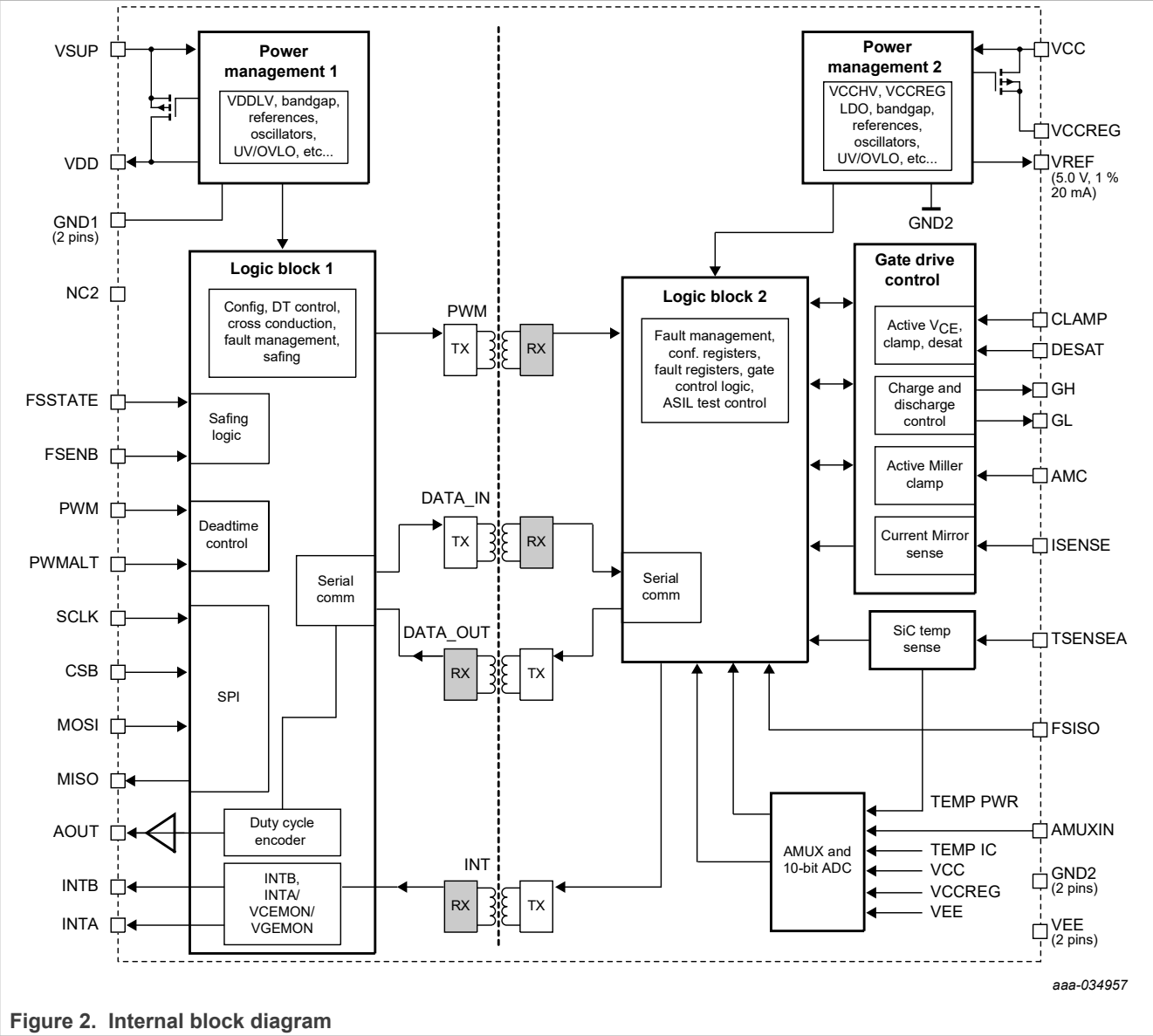
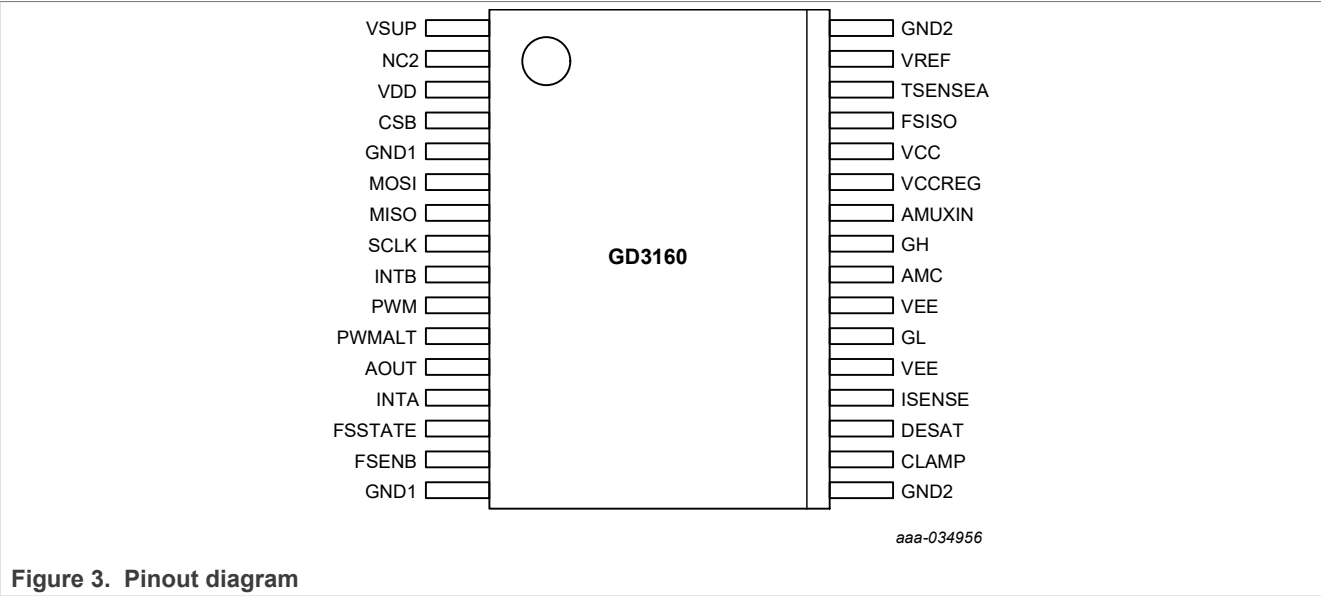


Figure 2. Internal block diagram

7 Pinning information

7.1 Pinning



7.2 Pin description

Table 2. Pin definitions

| Pin number                                    | Pin name | Pin type           | Definition   | Comments   |
|---|----------|--------------------|--|--|
| Pins 1 to 16 (low-voltage, non-isolated pins) |          |                    |  |  |
| 1   | VSUP     | Input/power        | Primary power supply for non-isolated low-voltage (LV) domain. | Main supply input is compatible with 12 V automotive battery range/transients, referenced to GND1. VSUP may either be (1) driven by 12V, or (2) tied to VDD and powered by an external, post-regulated 5 V supply. |
| 2   | NC2      | No connect         | No connection.   | NC2 must be connected to GND1.   |
| 3   | VDD      | Input-output/power | Power supply for non-isolated low-voltage (LV) logic.          | Main supply for logic on LV domain, referenced to GND1. VDD may either be (1) regulated internally to 3.3 V or 5.0 V from VSUP, or (2) tied to VSUP and powered by an external, post-regulated 5 V supply.         |
| 4   | CSB      | Input/digital      | SPI chip select.   | Active low CSB activates SPI link and framing.   |
| 5, 16   | GND1     | Ground 1           | Ground for non-isolated (LV) domain power and logic.           | Redundant GND1 pins provide ground reference for all non-isolated low-voltage (LV) domain signals. Isolated from all circuitry referenced to GND2.   |
| 6   | MOSI     | Input/digital      | SPI MOSI pin.  | Input data for GD3160 SPI. MOSI data latches on rising edge of SCLK, MSB first. Internal passive pulldown to GND1.   |
| 7   | MISO     | Output/digital     | SPI MISO pin.  | Data output for GD3160 SPI. GD3160 outputs MISO on falling edge of SCLK, MSB first.  |
| 8   | SCLK     | Input/digital      | SPI clock.   | GD3160 acknowledges SPI clock only when CSB is low. Internal passive pulldown to GND1.   |
| 9   | INTB     | Output/Digital     | Interrupt/Fault status output.                                 | INTB reports fault with active low (logic 0 reports fault). Internal passive pullup to VDD.  |
| 10  | PWM      | Input/digital      | PWM control command for gate output.                           | Logic high turns on power device gate. PWM pin is ignored during fail-safe, configuration, BIST, reset, and most fault modes. Internal passive pull down to GND1.  |
| 11  | PWMALT   | Input/digital      | Complementary PWM command for gate output.                     | Complementary PWMALT enforces deadtime constraint and prevents accidental shoot-through condition. Connect to GND1 if unused. Internal passive pull up to VDD.   |
| 12  | AOUT     | Output/analog      | Duty-cycle encoded output of isolated ADC.                     | 5.0 V, 3.9 kHz (or multiplexed with 5.6 kHz) readout is configurable by SPI. Pin left open if unused.  |

Table 2. Pin definitions...continued

| Pin number   | Pin name | Pin type            | Definition  | Comments   |
|--|----------|---------------------|---|--|
| 13   | INTA     | Output/digital      | Interrupt/fault status/monitor.   | Output pin reports fault via active pulldown interrupt, or reports VCE or VGE state via logic high/low. Pullup pin to VDD with a 50 kΩ resistor or left open if unused.  |
| 14   | FSSTATE  | Input/digital       | Fail-safe gate state control pin.   | Gate output control pin. Connect to GND1 if unused. Internal passive pulldown to GND1.   |
| 15   | FSENB    | Input/digital       | Fail-safe mode enable pin.  | Active-low pin enabling Fail-Safe mode (FSSTATE controls gate). Internal passive pulldown to GND1. Connect to VDD if unused.   |
| <b>Pins 17 to 32 (high-voltage, isolated pins)</b> |          |                     |   |  |
| 17, 32   | GND2     | Ground 2            | Ground for isolated (HV) domain power, analog, and logic.                       | Redundant GND2 pins provide ground reference for all isolated high-voltage (HV) domain. Isolated from all circuitry referenced to GND1. Connect to power device emitter/source.  |
| 18   | CLAMP    | Input/analog        | Sense terminal for VCE/VDS overvoltage during turn-off.                         | CLAMP detects Zener breakdown current and increase gate drive impedance and employ soft shutdown for turn-off. Connect to VEE if unused.   |
| 19   | DESAT    | Input-output/analog | Drive/sense terminal for VCE/VDS desaturation condition.                        | Connected to GND2 if unused.   |
| 20   | ISENSE   | Input/analog        | Current sense feedback pin.   | Resistive network converts current mirror into readable voltage signal on ISENSE. Connect to GND2 if unused.   |
| 21, 23   | VEE      | Input/power         | Negative gate supply voltage.   | VEE is the negative voltage on the isolated domain, and is referenced to GND2. Connect to GND2 if a negative supply is not used.   |
| 22   | GL       | Output/analog       | Pulldown pin for output gate turn-off/discharge event.                          | GL pin pulls gate to VEE.  |
| 24   | AMC      | Input-output/analog | Direct connect to gate for gate voltage sense and active Miller clamp function. | AMC provides low-impedance holdoff (active Miller clamp) and senses VGE/VGS for reporting and diagnostics.   |
| 25   | GH       | Output/analog       | Pullup pin for output gate turn-on event.                                       | GH pin pulls gate to VCCREG.   |
| 26   | AMUXIN   | Input/analog        | General-purpose input for isolated ADC.   | One of many SPI-selectable inputs for the isolated ADC. Connect to GND2 if unused.   |
| 27   | VCCREG   | Output/power        | Internally-regulated positive gate supply.                                      | Programmable gate supply derived from VCC, referenced to GND2. Connect to VCC if unused.   |
| 28   | VCC      | Input/power         | Positive voltage supply for isolated domain circuitry.                          | Referenced to GND2.  |
| 29   | FSISO    | Input/digital       | HV domain pin to enable the Fail-safe state.                                    | Active-high disables PWM, FSSTATE, and, according to the part number, turns on gate (MGD3160AM515EK, MGD3160AM315EK, MGD3160AM518EK or MGD3160AM318EK) or 3-states GATE (MGD3160AM535EK, MGD3160AM335EK, MGD3160AM538EK or MGD3160AM338EK).  |
| 30   | TSENSEA  | Input/analog        | Anode of temp sense diode/NTC of the power module.                              | TSENSEA reads back voltage from temperature sense element, and is referenced to GND2. Includes possible current driver for temp sense network. The temperature sense network cathode should be connected to GND2. Connect to VREF if unused. |
| 31   | VREF     | Output/power        | Internally regulated reference voltage for HV domain analog, ADC, and logic.    | Output for an internally generated 5.0 V, 20 mA regulator. Referenced to GND2.   |

## 8 Product characteristics

### 8.1 Range of functionality

**Table 3. Range of functionality**

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). Currents are positive into and negative out of the specified pins.

| Symbol  | Description (rating)   | Min  | Max  | Unit |
|---|--|------|------|------|
| T <sub>J</sub>  | Operating junction temperature   | −40  | 150  | °C   |
| f <sub>PWM</sub>  | PWM switching frequency  | 0    | 100  | kHz  |
| V <sub>VEE</sub>  | High-voltage domain negative supply voltage <sup>[1]</sup>   | −10  | 0.3  | V    |
| <b>VSUP not connected to VDD</b>  |  |      |      |      |
| V <sub>VSUP</sub>   | Low-voltage domain supply voltage, full performance (MGD3160AM515EK, MGD3160AM535EK, MGD3160AM518EK or MGD3160AM538EK 5.0 V option) <sup>[2]</sup> | 6    | 32   | V    |
|   | Low-voltage domain supply voltage, full performance (MGD3160AM315EK, MGD3160AM335EK, MGD3160AM318EK or MGD3160AM338EK 3.3 V option) <sup>[2]</sup> | 4.5  | 32   | V    |
| V <sub>VSUP_JS</sub>  | Low-voltage domain jump start voltage, 1 minute at 25 °C <sup>[3]</sup>  | —    | 28   | V    |
| V <sub>VSUP_LD</sub>  | Low-voltage domain load dump voltage, 400 ms at 25 °C <sup>[4]</sup><br><b>Note:</b> Load dump voltage test according to ISO16750-2 Test B         | —    | 40   | V    |
| <b>VSUP connected to VDD (MGD3160AM515EK, MGD3160AM535EK, MGD3160AM518EK or MGD3160AM538EK, 5.0 V option)</b> |  |      |      |      |
| V <sub>VDD</sub> , V <sub>VSUP</sub>  | Low-voltage domain supply voltage <sup>[5]</sup>   | 4.75 | 5.25 | V    |
| <b>VCC not connected to VCCREG</b>  |  |      |      |      |
| V <sub>VCC</sub>  | High-voltage domain positive supply voltage <sup>[1]</sup>   | —    | 25   | V    |
| V <sub>VCCREG</sub>   | High-voltage domain post regulated supply voltage <sup>[1]</sup>   | 9.3  | —    | V    |
| <b>VCC connected to VCCREG</b>  |  |      |      |      |
| V <sub>VCC</sub> , V <sub>VCCREG</sub>  | High-voltage domain positive supply voltage <sup>[1]</sup>   | 9.3  | 25   | V    |

[1] Ref = GND2

[2] Ref = GND1, VDD generated internally

[3] Jump start test according to ISO16750-2

[4] Load dump voltage test according to ISO16750-2 Test B

[5] Ref = GND1, VDD and VSUP connected, VDD generated externally

### 8.2 Absolute maximum ratings

All voltages are referenced to GND1 or GND2. Currents are positive into and negative out of the specified pins. Exceeding these ratings may cause malfunction or permanent device damage.

**Table 4. Absolute maximum ratings**

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). Currents are positive into and negative out of the specified pins.

| Symbol                                       | Description (Rating)  | Min  | Max | Unit |
|--|---|------|-----|------|
| <b>Power supplies and current references</b> |   |      |     |      |
| V <sub>VSUP</sub>                            | Low-voltage domain supply voltage <sup>[1]</sup>                      | −0.3 | 40  | V    |
| V <sub>VDD3p3</sub>                          | Low-voltage domain logic supply voltage, 3.3 V version <sup>[1]</sup> | −0.3 | 6.0 | V    |
| V <sub>VDD5</sub>                            | Low-voltage domain logic supply voltage, 5.0 V version <sup>[1]</sup> | −0.3 | 6.0 | V    |
| V <sub>VCC</sub>                             | High-voltage domain positive supply voltage <sup>[2]</sup>            | −0.3 | 25  | V    |
| V <sub>VEE</sub>                             | High-voltage domain negative supply voltage <sup>[2]</sup>            | −12  | 0.3 | V    |
| V <sub>VCC-VEE</sub>                         | High-voltage domain positive/negative supply                          | −0.3 | 37  | V    |
| V <sub>VCCREG</sub>                          | High-voltage domain post regulated supply voltage <sup>[2]</sup>      | −0.3 | 25  | V    |

**Table 4. Absolute maximum ratings...continued**

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). Currents are positive into and negative out of the specified pins.

| Symbol                          | Description (Rating)  | Min            | Max                         | Unit |
|---------------------------------|---|----------------|-----------------------------|------|
| $I_{VCCREG}$                    | VCCREG output current   | —              | −100                        | mA   |
| $V_{VREF}$                      | VREF voltage <sup>[2]</sup>   | −0.3           | 6.0                         | V    |
| $I_{VREF}$                      | VREF output current   | —              | −20                         | mA   |
| <b>Logic pins</b>               |   |                |                             |      |
| $V_{IN}$                        | Logic input pin voltage (FSSTATE, FSENb, PWM, PWMALT, SCLK, CSB, MOSI) <sup>[1]</sup> | −0.3           | 18                          | V    |
| $V_{OUT}$                       | Logic output pin voltage (MISO, INTB, INTA, AOUT) <sup>[1]</sup>                      | −0.3           | $V_{VDD} + 0.3\text{ V}$    | V    |
| $V_{INTB}$                      | INTB voltage <sup>[1]</sup>   | −0.3           | 6.3                         | V    |
| $V_{FSISO}$                     | Logic input pin voltage (FSISO) <sup>[2]</sup>  | −0.3           | 6.3                         | V    |
| <b>Gate drive output stage</b>  |   |                |                             |      |
| $V_{GH}$                        | GH voltage <sup>[2]</sup>   | $V_{EE} - 0.3$ | $V_{VCCREG} + 0.3\text{ V}$ | V    |
| $V_{GL}$                        | GL voltage <sup>[2]</sup>   | $V_{EE} - 0.3$ | $V_{VCCREG} + 0.3\text{ V}$ | V    |
| $V_{AMC}$                       | AMC voltage <sup>[2]</sup>  | $V_{EE} - 0.3$ | $V_{VCCREG} + 0.3\text{ V}$ | V    |
| $I_{SOURCEMAX}$                 | GH max. source current <sup>[3]</sup>   | —              | −15                         | A    |
| $I_{SINKMAX}$                   | GL, AMC max. sink current <sup>[3]</sup>  | —              | 15                          | A    |
| $V_{CLAMP}$                     | CLAMP voltage <sup>[2]</sup>  | $V_{EE} - 0.3$ | $V_{VCC} + 0.3\text{ V}$    | V    |
| $V_{DESAT}$                     | DESAT voltage <sup>[2]</sup>  | −0.3           | $V_{VCC} + 0.3\text{ V}$    | V    |
| <b>Temperature sense pin</b>    |   |                |                             |      |
| $V_{TSENSEA}$                   | TSENSEA voltage <sup>[2]</sup>  | −0.3           | 6.0                         | V    |
| <b>Interrupt pins</b>           |   |                |                             |      |
| $I_{INTA}$                      | Open drain DC output current <sup>[4]</sup>   | —              | −20                         | mA   |
| $I_{INTB}$                      | Open drain DC output current <sup>[4]</sup>   | —              | −20                         | mA   |
| <b>ISENSE sense pin</b>         |   |                |                             |      |
| $V_{ISENSE}$                    | ISENSE voltage <sup>[2]</sup>   | −2.0           | $V_{VCC} + 0.3\text{ V}$    | V    |
| <b>AMUXIN pin<sup>[5]</sup></b> |   |                |                             |      |
| $V_{AMUXIN}$                    | AMUXIN voltage <sup>[2]</sup>   | −0.3           | 6.0                         | V    |
| <b>ESD ratings</b>              |   |                |                             |      |
| $V_{ESDHBM}$                    | ESD voltage (HBM)<br>All pins <sup>[6]</sup>  | −2.0           | 2.0                         | kV   |
| $V_{ESDCDM}$                    | ESD voltage (CDM)<br>Corner pins<br>Other pins <sup>[7]</sup>                         | −750<br>−500   | 750<br>500                  | V    |
| $V_{ESDModule}$                 | ESD voltage (module level)<br>VSUP, GND1, GND2 pins <sup>[8]</sup>                    | −8.0           | 8.0                         | kV   |
| <b>Immunity</b>                 |   |                |                             |      |
| $dV_{ISO}/dt$                   | Common mode transient immunity <sup>[9]</sup>   | —              | 100                         | V/ns |
| <b>PWM frequency</b>            |   |                |                             |      |
| $f_{PWMMAX}$                    | Maximum switching frequency   | —              | 100                         | kHz  |

[1] Ref = GND1

[2] Ref = GND2

[3] 50 %, 100 nF, 10 kHz

[4]  $V_{INTB}, V_{INTA} < 1.0\text{ V}$

- [5] ADC performance is guaranteed by design up to 500 µA injected current on AMUXIN pin.
- [6] **Human Body Model (HBM) at device level**  
ANSI/ESDA/JEDEC JS-001: 2010 Model HBM (human body model)  
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)  
Test points: pin to GND1 and pin to GND2
- [7] **Charged Device Model (CDM)**  
ANSI/ESD S5.3.1-2009  
ESD Association Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Component Level
- [8] **Module Level ESD Tests**  
ISO 10605:2008/Cor. 1:2010(E)  
Road vehicles – Test methods for electrical disturbances from electrostatic discharge
- [9] Pulse width = 10 ns

8.3 Thermal characteristics

Table 5. Thermal ratings

Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol              | Description (rating)   | Min | Max | Unit |
|---------------------|--|-----|-----|------|
| Thermal ratings     |  |     |     |      |
| T <sub>J</sub>      | Operating junction temperature                                   | −40 | 150 | °C   |
| T <sub>STG</sub>    | Storage temperature  | −65 | 150 | °C   |
| T <sub>OTSDth</sub> | Overtemperature shutdown threshold of IC                         | 180 | 210 | °C   |
| T <sub>PPRT</sub>   | Peak package reflow temperature during reflow <sup>[1] [2]</sup> | —   | 260 | °C   |
| MSL                 | Moisture Sensitivity Level                                       | —   | 3   | —    |

- [1] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), contact NXP.
- [2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

Table 6. Thermal resistance characteristics

| Symbol                     | Description (rating)                                      | Min | Max | Unit |
|----------------------------|---|-----|-----|------|
| Thermal resistance ratings |   |     |     |      |
| R <sub>θJA</sub>           | Junction-to-Ambient thermal resistance <sup>[1] [2]</sup> | —   | 51  | °C/W |
| R <sub>θJB</sub>           | Junction-to-Board thermal resistance <sup>[3]</sup>       | —   | 34  | °C/W |

- [1] Per EIA/JESD51-2A Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
- [2] Per EIA/JESD51-7 High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- [3] JEDEC high-K thermal test board without thermal attachment.

## 8.4 Isolation and safety related specifications

**Table 7. Insulation specifications**

| Symbol  | Description (Rating)   | Value                          | Unit |
|---|--|--------------------------------|------|
| MGD3160AM515EK, MGD3160AM535EK, MGD3160AM315EK and MGD3160AM335EK |  |                                |      |
| CLR   | External clearance distance <sup>[1]</sup>   | > 7.72                         | mm   |
| CPG   | External creepage distance <sup>[2]</sup>  | > 7.72                         | mm   |
| DTI   | Internal clearance (Gap) distance through insulation   | > 80                           | µm   |
| CTI   | Comparative tracking index <sup>[3]</sup>  | > 400                          | V    |
| M <sub>Group</sub>  | Material (isolation) group <sup>[4]</sup>  | II                             | —    |
| IEC150<br>IEC300<br>IEC600  | Installation classification <sup>[5]</sup><br>Mains voltage ≤ 150 V <sub>RMS</sub><br>Mains voltage ≤ 300 V <sub>RMS</sub><br>Mains voltage ≤ 600 V <sub>RMS</sub> | I to IV<br>I to III<br>I to II | —    |
| MGD3160AM518EK, MGD3160AM538EK, MGD3160AM318EK and MGD3160AM338EK |  |                                |      |
| CLR   | External clearance distance <sup>[1]</sup>   | > 8.00                         | mm   |
| CPG   | External creepage distance <sup>[2]</sup>  | > 8.00                         | mm   |
| DTI   | Internal clearance (Gap) distance through insulation   | > 80                           | µm   |
| CTI   | Comparative tracking index <sup>[3]</sup>  | > 600                          | V    |
| M <sub>Group</sub>  | Material (isolation) group <sup>[4]</sup>  | I                              | —    |
| IEC150<br>IEC300<br>IEC600  | Installation classification <sup>[5]</sup><br>Mains voltage ≤ 150 V <sub>RMS</sub><br>Mains voltage ≤ 300 V <sub>RMS</sub><br>Mains voltage ≤ 600 V <sub>RMS</sub> | I to IV<br>I to III<br>I to II | —    |

[1] per IEC 60950-1 Table 2K

[2] per IEC 60950-1 Table 2N

[3] per DIN IEC 112/VDE 0303 Part 1

[4] per IEC 60664-1

[5] per IEC 60664-1 Table F.1

**Table 8. DIN V VDE 0884-10 (VDE V 0884-10) insulation characteristics**

| Symbol             | Description (Rating)   | Value             | Units            |
|--------------------|--|-------------------|------------------|
| CCLASS             | Climatic classification  | 40/125/21         | —                |
| PDEGREE            | Pollution degree   | 2                 | —                |
| V <sub>IORM</sub>  | Maximum repetitive peak isolation voltage                              | 1500              | V <sub>pk</sub>  |
| V <sub>IOWM</sub>  | Maximum working isolation voltage                                      | 1060              | V <sub>RMS</sub> |
| V <sub>IOTM</sub>  | Maximum transient isolation voltage <sup>[1]</sup>                     | 4000              | V <sub>pk</sub>  |
| V <sub>IOTM</sub>  | Maximum transient isolation voltage <sup>[2]</sup>                     | 8000              | V <sub>pk</sub>  |
| V <sub>IOSM</sub>  | Maximum surge isolation voltage <sup>[3]</sup>                         | 10000             | V <sub>pk</sub>  |
| V <sub>PD(m)</sub> | Input to output test voltage 100 % test method B1 <sup>[4]</sup>       | 2812              | V <sub>pk</sub>  |
|                    | Input to output test voltage type test method A <sup>[5]</sup>         | 2400              | V <sub>pk</sub>  |
|                    | Input to output test voltage type test subgroups 1 to 3 <sup>[6]</sup> | 1800              | V <sub>pk</sub>  |
| C <sub>IO</sub>    | Barrier capacitance, input to output                                   | < 3               | pF               |
| R <sub>IO</sub>    | Insulation resistance at T <sub>s</sub> , V <sub>IO</sub> = 500 V      | > 10 <sup>9</sup> | Ω                |
| T <sub>s</sub>     | Maximum junction temperature   | 150               | °C               |
| P <sub>s</sub>     | Safe total dissipated power  | 0.38              | W                |
| V <sub>ISO</sub>   | Withstand isolation voltage (1 minute) <sup>[7]</sup>                  | 5000              | V <sub>RMS</sub> |

[1] For part numbers MGD3160AM515EK, MGD3160AM535EK, MGD3160AM315EK, and MGD3160AM335EK

[2] For part numbers MGD3160AM518EK, MGD3160AM538EK, MGD3160AM318EK, and MGD3160AM338EK

- [3] per IEC 60065, 1.2 μ/50 μs waveform
- [4]  $V_{ini} = V_{IOTM}$ ,  $t_{ini} = 1\text{ s}$   
 $V_{PD(m)} = V_{IORM} \times 1.875$ ,  $t_m = 1\text{ s}$ , Partial discharge < 5pC
- [5]  $V_{ini} = V_{IOTM}$ ,  $t_{ini} = 60\text{ s}$   
 $V_{PD(m)} = V_{IORM} \times 1.6$ ,  $t_m = 10\text{ s}$ , Partial discharge < 5pC
- [6]  $V_{ini} = V_{IOTM}$ ,  $t_{ini} = 60\text{ s}$   
 $V_{PD(m)} = V_{IORM} \times 1.2$ ,  $t_m = 10\text{ s}$ , Partial discharge < 5pC
- [7]  $V_{TEST} = V_{ISO} = 5000\text{ V}_{RMS}$ ,  $t = 60\text{ s}$  (NXP qualification)  
 $V_{TEST} = 2500\text{ V}_{RMS(4243Vpk)}$ ,  $t = 1\text{ s}$  (100 % production) (MGD3160AM515EK, MGD3160AM535EK, MGD3160AM315EK and MGD3160AM335EK)  
 $V_{TEST} = 5000\text{ V}_{RMS(8500Vpk)}$ ,  $t = 1\text{ s}$  (100 % production) (MGD3160AM518EK, MGD3160AM538EK, MGD3160AM318EK and MGD3160AM338EK)

The GD3160 uses the same isolation technology as GD3100, but device certification and manufacturing certification are still pending until the device goes into production for the component programs listed in [Table 9](#).

Table 9. Regulatory information

| Standard    | Approval   |
|-------------|--|
| UL 1577     | Certified 5.0 kV rms for 1 min single protection, 5.0 kV rms.                    |
| VDE 0884-10 | Tested in accordance with DIN V VDE V 0884-10 reinforced isolation, 1.5 kV peak. |

## 9 Electrical characteristics

### 9.1 Power management

**Table 10. Power management electrical characteristics**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $+150$  °C, unless otherwise specified. All voltages referenced to GND1 or GND2. Currents are positive into and negative out of the specified pins.

| Symbol  | Parameter  | Min   | Typ  | Max  | Unit |
|---|--|-------|------|------|------|
| <b>Voltage supplies and references - low-voltage domain. Voltages reference to GND1</b>   |  |       |      |      |      |
| $I_{VSUP}$  | VSUP quiescent current <sup>[1]</sup>  | —     | 5    | 8    | mA   |
| $VSUP_{OV\_TH\_H}$  | VSUP overvoltage threshold (rising)  | 28    | —    | 32.0 | V    |
| $VSUP_{OV\_TH\_HYS}$  | VSUP overvoltage threshold hysteresis  | 0.25  | —    | 0.75 | V    |
| $VSUP_{UV\_TH\_L}$  | VSUP undervoltage threshold (falling)  | 5.5   | —    | 6.5  | V    |
| $VSUP_{UV\_TH\_HYS}$  | VSUP undervoltage threshold hysteresis   | 0.05  | —    | 0.25 | V    |
| $VSUP_{POR\_FALLING}$   | Low-voltage domain POR condition (falling), POR when $VSUP < VSUP_{POR\_FALLING}$ <sup>[2]</sup> | 2     | —    | —    | V    |
| $VSUP_{POR\_RISING}$  | Low-voltage domain POR clear (rising), POR clear when $VSUP > VSUP_{POR\_RISING}$ <sup>[2]</sup> | —     | —    | 3.75 | V    |
| $t_{VSUP\_FLT}$   | VSUP over/under voltage fault filter time  | 32    | 40   | 48   | µs   |
| $t_{VDD\_FLT\_FLT}$   | VDD over/under voltage fault filter time   | 16    | 20   | 24   | µs   |
| <b>GD3160 with 3.3 V VDD</b>  |  |       |      |      |      |
| $V_{VDD3p3}$  | Output of VDD regulator when powered by VSUP   | 3.20  | 3.30 | 3.40 | V    |
| $VDD_{OV\_TH\_H3p3}$  | VDD overvoltage threshold (rising)   | 3.60  | 3.75 | 3.90 | V    |
| $VDD_{OV\_TH\_HYS3p3}$  | VDD overvoltage threshold hysteresis   | 0.075 | 0.15 | 0.20 | V    |
| $VDD_{UV\_TH\_L3p3}$  | VDD undervoltage threshold (falling)   | 2.56  | 2.73 | 2.92 | V    |
| $VDD_{UV\_TH\_HYS3p3}$  | VDD undervoltage threshold hysteresis  | 0.075 | 0.15 | 0.20 | V    |
| <b>GD3160 with 5.0 V VDD <sup>[3]</sup></b>   |  |       |      |      |      |
| $V_{VDD5}$  | Output of VDD regulator when powered by VSUP   | 4.85  | 5.00 | 5.15 | V    |
| $VDD_{OV\_TH\_H5}$  | VDD overvoltage threshold (rising)   | 5.35  | 5.55 | 5.77 | V    |
| $VDD_{OV\_TH\_HYS5}$  | VDD overvoltage threshold hysteresis   | 0.075 | 0.15 | 0.20 | V    |
| $VDD_{UV\_TH\_L5}$  | VDD undervoltage threshold (falling)   | 4.12  | 4.30 | 4.48 | V    |
| $VDD_{UV\_TH\_HYS5}$  | VDD undervoltage threshold hysteresis  | 0.075 | 0.15 | 0.20 | V    |
| <b>Voltage supplies and references - high-voltage domain. Voltages referenced to GND2</b> |  |       |      |      |      |
| $VCC_{OV\_TH\_H}$   | VCC overvoltage threshold (rising edge)  | 23.0  | —    | 25.0 | V    |
| $VCC_{OV\_TH\_HYS}$   | VCC overvoltage threshold hysteresis   | 0.25  | —    | 0.90 | V    |
| $t_{VCC\_OV\_FLT}$  | VCC overvoltage fault filter time  | 32    | 40   | 48   | µs   |
| $VCC_{UV\_TH\_L}$   | VCC undervoltage threshold (falling edge)  | 5.5   | —    | 6.5  | V    |
| $VCC_{UV\_TH\_HYS}$   | VCC undervoltage threshold hysteresis  | 0.10  | 0.15 | 0.25 | V    |
| $VVCC_{POR\_FALLING}$   | High-voltage domain POR condition (falling) POR when $VCC < VVCC_{POR\_FALLING}$ <sup>[2]</sup>  | 2     | —    | —    | V    |
| $VVCC_{POR\_RISING}$  | High-voltage domain POR clear (rising) ,POR clear when $VCC > VVCC_{POR\_RISING}$ <sup>[2]</sup> | —     | —    | 3.75 | V    |
| $t_{VCC\_UV\_FLT}$  | VCC undervoltage fault filter time   | 16    | 20   | 24   | µs   |
| $I_{VCC}$   | VCC quiescent current <sup>[4]</sup>   | 6     | 7.5  | 11   | mA   |

**Table 10. Power management electrical characteristics...continued**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $+150$  °C, unless otherwise specified. All voltages referenced to GND1 or GND2. Currents are positive into and negative out of the specified pins.

| Symbol                               | Parameter   | Min    | Typ    | Max   | Unit |
|--------------------------------------|---|--------|--------|-------|------|
| VCCREG <sub>OUT</sub>                | VCCREG regulated output voltage, VCCREG[2:0] = '000' (VCC > 15.0 V)   | 13.75  | 14     | 14.28 | V    |
|                                      | VCCREG regulated output voltage, VCCREG[2:0] = '001' (VCC > 16.0 V)   | 14.72  | 15     | 15.28 | V    |
|                                      | VCCREG regulated output voltage, VCCREG[2:0] = '010' (VCC > 17.0 V)   | 15.7   | 16     | 16.3  | V    |
|                                      | VCCREG regulated output voltage, VCCREG[2:0] = '011' (VCC > 18.0 V)   | 16.67  | 17     | 17.33 | V    |
|                                      | VCCREG regulated output voltage, VCCREG[2:0] = '100' (VCC > 19.0 V)   | 17.64  | 18     | 18.36 | V    |
|                                      | VCCREG regulated output voltage, VCCREG[2:0] = '101' (VCC > 20.0 V)   | 18.62  | 19     | 19.38 | V    |
|                                      | VCCREG regulated output voltage, VCCREG[2:0] = '110' (VCC > 21.0 V)   | 19.6   | 20     | 20.4  | V    |
|                                      | VCCREG regulated output voltage, VCCREG[2:0] = '111' (VCC > 22.0 V)   | 20.57  | 21     | 21.43 | V    |
| VCCREG <sub>DO</sub>                 | VCCREG dropout voltage <sup>[5]</sup>                                 | —      | —      | 0.5   | V    |
| VCCREG <sub>UV_TH_L</sub>            | VCCREG undervoltage threshold (falling edge), UV_TH = '000'           | 9.50   | 10.00  | 10.50 | V    |
|                                      | VCCREG undervoltage threshold (falling edge), UV_TH = '001'           | 9.98   | 10.50  | 11.03 | V    |
|                                      | VCCREG undervoltage threshold (falling edge), UV_TH = '010'           | 10.45  | 11.00  | 11.55 | V    |
|                                      | VCCREG undervoltage threshold (falling edge), UV_TH = '011' (default) | 10.93  | 11.50  | 12.08 | V    |
|                                      | VCCREG undervoltage threshold (falling edge), UV_TH = '100'           | 11.40  | 12.00  | 12.60 | V    |
|                                      | VCCREG undervoltage threshold (falling edge), UV_TH = '101'           | 11.88  | 12.50  | 13.13 | V    |
|                                      | VCCREG undervoltage threshold (falling edge), UV_TH = '110'           | 12.35  | 13.00  | 13.65 | V    |
|                                      | VCCREG undervoltage threshold (falling edge), UV_TH = '111'           | 12.83  | 13.50  | 14.18 | V    |
| VCCREG <sub>UV_TH_HYS</sub>          | VCCREG undervoltage threshold hysteresis                              | 0.05   | 0.15   | 0.230 | V    |
| t <sub>VCCREG_FLT_FILT</sub>         | VCCREG undervoltage fault filter time                                 | 32     | 40     | 48    | µs   |
| V <sub>VREF</sub>                    | VREF regulated voltage <sup>[6]</sup>                                 | 4.938  | 5.00   | 5.079 | V    |
| V <sub>VREF_TVAR</sub>               | VREF variation with temperature <sup>[7] [2]</sup>                    | −15    | —      | 15    | mV   |
| VREF <sub>UV_TH_L</sub>              | VREF undervoltage threshold (falling)                                 | 4.12   | 4.30   | 4.49  | V    |
| VREF <sub>UV_TH_HYS</sub>            | VREF undervoltage threshold hysteresis                                | 0.10   | 0.15   | 0.225 | V    |
| t <sub>VREF_FLT_FILT</sub>           | VREF UV fault filter time   | 16     | 20     | 24    | µs   |
| I <sub>VEE</sub>                     | VEE quiescent current <sup>[8]</sup>                                  | −0.850 | −0.045 | −0.2  | mA   |
| VEE <sub>OOD_TH</sub>                | VEE out of range  | −2.0   | −1.5   | −1.0  | V    |
| t <sub>VEE_FLT_FILT</sub>            | VEE out of range fault filter time                                    | 32     | 40     | 48    | µs   |
| <b>Current limits and references</b> |   |        |        |       |      |
| I <sub>VDD_LIM</sub>                 | Current limit of VDD regulator  | −60    | −30    | −20   | mA   |
| I <sub>VREF_LIM</sub>                | Current limit of VREF regulator                                       | −60    | —      | −20   | mA   |
| I <sub>VCCREG_LIM</sub>              | Current limit of VCCREG regulator                                     | −1500  | −1100  | −800  | mA   |

[1] VSUP = 14 V, IGBT off

[2] Guaranteed by design

[3] When VDD is externally supplied, the applied voltage must be 4.75 to 5.25 V.

[4] VCC = 17 V, I<sub>VREF</sub> = 0 mA, IGBT off

[5] VCC < 15 V, I<sub>VCCREG</sub> = 100 mA

[6] VCCREG > VCCREG<sub>UV\_TH</sub>, I<sub>VREF</sub> = 0 to 20 mA

[7] T<sub>J</sub> = 25 to 150 °C, I<sub>VREF</sub> = 1.0 mA

[8] VEE = −8.0 V, I<sub>VREF</sub> = 0 mA, IGBT off

## 9.2 Digital inputs and outputs

[Table 11](#) and [Table 12](#) specify characteristics of the low-voltage digital I/O pins. [Table 13](#) specifies the FSISO digital input pin on the high-voltage (HV) domain.

**Table 11. Low-voltage digital I/O electrical characteristics**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+150\text{ }^{\circ}\text{C}$ , unless otherwise specified. All voltages referenced to GND1. Currents are positive into and negative out of the specified pins.

| Symbol  | Parameter   | Min               | Typ               | Max               | Unit          |
|---|---|-------------------|-------------------|-------------------|---------------|
| $V_{INL}$                                     | Logic low input voltage <sup>[1]</sup>  | —                 | —                 | $0.30 \times VDD$ | V             |
| $V_{INH}$                                     | Logic high input voltage <sup>[1]</sup>   | $0.70 \times VDD$ | —                 | —                 | V             |
| $V_{INhys}$                                   | Input voltage threshold hysteresis <sup>[1]</sup>   | $0.20 \times VDD$ | $0.25 \times VDD$ | $0.30 \times VDD$ | V             |
| $INPU_{LK}$                                   | Input leakage for pins with pullup resistor pins: CSB, PWMALT <sup>[2] [3]</sup>                              | —                 | —                 | 4.0               | $\mu\text{A}$ |
| $INPD_{LK}$                                   | Input leakage for pins with pulldown resistor pins: MOSI, SCLK, PWM, FSSTATE, FSENB, FSISO <sup>[3] [4]</sup> | -1.0              | —                 | —                 | $\mu\text{A}$ |
| $C_{IN}$                                      | Input capacitance, logic pins <sup>[3]</sup>  | —                 | —                 | 10                | pF            |
| $V_{OL}$                                      | Logic low output voltage <sup>[5]</sup>   | —                 | —                 | $0.2 \times VDD$  | V             |
| $V_{OLINT}$                                   | Logic low output voltage for open-drain interrupts <sup>[6]</sup>   | —                 | —                 | $0.2 \times VDD$  | V             |
| $V_{OH}$                                      | Logic high output voltage <sup>[7]</sup>  | $0.8 \times VDD$  | —                 | —                 | V             |
| $t_{RTRPT\_DLY}$                              | Real time reporting delay   | 200               | 220               | 240               | ns            |
| $t_{MIN}$                                     | Input pulse deglitch <sup>[8]</sup>   | 34                | —                 | 67                | ns            |
| $t_{ftdly}$                                   | Event detection delay to INTA or INTB low   | —                 | 1.28              | 1.6               | $\mu\text{s}$ |
| $t_{onmin}$                                   | Minimum on pulse width (PWM) <sup>[9]</sup>   | —                 | —                 | 220               | ns            |
| $t_{offmin}$                                  | Minimum off pulse width (PWM) <sup>[9]</sup>  | —                 | —                 | 220               | ns            |
| $R_{PU}$                                      | Pullup resistor for CSB, INTB, INTA   | 30                | 50                | 75                | k $\Omega$    |
| $R_{PU\_PWMALT}$                              | Pullup resistor for PWMALT  | 300               | 500               | 750               | k $\Omega$    |
| $R_{PD}$                                      | Pulldown resistor FSSTATE, FSENB, PWM, SCLK, MOSI   | 30                | 50                | 75                | k $\Omega$    |
| $t_{MINFSSTATE}$                              | FSSTATE input pulse deglitch  | 931               | 1000              | 1071              | ns            |
| $t_{MINFSENB0}$                               | FSENB input pulse deglitch (FSSTATE = 0 or PWM = 0)   | 0.465             | 0.5               | 0.536             | $\mu\text{s}$ |
| $t_{MINFSENB1}$                               | FSENB input pulse deglitch (FSSTATE = 1 or PWM = 1)   | 5.995             | 6.5               | 7.025             | $\mu\text{s}$ |
| $t_{MIN\_DT}$<br>(TIME_2 = 1) <sup>[10]</sup> | PWM deadtime, DEADT = '0000'  | 0.081             | 0.1               | 0.198             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '0001'  | 0.12              | 0.14              | 0.239             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '0010'  | 0.217             | 0.24              | 0.342             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '0011'  | 0.372             | 0.4               | 0.507             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '0100'  | 0.508             | 0.54              | 0.651             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '0101'  | 0.741             | 0.78              | 0.898             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '0110'  | 0.993             | 1.04              | 1.166             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '0111'  | 1.226             | 1.28              | 1.413             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '1000'  | 1.478             | 1.54              | 1.681             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '1001'  | 1.711             | 1.78              | 1.928             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '1010'  | 1.963             | 2.04              | 2.196             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '1011'  | 2.196             | 2.28              | 2.443             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '1100'  | 2.448             | 2.54              | 2.711             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '1101'  | 2.681             | 2.78              | 2.958             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '1110'  | 2.933             | 3.04              | 3.226             | $\mu\text{s}$ |
|   | PWM deadtime, DEADT = '1111' (default)  | 3.132             | 3.28              | 3.406             | $\mu\text{s}$ |

**Table 11. Low-voltage digital I/O electrical characteristics...continued**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+150\text{ }^{\circ}\text{C}$ , unless otherwise specified. All voltages referenced to GND1. Currents are positive into and negative out of the specified pins.

| Symbol                               | Parameter                     | Min   | Typ  | Max   | Unit          |
|--------------------------------------|-------------------------------|-------|------|-------|---------------|
| $t_{\text{MIN\_DT}}$<br>(TIME_2 = 0) | PWM deadtime, DEADT = '0000', | 0.128 | 0.16 | 0.329 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '0001'  | 0.206 | 0.24 | 0.411 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '0010'  | 0.4   | 0.44 | 0.617 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '0011'  | 0.71  | 0.76 | 0.947 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '0100'  | 0.982 | 1.04 | 1.235 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '0101'  | 1.448 | 1.52 | 1.729 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '0110'  | 1.952 | 2.04 | 2.265 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '0111'  | 2.418 | 2.52 | 2.759 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '1000'  | 2.922 | 3.04 | 3.295 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '1001'  | 3.388 | 3.52 | 3.789 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '1010'  | 3.892 | 4.04 | 4.325 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '1011'  | 4.358 | 4.52 | 4.819 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '1100'  | 4.862 | 5.04 | 5.355 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '1101'  | 5.328 | 5.52 | 5.849 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '1110'  | 5.832 | 6.04 | 6.385 | $\mu\text{s}$ |
|                                      | PWM deadtime, DEADT = '1111'  | 6.298 | 6.52 | 6.879 | $\mu\text{s}$ |

- [1] Pins: FSSTATE, FSENB, PWM, PWMALT, SCLK, CSB, MOSI  
 [2] CSB, PWMALT connected to VDD  
 [3] Guaranteed by design  
 [4] MOSI, SCLK, PWM, FSSTATE, FSENB connected to GND1; FSISO connected to GND2  
 [5] Pins: MISO, AOOUT, INTA (when RTRPT = 1), I = 3.0 mA  
 [6] Pins: INTB, INTA (when RTRPT = 0), I = 10 mA  
 [7] Pins: MISO, AOOUT, INTA (when RTRPT = 1), I = -2.0 mA  
 [8] Pins: PWM, PWMALT  
 [9]  $C_{\text{Load}} = 2\text{ nF}$ , guaranteed by design  
 [10] TIME\_2\_is Timer scaling bit of [MODE1 register](#)

**Table 12. SPI timing**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $+150\text{ }^{\circ}\text{C}$ , unless otherwise specified. All voltages referenced to GND1. Currents are positive into and negative out of the specified pins.

| Symbol               | Parameter   | Limit value |     |     | Unit |
|----------------------|---|-------------|-----|-----|------|
|                      |   | Min         | Typ | Max |      |
| $f_{\text{SPI}}$     | Frequency of SPI operation <sup>[1] [2]</sup>                                   | —           | —   | 10  | MHz  |
| $t_{\text{lead}}$    | Falling edge of CSB to rising edge of SCLK (required setup time) <sup>[2]</sup> | 50          | —   | —   | ns   |
| $t_{\text{lag}}$     | Falling edge of SCLK to rising edge of CSB (required setup time) <sup>[2]</sup> | 50          | —   | —   | ns   |
| $t_{\text{wh}}$      | High time of SCLK <sup>[2]</sup>  | 45          | —   | —   | ns   |
| $t_{\text{wl}}$      | Low time of SCLK <sup>[2]</sup>   | 45          | —   | —   | ns   |
| $t_{\text{su1}}$     | MOSI to rising edge of SCLK (required setup time) <sup>[2]</sup>                | 15          | —   | —   | ns   |
| $t_{\text{h}}$       | MOSI to rising edge of SCLK (required hold time) <sup>[2]</sup>                 | 15          | —   | —   | ns   |
| $t_{\text{SO(en)}}$  | Time from falling edge of CSB to MISO low impedance <sup>[2]</sup>              | —           | —   | 30  | ns   |
| $t_{\text{SO(dis)}}$ | Time from Rising Edge of CSB to MISO high Impedance <sup>[2]</sup>              | —           | —   | 30  | ns   |
| $t_{\text{valid}}$   | Time from falling edge of SCLK to MISO data valid <sup>[3] [2]</sup>            | —           | —   | 30  | ns   |

**Table 12. SPI timing...continued**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $+150$  °C, unless otherwise specified. All voltages referenced to GND1. Currents are positive into and negative out of the specified pins.

| Symbol                   | Parameter                | Limit value |     |     | Unit |
|--------------------------|--------------------------|-------------|-----|-----|------|
|                          |                          | Min         | Typ | Max |      |
| $t_{\text{xfer\_delay}}$ | Minimum message deadtime | 19          | —   | —   | μs   |
| $t_{\text{BIST}}$        | BIST duration            | —           | —   | 28  | ms   |

[1]  $T_{\text{SPI}} = 1/f_{\text{SPI}}$

[2] Guaranteed by design

[3]  $0.2 \times V_{\text{DD}} \leq \text{MISO} \leq 0.8 \times V_{\text{DD}}$ , CL = 50 pF

**Table 13. FSISO pin electrical characteristics**

VCC, VCCREG in regulation,  $T_J = -40$  °C to  $+150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.

| Symbol                | Parameter   | Min         | Typ         | Max         | Unit |
|-----------------------|---|-------------|-------------|-------------|------|
| $V_{\text{FSISOL}}$   | FSISO logic low input voltage <sup>[1]</sup>            | —           | —           | 0.3 x VREF  | V    |
| $V_{\text{FSISOH}}$   | FSISO logic high input voltage <sup>[1]</sup>           | 0.7 x VREF  | —           | 1.05 x VREF | V    |
| $V_{\text{FSISOHys}}$ | FSISO input voltage threshold hysteresis <sup>[1]</sup> | 0.20 x VREF | 0.25 x VREF | 0.32 x VREF | V    |
| $C_{\text{FSISOIN}}$  | FSISO input capacitance <sup>[2]</sup>                  | —           | —           | 10          | pF   |
| $R_{\text{FSISOPD}}$  | FSISO pulldown resistor                                 | 30          | 60          | 100         | kΩ   |
| $t_{\text{FSISOMIN}}$ | FSISO input pulse deglitch                              | 500         | 750         | 1100        | ns   |

[1] Reference = GND2

[2] Guaranteed by design

## 9.3 Gate drive outputs

**Table 14. Gate drive output stage electrical characteristics**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.

| Symbol                            | Parameter  | Min  | Typ  | Max | Unit |
|-----------------------------------|--|------|------|-----|------|
| <b>Static electrical ratings</b>  |  |      |      |     |      |
| $R_{\text{DSOnGH}}$               | Gate drive pullup transistor GH on-resistance  | —    | —    | 800 | mΩ   |
| $R_{\text{DSOnGL}}$               | Gate drive pulldown transistor GL on-resistance  | —    | —    | 500 | mΩ   |
| $R_{\text{DSOnAMC}}$              | Gate drive pulldown transistor AMC on-resistance   | —    | —    | 500 | mΩ   |
| $I_{\text{DSS\_GH}}$              | Gate drive pullup transistor saturation current <sup>[1]</sup>   | 14.0 | 19.0 | —   | A    |
| $I_{\text{DSS\_GL}}$              | Gate drive pulldown transistor saturation current <sup>[2]</sup>   | 14.0 | 19.0 | —   | A    |
| $I_{\text{DSS\_AMC}}$             | Active Miller clamp transistor saturation current <sup>[2]</sup>   | 14.0 | 19.0 | —   | A    |
| $I_{\text{LEAKGH}}$               | GH leakage current <sup>[1]</sup>  | −10  | —    | —   | μA   |
| $I_{\text{LEAKGL}}$               | GL leakage current <sup>[2]</sup>  | —    | —    | 150 | μA   |
| $I_{\text{LEAKAMC}}$              | AMC leakage current <sup>[3]</sup>   | —    | —    | 30  | μA   |
| <b>Switching and delay timing</b> |  |      |      |     |      |
| $t_{\text{ON\_DLY\_GH}}$          | PWM to GH turn-on delay <sup>[4]</sup>   | 75   | —    | 125 | ns   |
| $t_{\text{ON\_GH}}$               | PWM to GH turn on time <sup>[5]</sup>  | 100  | —    | 150 | ns   |
| $t_{\text{ON\_DLY\_GL}}$          | PWM to GL turn on delay <sup>[6]</sup>   | 75   | —    | 125 | ns   |
| $t_{\text{ON\_GL}}$               | PWM to GL turn on time <sup>[7]</sup>  | 100  | —    | 150 | ns   |
| $t_{\text{pd\_dist}}$             | PWM to output pulse delay distortion <sup>[8]</sup><br>$ t_{\text{ON\_DLY\_GH}} - t_{\text{ON\_DLY\_GL}} $ | −32  | —    | 32  | ns   |
| $t_{\text{AMC\_FLT}}$             | AMC turn on filter time  | 170  | 180  | 220 | ns   |

**Table 14. Gate drive output stage electrical characteristics...continued**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.

| Symbol  | Parameter   | Min  | Typ  | Max  | Unit |
|---|---|------|------|------|------|
| <b>Gate voltage monitor</b>                           |   |      |      |      |      |
| V <sub>GEON_TH</sub>                                  | V <sub>GE</sub> monitor threshold high <sup>[9]</sup>                     | -2.3 | -2.0 | -1.7 | V    |
| V <sub>AMC_TH</sub>                                   | Active Miller clamp threshold voltage (referenced to VEE) <sup>[10]</sup> | 1.7  | —    | 2.3  | V    |
| V <sub>GOFF</sub>                                     | Unpowered gate clamp voltage of holdoff circuit <sup>[11]</sup>           | —    | —    | 3.0  | V    |
| t <sub>RTMONDLY</sub><br>(TIME_2 = 1) <sup>[12]</sup> | PWM monitor delay time, RTMONDLY = '0000'                                 | —    | —    | —    | ns   |
|   | PWM monitor delay time, RTMONDLY = '0001'                                 | —    | —    | —    | ns   |
|   | PWM monitor delay time, RTMONDLY = '0010'                                 | 383  | 400  | 512  | ns   |
|   | PWM monitor delay time, RTMONDLY = '0011'                                 | 577  | 600  | 718  | ns   |
|   | PWM monitor delay time, RTMONDLY = '0100'                                 | 771  | 800  | 924  | ns   |
|   | PWM monitor delay time, RTMONDLY = '0101'                                 | 965  | 1000 | 1130 | ns   |
|   | PWM monitor delay time, RTMONDLY = '0110'                                 | 1159 | 1200 | 1336 | ns   |
|   | PWM monitor delay time, RTMONDLY = '0111'                                 | 1353 | 1400 | 1542 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1000'                                 | 1547 | 1600 | 1748 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1001'                                 | 1741 | 1800 | 1954 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1010' (default)                       | 1935 | 2000 | 2160 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1011'                                 | 2323 | 2400 | 2572 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1100'                                 | 2711 | 2800 | 2984 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1101'                                 | 3099 | 3200 | 3396 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1110'                                 | 3487 | 3600 | 3808 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1111'                                 | 3875 | 4000 | 4220 | ns   |
| t <sub>RTMONDLY</sub><br>(TIME_2 = 0) <sup>[12]</sup> | PWM monitor delay time, RTMONDLY = '0000'                                 | —    | —    | —    | ns   |
|   | PWM monitor delay time, RTMONDLY = '0001'                                 | 378  | 400  | 464  | ns   |
|   | PWM monitor delay time, RTMONDLY = '0010'                                 | 766  | 800  | 1024 | ns   |
|   | PWM monitor delay time, RTMONDLY = '0011'                                 | 1154 | 1200 | 1436 | ns   |
|   | PWM monitor delay time, RTMONDLY = '0100'                                 | 1542 | 1600 | 1848 | ns   |
|   | PWM monitor delay time, RTMONDLY = '0101'                                 | 1930 | 2000 | 2260 | ns   |
|   | PWM monitor delay time, RTMONDLY = '0110'                                 | 2318 | 2400 | 2672 | ns   |
|   | PWM monitor delay time, RTMONDLY = '0111'                                 | 2706 | 2800 | 3084 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1000'                                 | 3094 | 3200 | 3496 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1001'                                 | 3482 | 3600 | 3908 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1010'                                 | 3870 | 4000 | 4320 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1011'                                 | 4646 | 4800 | 5144 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1100'                                 | 5422 | 5600 | 5968 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1101'                                 | 6198 | 6400 | 6792 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1110'                                 | 6974 | 7200 | 7616 | ns   |
|   | PWM monitor delay time, RTMONDLY = '1111'                                 | 7750 | 8000 | 8440 | ns   |
| <b>Fault management</b>                               |   |      |      |      |      |

**Table 14. Gate drive output stage electrical characteristics...continued**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.

| Symbol   | Parameter  | Min   | Typ   | Max   | Unit |
|--|--|-------|-------|-------|------|
| V <sub>2LTO</sub>                                | Two-level turn-off voltage, 2LTOV = '0000'           | 6.22  | 6.48  | 6.74  | V    |
|  | Two-level turn-off voltage, 2LTOV = '0001'           | 6.4   | 6.67  | 6.94  | V    |
|  | Two-level turn-off voltage, 2LTOV = '0010'           | 6.59  | 6.87  | 7.14  | V    |
|  | Two-level turn-off voltage, 2LTOV = '0011' (default) | 6.8   | 7.08  | 7.37  | V    |
|  | Two-level turn-off voltage, 2LTOV = '0100'           | 7.02  | 7.32  | 7.61  | V    |
|  | Two-level turn-off voltage, 2LTOV = '0101'           | 7.26  | 7.56  | 7.87  | V    |
|  | Two-level turn-off voltage, 2LTOV = '0110'           | 7.52  | 7.83  | 8.15  | V    |
|  | Two-level turn-off voltage, 2LTOV = '0111'           | 7.8   | 8.13  | 8.45  | V    |
|  | Two-level turn-off voltage, 2LTOV = '1000'           | 8.12  | 8.46  | 8.8   | V    |
|  | Two-level turn-off voltage, 2LTOV = '1001'           | 8.46  | 8.81  | 9.16  | V    |
|  | Two-level turn-off voltage, 2LTOV = '1010'           | 8.83  | 9.19  | 9.56  | V    |
|  | Two-level turn-off voltage, 2LTOV = '1011'           | 9.23  | 9.62  | 10.0  | V    |
|  | Two-level turn-off voltage, 2LTOV = '1100'           | 9.69  | 10.09 | 10.49 | V    |
|  | Two-level turn-off voltage, 2LTOV = '1101'           | 10.2  | 10.62 | 11.04 | V    |
|  | Two-level turn-off voltage, 2LTOV = '1110'           | 10.76 | 11.21 | 11.66 | V    |
|  | Two-level turn-off voltage, 2LTOV = '1111'           | 11.4  | 11.88 | 12.36 | V    |
| I <sub>SSD</sub>                                 | Soft shutdown current, SSD_CUR = '000'               | 0.068 | 0.094 | 0.117 | A    |
|  | Soft shutdown current, SSD_CUR = '001'               | 0.149 | 0.186 | 0.224 | A    |
|  | Soft shutdown current, SSD_CUR = '010'               | 0.222 | 0.277 | 0.333 | A    |
|  | Soft shutdown current, SSD_CUR = '011'               | 0.294 | 0.367 | 0.440 | A    |
|  | Soft shutdown current, SSD_CUR = '100' (default)     | 0.455 | 0.541 | 0.628 | A    |
|  | Soft shutdown current, SSD_CUR = '101'               | 0.591 | 0.704 | 0.816 | A    |
|  | Soft shutdown current, SSD_CUR = '110'               | 0.729 | 0.858 | 0.986 | A    |
|  | Soft shutdown current, SSD_CUR = '111'               | 0.847 | 0.996 | 1.146 | A    |
| t <sub>SSD</sub><br>(TIME_2 = 0) <sup>[12]</sup> | Soft shutdown time, SSDT = '000'                     | 1880  | 2000  | 2120  | ns   |
|  | Soft shutdown time, SSDT = '001'                     | 2850  | 3000  | 3150  | ns   |
|  | Soft shutdown time, SSDT = '010'                     | 3820  | 4000  | 4180  | ns   |
|  | Soft shutdown time, SSDT = '011'                     | 4790  | 5000  | 5210  | ns   |
|  | Soft shutdown time, SSDT = '100'                     | 5760  | 6000  | 6240  | ns   |
|  | Soft shutdown time, SSDT = '101'                     | 6730  | 7000  | 7270  | ns   |
|  | Soft shutdown time, SSDT = '110'                     | 7700  | 8000  | 8300  | ns   |
|  | Soft shutdown time, SSDT = '111'                     | 8670  | 9000  | 9330  | ns   |
| t <sub>SSD</sub><br>(TIME_2 = 1) <sup>[12]</sup> | Soft shutdown time, SSDT = '000'                     | 940   | 1000  | 1060  | ns   |
|  | Soft shutdown time, SSDT = '001'                     | 1425  | 1500  | 1575  | ns   |
|  | Soft shutdown time, SSDT = '010'                     | 1910  | 2000  | 2090  | ns   |
|  | Soft shutdown time, SSDT = '011'                     | 2395  | 2500  | 2605  | ns   |
|  | Soft shutdown time, SSDT = '100' (default)           | 2880  | 3000  | 3120  | ns   |
|  | Soft shutdown time, SSDT = '101'                     | 3365  | 3500  | 3635  | ns   |
|  | Soft shutdown time, SSDT = '110'                     | 3850  | 4000  | 4150  | ns   |
|  | Soft shutdown time, SSDT = '111'                     | 4335  | 4500  | 4665  | ns   |
| t <sub>SSD_ACT</sub>                             | Soft shutdown activation time                        | —     | 15    | 30    | ns   |
| t <sub>LATCH</sub>                               | Soft shutdown latch enable time (one clock cycle)    | —     | 20    | 21    | ns   |

[1] V<sub>VCCREG</sub> = 15.0 V. Design limit

- [2] Design limit  
 [3] AMC = VCC, AMC off  
 [4] 90 % PWM to 10 %  $V_{GE}$ . Includes deglitch. Guaranteed by design.  
 [5] 90 % PWM to 90 %  $V_{GE}$ . Includes deglitch. C = 2.0 nF. Guaranteed by design.  
 [6] 10 % PWM to 90 %  $V_{GE}$ . Includes deglitch. Guaranteed by design.  
 [7] 10 % PWM to 10 %  $V_{GE}$ . Includes deglitch. C = 2.0 nF. Guaranteed by design.  
 [8] Guaranteed by design  
 [9] Reference voltage is VCCREG  
 [10] Referenced to VEE;  $V_{AMC} - V_{VEE}$   
 [11] VCCREG floating, pulldown gate current = 200 mA for 1 ms.  
 [12] TIME\_2 is Timer scaling bit of [MODE1 register](#)

## 9.4 Current sense protection

**Table 15. Short-circuit and overcurrent fault electrical characteristics**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.

| Symbol  | Parameter   | Min   | Typ  | Max   | Unit |
|---|---|-------|------|-------|------|
| <b>Short-circuit and overcurrent fault management</b> |   |       |      |       |      |
| $V_{SC\_TH}$  | Short-circuit voltage threshold, SCTH = '000'         | 0.460 | 0.5  | 0.540 | V    |
|   | Short-circuit voltage threshold, SCTH = '001'         | 0.713 | 0.75 | 0.788 | V    |
|   | Short-circuit voltage threshold, SCTH = '010'         | 0.950 | 1.00 | 1.050 | V    |
|   | Short-circuit voltage threshold, SCTH = '011'         | 1.188 | 1.25 | 1.313 | V    |
|   | Short-circuit voltage threshold, SCTH = '100'         | 1.425 | 1.50 | 1.575 | V    |
|   | Short-circuit voltage threshold, SCTH = '101'         | 1.900 | 2.00 | 2.100 | V    |
|   | Short-circuit voltage threshold, SCTH = '110'         | 2.375 | 2.50 | 2.625 | V    |
|   | Short-circuit voltage threshold, SCTH = '111'         | 2.850 | 3.00 | 3.150 | V    |
| $t_{2LTO\_FILT}$                                      | Two-level turn-off filter time                        | 80    | 100  | 120   | ns   |
| $t_{SC\_FILT}$  | Short-circuit filter time, SCFF = '0', SCFILT = '000' | 383   | 400  | 438   | ns   |
|   | Short-circuit filter time, SCFF = '0', SCFILT = '001' | 480   | 500  | 541   | ns   |
|   | Short-circuit filter time, SCFF = '0', SCFILT = '010' | 577   | 600  | 644   | ns   |
|   | Short-circuit filter time, SCFF = '0', SCFILT = '011' | 674   | 700  | 747   | ns   |
|   | Short-circuit filter time, SCFF = '0', SCFILT = '100' | 771   | 800  | 850   | ns   |
|   | Short-circuit filter time, SCFF = '0', SCFILT = '101' | 868   | 900  | 953   | ns   |
|   | Short-circuit filter time, SCFF = '0', SCFILT = '110' | 965   | 1000 | 1056  | ns   |
|   | Short-circuit filter time, SCFF = '0', SCFILT = '111' | 1062  | 1100 | 1159  | ns   |
| $t_{SC\_FILT}$  | Short-circuit filter time, SCFF = '1', SCFILT = '000' | 92    | 100  | 129   | ns   |
|   | Short-circuit filter time, SCFF = '1', SCFILT = '001' | 189   | 200  | 232   | ns   |
|   | Short-circuit filter time, SCFF = '1', SCFILT = '010' | 286   | 300  | 335   | ns   |
|   | Short-circuit filter time, SCFF = '1', SCFILT = '011' | 383   | 400  | 438   | ns   |
|   | Short-circuit filter time, SCFF = '1', SCFILT = '100' | 480   | 500  | 541   | ns   |
|   | Short-circuit filter time, SCFF = '1', SCFILT = '101' | 577   | 600  | 644   | ns   |
|   | Short-circuit filter time, SCFF = '1', SCFILT = '110' | 674   | 700  | 747   | ns   |
|   | Short-circuit filter time, SCFF = '1', SCFILT = '111' | 771   | 800  | 850   | ns   |

**Table 15. Short-circuit and overcurrent fault electrical characteristics...continued**

*VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.*

| Symbol               | Parameter   | Min   | Typ   | Max   | Unit |
|----------------------|---|-------|-------|-------|------|
| V <sub>OC_TH</sub>   | Overcurrent voltage threshold, OCTH = '000'           | 0.225 | 0.25  | 0.280 | V    |
|                      | Overcurrent voltage threshold, OCTH = '001'           | 0.460 | 0.500 | 0.540 | V    |
|                      | Overcurrent voltage threshold, OCTH = '010'           | 0.713 | 0.75  | 0.788 | V    |
|                      | Overcurrent voltage threshold, OCTH = '011' (default) | 0.950 | 1.000 | 1.050 | V    |
|                      | Overcurrent voltage threshold, OCTH = '100'           | 1.188 | 1.25  | 1.313 | V    |
|                      | Overcurrent voltage threshold, OCTH = '101'           | 1.425 | 1.5   | 1.575 | V    |
|                      | Overcurrent voltage threshold, OCTH = '110'           | 1.663 | 1.75  | 1.838 | V    |
|                      | Overcurrent voltage threshold, OCTH = '111'           | 1.900 | 2.000 | 2.100 | V    |
| t <sub>OC_FILT</sub> | Overcurrent filter time, OCFILT = '000'               | 0.4   | 0.5   | 0.6   | µs   |
|                      | Overcurrent filter time, OCFILT = '001'               | 0.9   | 1.0   | 1.1   | µs   |
|                      | Overcurrent filter time, OCFILT = '010'               | 1.4   | 1.5   | 1.6   | µs   |
|                      | Overcurrent filter time, OCFILT = '011'               | 1.8   | 2.0   | 2.2   | µs   |
|                      | Overcurrent filter time, OCFILT = '100'               | 2.3   | 2.5   | 2.7   | µs   |
|                      | Overcurrent filter time, OCFILT = '101'               | 2.8   | 3.0   | 3.2   | µs   |
|                      | Overcurrent filter time, OCFILT = '110'               | 3.3   | 3.5   | 3.7   | µs   |
|                      | Overcurrent filter time, OCFILT = '111'               | 3.8   | 4.0   | 4.2   | µs   |

## 9.5 Desaturation protection

**Table 16. Desaturation fault management**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.

| Symbol                               | Parameter   | Min   | Typ   | Max   | Unit |
|--------------------------------------|---|-------|-------|-------|------|
| <b>Desaturation fault management</b> |   |       |       |       |      |
| $I_{DESAT}$                          | DESAT current source, IDESAT = '00'                                   | -290  | -250  | -241  | μA   |
|                                      | DESAT current source, IDESAT = '01' (default)                         | -570  | -500  | -468  | μA   |
|                                      | DESAT current source, IDESAT = '10'                                   | -841  | -750  | -705  | μA   |
|                                      | DESAT current source, IDESAT = '11'                                   | -1112 | -1000 | -935  | μA   |
| $I_{DESAT\_OFF}$                     | DESAT and Segmented Drive blanking discharge current <sup>[1]</sup>   | 45    | 70    | 90    | mA   |
| $t_{DESAT\_LEB}$                     | DESAT leading edge blanking time, DESAT_LEB = '000'                   | 53    | 60    | 88    | ns   |
|                                      | DESAT leading edge blanking time, DESAT_LEB = '001'                   | 111   | 120   | 149   | ns   |
|                                      | DESAT leading edge blanking time, DESAT_LEB = '010'                   | 170   | 180   | 211   | ns   |
|                                      | DESAT leading edge blanking time, DESAT_LEB = '011' (default)         | 228   | 240   | 273   | ns   |
|                                      | DESAT leading edge blanking time, DESAT_LEB = '100'                   | 325   | 340   | 376   | ns   |
|                                      | DESAT leading edge blanking time, DESAT_LEB = '101'                   | 441   | 460   | 500   | ns   |
|                                      | DESAT leading edge blanking time, DESAT_LEB = '110'                   | 558   | 580   | 623   | ns   |
|                                      | DESAT leading edge blanking time, DESAT_LEB = '111'                   | 674   | 700   | 747   | ns   |
| $t_{DESAT\_FLT}$                     | Desaturation detection filter time, DESAT_FLT = '00'                  | 64    | 70    | 97    | ns   |
|                                      | Desaturation detection filter time, DESAT_FLT = '01' (default)        | 103   | 110   | 138   | ns   |
|                                      | Desaturation detection filter time, DESAT_FLT = '10'                  | 180   | 190   | 221   | ns   |
|                                      | Desaturation detection filter time, DESAT_FLT = '11'                  | 275   | 300   | 325   | ns   |
| $V_{DESAT\_TH}$                      | Desaturation detection voltage threshold, DESAT_TH = '0000'           | 0.94  | 1.00  | 1.09  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '0001'           | 1.44  | 1.50  | 1.58  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '0010'           | 1.93  | 2.00  | 2.10  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '0011'           | 2.43  | 2.50  | 2.60  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '0100'           | 2.90  | 3.00  | 3.10  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '0101'           | 3.40  | 3.50  | 3.60  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '0110'           | 3.90  | 4.00  | 4.12  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '0111'           | 4.40  | 4.50  | 4.62  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '1000'           | 4.90  | 5.00  | 5.13  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '1001'           | 5.40  | 5.50  | 5.65  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '1010' (default) | 5.85  | 6.00  | 6.15  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '1011'           | 6.35  | 6.50  | 6.65  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '1100'           | 6.85  | 7.00  | 7.15  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '1101'           | 7.80  | 8.00  | 8.16  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '1110'           | 8.80  | 9.00  | 9.20  | V    |
|                                      | Desaturation detection voltage threshold, DESAT_TH = '1111'           | 9.76  | 10.0  | 10.20 | V    |

[1]  $V_{DESAT} = 8.0$  V

## 9.6 VCE overvoltage protection

The following table shows the electrical characteristics associated with active VCE clamping.

**Table 17. Active  $V_{CE}$  clamping electrical characteristics**

$V_{DD}$ ,  $V_{CC}$ ,  $V_{CCREG}$ ,  $V_{EE}$  in regulation,  $T_J = -40$  to  $150$  °C, unless otherwise specified. All voltages referenced to GND2, unless otherwise specified. Currents are positive into and negative out of the specified pins.

| Symbol  | Parameter   | Min   | Typ   | Max   | Unit |
|---|---|-------|-------|-------|------|
| <b>VCE clamping operation</b>                 |   |       |       |       |      |
| $V_{CECL\_TH}$                                | VCE clamping threshold (rising edge) <sup>[1]</sup>                           | 2.125 | 2.50  | 2.875 | V    |
| $V_{CECL\_TH\_HYS}$                           | VCE clamp threshold hysteresis  | 0.300 | 0.410 | 0.520 | V    |
| $t_{VCECL}$                                   | VCE clamp intervention time   | —     | 40    | 50    | ns   |
| $t_{VCECR}$                                   | VCE clamp intervention release time (TIME_2 = 1) <sup>[2]</sup>               | 97    | 100   | 117   | ns   |
|   | VCE clamp intervention release time (TIME_2 = 0) <sup>[2]</sup>               | 194   | 200   | 235   | ns   |
| $t_{VCECR\_MAX}$                              | Maximum VCE clamp intervention release time                                   | 970   | 1000  | 1060  | ns   |
| <b>Segmented drive operation</b>              |   |       |       |       |      |
| $I_{VCESEN}$                                  | VCE sense current source for segmented drive                                  | −25   | −20   | −17   | mA   |
| $t_{segdrv\_filt}$                            | Segmented drive deglitch filter   | 60    | 80    | 100   | ns   |
| $t_{SEGDRVLY}$                                | Segmented drive activation delay, SEGDRVLY = '000' (default)                  | —     | 0     | —     | ns   |
|   | Segmented drive activation delay, SEGDRVLY = '001'                            | 14    | 20    | 46    | ns   |
|   | Segmented drive activation delay, SEGDRVLY = '010'                            | 34    | 40    | 67    | ns   |
|   | Segmented drive activation delay, SEGDRVLY = '011'                            | 53    | 60    | 88    | ns   |
|   | Segmented drive activation delay, SEGDRVLY = '100'                            | 73    | 80    | 108   | ns   |
|   | Segmented drive activation delay, SEGDRVLY = '101'                            | 92    | 100   | 129   | ns   |
|   | Segmented drive activation delay, SEGDRVLY = '110'                            | 111   | 120   | 149   | ns   |
|   | Segmented drive activation delay, SEGDRVLY = '111'                            | 131   | 140   | 170   | ns   |
| $V_{SEGDRV\_TH}$                              | Segmented drive voltage threshold, SEGDRV_TH = '000' <sup>[3]</sup>           | 2.85  | 3.00  | 3.15  | V    |
|   | Segmented drive voltage threshold, SEGDRV_TH = '001' <sup>[3]</sup>           | 3.80  | 4.00  | 4.20  | V    |
|   | Segmented drive voltage threshold, SEGDRV_TH = '010' <sup>[3]</sup>           | 4.75  | 5.00  | 5.25  | V    |
|   | Segmented drive voltage threshold, SEGDRV_TH = '011' (default) <sup>[3]</sup> | 5.70  | 6.00  | 6.30  | V    |
|   | Segmented drive voltage threshold, SEGDRV_TH = '100' <sup>[3]</sup>           | 6.65  | 7.00  | 7.35  | V    |
|   | Segmented drive voltage threshold, SEGDRV_TH = '101' <sup>[3]</sup>           | 7.60  | 8.00  | 8.40  | V    |
|   | Segmented drive voltage threshold, SEGDRV_TH = '110' <sup>[3]</sup>           | 8.55  | 9.00  | 9.45  | V    |
|   | Segmented drive voltage threshold, SEGDRV_TH = '111' <sup>[3]</sup>           | 9.50  | 10.0  | 10.5  | V    |
| $t_{SSD\_SEG}$<br>(TIME_2 = 1) <sup>[2]</sup> | Soft shutdown time for SEGDRV SSD   | 330   | 340   | 350   | ns   |
| $t_{SSD\_SEG}$<br>(TIME_2 = 0) <sup>[2]</sup> | Soft shutdown time for SEGDRV SSD   | 620   | 640   | 680   | ns   |

[1] Referenced to VEE

[2] TIME\_2 is Timer scaling bit of [MODE1 register](#)

[3] Referenced to GND2

## 9.7 Power device overtemperature

Table 18 shows the electrical characteristics specific to the external power device overtemperature detection block.

**Table 18. Power device overtemperature electrical characteristics**

VDD, VCC, VCCREG, VEE in regulation,  $T_J = -40$  to  $150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.

| Symbol                                 | Parameter  | Min                                 | Typ    | Max     | Unit |
|--|--|-------------------------------------|--------|---------|------|
| $t_{OT\_FILT}$                         | IGBT overtemperature shutdown fault filter time                  | 1.9                                 | 2.0    | 2.1     | ms   |
| $t_{OTW\_FILT}$                        | IGBT overtemperature warning fault filter time                   | 1.9                                 | 2.0    | 2.1     | ms   |
| <b>Current source when TISNS = '1'</b> |  |                                     |        |         |      |
| $I_{OT}$                               | IGBT temperature sense current reference, ITSNS = '00'           | <sup>[1]</sup> -0.2625              | -0.25  | -0.2375 | mA   |
|  | IGBT temperature sense current reference, ITSNS = '01'           | <sup>[1]</sup> -0.525               | -0.500 | -0.475  | mA   |
|  | IGBT temperature sense current reference, ITSNS = '10'           | <sup>[2]</sup> -0.7875              | -0.750 | -0.7125 | mA   |
|  | IGBT temperature sense current reference, ITSNS = '11' (default) | <sup>[3]</sup> -1.050               | -1.000 | -0.950  | mA   |
| $I_{OT\_TVAR}$                         | Sense current variation with temperature                         | -1.5                                | —      | 1.5     | %    |
| <b>TSENSEA offset settings</b>         |  |                                     |        |         |      |
| $T_{OSET}$                             | TSENSEA GND offset, TOFST = '00'                                 | <sup>[4]</sup> -0.006               | 0.0    | 0.006   | V    |
|  | TSENSEA GND offset, TOFST = '01'                                 | <sup>[4]</sup> <sup>[5]</sup> 0.477 | 0.50   | 0.507   | V    |
|  | TSENSEA GND offset, TOFST = '10'                                 | <sup>[4]</sup> <sup>[5]</sup> 0.968 | 1.000  | 1.008   | V    |
|  | TSENSEA GND offset, TOFST = '11'                                 | <sup>[4]</sup> <sup>[5]</sup> 1.467 | 1.500  | 1.517   | V    |

[1]  $0 \leq V_{TSENSEA} \leq 4.0$  V

[2]  $0 \leq V_{TSENSEA} \leq 3.9$  V

[3]  $0 \leq V_{TSENSEA} \leq 3.75$  V

[4] Includes offset error specified at  $\pm 1$  mV

[5] Includes gain error specified at  $\pm 1$  %

## 9.8 IC overtemperature

**Table 19. IC overtemperature electrical characteristics**

VCC, VCCREG in regulation,  $T_J = -40$  to  $+150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.

| Symbol                                   | Parameter  | Min   | Typ   | Max   | Unit   |
|--|--|-------|-------|-------|--------|
| $V_{FTSENSEIC}$                          | Temperature sense diode forward voltage <sup>[1]</sup> | 3.30  | 3.42  | 3.54  | V      |
| $R_{TSENSEIC}$                           | Temperature coefficient of sense diode <sup>[2]</sup>  | -2.10 | -2.00 | -1.90 | LSB/°C |
| <b>Overtemperature filter time of IC</b> |  |       |       |       |        |
| $t_{OTICfilt}$                           | Overtemperature filter time of IC                      | 16    | 20    | 24    | μs     |

[1] Junction temperature =  $25$  °C

[2] Guaranteed by design

## 9.9 AMUX and ADC electrical characteristics

**Table 20. AMUX and ADC electrical characteristics**

$V_{DD}$ ,  $V_{CC}$ ,  $V_{CCREG}$ ,  $V_{EE}$  in regulation,  $T_J = -40$  to  $+150$  °C, unless otherwise specified. All voltages referenced to GND2. Currents are positive into and negative out of the specified pins.  $0\text{ V} \leq V_{TSENSEA} \leq V_{REF}$ ,  $0\text{ V} \leq V_{AMUXIN} \leq V_{REF}$ ,  $V_{CC_{UV\_TH}} \leq V_{VCC} \leq 25\text{ V}$ ,  $Z_{IN} \leq 10\text{ K}$

| Symbol            | Parameter  | Min    | Typ   | Max   | Unit |
|-------------------|--|--------|-------|-------|------|
| $C_{AMUXIN}$      | AMUXIN input capacitance [1]                           | —      | 4.5   | 8.0   | pF   |
| $AMUXIN_{LK}$     | AMUXIN input leakage current [2]                       | -2.0   | —     | 2.0   | μA   |
| $t_{conv}$        | ADC conversion time [3]                                | —      | 3.0   | 5     | μs   |
| $V_{CC_{ACC}}$    | VCC measurement accuracy (with 30x attenuation) [4]    | -3.0   | —     | +3.0  | %    |
| $V_{CCREG_{ACC}}$ | VCCREG measurement accuracy (with 30x attenuation) [5] | -3.0   | —     | +3.0  | %    |
| $V_{EE_{ACC}}$    | VEE measurement accuracy (with 15x attenuation) [6]    | -3.0   | —     | +3.0  | %    |
| $V_{OS}$          | AMUX GND offset, AMUXINOS = '00' [7]                   | -0.006 | 0.0   | 0.006 | V    |
|                   | AMUX GND offset, AMUXINOS = '01' [7] [8]               | 0.477  | 0.50  | 0.507 | V    |
|                   | AMUX GND offset, AMUXINOS = '10' [7] [8]               | 0.968  | 1.000 | 1.008 | V    |
|                   | AMUX GND offset, AMUXINOS = '11' [7] [8]               | 1.467  | 1.500 | 1.517 | V    |
| $E_{DNL}$         | Differential linearity error [9] [10]                  | < -1   | —     | 1.0   | LSB  |
| $E_{INL}$         | Integral linearity error (best fit) [10] [11]          | -1.5   | —     | 1.5   | LSB  |
| $E_{ZOE}$         | Zero offset error [10] [12]                            | -2.0   | —     | 2.0   | LSB  |
| $TE$              | ADC total error [10] [13] [14]                         | -3.0   | —     | 3.0   | LSB  |
| $TE_{TVAR}$       | ADC total error variation with temperature [10] [1]    | -1.5   | —     | 1.5   | LSB  |
| $E_{scale}$       | Scale factor error [10] [15]                           | -1.0   | —     | 1.0   | LSB  |

[1] Guaranteed by design

[2]  $0 \leq V_{AMUXIN} \leq V_{REF}$

[3]  $Z_{in} \leq 10\text{ k}\Omega$

[4]  $V_{CC_{UV\_TH}} \leq V_{VCC} \leq 25\text{ V}$

[5]  $V_{CCREG_{UV\_TH}} \leq V_{VCCREG} \leq 25\text{ V}$

[6]  $-15\text{ V} \leq V_{VEE} \leq -1\text{ V}$ , the  $\pm 2$  LSB ADC Zero specification adds an effective  $\pm 30\text{ mV}$  offset

[7] Includes offset error specified at  $\pm 1\text{ mV}$

[8] Includes gain error specified at  $\pm 1\%$

[9] Deviation in code width from the ideal 1LSB code width. No missing codes.

[10] Testing is performed without PWM signal switching in static operation.

[11] Maximum deviation of a transition point from the corresponding point of the ideal transfer curve, with the measured offset and gain errors zeroed.

[12] Difference between the first measured transition point (lowest in voltage) and the first ideal transition point.

[13]  $0 \leq V_{AMUXIN} \leq V_{TSENSEA} < V_{REF}$  with AMUXRNG = 0 and AMUXINOS = '00';  $V_{CC_{UV\_TH}} \leq V_{VCC} \leq 25\text{ V}$ ;  $Z_{in} \leq 10\text{ k}\Omega$

[14] This error does not take VREF accuracy into account.

[15] Difference between the ideal slope between zero and full-scale and the actual slope between the measured zero point and full-scale.

## 9.10 LV/HV domain communications

**Table 21. LV/HV domain communications**

$V_{DD}$ ,  $V_{CC}$ ,  $V_{CCREG}$ ,  $V_{EE}$  in regulation,  $T_J = -40$  to  $+150$  °C, unless otherwise specified. All voltages referenced to GND1. Currents are positive into and negative out of the specified pins.

| Symbol                                     | Parameter                           | Limit value |     |     | Unit |
|--|-------------------------------------|-------------|-----|-----|------|
|  |                                     | Min         | Typ | Max |      |
| Low voltage to high voltage communications |                                     |             |     |     |      |
| t <sub>WDrefresh</sub>                     | LV domain watchdog refresh interval | 189         | 200 | 232 | μs   |

**Table 21. LV/HV domain communications...continued**  
*VDD, VCC, VCCREG, VEE in regulation, T<sub>J</sub> = -40 to +150 °C, unless otherwise specified. All voltages referenced to GND1. Currents are positive into and negative out of the specified pins.*

| Symbol                 | Parameter                     | Limit value |      |      | Unit |
|------------------------|-------------------------------|-------------|------|------|------|
|                        |                               | Min         | Typ  | Max  |      |
| t <sub>WDtimeout</sub> | Watchdog timeout, WDTO = '00' | [1] 247     | 260  | 294  | μs   |
| t <sub>WDtimeout</sub> | Watchdog timeout, WDTO = '01' | [2] 480     | 500  | 541  | μs   |
| t <sub>WDtimeout</sub> | Watchdog timeout, WDTO = '10' | [3] 965     | 1000 | 1056 | μs   |
| t <sub>WDtimeout</sub> | Watchdog timeout, WDTO = '11' | [4] 1935    | 2000 | 2086 | μs   |

[1] Minimum SPI freq = 450 kHz  
[2] Minimum SPI freq = 90 kHz  
[3] Minimum SPI freq = 35 kHz  
[4] Default minimum SPI freq = 15 kHz

## 10 Functional description

### 10.1 Device overview

The GD3160 is designed for a wide range of IGBT/SiC voltage ratings. Its logic interface and feedback signals are galvanically isolated from the high-voltage circuitry that directly drives the IGBT gate and monitors its temperature sense, DESAT, CLAMP, and current sense pins.

The GD3160 possesses two isolated domains, each with its own GND reference. Control and fault signals are transmitted between the non-isolated, low-voltage domain (LV domain, facing the MCU) and the isolated, high-voltage domain (HV domain, facing the power device) via magnetic coupling. GND1 must be connected to the logic controller's GND. GND2 must be connected to the power device emitter/source.

Pins 1 through 16 are connected to the low-voltage domain. These pins provide interface to all the control, programming, fault monitoring and fail-safe features. A power supply connected to the VSUP or VDD pins provide power for the GD3160's low-voltage domain. The GD3160 contains either a 3.3 V or 5.0 V regulator determining the low-voltage logic level used, depending on the part number ordered.

Pins 17 through 32 are connected to the high-voltage domain. These pins provide the interface to the IGBT/SiC gate, its power supplies and terminals (collector sense, temperature sense and current sense). A power supply connected to the VCC pin provides power for the GD3160's high-voltage domain.

VCC and VEE are the positive and negative power supplies used to charge and discharge the IGBT/SiC gate. VCCREG is the output of a post regulator, providing the positive gate supply voltage. This regulator may be used to alleviate VCC power supply requirements and minimize positive supply voltage variation when multiple gate voltage supplies are generated from a single source.

The gate-drive stage consists of three transistors and a current source. The GH transistor is a high-current pullup (gate charging) transistor connected between VCCREG and the GH pin. Pins GL and AMC are separate transistors that provide gate discharge paths. GL acts as the primary turn-off path with an external resistor used to control discharge current. The AMC pin directly monitors the gate voltage and provides an active Miller clamp, which holds the IGBT/SiC gate at the lowest gate supply while Off. The GH, GL, and AMC transistors are capable of currents up to 15 A for 2.0  $\mu$ s. There is also a soft shutdown current source in parallel with the GL transistor, which provides a slower gate discharge during a fault condition. Fault conditions may also trigger a two-level turn-off (2LTO), which decreases the IGBT's/SiC gate voltage while the possible fault is being validated. Reducing the gate voltage limits the maximum fault current and thereby reduces the safe operating area stress on the IGBT/SiC.

The GD3160 can be used with or without a negative gate drive voltage. Negative gate voltage is often used to ensure an IGBT/SiC is kept off when its opposing IGBT/SiC is turning on. However, using a negative supply increases gate drive losses and increases gate-drive power supply complexity. Using a low impedance turn-off circuit (such as the integrated AMC feature) is another way to alleviate or eliminate the problem of dV/dt induced turn on.

By monitoring the IGBT/SiC collector-emitter voltage through external circuitry, the GD3160 provides two critical protections and reports the VCE status:

1. When the IGBT/SiC is commanded on, its  $V_{CE}$  should be only a few volts, at most. A short-circuit condition causes the  $V_{CE}$  to exceed its normal on-state voltage. The GD3160's  $V_{CE}$  desaturation detection circuitry monitors  $V_{CE}$  for this condition.
2. Advanced active clamp techniques used by the GD3160 turn the gate Off at a reduced, controlled current when excessive  $V_{CE}$  is present. Reducing the gate discharge current reduces the collector-emitter overshoot, improves clamping tolerance, and reduces the size of the Zeners.
3. The VCE state may be reported through INTA, for precision motor control applications.

The current sense pin, ISENSE, can be used to monitor the sense cells of any power device with a current mirror, enabling quicker detection (when compared to desaturation detection) in response to a severe short-circuit or overcurrent condition.

The GD3160 also monitors power device temperature via temperature sense diodes, NTC, or PTC resistors and offers user-programmable overtemperature warning and shutdown. The temperature data or status may be reported via SPI. The GD3160's AMUXIN pin also allows measurement of other system parameters from the HV domain. These, as well as the power device temperature, may be reported through the SPI interface, or provided as a duty cycle encoded signal at the AOUT pin.

The GD3160 reports faults and status in multiple ways. The active-low INTB and INTA pins allow exclusive reporting of faults on either channel, allowing prioritization in the reported faults. Additionally, INTA may be configured instead for real-time VGE or VCE reporting for precision motor control applications. The SPI can also report fault details, as well as all status and configuration information.

10.2 State diagram

Figure 4 shows the power-up and power-down behavior and how the GD3160 transitions from state to state. The Normal mode is the only state in which the PWM pin directly controls IGBT's gate.

The PWM pin need not be Logic 0 to enter the Configuration mode, although this is highly recommended. When entering Normal mode from any state, the GD3160 immediately responds to the state of the PWM pin. A rising edge of PWM is not needed to re-enable PWMing.

10.2.1 Main domain state diagram

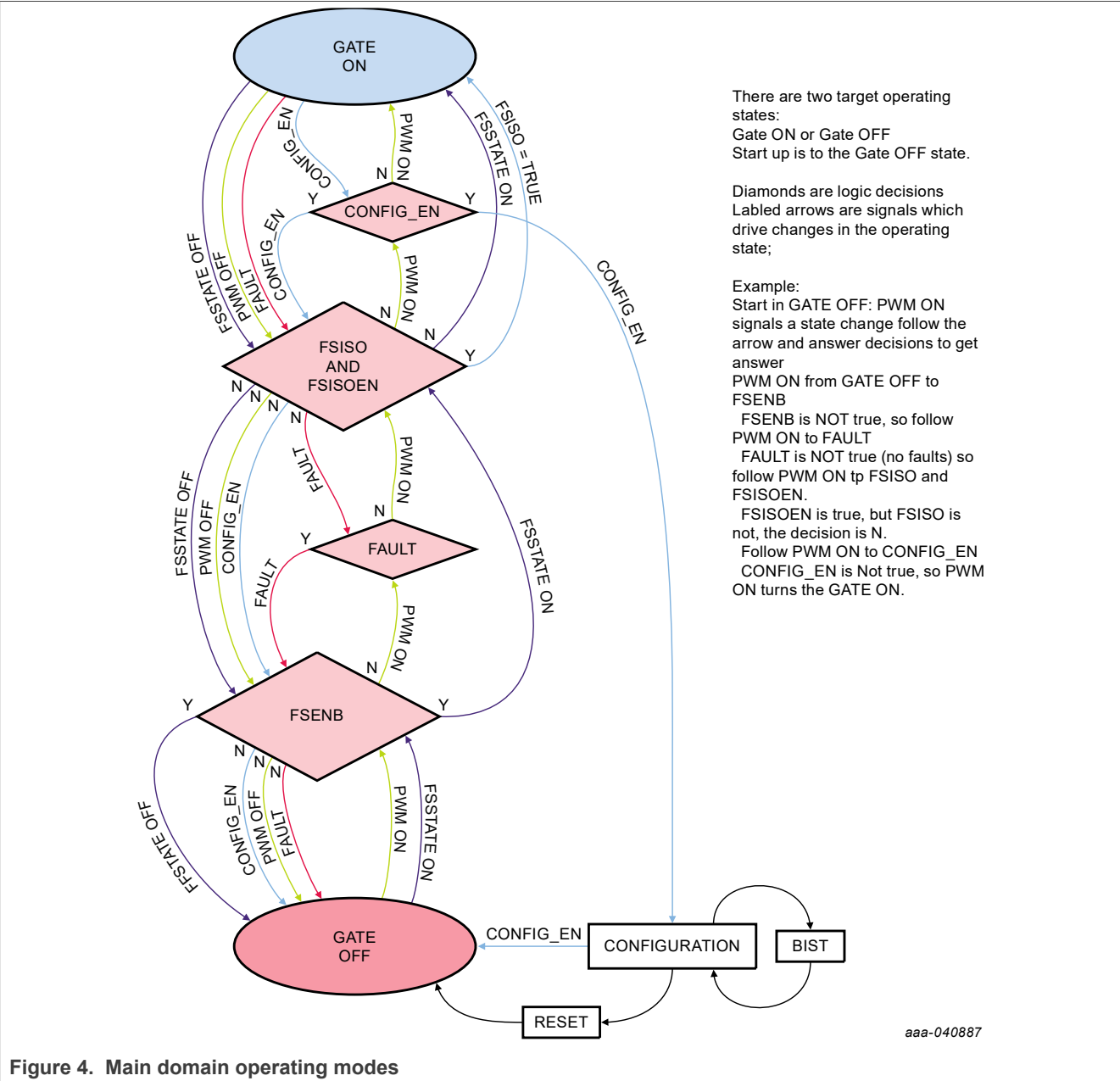


Figure 4. Main domain operating modes

## 11 Functional block operation

### 11.1 Power management

#### 11.1.1 Introduction

Because the GD3160 has integrated signal isolation, it has isolated ground references (GND1 and GND2) for both the low-voltage domain and the high-voltage domain. Ground reference for the low-voltage, non-isolated pins (pins 1 to 16) is GND1. Specifications use GND1 terminal as the reference pin for all low-voltage pins. GND2 is the reference for all isolated pins (pins 17 to 32).

VSUP (or VDD/VSUP) provides power for the low-voltage domain, which contains all the non-isolated circuitry. When power is provided by VSUP, an internal regulator provides 3.3 V or 5.0 V at VDD. The VDD regulator is not intended to power other external circuitry. In this configuration, the VDD pins of different GD3160's should not be connected together.

The GD3160 is available in two options: VDD of 3.3 V or 5.0 V. The two options are desired to allow interfacing to MCUs with 3.3 V or 5.0 V I/O.

- If VDD is 3.3 V, then the user must supply VSUP with a voltage source 4.5 V or greater, usually from a battery in a vehicle or a 5 V post-regulated supply. In this case, power for VDD is always derived from VSUP; an external VDD supply is not allowed. The MGD3160AM315EK, MGD3160AM318EK, MGD3160AM335EK, or MGD3160AM318EK cannot be powered exclusively by VDD = 3.3 V.
- If VDD is 5.0 V, the IC can be powered from a single voltage source at VSUP (usually from a vehicle battery or other post-regulated source). In this case, VDD is derived from VSUP. With 5.0 V VDD, the IC may also be powered from a single 5.0 V source. In this case, VSUP and VDD must be connected together on the PCB. This disables and bypasses the internal VDD regulator as the VSUP never surpasses  $VSUP_{UV\_TH}$ .

The isolated circuitry (on the high voltage domain) is powered by the VCC supply, which must be referenced to GND2. An on-board regulator (VCCREG) provides the option of post regulating the VCC supply. If this post regulator is not used, the VCC and VCCREG pins should be connected together on the PCB.

The GD3160's GND2 terminal should be connected to the IGBT's emitter sense terminal. A direct connection to the emitter is preferred.

The GD3160 can be used with or without a negative gate drive supply. If this supply is desired, the negative supply must be connected to the VEE pin and referenced to GND2. If it is not needed, the VEE pin must be connected to the GND2 pin. Each power management block also includes a 50 MHz clock for each voltage domain's logic.

#### 11.1.2 Power sources and regulators

The primary power supplies and voltage regulators and their uses are shown in the following table.

**Table 22. Power supplies and their functions**

| Power supply name | Purpose   | Nominal voltage                        | Reference mode | Maximum current | Externally supplied or internally generated                      |
|-------------------|---|--|----------------|-----------------|--|
| VSUP              | LV domain power source  | Vehicle battery                        | GND1           | —               | External   |
| VDD               | 3.3 V or 5.0 V regulator for internal use                           | 5.0 V (GD3160EK)<br>3.3 V (GD3160A3EK) | GND1           | —               | Internally derived from VSUP<br>5.0 V can be provided externally |
| VCC               | HV domain power source  | 17 V                                   | GND2           | —               | External   |
| VCCREG            | Positive gate supply  | 15 V                                   | GND2           | 100 mA          | External/Internal  |
| VEE               | Negative gate supply  | 0 V, -3.0 or -8.0 V                    | GND2           | —               | External   |
| VREF              | Internal 5.0 V regulator that can supply 20 mA to external circuits | 5.0 V                                  | GND2           | 20 mA           | Internal, from VCC   |

### 11.1.3 Recommended external capacitance

[Table 23](#) provides guidelines for the external capacitance used for the supplies and integrated regulators.

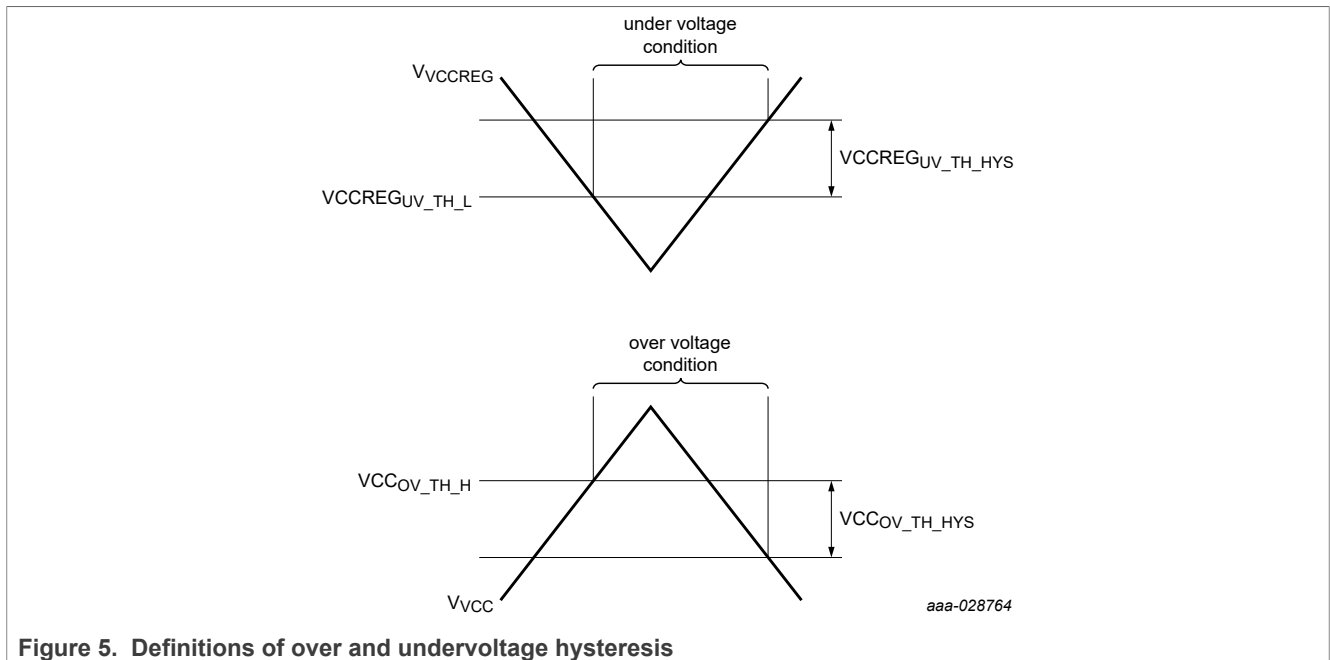
**Table 23. Recommended external capacitors**

| Symbol              | Description                      | Min  | Typ | Max | Unit | Notes/conditions  |
|---------------------|----------------------------------|------|-----|-----|------|---|
| C <sub>VSUP</sub>   | External capacitance VSUP-GND1   | 0.47 | 1   | 15  | μF   | For VDD regulator active (VSUP and VDD not connected): recommended separate capacitors (all MLCC, X7R) for best EMC performance: 10.0 μF and 0.1 μF in parallel.<br>For VDD regulator inactive (VSUP-VDD connected): recommended separate capacitors (all MLCC, X7R) for best EMC performance: 1.0 μF and 0.1 μF in parallel. |
| C <sub>VDD</sub>    | External capacitance VDD-GND1    | 0.47 | 1.1 | 2   | μF   | Recommended 1 μF (MLCC, X7R) for best EMC performance.  |
| C <sub>VCC</sub>    | External capacitance VCC-GND2    | 4.7  | —   | 10  | μF   | When VCC is not connected to VCCREG: recommended separate capacitors (all MLCC, X7R) for best EMC performance: 4.7 μF and 0.1 μF in parallel.   |
| C <sub>VCCREG</sub> | External capacitance VCCREG-GND2 | 4.7  | —   | 40  | μF   | Recommended separate capacitors (all MLCC, X7R) for best EMC performance: 4 μF x 4.7 μF and 0.1 μF in parallel.   |
| C <sub>VREF</sub>   | External capacitance VREF-GND2   | 0.47 | 1   | 2   | μF   | Recommended for best EMC performance 1.0 μF MLCC, X7R.  |
| C <sub>VEE</sub>    | External capacitance VEE-GND2    | 4.7  | —   | 10  | μF   | Recommended separate capacitors (all MLCC, X7R) for best EMC performance: 4.7 μF and 0.1 μF in parallel.  |

### 11.1.4 OV and UV threshold description

The GD3160 has overvoltage and undervoltage monitoring for its key power supplies: VSUP, VDD, VCC, VCCREG, and VREF. The exception to this rule is that VCCREG has no overvoltage monitoring because the VCC overvoltage circuit provides that protection. Some of the undervoltage or overvoltage circuits are used to control internal signals and do not create faults. For example, the VSUP undervoltage circuit does not create a fault; it is used to enable/disable the VDD regulator.

The over and undervoltage threshold specifications are defined in [Figure 5](#).



**Figure 5. Definitions of over and undervoltage hysteresis**

If  $V_{VCC}$  exceeds  $VCC_{OV\_TH}$ , the IGBT is latched off, and the fault bit is latched and reported via SPI and the INTA/INTB pins. LV/HV domain communications continue to run.

### 11.1.5 Power supply sequencing of the low-voltage domain

When voltage is applied to the VSUP (or VSUP/VDD if the pins are connected) at power up, internal logic supplies of the low-voltage domain turn on with the rise of VSUP. Once VSUP exceeds  $VSUP_{UV\_TH}$ , the VDD regulator is enabled.

When VDD exceeds  $VDD_{UV\_TH}$ , the low-voltage domain begins periodically sending a REQADC command (Request ADC) and monitoring the high-voltage domain's response. When the low-voltage domain receives a valid response from the high-voltage domain's, the low-voltage domain enters Normal mode state and is able to PWM the IGBT.

The power-up timing diagrams of the low-voltage domain are shown below. The two configurations shown are with and without the VSUP and VDD pins connected on the circuit board.

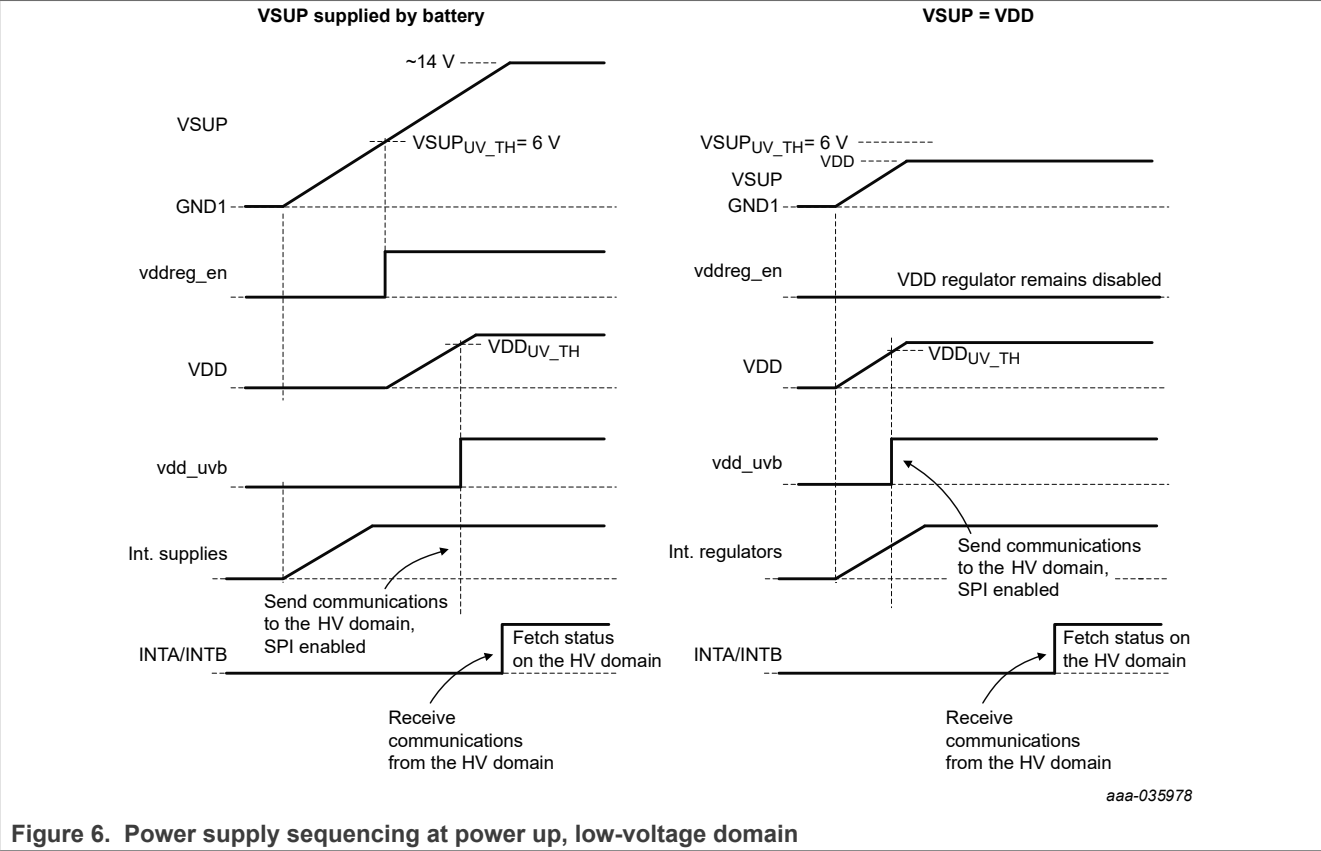


Figure 6. Power supply sequencing at power up, low-voltage domain

When VSUP voltage falls below  $VSUP_{UV\_TH}$  at power down, the VDD regulator is disabled. When VDD equals  $VDD_{UV\_TH}$  or below, the low-voltage domain no longer sends or receives SPI messages. Once VDD voltage falls below  $VDD_{UV\_TH}$ , the low-voltage domain no longer sends messages to or receives messages from the high-voltage domain. In addition, the low-voltage domain activates INTA or INTB as the internal power supplies allow.

The low-voltage domain power down timing diagrams are shown in [Figure 7](#).

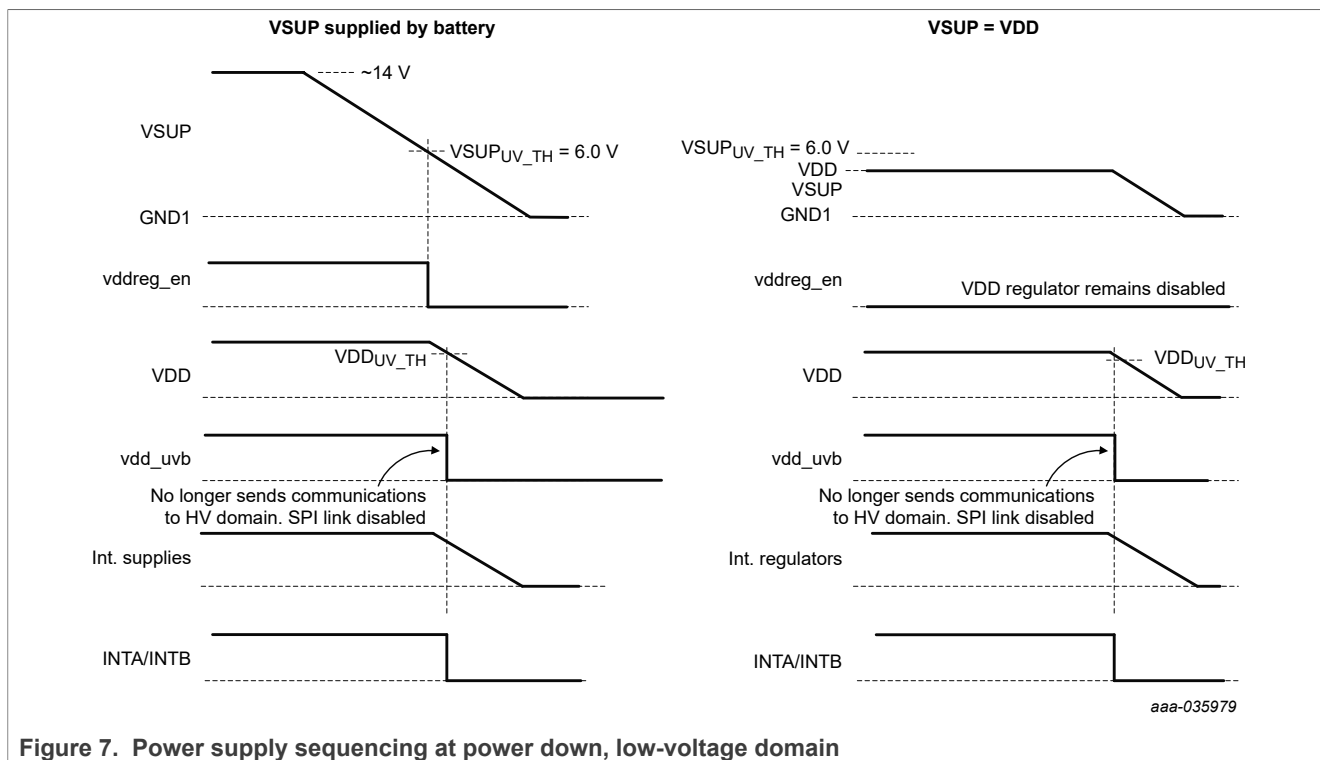


Figure 7. Power supply sequencing at power down, low-voltage domain

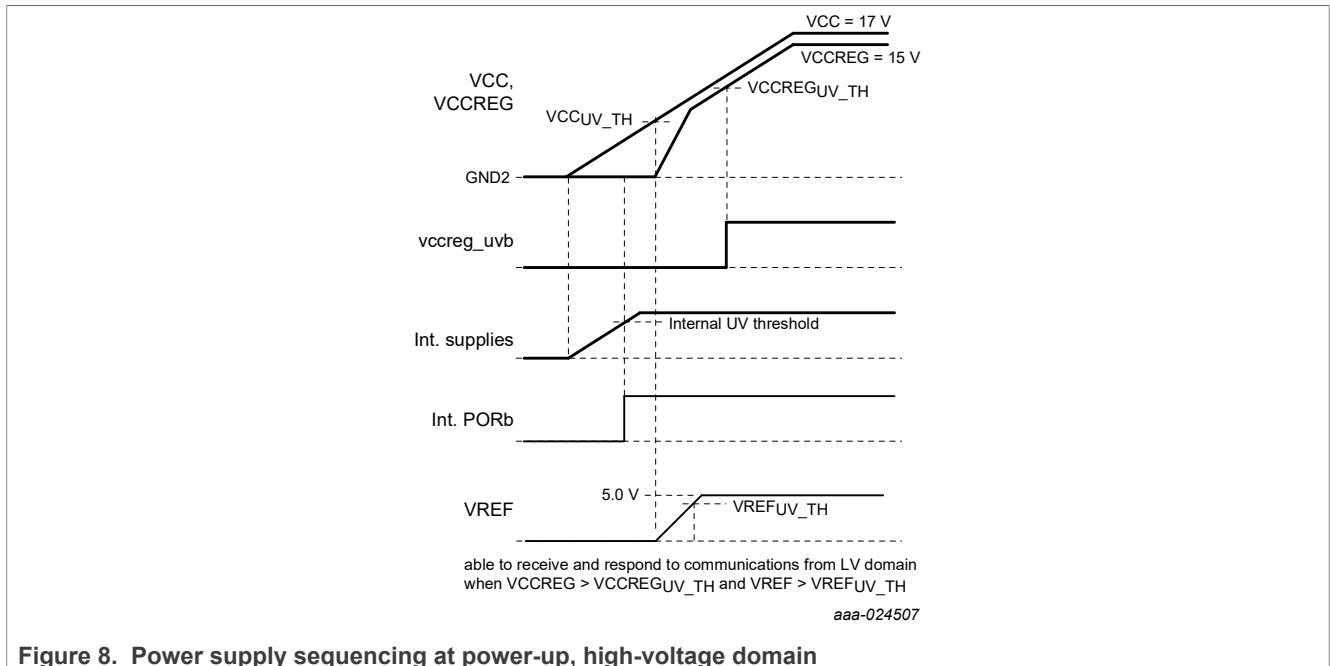
### 11.1.6 Power supply sequencing of the high-voltage domain

When voltage is applied to the VCC pin at power up, the internal logic supplies power up as VCC increases. When  $V_{VCC}$  exceeds  $V_{VCC\_UV\_TH}$  and the internal logic supplies are in regulation, the VCCREG and VREF regulators are enabled.

Once  $V_{VCCREG}$  exceeds  $V_{VCCREG\_UV\_TH}$  and  $V_{VREF}$  exceeds  $V_{VREF\_UV\_TH}$ , the high-voltage domain responds to PWM signals and DATA\_IN messages. In addition, the high-voltage domain begins reporting the fault status via the INT\_VGE communications link.

When VREF is in an undervoltage condition at power up (either slow to rise or too heavily loaded), the IGBT's gate is turned off and the high-voltage domain DATA communication remains disabled. In this VREF\_UV condition, OC, DESAT and VCC\_OV faults are disabled. As the ADC is also disabled, OT and OTW cannot be tripped.

The power-up timing diagram of the high-voltage domain is shown in [Figure 8](#).



**Figure 8. Power supply sequencing at power-up, high-voltage domain**

During decreasing VCC supply voltages, the internal logic supplies remain powered until they reach their POR levels. The high-voltage domain continues to respond to PWM or FSSTATE signals until VCCREG falls below VCCREG<sub>UV\_TH</sub>. The high-voltage domain continues to respond to DATA\_IN messages until the high-voltage domain internal logic supply falls below its POR threshold.

When VREF is in an undervoltage condition after power up (it had been in regulation), the IGBT's gate is turned off (unless FSISO is active high, and had been enabled), the ADC conversions return 000h and LV/HV domain communications remain enabled along with fault reporting via the SPI and via the INTA/INTB pins.

When VCCREG is in an undervoltage condition, the IGBT gate is turned off, unless FSISO is active and enabled. The VCCREG undervoltage fault is reported via the SPI and the INTA/INTB pins (per configuration).

A VCCREGUV fault will also be latched if VCC falls below VCC<sub>UV\_TH</sub> when VCCREGUV fault is masked.

The power-down timing diagram of the high-voltage domain is shown in [Figure 9](#).

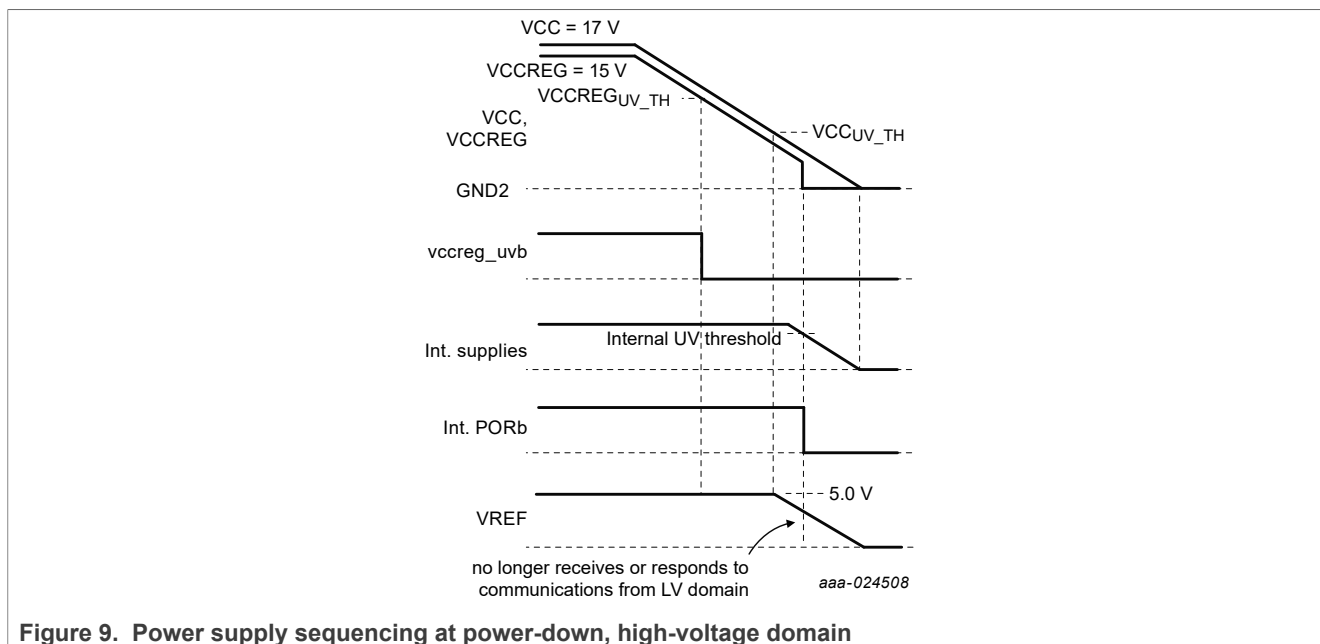


Figure 9. Power supply sequencing at power-down, high-voltage domain

### 11.1.7 Fault management at power up

The GD3160, in conjunction with the system's control logic, must maintain control of its IGBT's gate during adverse conditions, including power up. This includes the case when the controlling MCU is operating normally, as well as when it is faulted.

The GD3160's role is to maintain control of the IGBT gate during power up and power down and to respond to the logic signals from the control logic once all supplies are in regulation.

A special requirement of the GD3160 is that it must be able to respond to the safing logic and possibly turn on its IGBT even when the system's MCU is not operational. Because the safing logic may not have SPI capability, the safing logic may be incapable of clearing any latched faults that would disallow turning on the IGBT gate. Therefore, at power up, the GD3160 must not latch any false faults that may appear as regulators and references stabilize. It must power up in a non-faulted state if it is not faulted.

To avoid spurious latched faults at power up, faults are ignored until after all the power supplies and regulators (VDD, [VCCREG](#) and VREF) are in regulation. For example, at power up, LV/HV domain communication faults and SPI faults are not latched. Faults associated with the IGBT, such as overcurrent, short-circuit,  $V_{CE}$  desaturation, are managed similarly. These faults are latched only after power up. In summary, until all supplies are regulation, the IGBT's gate is disabled; after power up, latched faults disable the gate.

A watchdog fault will latch when VSUP, VDD, VCC, or VREF falls below POR threshold voltage levels and exceeds the programmable watchdog timeout duration. See [CONFIG6](#) register.

LV die and HV die registers reset to default values if supplies fall below POR threshold levels, but no watchdog fault is latched if the supply is recovered during the watchdog timeout period.

### 11.1.8 High-voltage domain supplies and monitors

Figure 10 provides a block diagram of the high-voltage domain supplies, regulators, and monitoring circuits.

VCC has fixed overvoltage and undervoltage thresholds, with programmable fault report mask capability. VREF has a similar fixed undervoltage threshold and programmable fault report mask capability.

The VCCREG pin integrates a regulator providing a stable and protected positive gate supply to the power device. The output voltage is programmable by VCCREG[2:0], and is protected by a configurable undervoltage threshold, determined by UV\_TH[2:0]. Undervoltage behavior is provided by the UV\_LATCH bit.

The VEE\_OORM bit in the MSK2 register enables/disables the VEE monitoring circuitry. When the fault monitoring is enabled (VEE\_OORM = 1), the GD3160 monitors the VEE pin for a VEE out of range. A voltage less negative than -1.5 V (nominal) is interpreted as a VEE out of range. The VEE monitoring threshold is not configurable.

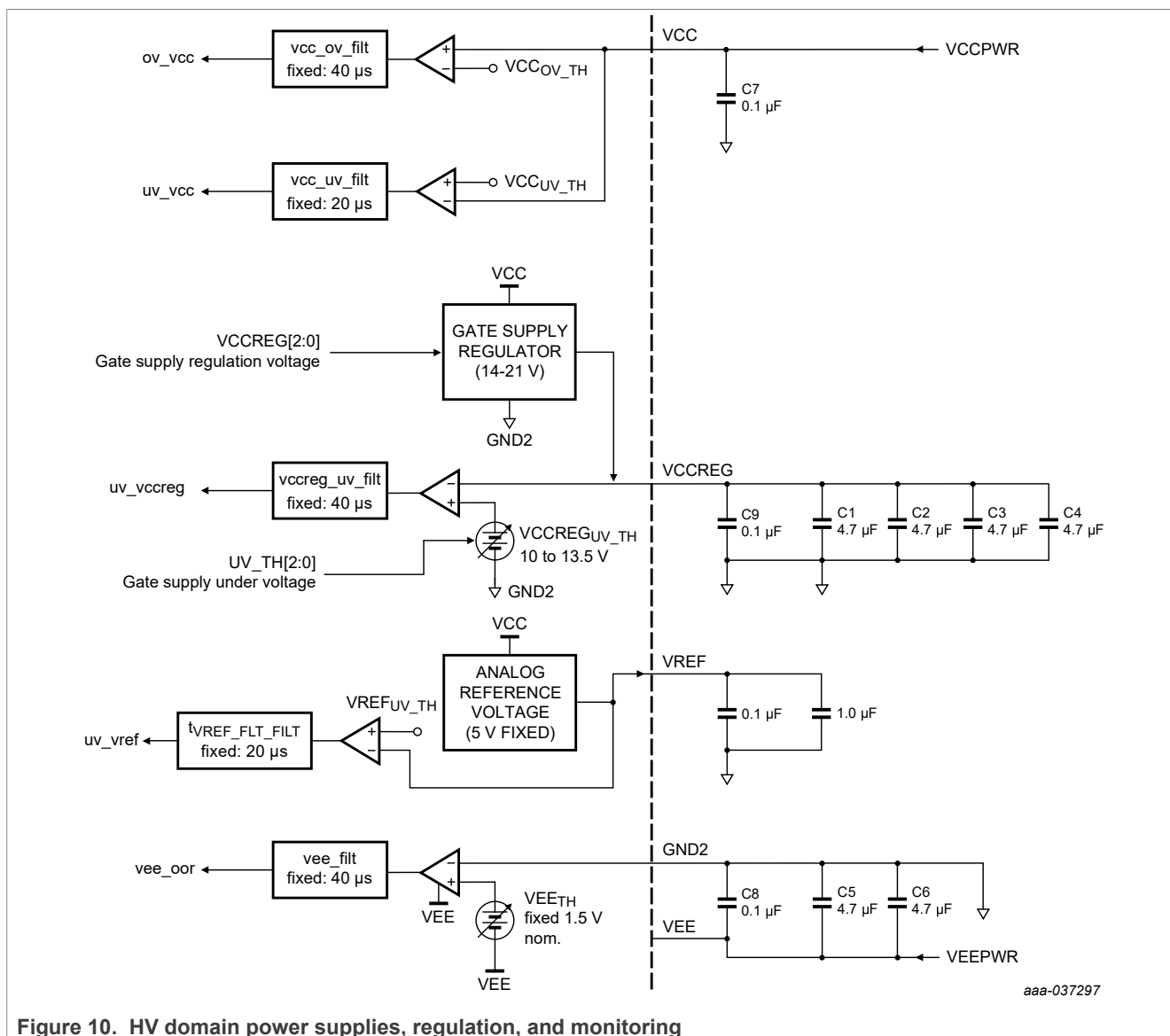


Figure 10. HV domain power supplies, regulation, and monitoring

## 11.2 Digital I/Os for control and configuration

### 11.2.1 Introduction

The control and configuration circuitry consists of the SPI pins and the logic input pins (PWM, PWMALT, FSSTATE, FSENB, and FSISO) for gate control and fail-safe configuration. Together, they control the IC's operating mode and state of the output stage. The FSSTATE, FSENB, and FSISO pins exert control by means of the system's safing logic.

### 11.2.2 Functional block diagram

[Figure 11](#) shows the basic features of the logic pins. The ESD structures are not shown.

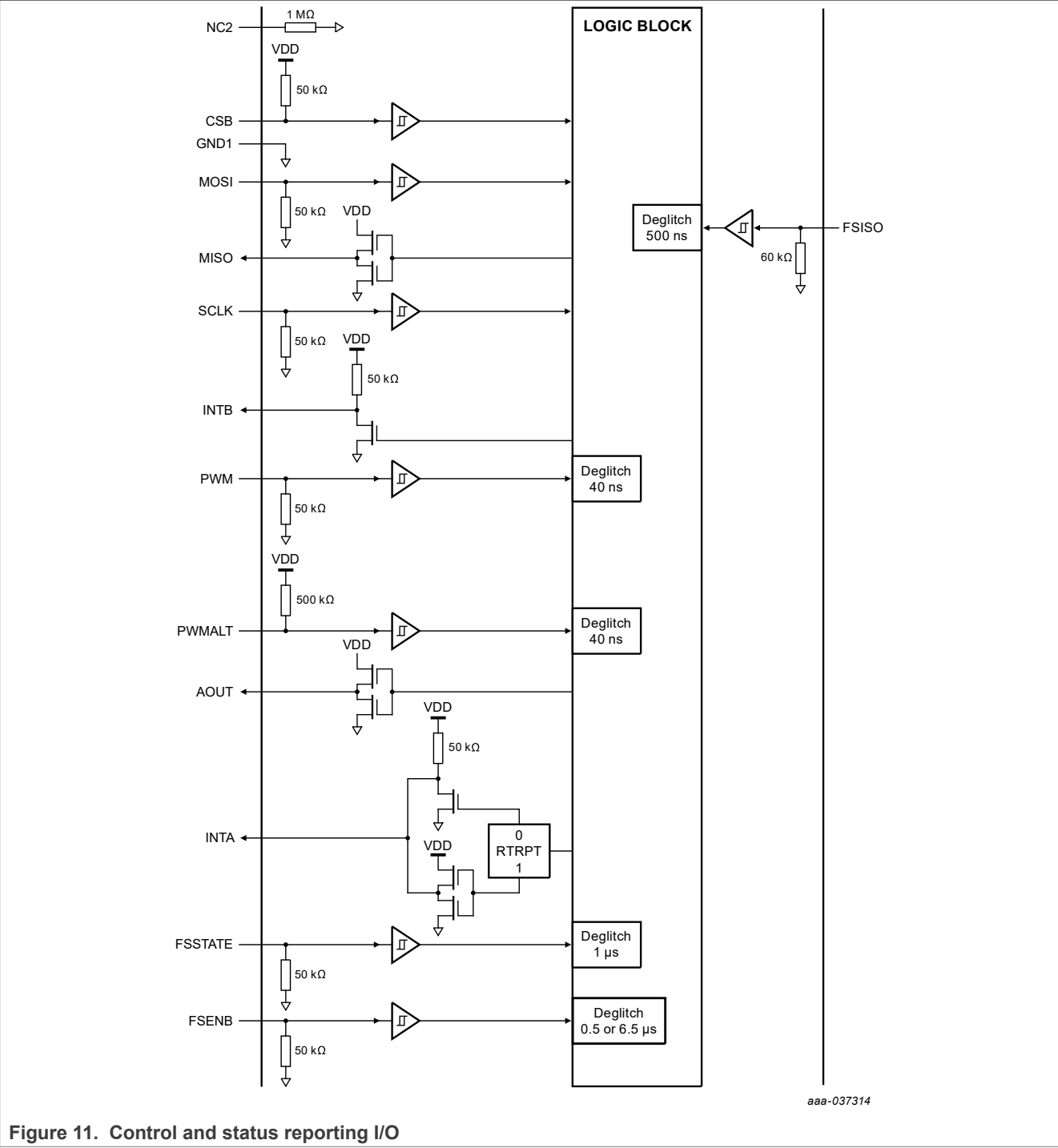


Figure 11. Control and status reporting I/O

### 11.2.3 Safing logic pins

The GD3160 has three pins that monitor system-level fail-safe signals. Such fail-safe signals can be created in safing logic that independently monitors the MCU and key system parameters, such as motor torque. When the safing logic detects a system-level fault, its commands can override the MCU and take direct control of the GD3160 operation.

Safing logic may be located in the low-voltage domain, where it is powered by the vehicle battery or a backup power supply derived from the high-voltage domain. The GD3160's FSENB and FSSTATE pins are useful in this architecture: FSENB places the GD3160 into Fail-safe mode, and FSSTATE commands a gate state within Fail-safe mode.

Safing logic may also be located in the high-voltage domain near the power device gate itself. For this architecture, the FSISO pin is useful to command the gate on (MGD3160AM515EK, MGD3160AM518EK, MGD3160AM315EK, or MGD3160AM318EK) or 3-state (MGD3160AM535EK, MGD3160AM538EK, MGD3160AM335EK, or MGD3160AM338EK) while the system is in Fail-safe mode.

Due to its proximity to the gate and independence from domain communications, FSISO receives higher priority than all PWM, FSENB/FSSTATE, and fault states. This priority is elaborated further in [Section 12.6](#).

#### 11.2.3.1 FSENB and FSSTATE pins

Two safing logic pins in the low-voltage domain, FSSTATE and FSENB, provide an independent means to control the power device's gate during a system-level fault. The FSENB pin alerts the GD3160 to a fail-safe condition, and the FSSTATE pin provides the desired on/off command of the gate in the fail-safe condition.

Because the GD3160 does not respond to its PWM or PWMALT pins when in Fail-safe mode, it no longer has the cross-conduction and deadtime protection those pins normally provide. The system's logic must provide cross-conduction protection by ensuring that the high-side and low-side IGBTs are not turned on or switched simultaneously and that sufficient deadtime is used when the gates change On/Off state.

The pulse suppression filter at the FSENB pin is relatively long compared to the filters on the other logic pins. This is to ensure that noise does not inadvertently cause an undesired fail-safe condition.

To simplify the safing logic's timing requirements, the filter time for the FSENB is a function of the state of the FSSTATE pin as shown in [Figure 12](#).

If an IGBT fault occurs (HV Die) the system's and the GD3160's priority is to protect the IGBT. Therefore, if an HV Die fault (VCCREG\_UV, VCC\_OV, OTS, Die2 COMMERR, Die2 WD, OT IGBT, VEE\_OOR, VREF UV, RESET MODE on Die2, CLAMP fault, SC, DESAT) is detected, the GD3160 keeps the IGBT OFF regardless of the state of FSSTATE and FSENB.

By default, the INTB pin does not report that the GD3160 is in a Fail-safe state. However, if desired, the GD3160 can be programmed to report its fail-safe status at the INTB pin. The INTBFS bit in the [CONFIG3](#) register is by default Logic 0 and in that setting causes the INTB pin to ignore the Fail-safe state. But when INTBFS = Logic 1, then INTB = 0 when FSENB = 0. See the description of the SPI for additional details. [Figure 13](#) shows how the system exits the Fail-safe state.

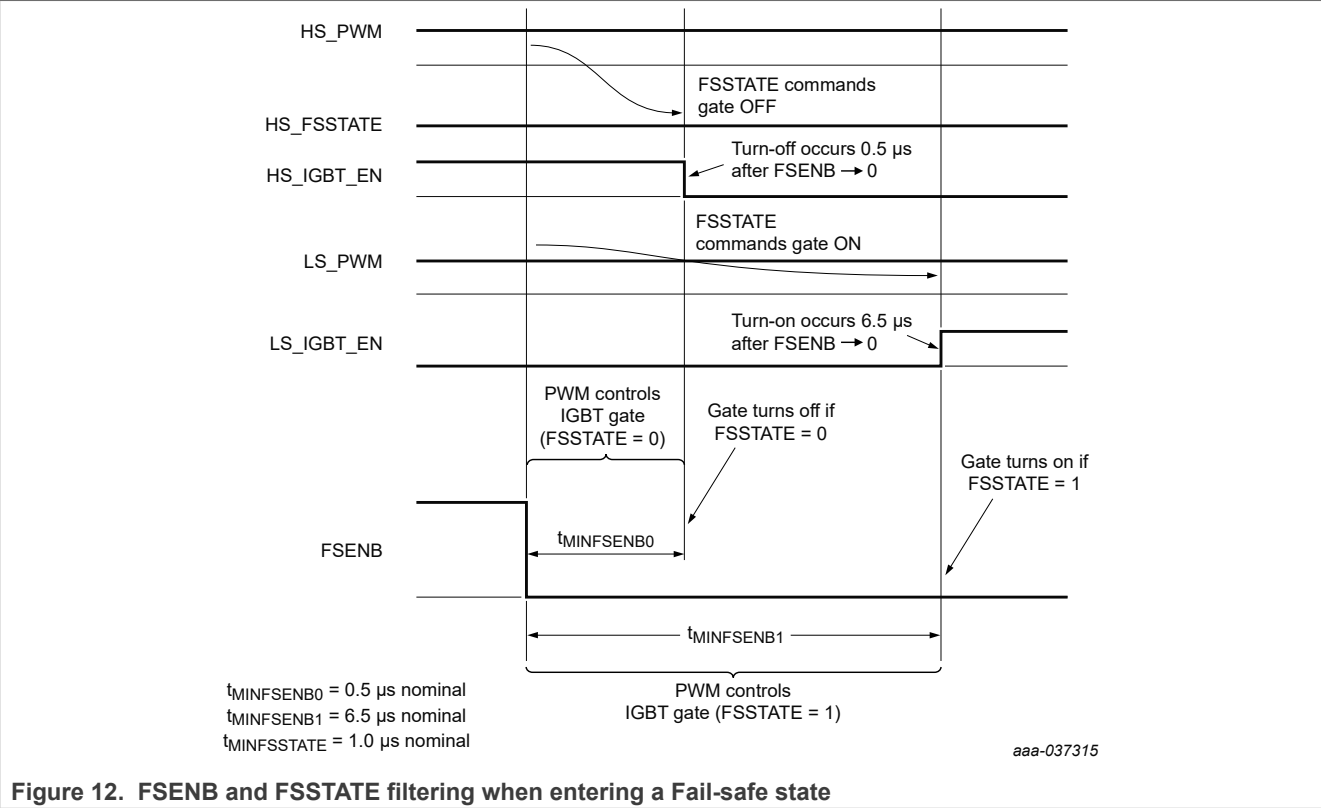


Figure 12. FSEN and FSSTATE filtering when entering a Fail-safe state

To ensure safe transition into PWM control, the delay time for the FSEN is a function of the state of the PWM pins, as shown in [Figure 13](#).

[Figure 13](#) shows the handling of control between FSSTATE and PWM as the system exits the fail-safe state. If PWM or FSSTATE transitions during the delay time between t<sub>MINFSEN0</sub> and t<sub>MINFSEN1</sub>, then transitions during the FSEN filter delay time, the PWM control is prioritized and the device immediately moves to follow PWM control. Normal mandatory deadtime is in effect with PWM pins, ensuring a safe transition. If the requested PWM state matches the current state under FSSTATE control, no additional 6 μs delay is added, and PWM control is assumed immediately after t<sub>MINFSEN0</sub> expires (0.5 μs after FSEN rising edge). In this way, PWM control is prioritized to minimize distortion of the PWM control. Mandatory deadtime again ensures safe switching once PWM activity restarts.

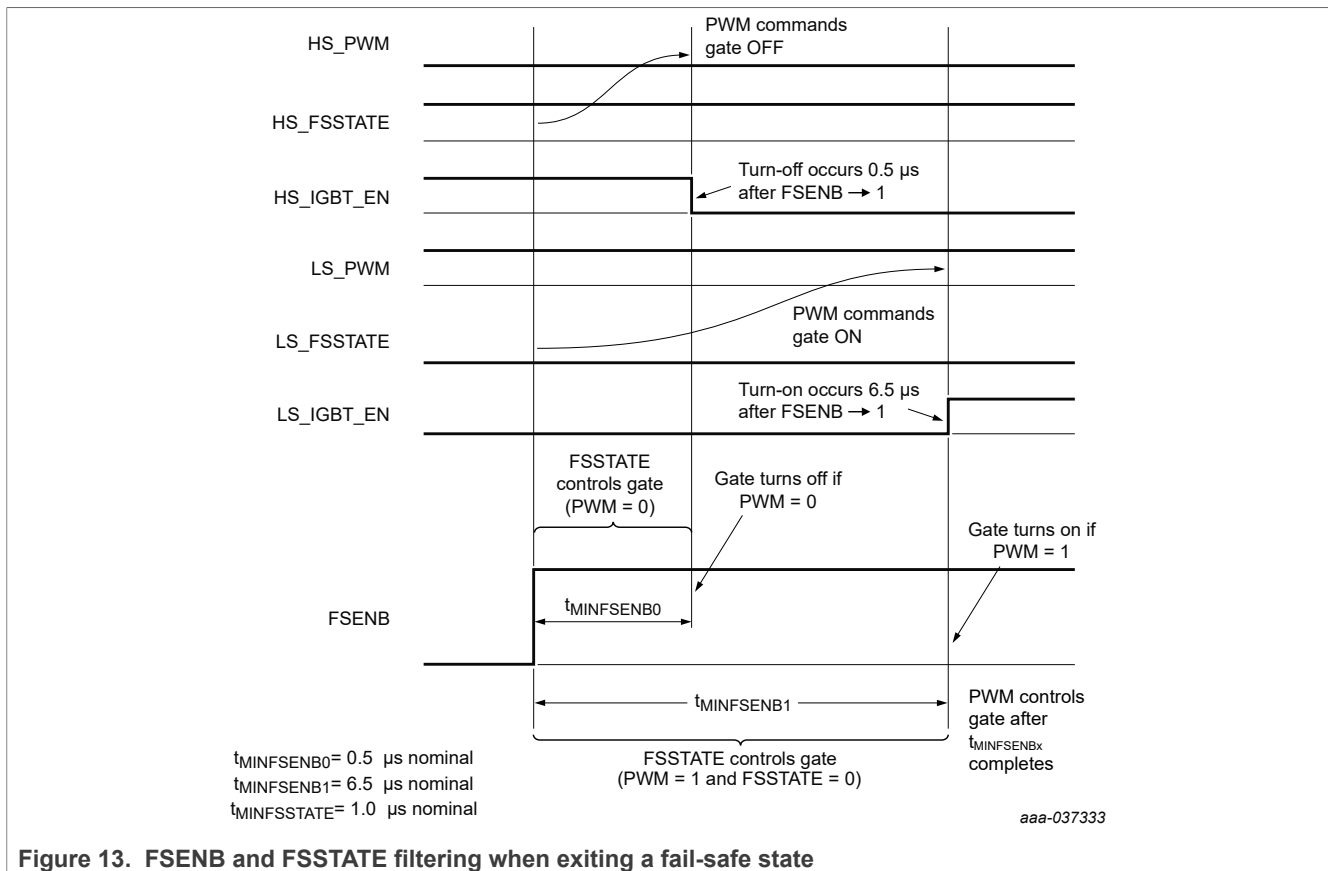


Figure 13. FSEN and FSSTATE filtering when exiting a fail-safe state

### 11.2.3.2 FSISO pin - Gate ON (MGD3160AM515EK, MGD3160AM518EK, MGD3160AM315EK, or MGD3160AM318EK)

FSISO provides fail-safe turn-on capability from the high-voltage domain. This is useful when the low-voltage domain is inactive and the gate must be turned ON.

Activating the FSISO pin (Logic 1) turns the gate ON, independent of other inputs, and sends INTB low (INTA operation is unchanged). The delay time from FSISO rising edge to the ON state is  $t_{\text{FSISOMIN}}$ .

As a fail-safe control local to the HV domain, FSISO receives the highest priority over all other controls or faults. For example, when the VCCREG (positive gate supply) or VREF are in undervoltage, a logic high at FSISO brings the gate high.

The logic state of FSISO pin and the gate can be read via the [STATUS3](#) register, and INTB is Logic 0 when FSISO is Logic 1. If the FSISO pin is enabled via the FSISOEN bit in the [MODE2](#) register and FSISO is Logic 1, then the gate is driven high (up to VCCREG) regardless of the FSEN and FSSTATE settings.

If this feature is not used, the FSISO pin should be connected to GND2 and the FSISOEN bit in the [MODE2](#) register should be set to Logic 0.

### 11.2.3.3 FSISO pin - Gate 3-state (MGD3160AM535EK, MGD3160AM538EK, MGD3160AM335EK, or MGD3160AM338EK)

FSISO provides fail-safe 3-state capability from the high-voltage domain. This is useful when the low-voltage domain is inactive and the gate must be 3-state (not driven either high or low). If this option is used, the system integrator must take into account  $t_{\text{FSISOMIN}}$  to make sure that gate is in 3-state before using external circuitry to control the gate ON or OFF.

Activating the FSISO pin (Logic 1) 3-states the gate, independent of other inputs, and sends INTB low (INTA operation is unchanged). The delay time from FSISO rising edge to the 3-state is  $t_{FSISO\text{MIN}}$ .

As a fail-safe control local to the HV domain, FSISO receives the highest priority over all other controls or faults. For example, when the VCCREG (positive gate supply) or VREF are in undervoltage, a logic high at FSISO brings the gate tristate.

The logic state of FSISO pin and the gate can be read via the [STATUS3](#) register (3-state will be reported as OFF), and INTB is Logic 0 when FSISO is Logic 1. If the FSISO pin is enabled via the FSISOEN bit in the [MODE2](#) register and FSISO is Logic 1, then the gate is 3-state (GH off, GL off) regardless of the FSENB and FSSTATE settings.

If this feature is not used, the FSISO pin should be connected to GND2 and the FSISOEN bit in the [MODE2](#) register should be set to Logic 0.

#### 11.2.4 SPI pins (CSB, SCLK, MOSI, MISO)

GD3160's SPI pins (CSB, SCLK, MOSI, and MISO) provide configuration and fault/status report capabilities. They are also used to determine the operating state and obtain detailed fault information. The ADC reports its output through the SPI. For SPI circuitry details, see [Section 11.13](#).

#### 11.2.5 PWM and PWMALT pins

During normal operation, the PWM pin controls the ON/OFF state of the output stage. The GD3160 is designed to minimize the turn on and turn off delays, minimize the difference between those delays, and minimize pulse-width jitter.

The PWMALT pin should be connected to the PWM signal that controls the IGBT in the opposite side of the half-bridge. It disallows simultaneously turning on both IGBTs and it enforces a minimum deadtime ( $t_{\text{min\_DT}}$ ) between the logic edges, as shown in [Figure 14](#).

An internal pulldown resistor at PWM and an internal pullup resistor at PWMALT ensure that the output stage is OFF when neither pin is actively driven.

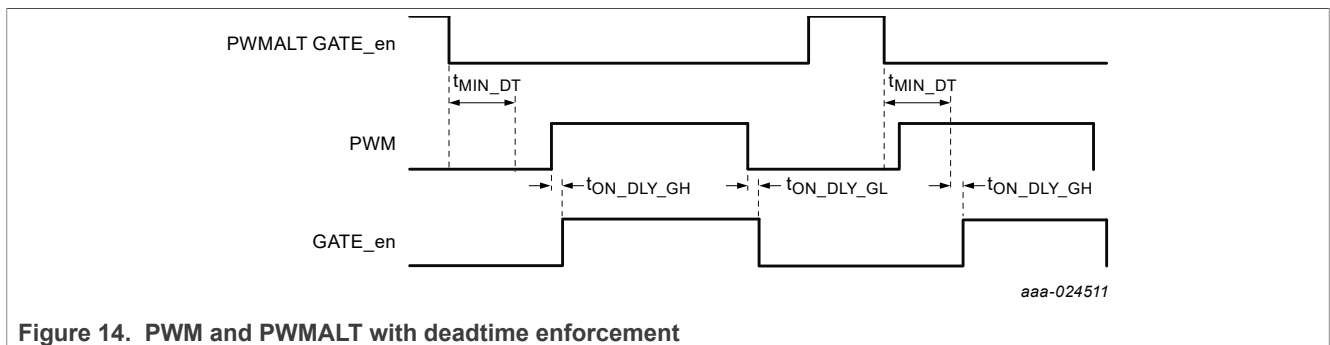


Figure 14. PWM and PWMALT with deadtime enforcement

If PWMALT goes high while PWM is already high, then the gate turns off immediately, without inserting  $t_{\text{min\_DT}}$ . If PWM goes high, while PWMALT is already high, a deadtime fault will be latched. In fact,  $t_{\text{min\_DT}}$  is only applied on the falling edge of PWMALT, to ensure that the gate does not go high before the programmable deadtime  $t_{\text{min\_DT}}$  expires.

11.3 Gate drive output stage and diagnostics

11.3.1 Introduction

The most prominent components in the output stage are the pullup transistor (GH) and the two pulldown transistors (GL and AMC). A soft shutdown circuit is in parallel with the GL transistor. The gate drive output stage also includes the drivers' level shift circuitry, gate drive buffers and diagnostics circuitry. All drive transistors are power MOSFETs, which allows full rail-to-rail control of the voltage at the IGBT's gate.

11.3.2 Functional block diagram

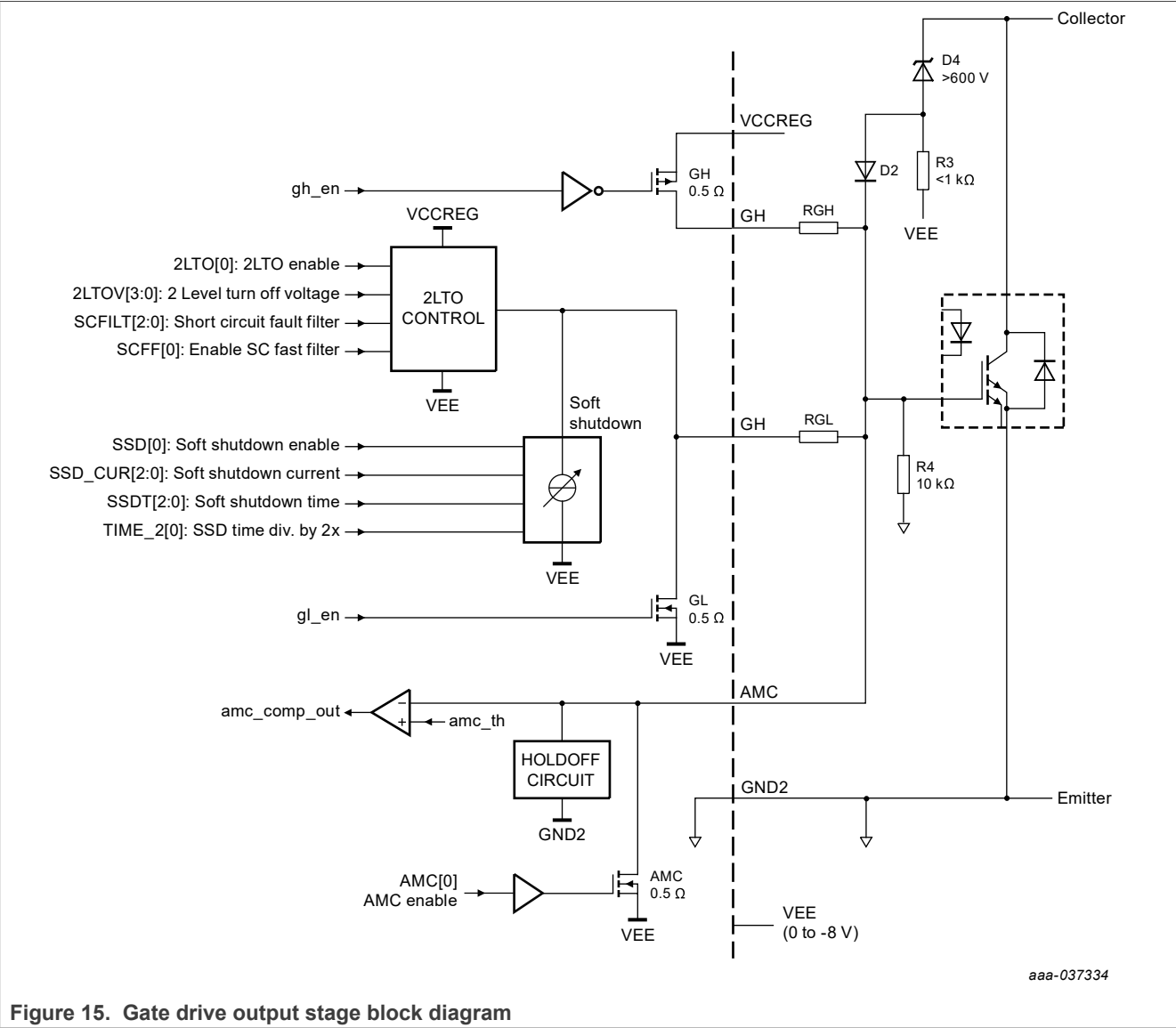


Figure 15. Gate drive output stage block diagram

### 11.3.3 Types of gate drive

#### 11.3.3.1 Normal mode turn on and turn off

When the voltage at the PWM pin goes high, the signal is deglitched by an input pulse suppression filter ( $t_{\text{MIN}}$ ). Once the signal is validated, all pulldown transistors (GL, AMC, SSD) are turned off and GH is turned on.  $V_{\text{CE}}$  desaturation faults are blanked for  $t_{\text{DESAT\_LEB}}$ . Once  $t_{\text{DESAT\_LEB}}$  expires,  $I_{\text{DESAT}}$  is turned on to monitor the collector-emitter voltage. The SSD (soft shutdown) and the two-level turn-off (2LTO) circuits are not activated during non-faulted switching.

When the voltage at the PWM pins goes low (the same 40 ns deglitch filter is applied) pullup transistor GH is turned off and the primary pulldown transistor, GL, is turned on and the gate resistor in series with the GL pin controls turn-off speed.

#### 11.3.3.2 Soft shutdown

The GD3160 includes integrated soft shutdown (SSD) functionality, which is a current-limited turn-off functionality, used for fault handling and specific turn-off scenarios.

The soft shutdown operation turns the power device gate off more slowly than normal turn-off: this reduces fast or high  $di/dt$  in the load current, and reduces VCE overshoot and SOA stress on the power device.

The SSD circuit is connected between the GL and VEE pins. [Table 14](#) and [Section 11.13](#) provide details of the ISSD programming options.

For controlled operation, soft shutdown is usually only run for a fixed time, or until the active Miller clamp can activate. There is a capacity to program the duration (SSDT parameter) and utilize a "fast" mode (TIME\_2 configuration bit) for low gate charge devices, like SiC MOSFETs.

Soft shutdown can be enabled or disabled in the MODE1 register. It is recommended that soft shutdown be enabled (set SSD = 1) for all manner of power devices, including IGBTs, SiC MOSFETs, and so on. All power devices benefit from the reduced voltage stress provided by soft shutdown gate current. Soft shutdown is used in many different functions. It is especially required to be enabled (SSD = 1 in the MODE1 register) for the following applications:

- Driving an IGBT (SSD reduces voltage stress, which cannot exceed maximum VCE)
- Driving fast-switching MOSFETs safely (SSD reduces voltage stress during turn-off events)
- Using the overcurrent feature (OCSNS = 1) based on the ISENSE pin. SSD is used to shut down an overcurrent condition.
- Using the segmented drive function (SEGDRV = 1). SSD is used to mitigate potential VCE overvoltage.
- Using the active clamp (ACTCLMP = 1). SSD is used during gate turn-off during VCE overvoltage clamp event.

#### 11.3.3.3 Two-level turn-off

The GD3160 includes a two-level turn-off (2LTO) feature that momentarily reduces the gate voltage and limits the maximum collector current while validating a fault condition.

The 2LTO feature may be enabled or disabled using the 2LTO bit in the MODE1 register, depending on application needs.

The GD3160 must have two-level turn-off enabled (set 2LTO = 1) in the following applications:

- Driving an IGBT (2LTO ideally handles the plateau region while turning off substantial collector current)
- Devices with integrated current mirror (connected to the ISENSE pin)

The 2LTO feature can be useful, but is not absolutely required (may set 2LTO = 0), in the following applications:

- Driving a SiC MOSFET without integrated current mirror (MOSFETs do not possess the hard plateau that IGBTs do)
- Smaller gate charge devices (roughly  $Q_G < 2000$  nC). Voltage regulation is not as useful for smaller  $Q_G$  devices, soft shutdown (SSD) might be capable of achieving the fastest turnoff. Empirical testing might be in order to confirm the best settings.

The 2LTO feature may be activated when a high-current fault (e.g. desaturation or short-circuit) is first detected. The 2LTO feature holds the gate at a programmable voltage level for a programmable duration (see 2LTOV and SC\_FILT bit settings in [the CONFIG2 register](#)) while validating the fault. In this way, the GD3160 provides not only customizable protection thresholds, but also a customizable faulted turn-off sequence appropriate for both the power device and application.

During the 2LTO interval the voltage at the GL pin is initially less than the voltage at the IGBT's gate. This difference in potential and the resistor in series with the GL pin determine how rapidly the gate is discharged to  $V_{2LTO}$  and the resultant collector current  $di/dt$ . If the fault condition is not validated (for example, marginal detection or lower gate voltage reduced the current) then GD3160 will recharge the gate to full VCCREG gate supply and continue to PWM the gate. Unlike soft shutdown, 2LTO is not a one-way trip. However, to prevent endless looping on a marginal fault detection, if the 2LTO is tripped a second time within one PWM cycle, the fault is considered validated, and the gate is turned off.

#### 11.3.3.4 Active Miller clamp and holdoff

The GD3160 must keep the IGBT in the OFF state when the high-voltage domain is unpowered. It must clamp any leakage currents that might raise the IGBT's gate-emitter voltage to more than the IGBT's threshold voltage. The holdoff circuitry connected between the AMC (connected to the gate) and GND2 (connected to the source/emitter) pins limits the voltage to  $V_{GOFF}$ .

The gate holdoff circuit is active when the internal logic supply is less than POR, and when VCC is in undervoltage ( $V_{CC} < V_{CC_{UV\_TH}}$ ) and while FSISO is inactive (either FSISO pin is logic low, or FSISO is disabled by  $FSISOEN = 0$ ). The holdoff circuit is inactive when the high-voltage domain internal power supplies are powered up and in regulation.

At the end of the turn-off transition,  $V_{GE}$  falls below  $AMC_{th}$  ( $\sim 2.0$  V greater than VEE). After the AMC turn on filter time,  $t_{AMC\_FILT}$ , the AMC transistor turns on and clamps the power device gate to VEE. The AMC transistor is not turned off until the next PWM rising edge. This feature is shown in [Figure 16](#). The AMC feature is enabled by default, but can be disabled by SPI command.

If the AMC feature is disabled with the SPI, the AMC transistor is never turned on.

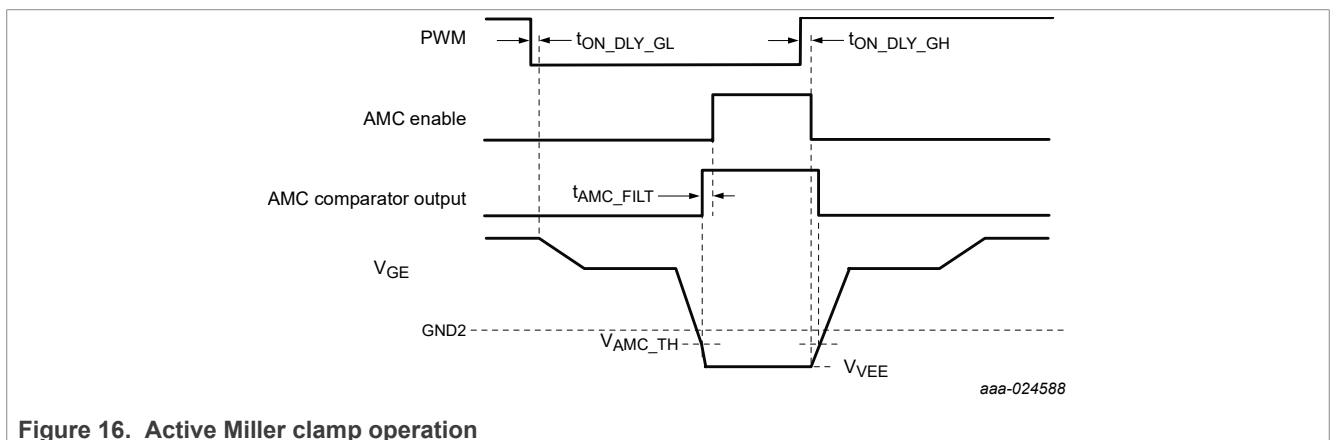


Figure 16. Active Miller clamp operation

## 11.4 Current sense protection

### 11.4.1 Introduction

The GD3160 protects power devices with a current-sense mirror that provides instantaneous readout of the power device's load current. The ISENSE pin senses the current mirror output (converted to a voltage) and differentiates between short-circuit and overcurrent events, and modulates the gate drive accordingly.

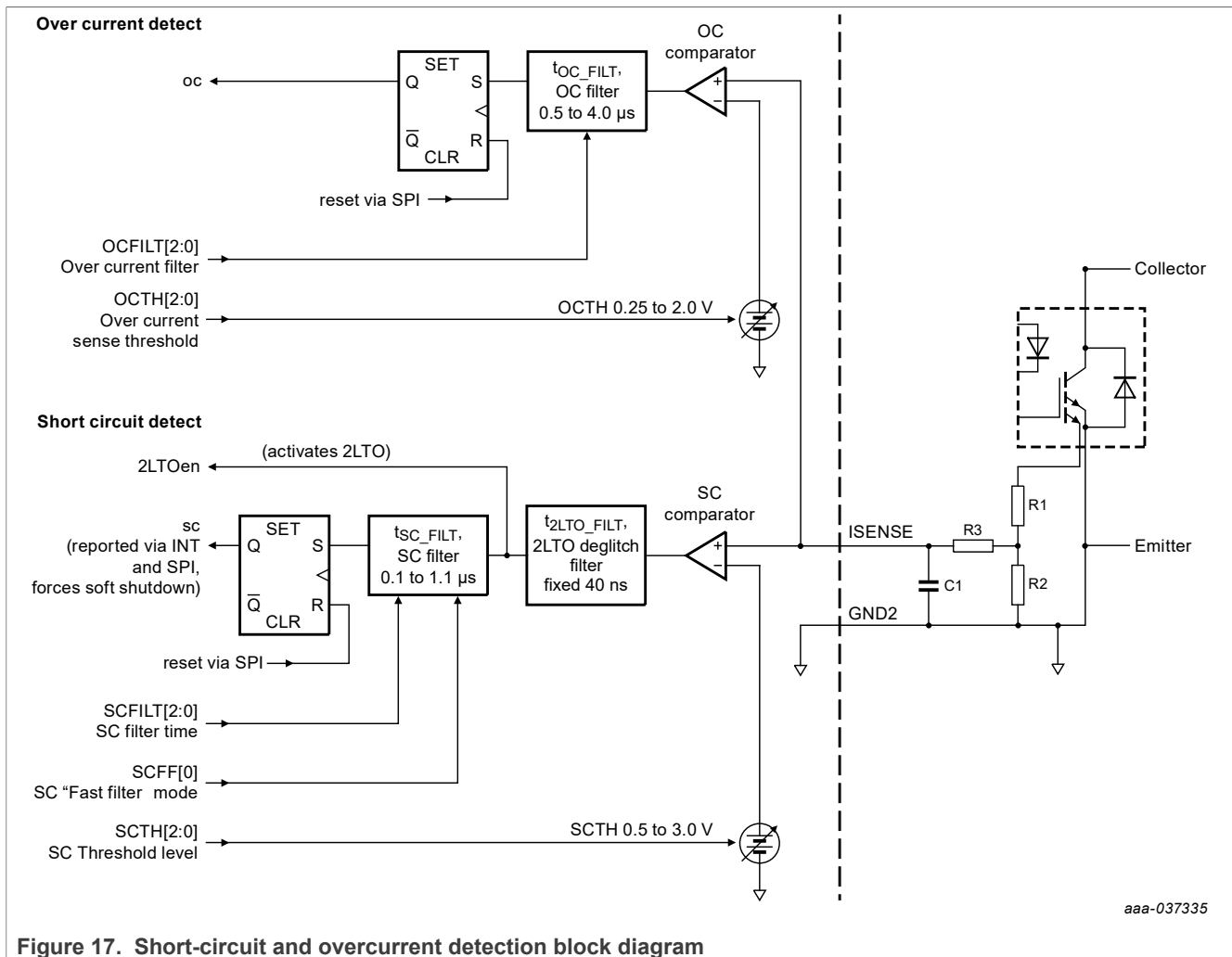
After determining an overcurrent or short-circuit event, the GD3160 safely latches the gate off using the two-level turn-off (2LTO) and soft shutdown (SSD) per configuration parameters.

### 11.4.2 Short-circuit fault management via the ISENSE pin

The features of the short-circuit and overcurrent detection block are:

- Current sense monitoring comparators with programmable thresholds for overcurrent and short-circuit current
- Fast detection and response to short-circuits
- 2LTO to limit the maximum fault current
- Programmable delay time for activating soft shutdown for short-circuits
- Programmable filter time for overcurrent detection

The GD3160's overcurrent and short-circuit detection block diagram is shown in [Figure 17](#):



**Figure 17. Short-circuit and overcurrent detection block diagram**

Implementing short-circuit and overcurrent protection with this circuitry is fairly straightforward. R1, R2, SCTH, and OCTH are selected based on the IGBT's current sense ratio and the desired SC and OC fault thresholds. The SC and OC fault thresholds are set to less than the IGBT's expected  $V_{CE(sat)}$ .

The circuit responds differently to a short-circuit versus an overcurrent fault. If the short-circuit comparator trips for longer than  $t_{2LTO\_FILT}$ , the GD3160 initiates a 2LTO by immediately reducing the IGBT's  $V_{GE}$  to a lower value. If the comparator remains tripped for a programmable duration ( $t_{SC\_FILT}$ ), then the fault is latched and the IGBT is turned off by the SSD circuitry. If the comparator does not remain tripped, the gate-drive transistor GH turns on once again and returns  $V_{GE}$  to its normal on-state voltage. For full short-circuit protection performance, enabling both 2LTO and SSD is recommended to achieve the described operation.

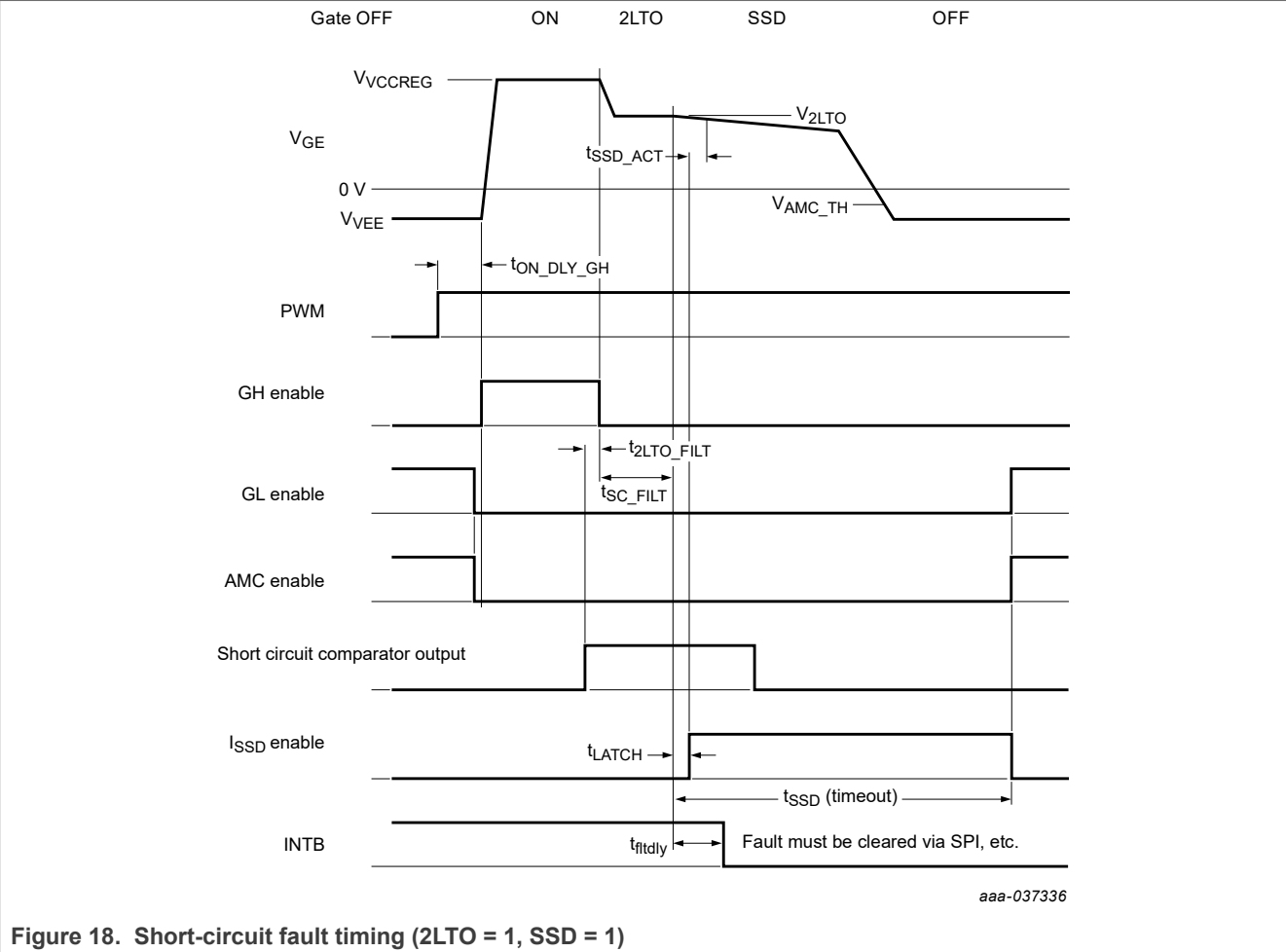


Figure 18. Short-circuit fault timing (2LTO = 1, SSD = 1)

### 11.4.3 Overcurrent fault management with the ISENSE pin

An overcurrent (OC) at the ISENSE pin is defined by lower threshold than short-circuit, but a longer filter time. When the OC fault is validated (threshold/filter criteria are satisfied per the OCTH and OCFILT settings), the OC fault is latched, reported over the INTA/INTB pins, the gate is turned off by the maximum SSD current value (1.0 A) after the falling edge of PWM. The gate is not latched off, however, and the gate continues to follow PWM control.

After an OC fault, SSD expires at either the programmed timeout or when AMC voltage criteria are met, or if a valid PWM rising edge is received, as shown in [Figure 19](#).

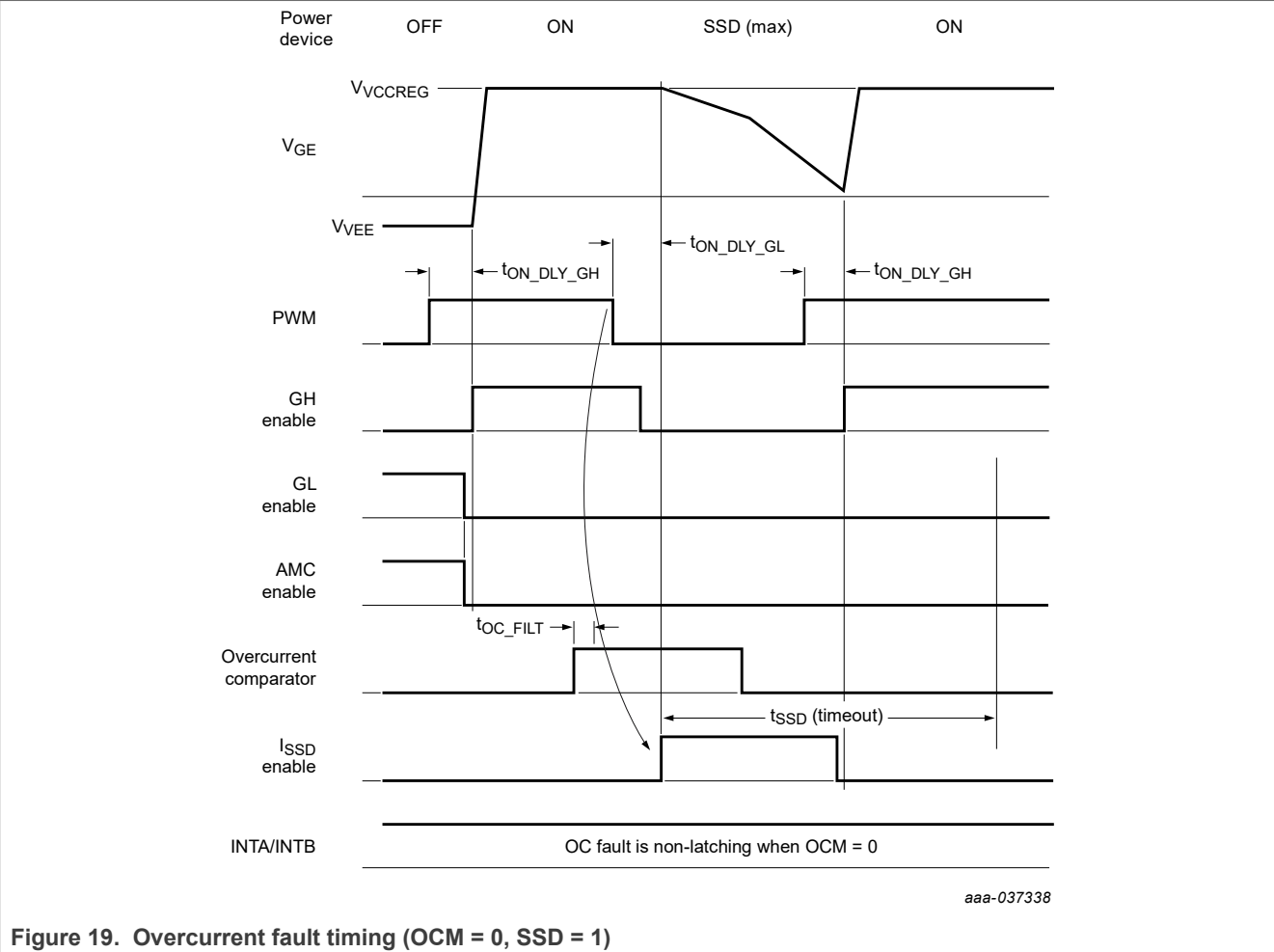


Figure 19. Overcurrent fault timing (OCM = 0, SSD = 1)

To prevent cross conduction while handling an overcurrent fault, the selected deadtime on the opposite leg gate driver must be greater than the time it takes the maximum SSD value (roughly 1A) to discharge the gate. This requirement is summarized by [Equation 1](#).

DEAD[3:0]> QG / SSDMAX

(1)

11.5 Desaturation fault protection

11.5.1 Introduction

The GD3160 can also directly monitor the IGBT's/SiC V<sub>CE</sub>/V<sub>DS</sub> when the IGBT is turned ON. If an abnormally high V<sub>CE</sub> is detected, the SSD circuitry quickly (but not abruptly) turns OFF the IGBT and latches and reports the fault.

11.5.2 Features

The features of the V<sub>CE</sub> desaturation detection block include:

- Desaturation voltage threshold programmable via SPI
- Desaturation blanking time at turn on programmable via SPI

- An internal 250  $\mu\text{A}$  to 1.0 mA programmable current source,  $I_{\text{DESAT}}$ , used to monitor a desaturation event
- Fault reporting circuitry, which is used by the Logic block to report the fault and by the gate drive circuitry to turn off the IGBT

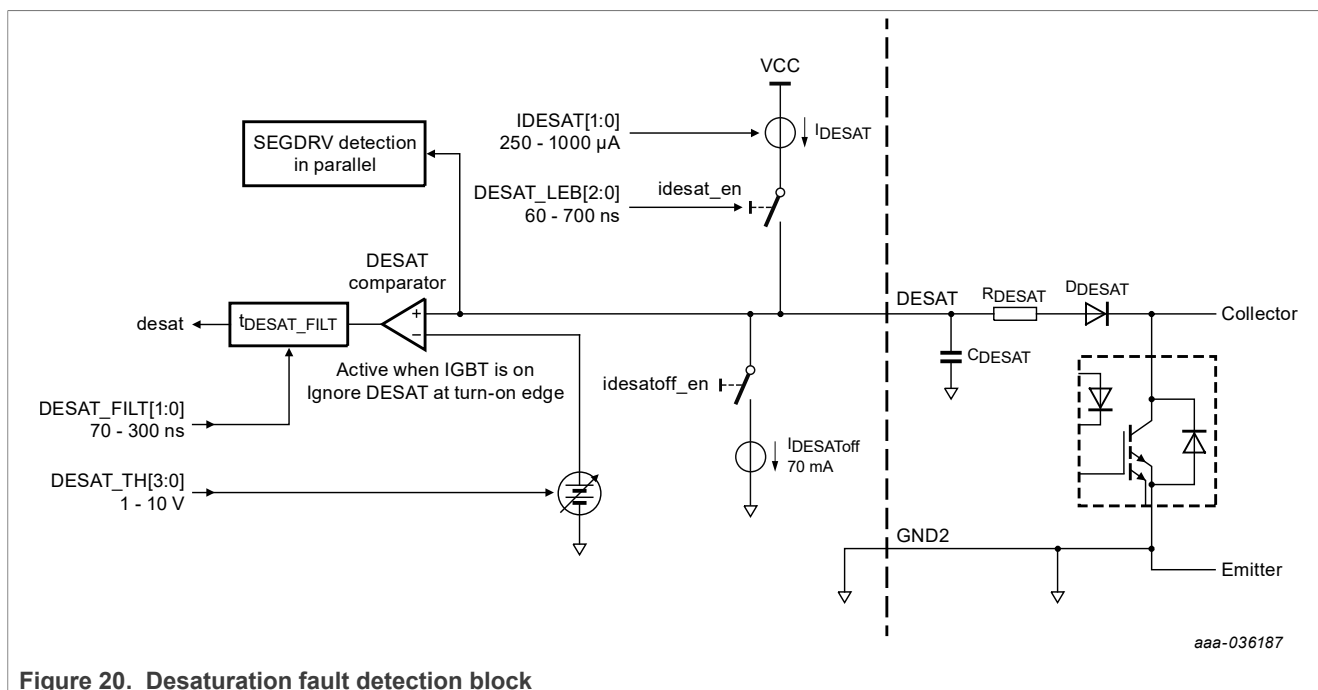


Figure 20. Desaturation fault detection block

### 11.5.3 Protection and diagnostic features

The GD3160's desaturation detection circuitry monitors the IGBT's  $V_{\text{CE}}$  and quickly responds if desaturation is detected. Responding within a few microseconds reduces the IGBT heating prior to turn off. Turning off gently is required to minimize the peak  $V_{\text{CE}}$  transient associated with parasitic circuit and IGBT package inductance.

$C_{\text{DESAT}}$ ,  $R_{\text{DESAT}}$  and  $D_{\text{DESAT}}$  are key external components for this circuit block.  $D_{\text{DESAT}}$  provides a discharge path to keep  $V_{\text{DESAT}}$  low when the IGBT is on and not shorted. When the IGBT turns on in a non-faulted condition, it pulls the cathode of  $D_{\text{DESAT}}$  to its  $V_{\text{CE(sat)}}$  voltage. The current source  $I_{\text{DESAT}}$  is able to charge  $C_{\text{DESAT}}$  only to  $V_{\text{CE(sat)}} + D_{\text{DESAT}} + I_{\text{DESAT}} * R_{\text{DESAT}}$ . The total is below the desaturation threshold.

Figure 21, Figure 22 and Figure 23 show the circuit's key digital and analog signals when the fault occurs when the IGBT is already ON.

Regarding DESAT fault:

- If 2LTO = 1 when a DESAT fault is detected, the 2LTO circuit is engaged at the expiration of  $t_{\text{DESAT\_FILT}}$ .
- If the fault persists (comparator remains tripped) for the duration of  $t_{\text{SC\_FILT}}$ , then when  $t_{\text{SC\_FILT}}$  expires, ISSD is enabled.
- If the fault disappears (comparator does not remain tripped) during  $t_{\text{SC\_FILT}}$ , then GH is re-enabled and no fault is reported.
- If the fault reappears during the same PWM cycle, the fault shall be immediately latched and reported, and SSD should begin.

The programmable  $t_{\text{SSD}}$ , soft shutdown time, sets the duration of the soft shutdown interval. During this time,  $I_{\text{SSD}}$  controls the gate discharge speed. The Soft Shutdown Time should be programmed to be longer than the expected turn off time during a fault. When the  $t_{\text{SSD}}$  timer expires, the GL transistor (and AMC transistor, if enabled) is turned on to provide a low impedance discharge path for the IGBT's gate. This behavior is illustrated in the next three timing diagrams.

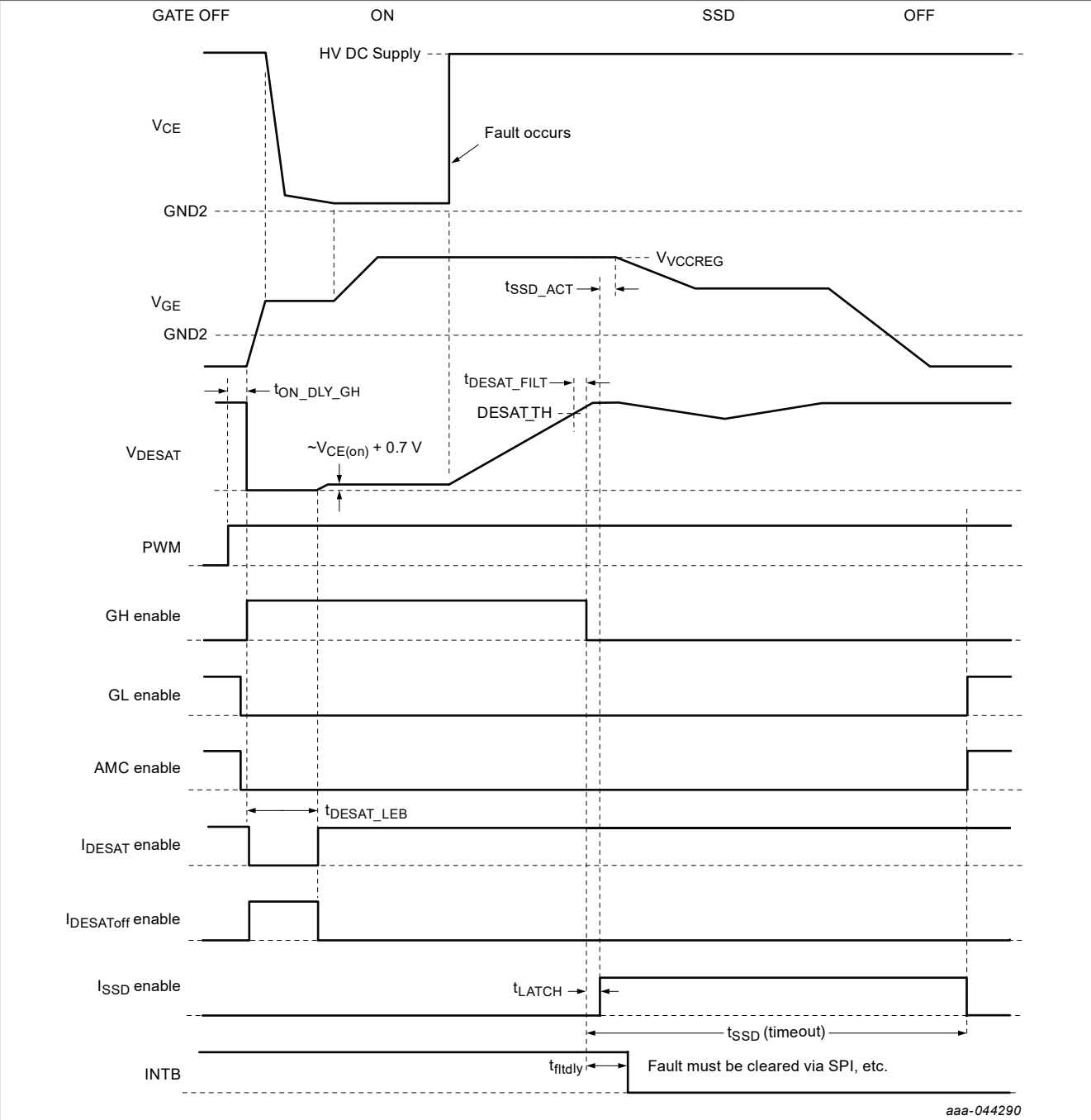
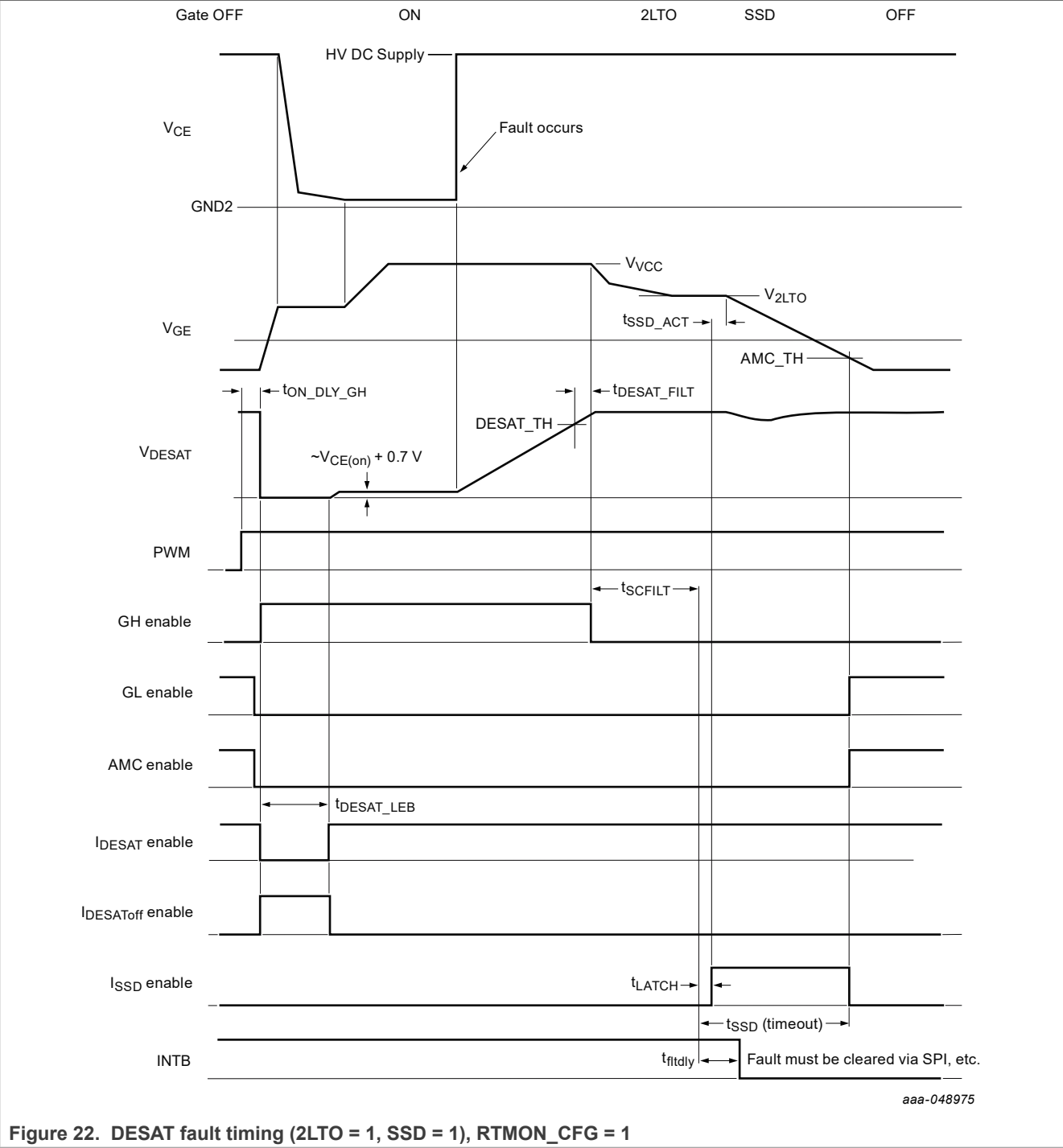
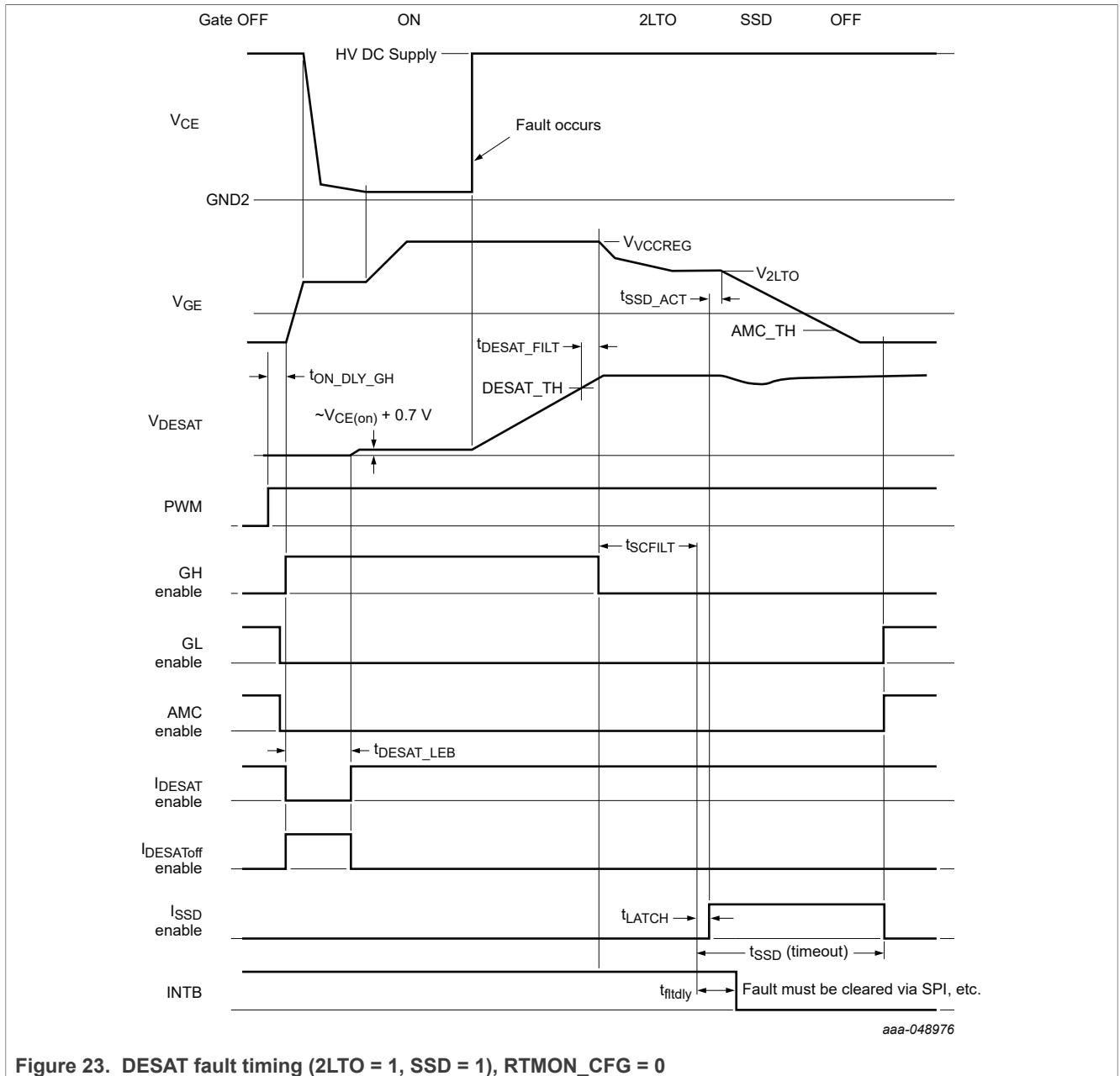


Figure 21. DESAT fault timing (2LTO = 0, SSD = 1), RTMON\_CFG = 1





## 11.6 VCE overvoltage protection

### 11.6.1 Introduction

The GD3160 contains two provisions that protect the power device from VCE or VDS overvoltage scenarios.

1. Advanced active clamp
2. Segmented drive operation

Advanced active clamp is intended to alter the gate drive in the presence of a high VCE/VDS condition, typically by means of high-voltage Zeners directly connected to the collector or drain. The GD3160 active clamp fault response may be configured as non-latching (default behavior, single-cycle intervention and continue PWMing)

or as latching behavior (one-time intervention disables PWMing and shuts down the gate) based on application needs.

Segmented drive is a proactive, non-latching, non-faulted function that waveshapes the gate drive when high collector or drain  $dV/dt$  is detected by the DESAT pin during turn-off. Gate current during turn-off is modulated between the full turn-off (usually limited by the GL resistor) and a limited soft shutdown current.

Segmented drive is usually recommended when a clean, direct connection to the collector or drain is feasible. Segmented drive offers reduced bill of materials cost and more flexibility and range of detection than the advanced active clamp. Because they modulate the gate differently, only one function (between ACTCLMP and SEGDRV) can be enabled at one time.

### 11.6.2 $V_{CE}$ advanced active clamp

To enable the active  $V_{CE}$  clamp operation, set the bits ACTCLMP = 1 and SEGDRV = 0 in the [MODE1](#) register. The active  $V_{CE}$  clamp circuit senses the breakdown of a high-voltage Zener diode connected between the IGBT's collector and its gate. This circuit is intended to activate only at turn-off when the collector voltage is excessive.

Zener breakdown is sensed when the voltage at the CLAMP pin exceeds its threshold,  $V_{CECL\_TH}$ . When Zener breakdown is detected, the gate drive logic disables the normal turn-off path (GL driver) and engages the SSD driver at its lowest programmable setting. If the active clamp circuitry is enabled and becomes engaged, the INTA/INTB pins respond as configured, and the CLAMP bit in the [STATUS1](#) register is set to Logic 1, readable by SPI. PWMing the IGBT is disabled.

To disable the active  $V_{CE}$  clamp function, set the bit ACTCLMP = 0 or SEGDRV = 1.

The  $V_{CE}$  clamp detection circuitry has an intervention time,  $t_{VCECL}$ . The time  $t_{VCECL}$  is the time between the detection of VCLAMP exceeding the  $V_{CE}$  clamping threshold ( $V_{CECL\_TH}$ ) and activation of the active clamping circuitry (GL turn off and ISSD turn on).

When the  $V_{CE}$  clamp is activated, GL is turned off and the minimum SSD current  $I_{SSD}$  is used, regardless of the SSD mode bit settings. The  $V_{CE}$  clamp circuitry is engaged for either the minimum release time,  $t_{VCECR}$ , or the time the CLAMP pin exceeds the threshold ( $V_{CECL\_TH}$ ) with hysteresis considered ( $V_{CECL\_TH\_HYS}$ ), whichever is longer. If the TIME\_2 = 1 (reducing fault handling times), then the minimum release time,  $t_{VCECR}$ , is cut in half (typ. 100 ns). The maximum  $V_{CE}$  clamp intervention time duration is limited to  $t_{VCECR\_MAX}$ .

After the clamp intervention time has ended, GL is used to turn off the gate, and AMC is activated when threshold criteria are met.

The active  $V_{CE}$  clamp can be operated in a non-latching mode, by setting the CLAMPM mask bit (in the [MSK2](#) register) to Logic 1.

The CLAMPM mask bit (in the [MSK1](#) register) determines how the clamp activation is reported, and whether the fault is latched or not. When CLAMPM = 1, the  $V_{CE}$  clamp operation is treated as a latched fault (the fault bit CLAMP in the [STATUS1](#) register is latched at Logic 1 following the clamp activation), INTA/INTB are pulled low, and PWM is disabled following the fault. When CLAMPM = 0, the  $V_{CE}$  clamp operation is treated as a non-latching, non-fault case: there is no action on INTA/INTB, and the PWM remains enabled following the clamp activation. The CLAMP bit in STATUS is logic high while the active clamp is activated.

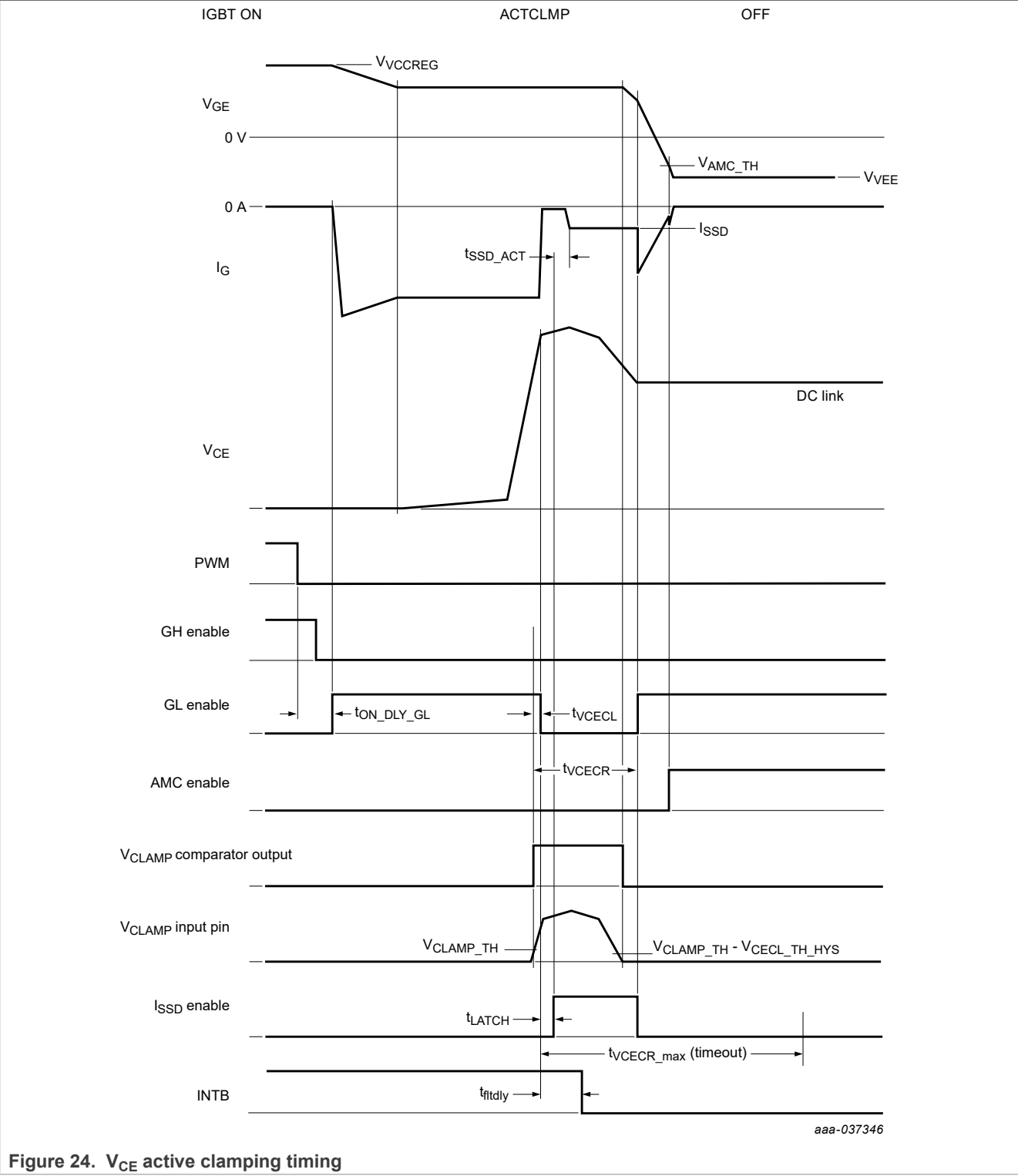


Figure 24. V<sub>CE</sub> active clamping timing

### 11.6.3 Segmented drive operation

Segmented drive refers to the GD3160's capability to waveshape the turn-off current and modulate the gate impedance during turn-off, for the purposes of mitigating potentially high  $V_{CE}$  overshoot. Segmented drive is exclusively a non-fault, non-latching mode of operation during turn-off, whereas  $V_{CE}$  active clamp (see [Section 11.6.2](#)) is a fault protection responding to high  $V_{CE}$  at any time.

To enable segmented drive, set bits  $SEGDRV = 1$ ,  $ACTCLMP = 0$  and  $TIME\_2$  to select  $t_{ssd\_seg}$  duration (either 640 ns typ or 340 ns typ) in the [MODE1](#) register. Active clamp and segmented drive can potentially overlap, and they will reduce each other's effectiveness if both are enabled. Segmented drive is only activated during the turn-off sequence; there is no effect while the gate is On.

Two following figures show the segmented drive circuitry and the associated waveforms. When the IGBT is commanded off in Segmented Drive mode, pulldown transistor GL turns on and the IGBT's gate quickly discharges to its plateau voltage. When  $V_{CE}$  begins to rise, it does so relatively slowly because the IGBT's input capacitance is quite high at this time. A comparator monitors  $V_{CE}$  as it rises. When  $V_{CE}$  exceeds the trip threshold just before  $V_{CE}$  increases abruptly, GL is turned off, SSD current typically starts after 15 ns ( $t_{SSD\_ACT}$ ) and  $I_{SSD}$  turns on to discharge the gate for a maximum of  $t_{SSD\_SEG}$  defined by  $TIME\_2$  in the [MODE1](#) register or until  $V_{AMC\_TH}$  is reached. Segmented drive uses a user-programmable threshold ( $SEGDRV_{TH}$ ) determined by the  $SEGDRV\_TH$  bits in [CONFIG4](#). A programmable delay,  $t_{SEGDRVLY}$ , can be inserted to delay the change to the SSD current.

The external capacitor  $C_{DESAT\_TH}$  must not slow the detection of the  $V_{CE}$  magnitude needed to trigger the segmented drive. To overcome the presence of  $C_{DESAT\_TH}$ , the GD3160 uses a strong pullup current source, ( $I_{VCESEN}$ ), so that the voltage at DESAT follows  $V_{CE}$  during IGBT turn-off. Additional details of the desaturation detection are provided in [Section 9.5](#).

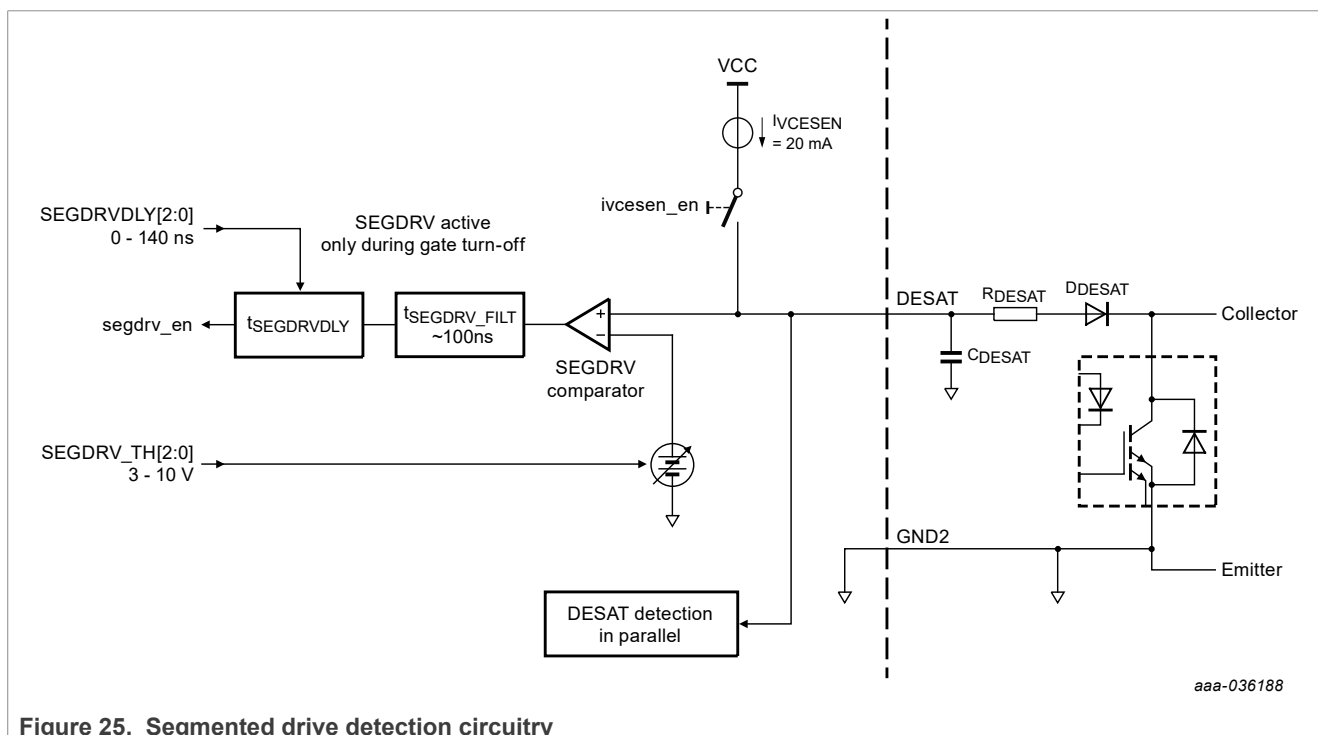


Figure 25. Segmented drive detection circuitry

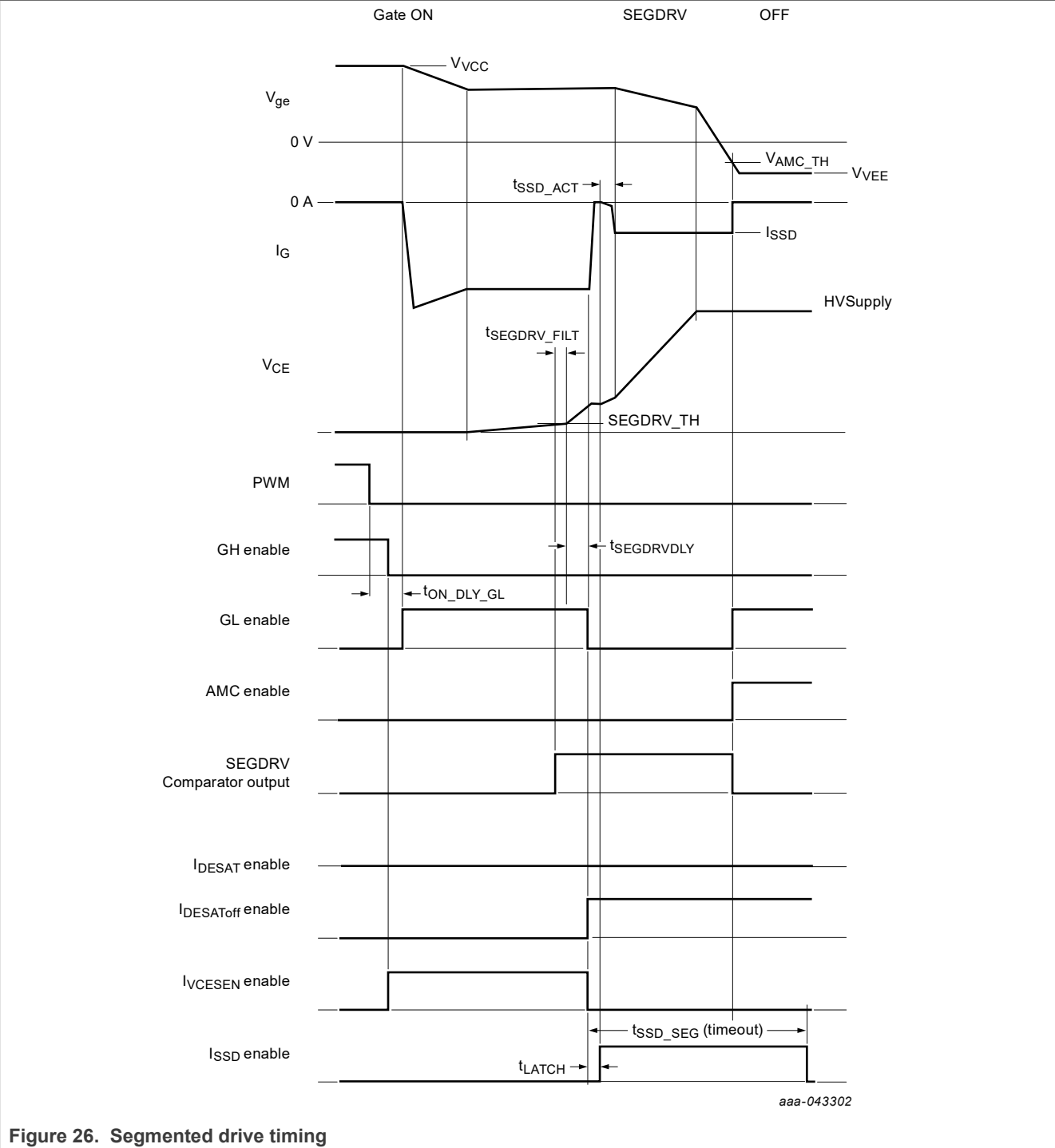


Figure 26. Segmented drive timing

## 11.7 Fault status and analog reporting

### 11.7.1 Introduction

The GD3160 reports the status of faults and real-time power device conditions (such as VGE, VCE, power device temperature) via the INTA and INTB interrupt pins, as well as the analog reporting AOUT pin.

### 11.7.2 INTB pin

The INTB rapidly reports faults and status changes. Once any fault is filtered and validated by its detection circuitry, the presence of a fault is reported at the INTB pin within 1.6  $\mu$ s. Fault type and warning data are received by the SPI registers within 500 ns of validating the fault or warning.

All faults that can trigger the INTB are independently selected in SPI registers [MSK1](#) and [MSK2](#). The INTB's open drain active pulldown is released when the fault is cleared. Clearing a fault requires actively clearing it with an SPI write command to the status register address. Each fault bit is cleared only if the fault is no longer present. Unlike the INTA pin, the INTB pin is only configurable for fault reporting. Most faults have configurable report masks (the [RMSK1](#) and [RMSK2](#) registers) to route faults to either INTA or INTB, but some faults are restricted to only report on INTB, including:

- SPIERR
- CONFCRCERR
- RTMON\_FLT
- WDOG\_FLT
- COMERR
- BIST\_FAIL
- VDD\_UVOV

Faults that have no mask, but can be allocated to either INTA or INTB are given below:

- OTSD\_IC
- DESAT
- SC
- VREF\_UV

11.7.3 AOUT pin

During Normal operating mode the duty cycle at the AOUT pin is a function of the ADC value according to [Figure 27](#). The base frequency is 3.9 kHz  $\pm 3\%$ .

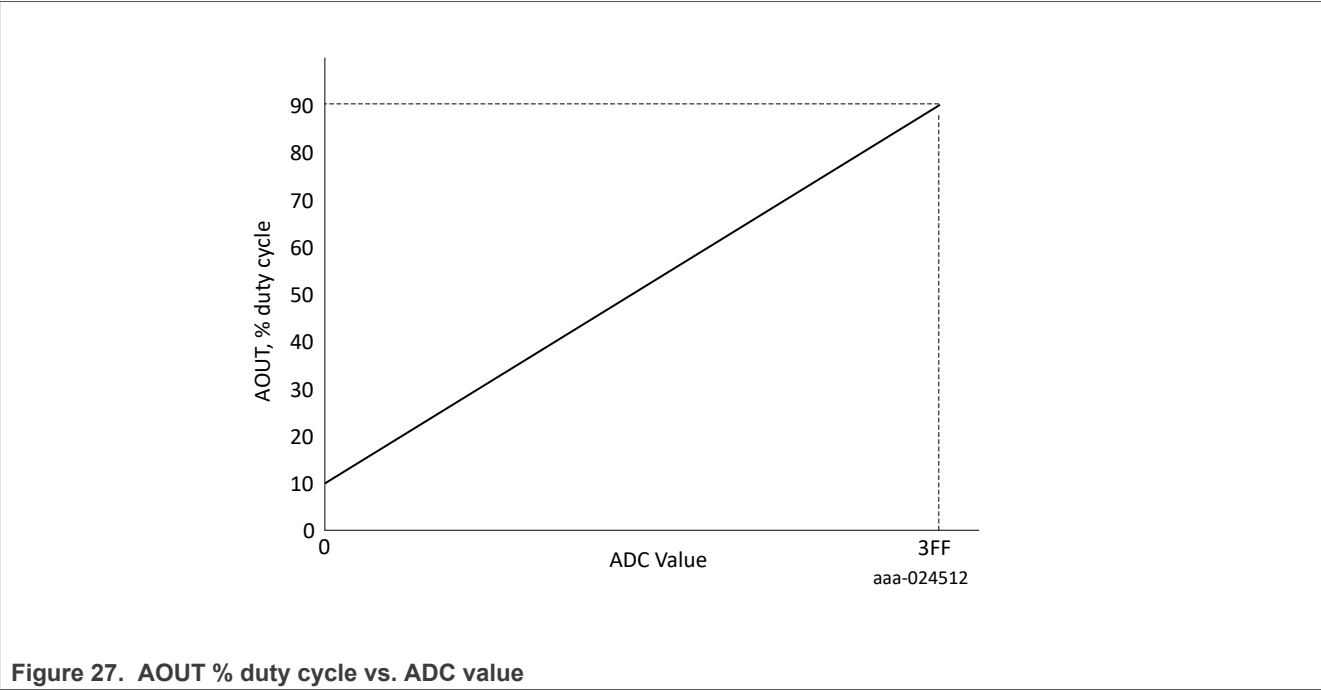


Figure 27. AOUT % duty cycle vs. ADC value

When the GD3160 is in the Wait mode, the duty cycle at the AOUT pin is 5.0 %. When the GD3160 is in BIST mode, the duty cycle is 0 %. When the GD3160 completes a BIST routine, the AOUT pin returns to normal operation.

The AOUT pin can be configured to simultaneously transmit two signals (when the bit AOUT = '1' in the MODE1 register). If this feature is enabled, the TSENSEA voltage is encoded by duty cycle at 3.9 kHz, and a second interleaved signal is encoded by duty cycle at a 5.6 kHz frequency ( $\pm 3\%$ ). The second signal is chosen via the SPI according to the AOUT\_SEL bits ([CONFIGAOUT](#) register) and delivered in a repeating, interleaved pattern determined by the AOUTCONF bits ([CONFIG5](#) register).

When ADC updates are not available (for example, during SPI) the PWM duty cycle on AOUT signal will reflect the last valid ADC value. [Figure 28](#) describes the AOUT pin signal with two interleaved duty cycles (AOUT = '1' in MODE1 register).

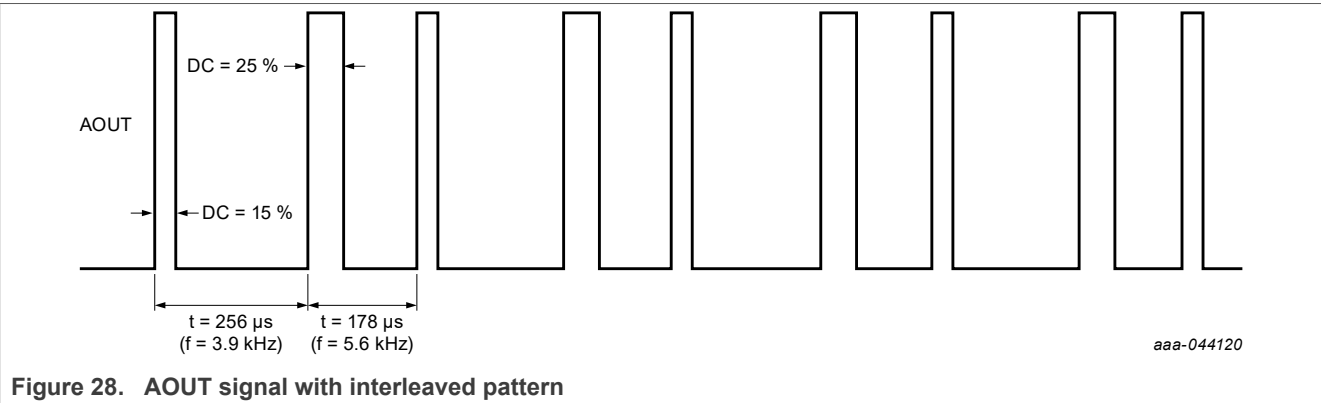


Figure 28. AOUT signal with interleaved pattern

11.8 VGE real-time monitoring (RTMON)

If RTMON\_FLTM = '1' and RTMON\_CFG = '0', after a programmable delay time,  $t_{RTMONDLY}$ , the low-voltage domain compares the PWM input to the actual state of the gate. For this purpose, as shown in Figure 29, it is required that  $t_{RTMONDLY} > t_{ON\_DLY\_GH} + t_{RTRPT\_DLY}$ . If VGE fails to respond to the PWM command, the fault is latched and reported via the SPI and at the INTA/INTB pin and the IGBT's gate is commanded off.

Figure 29 shows how the low-voltage domain monitors the state of the power device gate.

The ON/OFF state of the gate is determined by thresholds referred to the VCCREG (positive gate supply) and VEE (negative gate supply) to support a variable gate supply range.

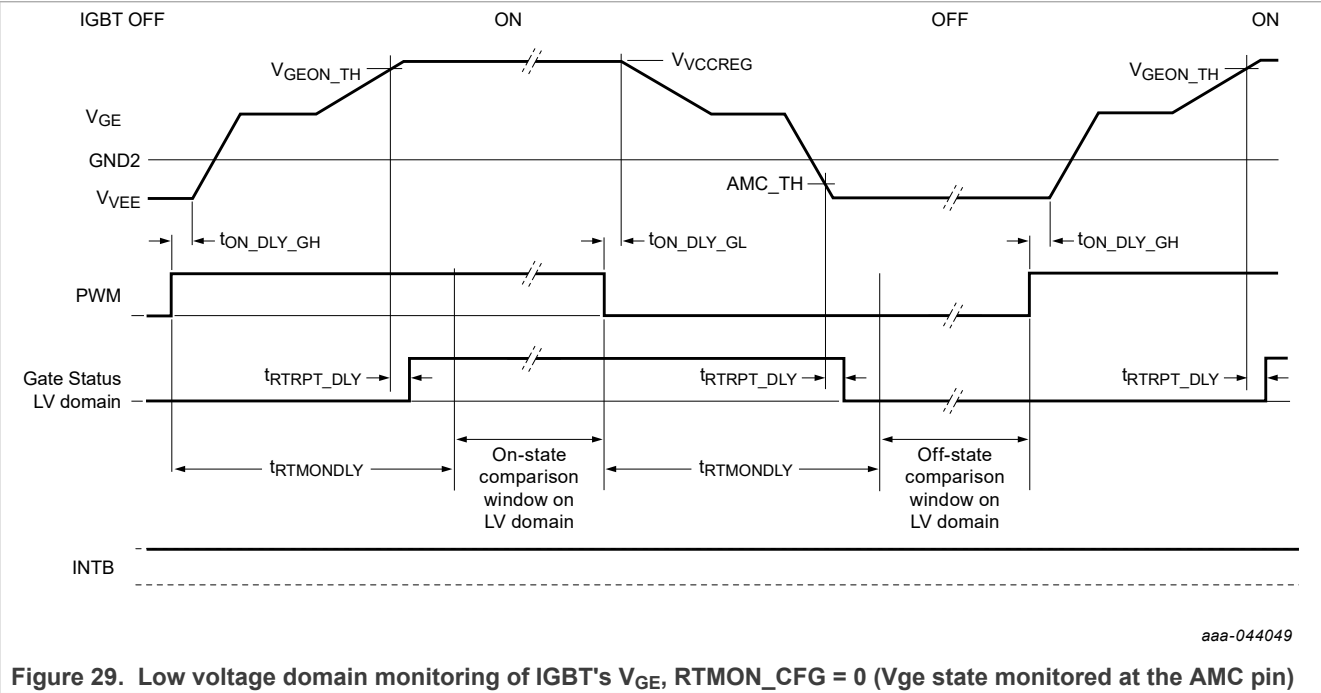


Figure 29. Low voltage domain monitoring of IGBT's  $V_{GE}$ ,  $RTMON\_CFG = 0$  (Vge state monitored at the AMC pin)

11.9 INTA fault reporting and real-time reporting

11.9.1 INTA overview

The INTA is an interrupt-style pin that can be configured for one of three different fault/status report functions, programmable by SPI. The INTA allocation is determined by the RTRPT and RTMON\_CFG bits in the [MODE2](#) register.

- 1. High severity fault/status report
- 2. Real-time collector voltage monitor/report
- 3. Real-time gate state monitor/report

Table 24. INTA configuration options

| RTRPT mode bit | RTMON_CFG mode bit | INTA operation   |
|----------------|--------------------|--|
| 0              | X                  | Real-time reporting disabled<br>INTA configured as a fault report <ul style="list-style-type: none"><li>• Configure report mask with <a href="#">RMSK1</a> and <a href="#">RMSK2</a> registers</li></ul> |
| 1              | 0                  | Real-time report enabled<br>INTA reports VGE status  |
| 1              | 1                  | Real-time report enabled<br>INTA reports VCE status  |

11.9.2 INTA fault reporting

When INTA is configured as a fault reporter, the INTA pin is configured as an open-drain output with a 50 kΩ passive pullup. Once a fault has been detected and validated, the fault is indicated to the INTA pin within 1.6 μs. Fault type and warning data are received by the SPI registers within 500 ns of validating the fault or warning condition.

In this configuration, INTA will be pulled low within 1.6 μs when a fault – which is allocated for INTA, and not masked as a whole – is validated. The fault mask for the entire GD3160 device is set by the [MSK1](#) and [MSK2](#) registers. The allocation (for unmasked faults) between INTA and INTB pins is determined by the [RMSK1](#) and [RMSK2](#) registers.

11.9.3 INTA real-time VCE reporting

When INTA is configured as a real-time VCE reporter, the INTA pin is transistor-driven to VDD and GND1, and reports the state of the collector/drain voltage as seen at the DESAT pin. The DESAT pin therefore needs to be connected to the power device collector or drain pin.

When V<sub>CE</sub> or V<sub>DS</sub> voltage is above the DESAT threshold (set by DESAT\_TH bits), the INTA pin is pulled to logic low after a delay of t<sub>RTRPT\_DLY</sub>, indicating the power device is off. When V<sub>CE</sub> or V<sub>DS</sub> voltage is below the DESAT threshold, the INTA pin is actively pulled logic high, indicating the power device is on.

An example timing diagram (with segmented drive disabled) showing V<sub>CE</sub>/V<sub>DS</sub> status reporting is given in [Figure 30](#).

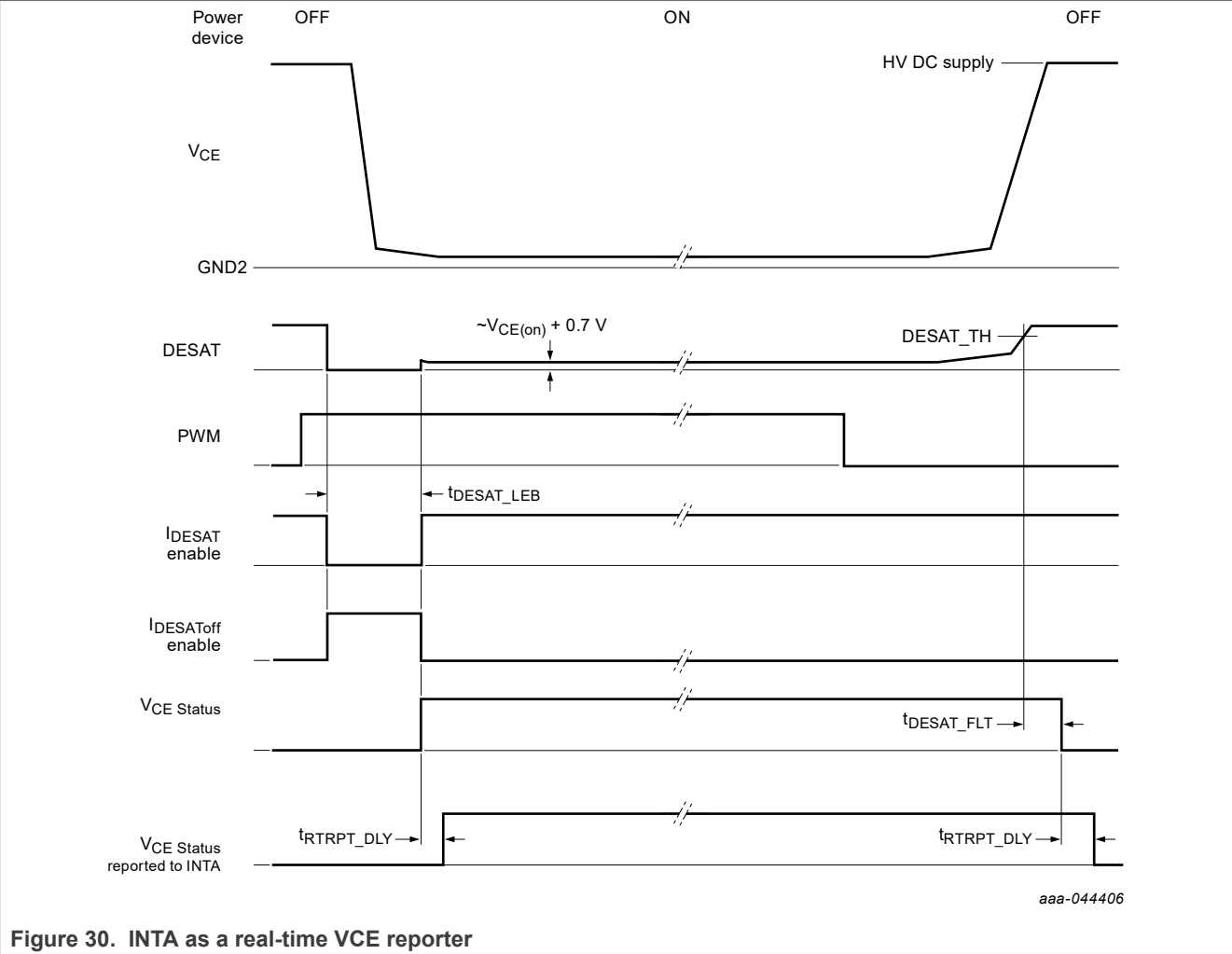


Figure 30. INTA as a real-time VCE reporter

When the GD3160 is configured for real-time reporting (RTRPT = 1 and RTMON\_CFG = 1), the I<sub>DESAT</sub> current source is always on, except during the DESAT leading edge blanking time, and when segmented drive is activated during turn-off. INTA reports a high V<sub>CE</sub>/V<sub>DS</sub> after segmented drive has completed during the turn-off.

The desaturation fault detection is active and monitored in parallel at the same time as the real-time. There is no interference or exclusivity between desaturation fault detection and the real-time V<sub>CE</sub>/V<sub>DS</sub> report.

11.9.4 INTA real-time VGE reporting

When INTA is configured as a real-time VGE reporter, the INTA pin is transistor-driven to VDD and GND1, and reports gate high/low status, as seen at the AMC pin. The AMC will therefore need to be directly connected to the power device gate pin, even if the active Miller clamp function is disabled.

An example of real-time gate voltage reporting is shown in [Figure 31](#).

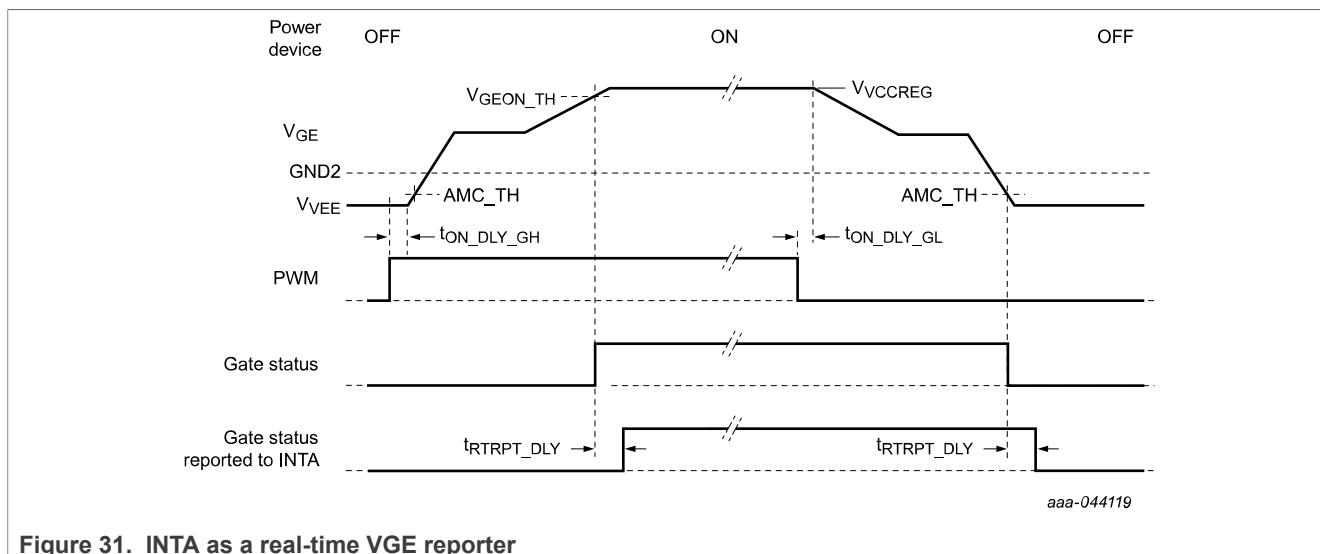


Figure 31. INTA as a real-time VGE reporter

When the gate voltage has surpassed  $V_{GEON\_TH}$ , the gate monitor circuitry interprets this as ON status, and INTA is actively pulled to logic high. When the gate falls below  $V_{AMC\_TH}$ , the gate monitor circuitry interprets an OFF status and INTA is pulled to logic low. The delay between gate voltage passing thresholds is a maximum 240 ns, represented by  $t_{RTRPT\_DLY}$  in Figure 31.

## 11.10 Power device overtemperature detection circuitry

### 11.10.1 Introduction

Directly monitoring the power device's temperature provides four advantages.

The first benefit is that the IGBT (and the system) can be protected against catastrophic IGBT failure from excessive temperature or a violation of its safe operating area at elevated temperature.

The second benefit is that the inverter need not be unnecessarily derated at high power because the IGBT's temperature is not known. Monitoring the IGBT's die temperature allows the controller to continue operating at conditions that might otherwise risk failure.

The third benefit is that the IGBT's temperature can be monitored for long term wear out mechanisms.

The fourth benefit is that the OTW signal allows the system to respond to unexpectedly high temperature before an OTSD fault triggers shutdown autonomously, which may not be desired.

### 11.10.2 Features

The features of the overtemperature detection circuitry are:

- Accurate current source available to drive temperature sense diodes, or disabled for thermistor-based measurements
- A 10-bit ADC to monitor the voltage across the temperature sense element
- On-the-fly programmable overtemperature and overtemperature warning thresholds
- 2.0 ms filters for overtemperature and OT warning
- 10-bit temperature value provided in the SPI temperature register and available as a duty cycle encoded signal at the AOUT pin
- Configurable gain and offset parameters to increase dynamic range of temperature measurements

Setting the TISNS\_EN bit to '1' in the [MODE2](#) register to Logic 1 enables the sense current,  $I_{OT}$ . Setting the TISNS\_EN bit to '0' disables the current source, to interface with resistive temperature-coefficient devices, such as NTCs, and so on.

OT and OTW thresholds are programmed at power up or on-the-fly and reside in the SPI registers OT\_TH and OTW\_TH. The intent is for OT\_TH and OTW\_TH to be calibrated at the system-level, considering on the characteristics of the temperature sense device. If OTW\_TH is set higher value than OT\_TH, the GD3160 detects negative temperature coefficient behavior, and enforces an overtemperature fault at measurements below OT\_TH. If OTW\_TH is set below OT\_TH, the GD3160 interprets the network as a positive temperature coefficient, and enforces the overtemperature (OT) fault at measurements above the OT\_TH.

An OTW fault is latched in the logic, reported via the SPI and the INTB pin but it does not turn off the IGBT's gate. An OTSD fault is latched in the logic, reported via the SPI and the INTB pin and turns off the IGBT's gate with its normal turn-off circuitry (no 2LTO or SSD). In case OTW fault is triggered and remains, RTMON\_FLT reporting is automatically masked, (not reported on INTB or SPI and no action on the gate).

When no SPI message has been received for  $\sim 200\ \mu\text{s}$ , the temperature sense ADC value is updated automatically as part of the LV/HV domain's watchdog refresh activity.

[Section 11.12](#) explains how the TSENSEA voltage can be monitored at the AOUT pin and the SPI.

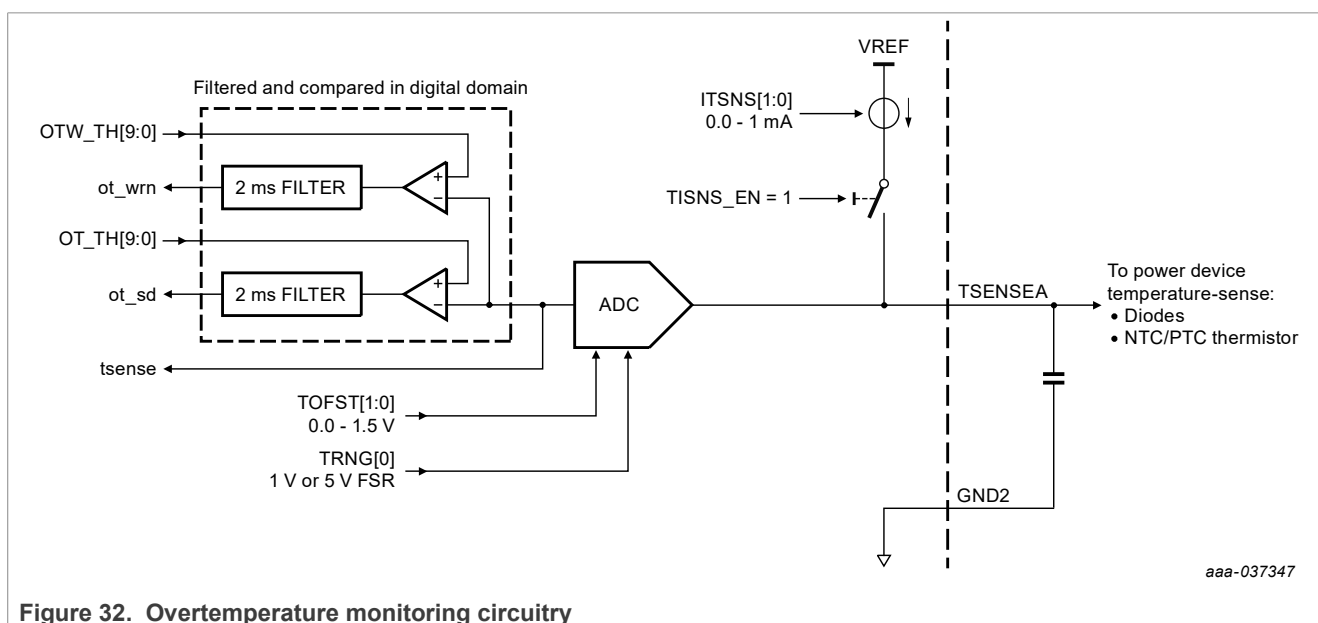


Figure 32. Overtemperature monitoring circuitry

## 11.11 Overtemperature detection of the GD3160

### 11.11.1 Introduction

The GD3160 monitors the temperature of its gate drive transistors and primary voltage regulators. The temperature sense circuitry protects the GD3160 and reports the temperature as a converted digital value.

The post-converted die temperature result is read directly from the [Request ADC Response](#) register (ADCVAL[9:0]).

### 11.11.2 Features

One of the three temperature sense circuits monitors the VDD regulator temperature on the low-voltage domain. A circuit on the high-voltage domain monitors the temperature near the GH drive transistor, the VCCREG pass transistor, and the VREF regulator. A second circuit on the high-voltage domain monitors the temperature near the GL and AMC transistors.

Any of the three temperature sensors can trigger an overtemperature shutdown of the IC. When the GD3160's temperature reaches its overtemperature shutdown threshold,  $T_{OTSDth}$ , the GD3160 reports the condition at the INTB pin and in the OTSD\_IC bit in the [STATUS1](#) register.

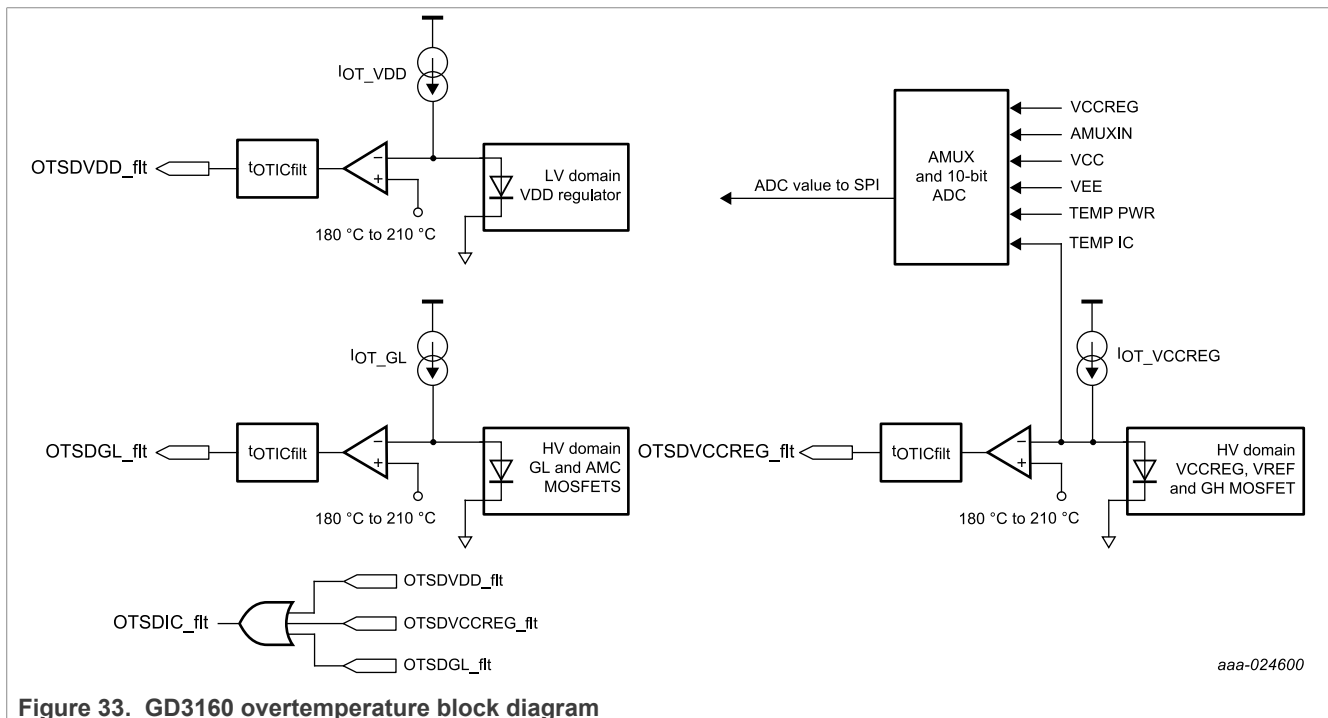
Regardless of the fault's source, an overtemperature signal disables PWMing by turning off the GH transistor and turning on the GL and AMC transistors (if the AMC feature is enabled). If the condition is detected on the high-voltage domain, the GD3160 turns off GH, VCCREG and VREF. If the VDD regulator is reporting the condition, the VDD regulator remains on. This leaves open the possibility that the MCU can manage the fault.

All overtemperature shutdown circuits have a low pass filter,  $t_{OTICfilt}$ ; its nominal value is 20  $\mu$ s. The specification is provided in the [Section 9.3](#).

There are two ways to read the voltage reported by the GH temperature sensor.

1. Send a REQADC SPI command requesting GH die temperature in [AMUX\\_SEL\[2:0\]](#) bits
2. Configure the AOUT pin to report die temperature at 5.6 kHz using the AOUT configuration bits in the [CONFIG5](#) and [CONFIGAOUT](#) registers.

[Figure 33](#) shows the block diagram of the temperature sensing circuitry on the GD3160.



**Figure 33. GD3160 overtemperature block diagram**

The internal die temperature at GH can be determined by [Equation 2](#).

$$T_{GH}(\text{degC}) = 372 - (\text{ADC}_{DEC} / 1.982) \quad (2)$$

## 11.12 AMUX and analog-to-digital converter

### 11.12.1 Introduction

The GD3160 has an analog multiplex circuit (AMUX) that provides signals to a 10-bit analog-to-digital converter (ADC). The circuit's primary purpose is to monitor the IGBT's temperature by sensing the voltage at the TSENSEA pin.

The AMUX and ADC allow reading and conversion of the voltages at the TSENSEA, AMUXIN, VCC, VCCREG, and VEE pins, as well as the output of the internal GH temperature sensor. The converted data can be monitored via the SPI or the AOUT pin with the appropriate SPI commands and register settings.

### 11.12.2 AMUX and ADC features

A block diagram of the AMUX-ADC circuitry is shown in [Figure 34](#). The ADC's full-scale voltage range depends on the signal it is sensing. For TSENSEA, AMUXIN and GH temperature the full-scale voltage is VREF, or nominally 5.0 V.

For VCC and VCCREG, which are attenuated 30x, the full-scale voltage is 1.0 V. GND2 is the ground reference for all ADC conversions. For reading VEE, the voltage is attenuated by 15x. See [Equation 3](#).

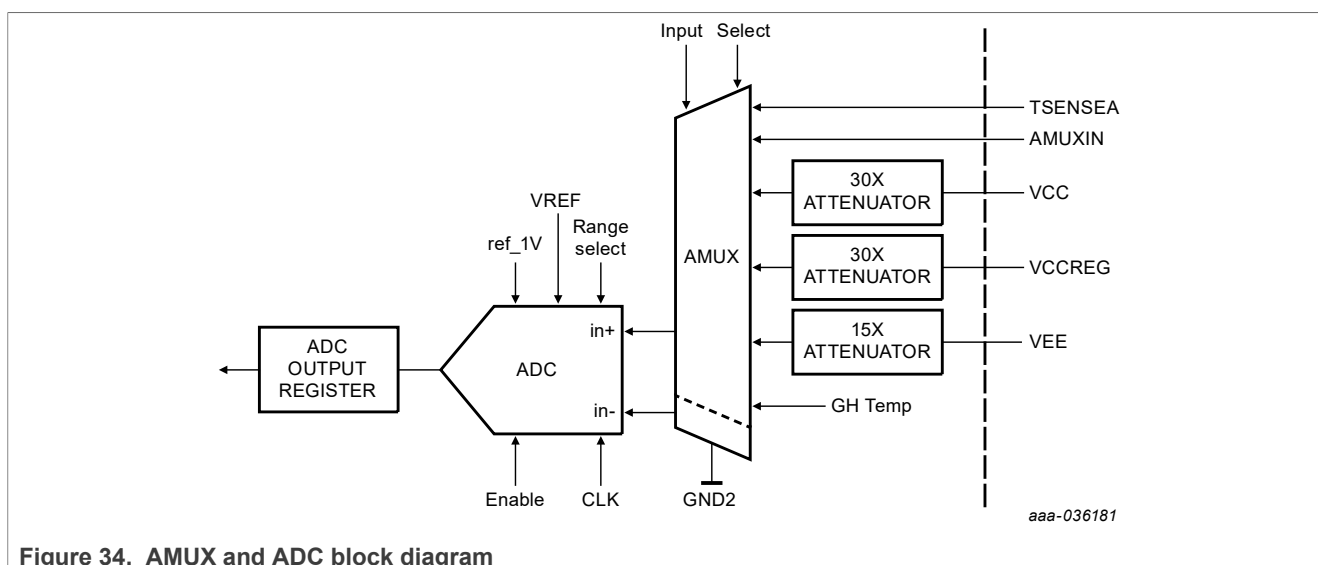


Figure 34. AMUX and ADC block diagram

The AMUX circuit provides the signals for conversion based on SPI register settings. The ADC output register is refreshed as part of the normal watchdog operation or when commanded via SPI. When there is no SPI activity for 200  $\mu$ s, the low-voltage domain autonomously sends a REQADC command to the high-voltage domain, requesting the TSENSEA voltage (or periodically, the AOUT\_SEL quantity, if AOUT = 1 in the [MODE1](#) register). The high voltage responds with the converted result of the requested quantity. This routinely supplies the low-voltage domain with data available to construct the AOUT response.

If a signal other than TSENSEA is desired, then the MCU can send a SPI message to read that signal at any time. A REQADC command returns the value of the signal specified by the AMUX\_SEL [2:0] bits in the REQADC command. This SPI communication also resets the watchdog timer.

The AOUT pin also reports the signal selected by the AMUX block. Normally and by default, the AOUT duty cycle provides the encoded TSENSEA voltage. However, setting the AOUT bit in the [MODE1](#) register to Logic 1 instructs the high-voltage domain to report one of the other signals, as well as IGBT temperature. When two signals are requested, they appear at AOUT alternatively at 3.9 kHz and 5.6 kHz periods. In this case, AOUT encodes TSENSEA followed by the signal specified by the AOUT\_SEL [2:0] bits in the [CONFIG4](#) register.

The GD3160 monitors the temperatures of the VDD regulator on the low-voltage domain, the GL transistor on the high-voltage domain, and the GH transistor on the high-voltage domain. The GH sensing element is near the VCCREG regulator, so it is protected, too. The VDD and GL circuits are used for overtemperature shutdown only. Their temperatures cannot be read via the SPI or the AOUT pin. Temperature values are available only for the GH temperature sensor on the high-voltage domain.

The output conversion values for AMUXIN and TSENSE are 000h to 3FFh (000h for 0 V; 3FF for VREF).

For VCC and VCCREG, the conversion values are 000h to 3FFh (000h for 0 V; 3FF for 30 V).

For VEE measurement through the AMUX, the conversion values are 000h (when VEE = –15 V) and 3FFh (when VEE = 0 V). The voltage at the VEE pin (referred to as GND2, negative in most cases) is converted by the ADC in [Equation 3](#):

$$ADC_{VEE} = \left( 1 + \frac{VEE}{15V} \right) * (1023 \text{ LSB}) \quad (3)$$

To perform a read of the ADC, set the bits AMUX\_SEL [2:0] according to the signal to be read. Next perform a read of the REQADC register. The result is then returned in the REQADC register. Note that the REQADC register is read only.

## 11.13 24-bit serial peripheral interface

### 11.13.1 Introduction

The serial peripheral interface (SPI) has the following features:

- Full duplex, four-wire synchronous communication
- Responder mode operation only
- Fixed SCLK polarity and phase requirements
- Fixed 16-bit command word with 8-bit cyclic redundancy check (CRC)
- SCLK operation up to 10 MHz
- Compatible with daisy-chain operation

SPI communication follows [Figure 35](#):

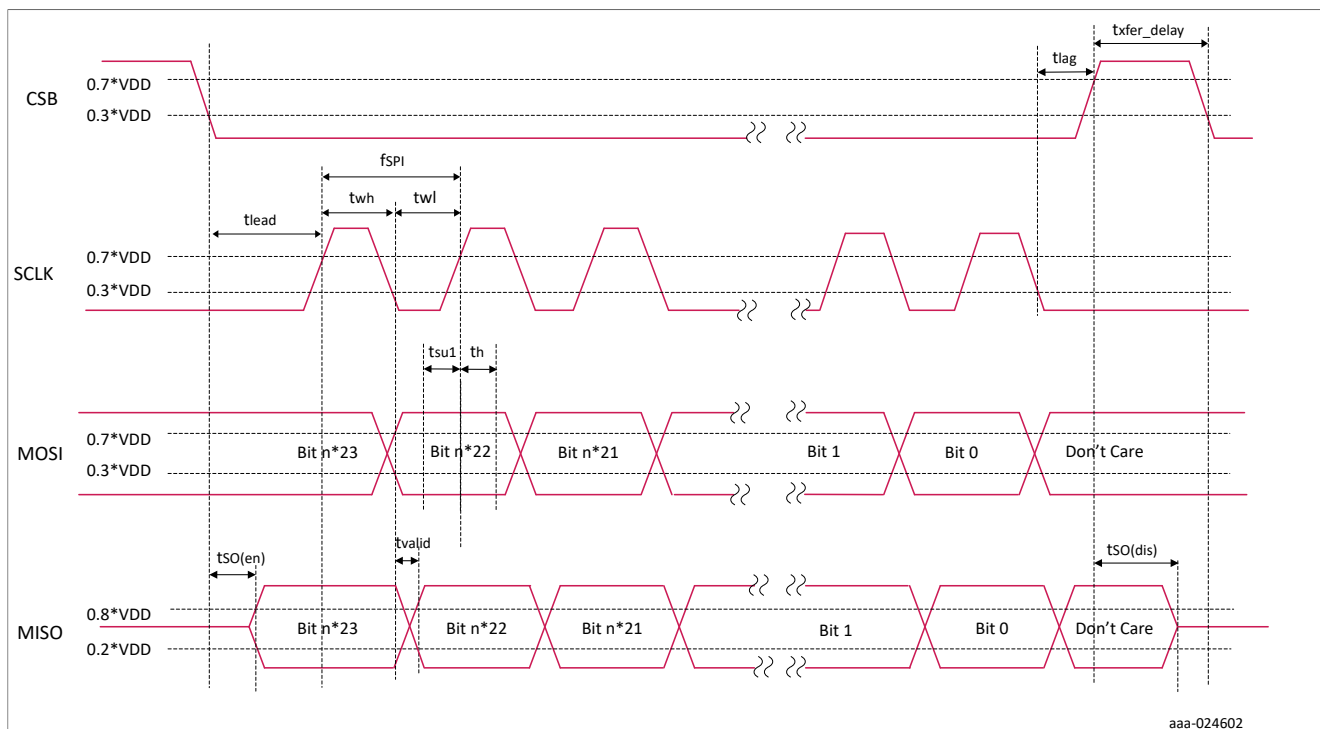


Figure 35. SPI timing

## SPI protocol:

- SPI MOSI data is read on SCLK rising edge.
- MISO data is changed on SCLK falling edge.
- SPI communication is MSB first.
- SPI command is composed of a multiple of 24 SCLK cycles.
- The number of clock cycles occurring on the pin SCLK while the CSB pin is asserted low must be a multiple of 24.
- The serial output data is available on the rising edge of SCLK and transitions on the falling edge of SCLK.
- The content of MISO reported by the GD3160 depends on the previously selected register address.
- On first SPI communication after a supply reset, the [MODE1](#) register is sent on the MISO line.
- If the number of clock pulses within CSB low is not a multiple of 24, then the current SPI write command is ignored. The error is logged in the [STATUS2](#) register; the SPIERR bit is set.
- Messages written to invalid locations (such as test or reserved registers) are ignored.
- When VDD is in under voltage condition, there will be no response on SPI. Both incoming and outgoing messages are suspended.

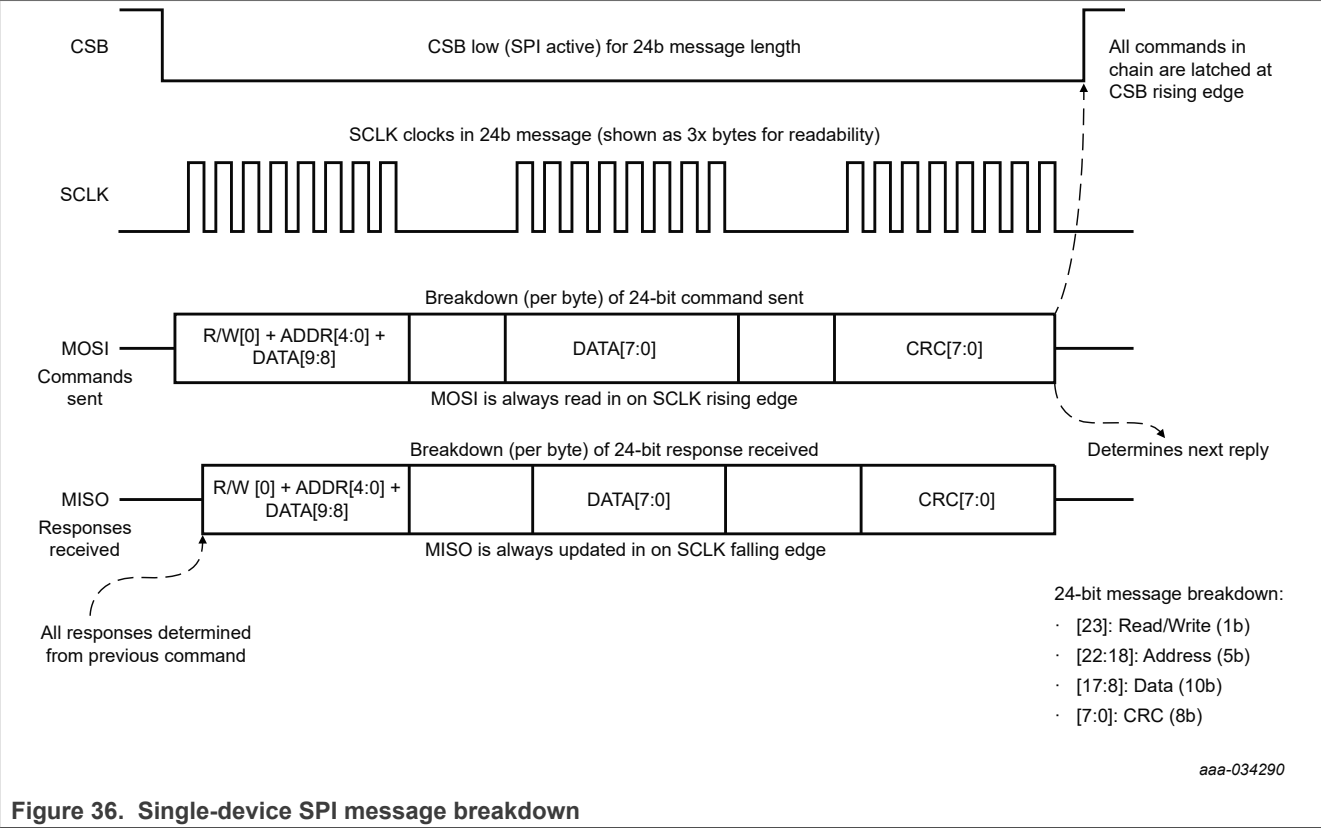


Figure 36. Single-device SPI message breakdown

11.13.2 SPI CRC

When transmitting a message, both the GD3160 and the SPI master calculate the CRC of the first 16 SPI bits [23:8] and append an eight bit CRC value as bits [7:0]. This completes the 24-bit SPI message.

The CRC is calculated using the polynomial  $x^8 + x^5 + x^3 + x^2 + x + 1$  (100101111) with a seed value of binary 11111111 (if the lookup table method is used, the seed value is 0x42). If the CRC of the received message matches its calculated CRC, then the message was received correctly (for CRC calculation example refer to "GD31xx Device Driver Example Code" on [www.nxp.com/GD3160](http://www.nxp.com/GD3160)).

If the CRC of the received message does not match the calculated CRC, there was a receive error and the data is not saved or used. The error is also logged in the [STATUS2](#) register; the SPIERR bit is set.

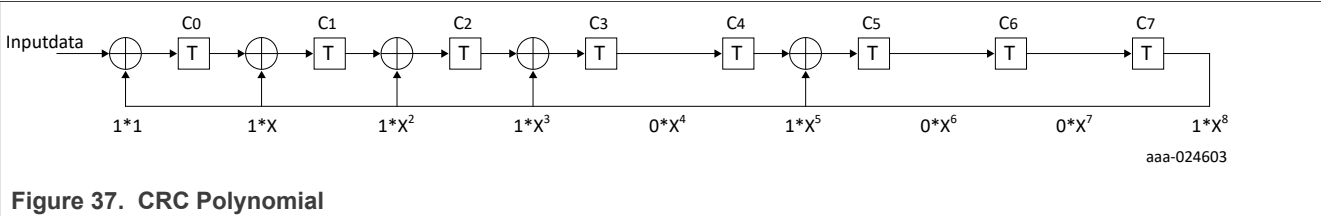


Figure 37. CRC Polynomial

11.13.3 Protection of register configuration

Most of the SPI registers are protected from inadvertent modification. They are intended to be configured at power up and left unchanged during normal operation, while the IGBT is being PWMed. This protection ensures that operating modes, fault masks, fault thresholds, and fault filter times are unchanged unless the GD3160 receives clear instructions to change them.

The registers that are protected are the CONFIG1 to 7 registers, the MODE1 and 2 registers, the RMSK1 and RMSK2 registers, and the MSK1 and 2 registers, except for VCCREG, SEGDRV\_TH and SEGDRVLY settings. The GD3160 must be in Configuration mode (CONFIG\_EN bit in the MODE2 register = Logic 1) to alter these registers.

A CRC of all the protected registers is calculated every watchdog cycle. This value is compared to a CRC that was calculated when the IC exited Configuration mode, including when the CONFIGAOUT, OT\_TH, or OTW\_TH registers were updated. A discrepancy between the two CRCs triggers a CONFIGCRCERR and is reported at the INTB pin and in the STATUS 2 register.

### 11.13.4 Clearing fault bits

There are several ways to clear a fault bit (contained in the [STATUS1](#) and [STATUS2](#) registers) on GD3160. Clearing a fault does not require reading the register beforehand.

1. Writing a Logic 1 to the faulted bit in the STATUS1 or STATUS2 register. Writing a Logic 1 to the faulted bit will clear the faulted bit if the fault is no longer present. This procedure clears the BIST\_FAIL, POR\_1, and POR\_2 bits, if set. This is the most common method of clearing a fault.
2. Reset the GD3160 logic by toggling the RESET bit in the MODE2 register. Logic 1 at the RESET bit not only resets the SPI fault bits, it also returns all the low-voltage and high-voltage domains configurable registers to their default values. When Logic 0 is written, the fault bit(s) will be Logic 0 unless the fault is still present.
3. Conduct BIST test by toggling the BIST bit in the MODE2 register. Logic 1 at this bit forces the low-voltage and high-voltage domains to conduct a BIST. Upon exiting BIST, the low-voltage and high-voltage domain's logic will be reset to the default state. The only exception is that the BIST procedure will not clear the BIST\_FAIL bit, if that happens to be set.
4. All SPI registers, including fault bits, will be reset to their default values at power up or upon a POR of the low-voltage domain logic supply.

Exceptions for VDD undervoltage:

- To avoid reporting spurious faults at power up, the GD3160 latches no faults until VDD is in regulation. If a VDD\_UVOV fault is detected, the VDD supply may have fallen to a level that triggers a logic POR. The MCU can respond by assuming a POR has occurred and reinitialize the GD3160 or it can read a programmed register to see if it has changed.

Exception when HV domain remains powered:

- When VDD falls below VDDUV\_TH, the low-voltage domain no longer sends messages to the high-voltage domain. The high-voltage domain detects a loss communication and reverts to its fail-safe mode. When VDD returns to a regulated state, the high-voltage domain may have residual latched faults.

### 11.13.5 Daisy chain operation

Daisy chain operation reduces the total MCU pin count for SPI and increases message length and polling times. The recommended implementation for inverter applications requiring functional safety is to have two parallel chains of three devices: one daisy chain for three high-side gate drivers, one daisy chain for three low-side gate drivers).

All GD3160 in each group have a single CSB connection. The MCU's MOSI pin is connected to the MOSI pin of the first GD3160 in the chain. The MISO pin of the first GD3160 is connected to the MOSI pin of the 2nd GD3160, and so on. An example implementation is shown in [Figure 38](#).

Data from the MCU is clocked through the daisy chain to each device while the CSB bit is commanded low by the MCU. During each SCLK clock cycle, output status from the daisy chain is transferred to the MCU via the MISO line. On the rising edge of CSB, data stored in the input registers is latched within each GD3160. An example implementation is shown in [Figure 39](#).

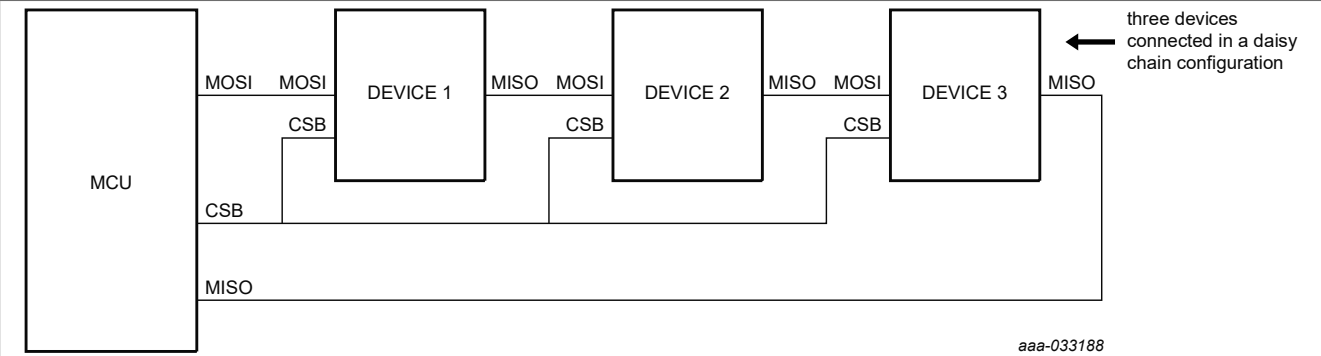


Figure 38. Daisy chain connection

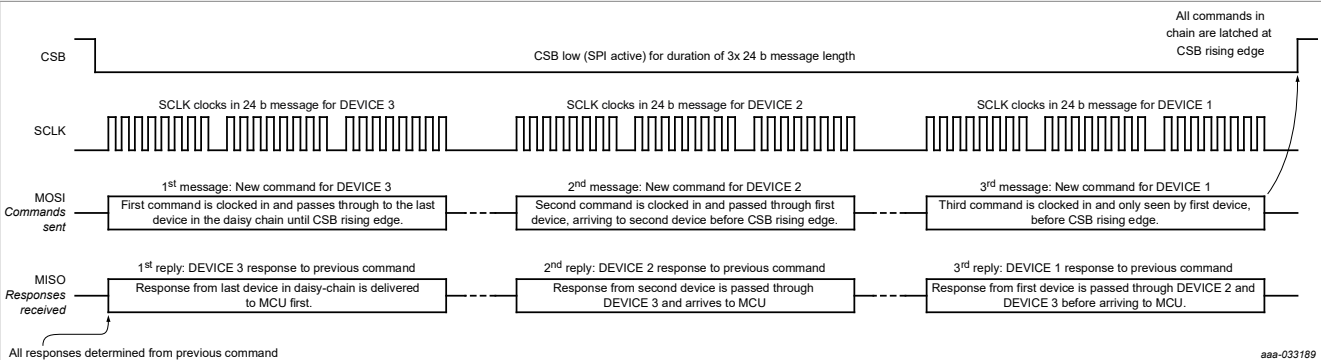


Figure 39. Daisy chain data transmission

11.14 SPI registers

The SPI registers and their definitions are shown in [Table 25](#).

Table 25. SPI registers

| SPI COMMANDS                |                         | Rb/W | ADDR[4:0]    | DATA9         | DATA8           | DATA7           | DATA6           | DATA5         | DATA4         | DATA3         | DATA2           | DATA1           | DATA0           | CRC   |
|-----------------------------|-------------------------|------|--------------|---------------|-----------------|-----------------|-----------------|---------------|---------------|---------------|-----------------|-----------------|-----------------|-------|
| Name                        | Description             | [23] | [22:18]      | [17]          | [16]            | [15]            | [14]            | [13]          | [12]          | [11]          | [10]            | [9]             | [8]             | [7:0] |
| <a href="#">MODE1</a>       | Operating Mode 1        | 0/1  | 0x00         | AOUT          | SEGDRV          | AMC             | TIME_2          | SSD           | 2LTO          | ACTCLMP       | DESAT           | SCSNS           | OCSNS           | -     |
| <a href="#">MODE2</a>       | Operating Mode 2        | 0/1  | 0x01         | SCFF          | RTRPT           | RTMON_CFG       | FSISOEN         | TISNS_EN      | —             | BIST          | CONFIG_EN       | RESET           | -               | -     |
| <a href="#">CONFIG1</a>     | Configuration 1         | 0/1  | 0x02         | UV_LATCH      | UV_TH [2]       | UV_TH [1]       | UV_TH [0]       | OCTH [2]      | OCTH [1]      | OCTH [0]      | OCFILT [2]      | OCFILT [1]      | OCFILT [0]      | -     |
| <a href="#">CONFIG2</a>     | Configuration 2         | 0/1  | 0x03         | 2LTOV [3]     | 2LTOV [2]       | 2LTOV [1]       | 2LTOV [0]       | SCTH [2]      | SCTH [1]      | SCTH [0]      | SCFILT [2]      | SCFILT [1]      | SCFILT [0]      | -     |
| <a href="#">CONFIG3</a>     | Configuration 3         | 0/1  | 0x04         | INTBFS        | SEG_DRV DLY [2] | SEG_DRV DLY [1] | SEG_DRV DLY [0] | SSD_CUR [2]   | SSD_CUR [1]   | SSD_CUR [0]   | SSDT [2]        | SSDT [1]        | SSDT [0]        | -     |
| <a href="#">CONFIG4</a>     | Configuration 4         | 0/1  | 0x05         | DESAT_FLT [1] | DESAT_FLT [0]   | SEGDRV_TH [2]   | SEGDRV_TH [1]   | SEGDRV_TH [0] | IDESAT [1]    | IDESAT [0]    | DESAT_LEB [2]   | DESAT_LEB [1]   | DESAT_LEB [0]   | -     |
| <a href="#">CONFIG5</a>     | Configuration 5         | 0/1  | 0x06         | DEADT [3]     | DEADT [2]       | DEADT [1]       | DEADT [0]       | —             | AOU_TCONF [1] | AOU_TCONF [0] | COMERR_CONF [2] | COMERR_CONF [1] | COMERR_CONF [0] | -     |
| <a href="#">CONFIG6</a>     | Configuration 6         | 0/1  | 0x07         | VCCREG[2]     | VCCREG[1]       | VCCREG[0]       | —               | WDTO [1]      | WDTO [0]      | RTMONDLY [3]  | RTMONDLY [2]    | RTMONDLY [1]    | RTMONDLY [0]    | -     |
| <a href="#">CONFIG7</a>     | Configuration 7         | 0/1  | 0x08         | —             | —               | —               | —               | —             | —             | DESAT_TH [3]  | DESAT_TH [2]    | DESAT_TH [1]    | DESAT_TH [0]    | -     |
| <a href="#">OT_TH</a>       | Config OT Threshold     | 0/1  | 0x09         | OT_TH [9]     | OT_TH [8]       | OT_TH [7]       | OT_TH [6]       | OT_TH [5]     | OT_TH [4]     | OT_TH [3]     | OT_TH [2]       | OT_TH [1]       | OT_TH [0]       | -     |
| <a href="#">OTW_TH</a>      | Conf. OT Warn Thresh    | 0/1  | 0x0A         | OTW_TH [9]    | OTW_TH [8]      | OTW_TH [7]      | OTW_TH [6]      | OTW_TH [5]    | OTW_TH [4]    | OTW_TH [3]    | OTW_TH [2]      | OTW_TH [1]      | OTW_TH [0]      | -     |
| <a href="#">STATUS1</a>     | Status 1                | 0/1  | 0x0B         | VCCOV         | VCC_REGUV       | VSUPOV          | OTSD_IC         | OTSD          | OTW           | CLAMP         | DESAT           | SC              | OC              | -     |
| <a href="#">MSK1</a>        | Status Mask 1           | 0/1  | 0x0C         | VCCOVM        | VCC_REGUVM      | VSUPOVM         | —               | OTSDM         | OTWM          | CLAMPM        | —               | —               | OCM             | -     |
| <a href="#">RMSK1</a>       | Report Mask 1           | 0/1  | 0x0D         | VCCOVA        | VCC_REGUVA      | VSUPOVA         | OTSD_ICA        | OTSDA         | OTWA          | CLAMPA        | DESATA          | SCA             | OCA             | -     |
| <a href="#">STATUS2</a>     | Status 2                | 0/1  | 0x0E         | BIST_FAIL     | VDD_UVOV        | DTFLT           | SPIERR          | CONFCCR_CERR  | RTMON_FLT     | WDOG_FLT      | COMERR          | VREF_UV         | VEE_OOR         | -     |
| <a href="#">MSK2</a>        | Status Mask 2           | 0/1  | 0x0F         | —             | —               | DTFLTM          | SPIERRM         | CONFCCR_CERRM | RTMON_FLTM    | WDOG_FLTM     | COMERRM         | —               | VEE_OORM        | -     |
| <a href="#">RMSK2</a>       | Report Mask 2           | 0/1  | 0x10         | —             | —               | DTFLTA          | —               | —             | —             | —             | —               | VREF_UVA        | VEE_OORA        | -     |
| <a href="#">STATUS3</a>     | Status 3                | 0/1  | 0x11         | POR_1         | POR_2           | FSISO           | PWM             | PWMALT        | FSSTATE       | FSENB         | INTB            | INTA            | VRTMON          | -     |
| <a href="#">CONFIGA_OUT</a> | AOUT Configuration      | 0/1  | 0x12         | ITSNS[1]      | ITSNS[0]        | TOFST[1]        | TOFST[0]        | TRNG          | AMU_XINRNG    | AMUXINOS[1]   | AMUXINOS[0]     | AOUT_SEL [1]    | AOUT_SEL [0]    | -     |
| <a href="#">REQADC</a>      | REQUEST ADC (command)   | 0    | 0x13         | —             | —               | —               | —               | —             | —             | AMUX_SEL [3]  | AMUX_SEL [2]    | AMUX_SEL [1]    | AMUX_SEL [0]    | -     |
|                             | REQUEST ADC (response)  | 0    | 0x13         | ADCVAL [9]    | ADCVAL [8]      | ADCVAL [7]      | ADCVAL [6]      | ADCVAL [5]    | ADCVAL [4]    | ADCVAL [3]    | ADCVAL [2]      | ADCVAL [1]      | ADCVAL [0]      | -     |
| <a href="#">REQBIST</a>     | REQUEST BIST (command)  | 0    | 0x14         | 0             | 0               | 0               | 0               | 0             | 0             | 0             | 0               | 0               | 0               | -     |
|                             | REQUEST BIST (response) | 0    | 0x14         | REQBIST [9]   | REQBIST [8]     | REQBIST [7]     | REQBIST [6]     | REQBIST [5]   | REQBIST [4]   | REQBIST [3]   | REQBIST [2]     | REQBIST [1]     | REQBIST [0]     | -     |
| <a href="#">ID</a>          | Device ID               | 0    | 0x15         | —             | —               | VDD3            | LVDC[2]         | LVDC[1]       | LVDC[0]       | FS3ST         | HVDC[2]         | HVDC[1]         | HVDC[0]         | -     |
| —                           | Not used                | —    | 0x16 to 0x1F | —             | —               | —               | —               | —             | —             | —             | —               | —               | -               | -     |

11.14.1 MODE1 register (ADDR = 0x00)

The MODE1 register settings enable or disable major functions of the GD3160, mostly regarding power device protections.

Table 26. MODE1 register bit readout

|                             | Rb/W | ADDR [4:0] | DATA9 | DATA8  | DATA7 | DATA6  | DATA5 | DATA4 | DATA3   | DATA2 | DATA1 | DATA0 | CRC   |
|-----------------------------|------|------------|-------|--------|-------|--------|-------|-------|---------|-------|-------|-------|-------|
| Bit #                       | [23] | [22:18]    | [17]  | [16]   | [15]  | [14]   | [13]  | [12]  | [11]    | [10]  | [9]   | [8]   | [7:0] |
| Name/Value                  | 0/1  | 0x00       | AOUT  | SEGDRV | AMC   | TIME_2 | SSD   | 2LTO  | ACTCLMP | DESAT | SCSNS | OCSNS | —     |
| Write locked in normal mode | —    | —          | yes   | yes    | yes   | yes    | yes   | yes   | yes     | yes   | yes   | yes   | —     |
| Default                     | —    | —          | 0     | 0      | 1     | 1      | 1     | 1     | 0       | 1     | 0     | 0     | —     |

Table 27. MODE1 register description

| Bit     | Bit function  | Logic 0   | Logic 1  |
|---------|---|---|--|
| AOUT    | Configure operation of AOUT pin, reporting one or two signals                                 | AOUT reports power device temperature only, continuously running at ~3.9 kHz. Duty cycle is a function of the ADC-converted TSENSEA result (10 % = 0x000, 90 % = 0x3FF). <sup>[1]</sup> | AOUT reports power device temperature and a second quantity, set by AOUT_SEL. Signals appear at AOUT alternatively at ~3.9 kHz and ~5.6 kHz periods. |
| SEGDRV  | Segmented drive enable/disable bit  | Segmented drive feature disabled. <sup>[1]</sup>  | Segmented drive feature enabled.   |
| AMC     | Active Miller clamp enable/disable bit  | Active Miller clamp feature disabled. AMC transistor is deactivated, but the AMC_th comparator is still operational.  | Active Miller clamp feature enabled. <sup>[1]</sup>  |
| TIME_2  | Timer scaling bit for SSDT, RTMONDLY, DEADT, t <sub>VCECR</sub> and t <sub>SSD_SEG</sub>      | Timers are multiplied by 2.   | Timers are not scaled. <sup>[1]</sup>  |
| SSD     | Soft shutdown enable/disable bit (for DESAT and SC conditions only, otherwise SSD is enabled) | Soft shutdown disabled.   | Soft shutdown enabled. <sup>[1]</sup>  |
| 2LTO    | Two-level turn-off enable/disable bit (for DESAT and SC conditions only)                      | Two-level turn-off disabled.  | Two-level turn-off enabled. <sup>[1]</sup>   |
| ACTCLMP | V <sub>CE</sub> Active clamping enable/disable bit  | V <sub>CE</sub> Active clamping disabled. <sup>[1]</sup>  | V <sub>CE</sub> Active clamping enabled, if SEGDRV = 0.  |
| DESAT   | V <sub>CE</sub> DESAT fault management enable/disable bit                                     | V <sub>CE</sub> DESAT fault management disabled.  | V <sub>CE</sub> DESAT fault management enabled. <sup>[1]</sup>   |
| SCSNS   | Short current fault management enable/disable bit   | Disable short current fault management. <sup>[1]</sup>  | Enable short current fault management.   |
| OCSNS   | Overcurrent fault management enable/disable bit   | Disable overcurrent fault management. <sup>[1]</sup>  | Enable overcurrent fault management, if SEGDRV = 0 and ACTCLAMP = 0.   |

[1] Default value

### 11.14.2 MODE2 register (ADDR = 0x01)

The MODE2 register settings enable or disable critical features of the GD3160, and include commands for entering configuration mode (CONFIG), configuring INTA (RTRPT, RTMON\_CFG), enabling built-in self-test (BIST), resetting the device (RESET), enabling control by FSISO, and others.

Table 28. Mode2 register bit readout

|                             | Rb/W | ADDR [4:0] | DATA9 | DATA8 | DATA7     | DATA6   | DATA5    | DATA4 | DATA3 | DATA2     | DATA1 | DATA0 | CRC   |
|-----------------------------|------|------------|-------|-------|-----------|---------|----------|-------|-------|-----------|-------|-------|-------|
| Bit #                       | [23] | [22:18]    | [17]  | [16]  | [15]      | [14]    | [13]     | [12]  | [11]  | [10]      | [9]   | [8]   | [7:0] |
| Name/Value                  | 0/1  | 0x01       | SCFF  | RTRPT | RTMON_CFG | FSISOEN | TISNS_EN | —     | BIST  | CONFIG_EN | RESET | —     | —     |
| Write locked in normal mode | —    | —          | yes   | yes   | yes       | yes     | yes      | yes   | yes   | no        | yes   | yes   | —     |
| Default                     | —    | —          | 1     | 0     | 0         | 1       | 1        | 0     | 0     | 0         | 0     | 0     | —     |

Table 29. Mode2 register description

| Bit       | Bit function  | Logic 0  | Logic 1   |
|-----------|---|--|---|
| SCFF      | Short-circuit Fast-filter mode                        | Normal short-circuit filter (SCFILT) times used.                                   | Short-circuit filter times (SCFILT) are 300 ns faster. <sup>[1]</sup>   |
| RTRPT     | Real-time report (VGE/VCE) on INTA enable/disable bit | Real-time report disabled. INTA is used for fault monitor/report. <sup>[1]</sup>   | Real-time report on INTA enabled (all fault reporting on INTB).   |
| RTMON_CFG | Real-time monitor/report selection                    | Report/Monitor using VGE. <sup>[1]</sup>   | Report using VCE. This will also automatically mask the RFTMON_FLT. Real time Monitoring using VCE is not possible. |
| FSISOEN   | FSISO enable/disable                                  | FSISO pin is not active; pin state is ignored.                                     | FSISO pin is active. FSISO pin controls gate output when high. <sup>[1]</sup>                                       |
| TISNS_EN  | Temperature sense excitation selection                | Internal current source disabled. For use with thermistor-based solutions. (use an | Current source (0.25 mA to 1.0 mA, per ITSNS[1:0]) activated. For use with diode-based solutions. <sup>[1]</sup>    |

Table 29. Mode2 register description...continued

| Bit       | Bit function                              | Logic 0  | Logic 1   |
|-----------|---|--|---|
|           |   | external resistor network to bias from VREF)                                 |   |
| BIST      | BIST enable/disable                       | BIST feature is not active <sup>[1]</sup>                                    | Requests BIST of LV and HV die. PWMing is disabled until BIST is complete and BIST is reset to Logic 0. IGBT is OFF during BIST.  |
| CONFIG_EN | SPI register configuration enable/disable | Configuration of SPI registers is disabled. Normal operation. <sup>[1]</sup> | Enables Configuration of the SPI registers. IGBT gate is OFF during Configuration. CRC value of configured registers is calculated and stored on CSB rising edge when exiting configuration. PWMing is allowed on the next PWM rising edge after bit = 0. INTB pin reports faults normally. |
| RESET     | Reset enable/disable                      | GD31SiC not in Reset. Normal operating mode. <sup>[1]</sup>                  | GD31SiC in reset. All configuration registers are set to default values. PWMing is disabled. Configuration is disabled. IGBT is OFF. INTB = 0.  |

[1] Default value

### 11.14.3 CONFIG1 register (ADDR = 0x02)

The CONFIG1 register contains ranges for overcurrent (voltage) threshold level, overcurrent filter time, gate supply undervoltage threshold level, and selects behavior following a gate supply undervoltage event (latching or non-latching turn-off).

Table 30. CONFIG1 register bit readout

|                             | Rb/W | ADDR [4:0] | DATA9    | DATA8     | DATA7     | DATA6     | DATA5    | DATA4    | DATA3    | DATA2      | DATA1      | DATA0      | CRC   |
|-----------------------------|------|------------|----------|-----------|-----------|-----------|----------|----------|----------|------------|------------|------------|-------|
| Bit #                       | [23] | [22:18]    | [17]     | [16]      | [15]      | [14]      | [13]     | [12]     | [11]     | [10]       | [9]        | [8]        | [7:0] |
| Name/Value                  | 0/1  | 0x02       | UV_LATCH | UV_TH [2] | UV_TH [1] | UV_TH [0] | OCTH [2] | OCTH [1] | OCTH [0] | OCFILT [2] | OCFILT [1] | OCFILT [0] | —     |
| Write locked in normal mode | —    | —          | yes      | yes       | yes       | yes       | yes      | yes      | yes      | yes        | yes        | yes        | —     |
| Default                     | —    | —          | 0        | 0         | 1         | 1         | 0        | 1        | 1        | 0          | 1          | 1          | —     |

Table 31. CONFIG1 bit description

| Bit      | Bit function                           | Logic 0   | Logic 1  |
|----------|--|---|--|
| UV_LATCH | Configure VCCREG undervoltage behavior | PWM is gated by VCCREG undervoltage condition, but not latched off. INTA or INTB follows the VCCREG UV condition. VCCREG_UV SPI fault bit is latched. PWM disabled during VCCREG UV condition only. PWM is allowed upon VCCREG recovery. <sup>[1]</sup> | PWM is latched off upon VCCREG undervoltage condition, until fault is cleared. INTA or INTB follows the VCCREG UV fault. SPI fault bit is latched. PWM is disabled until the VCCREG_UV fault bit is cleared. |

[1] Default value

Table 32. CONFIG1 parameter ranges

| Bit value [2:0] | VCCREG undervoltage threshold UV_TH[2:0] | Overcurrent fault detection threshold OCTH[2:0] | Overcurrent fault detection filter time OCFILT[2:0] |
|-----------------|--|---|---|
| 0x00            | 10.0 V                                   | 0.25 V  | 0.5 µs  |
| 0x01            | 10.5 V                                   | 0.50 V  | 1.0 µs  |
| 0x02            | 11.0 V                                   | 0.75 V  | 1.5 µs  |
| 0x03            | 11.5 V <sup>[1]</sup>                    | 1.00 V <sup>[1]</sup>                           | 2.0 µs <sup>[1]</sup>                               |
| 0x04            | 12.0 V                                   | 1.25 V  | 2.5 µs  |
| 0x05            | 12.5 V                                   | 1.50 V  | 3.0 µs  |

Table 32. CONFIG1 parameter ranges...continued

| Bit value [2:0] | VCCREG undervoltage threshold UV_TH[2:0] | Overcurrent fault detection threshold OCTH[2:0] | Overcurrent fault detection filter time OCFILT[2:0] |
|-----------------|--|---|---|
| 0x06            | 13.0 V                                   | 1.75 V  | 3.5 µs  |
| 0x07            | 13.5 V                                   | 2.00 V  | 4.0 µs  |

[1] Default value

#### 11.14.4 CONFIG2 register (ADDR = 0x03)

The CONFIG2 register contains selectable ranges for two-level turn-off voltage, short-circuit (voltage) threshold level, and short-circuit filter time. In setting the short-circuit filter time, the G3160 also refers to the SCFF bit in MODE2 for Fast filter mode, decreasing the short-circuit filter time.

Table 33. CONFIG2 register bit readout

|                             | Rb/W | ADDR [4:0] | DATA9     | DATA8     | DATA7     | DATA6     | DATA5    | DATA4    | DATA3    | DATA2      | DATA1      | DATA0      | CRC   |
|-----------------------------|------|------------|-----------|-----------|-----------|-----------|----------|----------|----------|------------|------------|------------|-------|
| Bit #                       | [23] | [22:18]    | [17]      | [16]      | [15]      | [14]      | [13]     | [12]     | [11]     | [10]       | [9]        | [8]        | [7:0] |
| Name/Value                  | 0/1  | 0x03       | 2LTOV [3] | 2LTOV [2] | 2LTOV [1] | 2LTOV [0] | SCTH [2] | SCTH [1] | SCTH [0] | SCFILT [2] | SCFILT [1] | SCFILT [0] | —     |
| Write locked in normal mode | —    | —          | yes       | yes       | yes       | yes       | yes      | yes      | yes      | yes        | yes        | yes        | —     |
| Default                     | —    | —          | 0         | 0         | 1         | 1         | 0        | 1        | 0        | 1          | 0          | 0          | —     |

| Bit value [3:0] | Two-level turn-off (2LTO) voltage level 2LTOV[3:0] | Short-circuit fault detection threshold SCTH[2:0] | Short-circuit fault detection filter time SCFILT[2:0] + SCFF = 0 <sup>[1]</sup> | Short-circuit fault detection filter time SCFILT[2:0] + SCFF = 1 <sup>[1]</sup> |
|-----------------|--|---|---|---|
| 0x00            | 6.48 V   | 0.50 V  | 400 ns  | 100 ns  |
| 0x01            | 6.67 V   | 0.75 V  | 500 ns  | 200 ns  |
| 0x02            | 6.87 V   | 1.00 V <sup>[2]</sup>                             | 600 ns  | 300 ns  |
| 0x03            | 7.08 V <sup>[2]</sup>                              | 1.25 V  | 700 ns  | 400 ns  |
| 0x04            | 7.32 V   | 1.50 V  | 800 ns <sup>[3]</sup>   | 500 ns <sup>[2]</sup>   |
| 0x05            | 7.56 V   | 2.00 V  | 900 ns  | 600 ns  |
| 0x06            | 7.83 V   | 2.50 V  | 1000 ns   | 700 ns  |
| 0x07            | 8.13 V   | 3.00 V  | 1100 ns   | 800 ns  |
| 0x08            | 8.46 V   | —   | —   | —   |
| 0x09            | 8.81 V   | —   | —   | —   |
| 0x0A            | 9.19 V   | —   | —   | —   |
| 0x0B            | 9.62 V   | —   | —   | —   |
| 0x0C            | 10.09 V  | —   | —   | —   |
| 0x0D            | 10.62 V  | —   | —   | —   |
| 0x0E            | 11.21 V  | —   | —   | —   |
| 0x0F            | 11.88 V  | —   | —   | —   |

[1] SCFF is Short-circuit Fast Filter mode bit of [MODE2 register](#)

[2] Default value

[3] Default value upon changing SCFF value bit.

### 11.14.5 CONFIG3 register (ADDR = 0x04)

The CONFIG3 register contains selectable ranges for soft shutdown current, soft shutdown duration time, segmented drive activation delay, and selection of INTB behavior while in Fail-safe mode. The segmented drive activation delay time (SEGDRVLY) is permanently unlocked, and can be changed in real-time without entering CONFIG mode.

Table 34. CONFIG3 register bit readout

|                             | Rb/W | ADDR<br>[4:0] | DATA9  | DATA8       | DATA7       | DATA6       | DATA5      | DATA4      | DATA3      | DATA2   | DATA1   | DATA0   | CRC   |
|-----------------------------|------|---------------|--------|-------------|-------------|-------------|------------|------------|------------|---------|---------|---------|-------|
| Bit #                       | [23] | [22:18]       | [17]   | [16]        | [15]        | [14]        | [13]       | [12]       | [11]       | [10]    | [9]     | [8]     | [7:0] |
| Name/Value                  | 0/1  | 0x04          | INTBFS | SEGDRVLY[2] | SEGDRVLY[1] | SEGDRVLY[0] | SSD_CUR[2] | SSD_CUR[1] | SSD_CUR[0] | SSDT[2] | SSDT[1] | SSDT[0] | —     |
| Write locked in Normal mode | —    | —             | yes    | no          | no          | no          | yes        | yes        | yes        | yes     | yes     | yes     | —     |
| Default                     | —    | —             | 0      | 0           | 0           | 0           | 1          | 0          | 0          | 1       | 0       | 0       | —     |

Table 35. CONFIG3 bit descriptions

| Bit    | Bit function   | Logic 0  | Logic 1  |
|--------|--|--|--|
| INTBFS | Configure the behavior of the INTB pin in Fail-safe mode | The state of FSENB does not affect INTB. INTB does not indicate the G3160 is in Fail-safe mode. <sup>[1]</sup> | INTB indicates the GD3160 is in Fail-safe mode. When FSENB = 0, then INTB = 0. |

[1] Default value

Table 36. CONFIG3 parameter ranges

| Bit value<br>[2:0] | Segmented drive activation delay<br>SEGDRVLY[2:0] | Soft shutdown current<br>SSD_CUR[2:0] | Soft shutdown time duration, no scaling<br>SSDT[2:0] + TIME_2 = 0 <sup>[1]</sup> | Soft shutdown time duration, scaled down<br>SSDT[2:0] + TIME_2 = 1 <sup>[1]</sup> |
|--------------------|---|---------------------------------------|--|---|
| 0x00               | 0 ns <sup>[2]</sup>                               | 0.10 A                                | 2000 ns  | 1000 ns   |
| 0x01               | 20 ns   | 0.20 A                                | 3000 ns  | 1500 ns   |
| 0x02               | 40 ns   | 0.30 A                                | 4000 ns  | 2000 ns   |
| 0x03               | 60 ns   | 0.40 A                                | 5000 ns  | 2500 ns   |
| 0x04               | 80 ns   | 0.50 A <sup>[2]</sup>                 | 6000 ns <sup>[3]</sup>   | 3000 ns <sup>[2]</sup>  |
| 0x05               | 100 ns  | 0.70 A                                | 7000 ns  | 3500 ns   |
| 0x06               | 120 ns  | 0.90 A                                | 8000 ns  | 4000 ns   |
| 0x07               | 140 ns  | 1.00 A                                | 9000 ns  | 4500 ns   |

[1] TIME\_2 is Timer scaling bit of [MODE1 register](#)

[2] Default value

[3] Default value upon changing TIME\_2 bit.

### 11.14.6 CONFIG4 register (ADDR = 0x05)

The CONFIG4 register contains selectable ranges for leading edge blanking, detection filter time, and the charge current associated with a desaturation fault, as well as the segmented drive voltage threshold. The segmented drive threshold value (SEGDRV\_TH) is permanently unlocked, and can be changed in real-time without entering CONFIG mode.

Table 37. CONFIG4 register bit readout

|                                   | Rb/W | ADDR<br>[4:0] | DATA9             | DATA8             | DATA7             | DATA6             | DATA5             | DATA4         | DATA3         | DATA2             | DATA1             | DATA0             | CRC   |
|-----------------------------------|------|---------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------------|---------------|-------------------|-------------------|-------------------|-------|
| Bit #                             | [23] | [22:18]       | [17]              | [16]              | [15]              | [14]              | [13]              | [12]          | [11]          | [10]              | [9]               | [8]               | [7:0] |
| Name/Value                        | 0/1  | 0x05          | DESAT_<br>FLT [1] | DESAT_<br>FLT [0] | SEGDRV_<br>TH [2] | SEGDRV_<br>TH [1] | SEGDRV_<br>TH [0] | IDESAT<br>[1] | IDESAT<br>[0] | DESAT_<br>LEB [2] | DESAT_<br>LEB [1] | DESAT_<br>LEB [0] | —     |
| Write locked<br>in normal<br>mode | —    | —             | yes               | yes               | no                | no                | no                | yes           | yes           | yes               | yes               | yes               | —     |
| Default                           | —    | —             | 0                 | 1                 | 0                 | 1                 | 1                 | 0             | 1             | 0                 | 1                 | 1                 | —     |

Table 38. CONFIG4 parameter ranges

| Bit value [2:0] | Desaturation detection<br>filter time<br>DESAT_FLT[1:0] | Segmented drive<br>voltage threshold<br>SEGDRV_TH[2:0] | Charge current for<br>desaturation detection<br>IDESAT[1:0] | Desaturation detection<br>leading edge blanking time<br>DESAT_LEB[2:0] |
|-----------------|---|--|---|--|
| 0x00            | 70.0 ns   | 3.0 V  | 250 $\mu$ A   | 60 ns  |
| 0x01            | 110.0 ns <sup>[1]</sup>                                 | 4.0 V  | 500 $\mu$ A <sup>[1]</sup>                                  | 120 ns   |
| 0x02            | 190.0 ns  | 5.0 V  | 750 $\mu$ A   | 180 ns   |
| 0x03            | 300.0 ns  | 6.0 V <sup>[1]</sup>                                   | 1000 $\mu$ A  | 240 ns <sup>[1]</sup>  |
| 0x04            | —   | 7.0 V  | —   | 340 ns   |
| 0x05            | —   | 8.0 V  | —   | 460 ns   |
| 0x06            | —   | 9.0 V  | —   | 580 ns   |
| 0x07            | —   | 10.0 V   | —   | 700 ns   |

[1] Default value

### 11.14.7 CONFIG5 register (ADDR = 0x06)

The CONFIG5 register contains selectable ranges for mandatory PWM deadtime, distribution of results on AOUT and die-to-die communication error tracking. The AOUTCONF bit determines the ratio of readings from the power device temperature (TSENSEA) vs. quantity determined by AOUT\_SEL (including AMUXIN, VCC, VCCREG, VEE, and others) as reported over the AOUT pin.

Table 39. CONFIG5 register

|                                   | Rb/W | ADDR<br>[4:0] | DATA9     | DATA8     | DATA7     | DATA6     | DATA5 | DATA4            | DATA3            | DATA2              | DATA1              | DATA0              | CRC   |
|-----------------------------------|------|---------------|-----------|-----------|-----------|-----------|-------|------------------|------------------|--------------------|--------------------|--------------------|-------|
| Bit #                             | [23] | [22:18]       | [17]      | [16]      | [15]      | [14]      | [13]  | [12]             | [11]             | [10]               | [9]                | [8]                | [7:0] |
| Name/Value                        | 0/1  | 0x06          | DEADT [3] | DEADT [2] | DEADT [1] | DEADT [0] | —     | AOUT<br>CONF [1] | AOUT<br>CONF [0] | COMERR<br>CONF [2] | COMERR<br>CONF [1] | COMERR<br>CONF [0] | —     |
| Write locked<br>in normal<br>mode | —    | —             | yes       | yes       | yes       | yes       | —     | yes              | yes              | yes                | yes                | yes                | —     |
| Default                           | —    | —             | 1         | 1         | 1         | 1         | 0     | 0                | 0                | 1                  | 1                  | 0                  | —     |

Table 40. CONFIG5 parameter ranges

| Bit value<br>[3:0] | PWM deadtime<br>DEADT[3:0] + TIME_2 = 0 <sup>[1]</sup> | PWM deadtime<br>DEADT[3:0] + TIME_2 = 1 <sup>[1]</sup> | TSENSEA vs. AOUT_SEL<br>readings ratio at AOUT<br>AOUTCONF[1:0] | Number of errors to set a<br>COMERR fault<br>COMERRCONF[2:1] | Number of valid messages to<br>decrement COMERR counter<br>COMERRCONF[0] |
|--------------------|--|--|---|--|--|
| 0x00               | 0.16 $\mu$ s   | 0.10 $\mu$ s   | 1/1 <sup>[2]</sup>  | 4  | 1 <sup>[2]</sup>   |
| 0x01               | 0.24 $\mu$ s   | 0.14 $\mu$ s   | 1/2   | 8  | 4  |
| 0x02               | 0.44 $\mu$ s   | 0.24 $\mu$ s   | 1/4   | 16   | —  |
| 0x03               | 0.76 $\mu$ s   | 0.40 $\mu$ s   | 1/8   | 32 <sup>[2]</sup>  | —  |
| 0x04               | 1.04 $\mu$ s   | 0.54 $\mu$ s   | —   | —  | —  |
| 0x05               | 1.52 $\mu$ s   | 0.78 $\mu$ s   | —   | —  | —  |
| 0x06               | 2.04 $\mu$ s   | 1.04 $\mu$ s   | —   | —  | —  |
| 0x07               | 2.52 $\mu$ s   | 1.28 $\mu$ s   | —   | —  | —  |

Table 40. CONFIG5 parameter ranges...continued

| Bit value [3:0] | PWM deadtime<br>DEADT[3:0] + TIME_2 = 0 <sup>[1]</sup> | PWM deadtime<br>DEADT[3:0] + TIME_2 = 1 <sup>[1]</sup> | TSENSEA vs. AOUT_SEL<br>readings ratio at AOUT<br>AOUTCONF[1:0] | Number of errors to set a<br>COMERR fault<br>COMERRCONF[2:1] | Number of valid messages to<br>decrement COMERR counter<br>COMERRCONF[0] |
|-----------------|--|--|---|--|--|
| 0x08            | 3.04 µs  | 1.54 µs  | —   | —  | —  |
| 0x09            | 3.52 µs  | 1.78 µs  | —   | —  | —  |
| 0x0A            | 4.04 µs  | 2.04 µs  | —   | —  | —  |
| 0x0B            | 4.52 µs  | 2.28 µs  | —   | —  | —  |
| 0x0C            | 5.04 µs  | 2.54 µs  | —   | —  | —  |
| 0x0D            | 5.52 µs  | 2.78 µs  | —   | —  | —  |
| 0x0E            | 6.04 µs  | 3.04 µs  | —   | —  | —  |
| 0x0F            | 6.52 µs <sup>[3]</sup>                                 | 3.28 µs <sup>[2]</sup>                                 | —   | —  | —  |

[1] TIME\_2 is Timer scaling bit of [MODE1 register](#)

[2] Default value

[3] Default value upon changing TIME\_2 bit

### 11.14.8 CONFIG6 register (ADDR = 0x07)

The CONFIG6 register contains selectable ranges for the gate supply (VCCREG[2:0]), the LV/HV domain watchdog timeout (WDTO[1:0]), and the PWM/real-time feedback coherency check delay (RTMONDLY[3:0]).

The VCCREG setpoint is permanently unlocked. It can be changed in real-time without entering CONFIG mode.

Table 41. CONFIG6 register bit readout

|                                   | Rb/W | ADDR<br>[4:0] | DATA9         | DATA8         | DATA7         | DATA6 | DATA5    | DATA4    | DATA3           | DATA2           | DATA1           | DATA0           | CRC   |
|-----------------------------------|------|---------------|---------------|---------------|---------------|-------|----------|----------|-----------------|-----------------|-----------------|-----------------|-------|
| Bit #                             | [23] | [22:18]       | [17]          | [16]          | [15]          | [14]  | [13]     | [12]     | [11]            | [10]            | [9]             | [8]             | [7:0] |
| Name/Value                        | 0/1  | 0x07          | VCCREG<br>[2] | VCCREG<br>[1] | VCCREG<br>[0] | —     | WDTO [1] | WDTO [0] | RTM<br>ONLY [3] | RTM<br>ONLY [2] | RTM<br>ONLY [1] | RTM<br>ONLY [0] | —     |
| Write locked<br>in normal<br>mode | —    | —             | no            | no            | no            | —     | yes      | yes      | yes             | yes             | yes             | yes             | —     |
| Default                           | —    | —             | 0             | 0             | 1             | 0     | 1        | 1        | 1               | 0               | 1               | 0               | —     |

Table 42. CONFIG6 parameter ranges

| Bit value [3:0] | Positive gate supply regulation<br>setpoint<br>VCCREG[2:0] | Die-to-die communications watchdog<br>timeout<br>WDTO[1:0] | PWM vs. real-time monitor<br>delay<br>RTMONDLY[3:0] + TIME_2 =<br>0 <sup>[1]</sup> | PWM vs. Real-time monitor<br>delay<br>RTMONDLY[3:0] + TIME_2 =<br>1 <sup>[1]</sup> |
|-----------------|--|--|--|--|
| 0x00            | 14.0 V   | 260 µs   | — <sup>[2]</sup>   | — <sup>[2]</sup>   |
| 0x01            | 15.0 V <sup>[3]</sup>                                      | 500 µs   | 400 ns   | — <sup>[2]</sup>   |
| 0x02            | 16.0 V   | 1000 µs  | 800 ns   | 400 ns   |
| 0x03            | 17.0 V   | 2000 µs <sup>[3]</sup>                                     | 1200 ns  | 600 ns   |
| 0x04            | 18.0 V   | —  | 1600 ns  | 800 ns   |
| 0x05            | 19.0 V   | —  | 2000 ns  | 1000 ns  |
| 0x06            | 20.0 V   | —  | 2400 ns  | 1200 ns  |
| 0x07            | 21.0 V   | —  | 2800 ns  | 1400 ns  |
| 0x08            | —  | —  | 3200 ns  | 1600 ns  |
| 0x09            | —  | —  | 3600 ns  | 1800 ns  |
| 0x0A            | —  | —  | 4000 ns <sup>[4]</sup>   | 2000 ns <sup>[3]</sup>   |
| 0x0B            | —  | —  | 4800 ns  | 2400 ns  |
| 0x0C            | —  | —  | 5600 ns  | 2800 ns  |
| 0x0D            | —  | —  | 6400 ns  | 3200 ns  |
| 0x0E            | —  | —  | 7200 ns  | 3600 ns  |

Table 42. CONFIG6 parameter ranges...continued

| Bit value [3:0] | Positive gate supply regulation setpoint VCCREG[2:0] | Die-to-die communications watchdog timeout WDTO[1:0] | PWM vs. real-time monitor delay RTMONDLY[3:0] + TIME_2 = 0 <sup>[1]</sup> | PWM vs. Real-time monitor delay RTMONDLY[3:0] + TIME_2 = 1 <sup>[1]</sup> |
|-----------------|--|--|---|---|
| 0x0F            | —  | —  | 8000 ns   | 4000 ns   |

[1] TIME\_2\_is timer scaling bit of [MODE1 register](#)  
[2] Not used  
[3] Default value  
[4] Default value upon changing TIME\_2 bit

11.14.9 CONFIG7 register (ADDR = 0x08)

The CONFIG7 register contains the selectable range for desaturation threshold voltage.

Table 43. CONFIG7 register bit readout

|                             | Rb/W | ADDR [4:0] | DATA9 | DATA8 | DATA7 | DATA6 | DATA5 | DATA4 | DATA3        | DATA2        | DATA1        | DATA0        | CRC   |
|-----------------------------|------|------------|-------|-------|-------|-------|-------|-------|--------------|--------------|--------------|--------------|-------|
| Bit #                       | [23] | [22:18]    | [17]  | [16]  | [15]  | [14]  | [13]  | [12]  | [11]         | [10]         | [9]          | [8]          | [7:0] |
| Name/Value                  | 0/1  | 0x08       | —     | —     | —     | —     | —     | —     | DESAT_TH [3] | DESAT_TH [2] | DESAT_TH [1] | DESAT_TH [0] | —     |
| Write locked in normal mode | —    | —          | —     | —     | —     | —     | —     | —     | yes          | yes          | yes          | yes          | —     |
| Default                     | —    | —          | 0     | 0     | 0     | 0     | 0     | 0     | 1            | 0            | 1            | 0            | —     |

Table 44. CONFIG7 parameter ranges

| Bit value [3:0] | Desaturation fault threshold-voltage level DESAT_TH[3:0] |
|-----------------|--|
| 0x00            | 1.00 V   |
| 0x01            | 1.50 V   |
| 0x02            | 2.00 V   |
| 0x03            | 2.50 V   |
| 0x04            | 3.00 V   |
| 0x05            | 3.50 V   |
| 0x06            | 4.00 V   |
| 0x07            | 4.50 V   |
| 0x08            | 5.00 V   |
| 0x09            | 5.50 V   |
| 0x0A            | 6.00 V <sup>[1]</sup>                                    |
| 0x0B            | 6.50 V   |
| 0x0C            | 7.00 V   |
| 0x0D            | 8.00 V   |
| 0x0E            | 9.00 V   |
| 0x0F            | 10.00 V  |

[1] Default value

#### 11.14.10 OT\_TH register (ADDR = 0x09)

The OT\_TH register sets the threshold level for a power device overtemperature event. The post-converted TSENSEA result is automatically compared to this threshold to evaluate for an overtemperature fault. The OT\_TH register is permanently unlocked; CONFIG mode is not required to modify the OT\_TH register values. These values may be changed on-the-fly and may be changed according to system or application demands.

Table 45. OT\_TH register bit readout

|                                   | Rb/W | ADDR<br>[4:0] | DATA9        | DATA8        | DATA7        | DATA6        | DATA5        | DATA4        | DATA3        | DATA2        | DATA1        | DATA0        | CRC   |
|-----------------------------------|------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-------|
| Bit #                             | [23] | [22:18]       | [17]         | [16]         | [15]         | [14]         | [13]         | [12]         | [11]         | [10]         | [9]          | [8]          | [7:0] |
| Name/Value                        | 0/1  | 0x09          | OT_TH<br>[9] | OT_TH<br>[8] | OT_TH<br>[7] | OT_TH<br>[6] | OT_TH<br>[5] | OT_TH<br>[4] | OT_TH<br>[3] | OT_TH<br>[2] | OT_TH<br>[1] | OT_TH<br>[0] | —     |
| Write locked<br>in normal<br>mode | —    | —             | no           | no           | no           | no           | no           | no           | no           | no           | no           | no           | —     |
| Default                           | —    | —             | 0            | 0            | 1            | 1            | 1            | 1            | 1            | 1            | 1            | 1            | —     |

The characteristic for the overtemperature shutdown threshold, given as a voltage at the TSENSEA pin, is given in [Equation 4](#).

$$V_{OT\_TH} = OT\_TH[9:0] \times \frac{5.0V}{1023} \quad (4)$$

#### 11.14.11 OTW\_TH register (ADDR = 0x0A)

The OTW\_TH register sets the threshold level for a power device overtemperature warning event. The post-converted TSENSEA result is automatically compared to this threshold to evaluate for an overtemperature warning condition. The OTW\_TH register is permanently unlocked; CONFIG mode is not required to modify the OTW\_TH register values. These values may be changed on-the-fly and may be changed according to system or application demands.

Table 46. OTW\_TH (IGBT overtemperature warning threshold register)

|                                   | Rb/W | ADDR<br>[4:0] | DATA9         | DATA8         | DATA7         | DATA6         | DATA5         | DATA4         | DATA3         | DATA2         | DATA1         | DATA0         | CRC   |
|-----------------------------------|------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|-------|
| Bit #                             | [23] | [22:18]       | [17]          | [16]          | [15]          | [14]          | [13]          | [12]          | [11]          | [10]          | [9]           | [8]           | [7:0] |
| Name/Value                        | 0/1  | 0x0A          | OTW_TH<br>[9] | OTW_TH<br>[8] | OTW_TH<br>[7] | OTW_TH<br>[6] | OTW_TH<br>[5] | OTW_TH<br>[4] | OTW_TH<br>[3] | OTW_TH<br>[2] | OTW_TH<br>[1] | OTW_TH<br>[0] | —     |
| Write locked<br>in normal<br>mode | —    | —             | no            | no            | no            | no            | no            | no            | no            | no            | no            | no            | —     |
| Default                           | —    | —             | 1             | 1             | 1             | 1             | 1             | 1             | 1             | 1             | 1             | 1             | —     |

The characteristic for the overtemperature warning shutdown threshold, given as a voltage at the TSENSEA pin, is given in [Equation 5](#).

$$V_{OTW\_TH} = OTW\_TH[9:0] \times \frac{5.0V}{1023} \quad (5)$$

#### 11.14.12 STATUS1 register (ADDR = 0x0B)

The STATUS1 register details fault status. Fault bits are cleared on power up, and if not masked, upon a fault the corresponding fault bit is set to '1' and latched. Write '1' operations to the STATUS1 register are used to clear latched faults (the GD3160 does not need to be in CONFIG mode to do this) and return the device to normal functionality.

Table 47. STATUS1 register bit readout

|            | Rb/W | ADDR [4:0] | DATA9 | DATA8    | DATA7  | DATA6   | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 | CRC   |
|------------|------|------------|-------|----------|--------|---------|-------|-------|-------|-------|-------|-------|-------|
| Bit #      | [23] | [22:18]    | [17]  | [16]     | [15]   | [14]    | [13]  | [12]  | [11]  | [10]  | [9]   | [8]   | [7:0] |
| Name/Value | 0/1  | 0x0B       | VCCOV | VCCREGUV | VSUPOV | OTSD_IC | OTSD  | OTW   | CLAMP | DESAT | SC    | OC    | —     |
| Default    | —    | —          | 0     | 0        | 0      | 0       | 0     | 0     | 0     | 0     | 0     | 0     | —     |

Table 48. STATUS1 register description

| Bit                     | Logic 1 indicates:                                 | Fault latched | PWMing disabled                 | IGBT turn off method            |
|-------------------------|--|---------------|---------------------------------|---------------------------------|
| VCCOV                   | VCC overvoltage                                    | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal                          |
| VCCREGUV <sup>[1]</sup> | VCCREG undervoltage                                | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal                          |
| VSUPOV                  | VSUP overvoltage                                   | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal                          |
| OTSD_IC                 | Overtemperature shutdown of LV domain or HV domain | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal                          |
| OTSD                    | Overtemperature shutdown of IGBT                   | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal                          |
| OTW                     | Overtemperature warning of IGBT                    | Yes           | No                              | Not turned off                  |
| CLAMP <sup>[2]</sup>    | V <sub>CE</sub> clamp event                        | Yes           | Yes, GL = 1, AMC = 1 if enabled | ISSD defaults to lowest setting |
| DESAT                   | V <sub>CE</sub> desaturation event                 | Yes           | Yes, GL = 1, AMC = 1 if enabled | SSD, 2LTO if enabled            |
| SC                      | IGBT short-circuit                                 | Yes           | Yes, GL = 1, AMC = 1 if enabled | SSD, 2LTO if enabled            |
| OC                      | IGBT overcurrent                                   | Yes           | No                              | SSD, if enabled                 |

[1] At power up, a VCCREGUV fault should not be latched or reported. The UV\_LATCH bit allows PWMing if the VCCREG supply recovers from an UV condition. INTB follows fault condition.

[2] During V<sub>CE</sub> clamp activation, ISSD is activated regardless of the SSD mode bit.

### 11.14.13 MSK1 register (ADDR = 0x0C)

The MSK1 register determines bit-for-bit the faults to be reported to INTB or INTA from the STATUS1 register. The GD3160 must be in CONFIG mode for the mask settings to be changed. A value of 0 for the fault mask bit means that the corresponding fault is masked, a value of 1 means that the corresponding fault is unmasked. Response when masked or unmasked for each fault is described in [Table 69](#). Not all faults may be masked (such as SC and DESAT).

Table 49. MSK1 register bit readout

|                             | Rb/W | ADDR [4:0] | DATA9  | DATA8     | DATA7   | DATA6 | DATA5 | DATA4 | DATA3  | DATA2 | DATA1 | DATA0 | CRC   |
|-----------------------------|------|------------|--------|-----------|---------|-------|-------|-------|--------|-------|-------|-------|-------|
| Bit #                       | [23] | [22:18]    | [17]   | [16]      | [15]    | [14]  | [13]  | [12]  | [11]   | [10]  | [9]   | [8]   | [7:0] |
| Name/Value                  | 0/1  | 0x0C       | VCCOVM | VCCREGUVM | VSUPOVM | —     | OTSDM | OTWM  | CLAMPM | —     | —     | OCM   | —     |
| Write locked in normal mode | —    | —          | yes    | yes       | yes     | —     | yes   | yes   | yes    | —     | —     | yes   | —     |
| Default                     | —    | —          | 1      | 1         | 0       | 0     | 0     | 0     | 1      | 0     | 0     | 1     | —     |

Table 50. MSK1 register description

| Bit                      | Logic 0 = masked  | Logic 1 = not masked                      |
|--------------------------|---|---|
| VCCOVM                   | PWMing remains enabled, fault not latched or reported.              | PWM disabled. GL = 1, AMC = 1 if enabled. |
| VCCREGUVM <sup>[1]</sup> | PWMing remains enabled until VCC falls below VCC <sub>UV_TH</sub> . | PWM disabled. GL = 1, AMC = 1 if enabled. |

Table 50. MSK1 register description...continued

| Bit     | Logic 0 = masked  | Logic 1 = not masked                      |
|---------|---|---|
| VSUPOVM | PWMing remains enabled, fault not latched or reported.  | PWM disabled. GL = 1, AMC = 1 if enabled. |
| OTSDM   | PWMing remains enabled, OTSD fault not latched or reported. Temp reported in ADCVAL and AOUT. | PWM disabled. GL = 1, AMC = 1 if enabled. |
| OTWM    | PWMing remains enabled, OTW fault not latched or reported. Temp reported in ADCVAL.           | PWM enabled.                              |
| CLAMPM  | PWMing remains enabled, fault not latched or reported.  | PWM disabled. GL = 1, AMC = 1 if enabled. |
| OCM     | No mask.  | PWM enabled.                              |

[1] At power up, a VCCREGUV fault should not be latched or reported. The UV\_LATCH bit (in CONFIG1) allows PWMing if the VCCREG supply recovers from an UV condition. INTB follows fault condition. SPI bit is latched.

#### 11.14.14 RMSK1 register (ADDR = 0x0D)

The RMSK1 register values determine which interrupt pin (either INTB or INTA) an unmasked fault is to be reported. A value of '0' reports the fault to INTB, and a value of '1' reports the fault to INTA. Recall that for INTA to be configured as a fault pin, the RTRPT bit must be set accordingly in the MODE2 register.

Table 51. RMSK1 register bit readout

|                             | Rb/<br>W | ADDR<br>[4:0] | DATA9  | DATA8     | DATA7   | DATA6    | DATA5 | DATA4 | DATA3  | DATA2  | DATA1 | DATA0 | CRC   |
|-----------------------------|----------|---------------|--------|-----------|---------|----------|-------|-------|--------|--------|-------|-------|-------|
| Bit #                       | [23]     | [22:18]       | [17]   | [16]      | [15]    | [14]     | [13]  | [12]  | [11]   | [10]   | [9]   | [8]   | [7:0] |
| Name/Value                  | 0/1      | 0x0D          | VCCOVA | VCCREGUVA | VSUPOVA | OTSD_ICA | OTSDA | OTWA  | CLAMPA | DESATA | SCA   | OCA   | —     |
| Write locked in normal mode | —        | —             | yes    | yes       | yes     | yes      | yes   | yes   | yes    | yes    | yes   | yes   | —     |
| Default                     | —        | —             | 0      | 0         | 0       | 0        | 1     | 0     | 0      | 1      | 1     | 0     | —     |

| Bit       | Bit function                                | Logic 0                             | Logic 1                             |
|-----------|---|-------------------------------------|-------------------------------------|
| VCCOVA    | Select INTx pin to report VCCOV fault to    | Report fault on INTB <sup>[1]</sup> | Report fault on INTA                |
| VCCREGUVA | Select INTx pin to report VCCREGUV fault to | Report fault on INTB <sup>[1]</sup> | Report fault on INTA                |
| VSUPOVA   | Select INTx pin to report VSUPOV fault to   | Report fault on INTB <sup>[1]</sup> | Report fault on INTA                |
| OTSD_ICA  | Select INTx pin to report OTSD_IC fault to  | Report fault on INTB <sup>[1]</sup> | Report fault on INTA                |
| OTSDA     | Select INTx pin to report OTSD fault to     | Report fault on INTB                | Report fault on INTA <sup>[1]</sup> |
| OTWA      | Select INTx pin to report OTW fault to      | Report fault on INTB <sup>[1]</sup> | Report fault on INTA                |
| CLAMPA    | Select INTx pin to report CLAMP fault to    | Report fault on INTB <sup>[1]</sup> | Report fault on INTA                |
| DESATA    | Select INTx pin to report DESAT fault to    | Report fault on INTB                | Report fault on INTA <sup>[1]</sup> |
| SCA       | Select INTx pin to report SC fault to       | Report fault on INTB                | Report fault on INTA <sup>[1]</sup> |
| OCA       | Select INTx pin to report OC fault to       | Report fault on INTB <sup>[1]</sup> | Report fault on INTA                |

[1] Default value

#### 11.14.15 STATUS2 register (ADDR = 0x0E)

The STATUS2 register details fault status. Fault bits are cleared on power up, and if not masked, upon a fault the corresponding fault bit is set to '1' and latched. Write '1' operations to the STATUS2 register are used to clear latched faults and return the device to normal functionality.

Table 52. STATUS2 register bit readout

|            | Rb/W | ADDR<br>[4:0] | DATA9     | DATA8    | DATA7 | DATA6  | DATA5      | DATA4     | DATA3    | DATA2  | DATA1   | DATA0   | CRC   |
|------------|------|---------------|-----------|----------|-------|--------|------------|-----------|----------|--------|---------|---------|-------|
| Bit #      | [23] | [22:18]       | [17]      | [16]     | [15]  | [14]   | [13]       | [12]      | [11]     | [10]   | [9]     | [8]     | [7:0] |
| Name/Value | 0/1  | 0x0e          | BIST_FAIL | VDD_UVOV | DTFLT | SPIERR | CONFRCRERR | RTMON_FLT | WDOG_FLT | COMERR | VREF_UV | VEE_OOR | —     |
| Default    | —    | —             | 0         | 0        | 0     | 0      | 0          | 0         | 0        | 0      | 0       | 0       | —     |

Table 53. STATUS2 register description

| Bit                      | Logic 1 indicates:   | Fault latched | PWMing disabled                 | IGBT turn OFF method |
|--------------------------|--|---------------|---------------------------------|----------------------|
| BIST_FAIL <sup>[1]</sup> | BIST failure.  | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal               |
| VDD_UVOV <sup>[2]</sup>  | VDD out of range.  | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal               |
| DTFLT                    | PWM deadtime violation.  | Yes           | No                              | —                    |
| SPIERR                   | SPI framing or CRC error.  | Yes           | No                              | —                    |
| CONFRCRERR               | LV domain or HV domain detected a CRC change in its CONFIG registers.                                  | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal               |
| RTMON_FLT                | Only valid if RTMON_CFG=0. LV domain detected that VGE(RTMON_CFG = 0) is not tracking commanded state. | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal               |
| WDOG_FLT                 | LV domain or HV domain detects a loss of LV/HV domain communication.                                   | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal               |
| COMERR                   | LV/HV domain communications CRC error or framing error.  | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal               |
| VREF_UV <sup>[3]</sup>   | VREF out of range.   | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal               |
| VEE_OOR                  | VEE out of range.  | Yes           | Yes, GL = 1, AMC = 1 if enabled | Normal               |

[1] BIST\_FAIL bit provides pass/fail results. Detailed BIST results are placed in the REQBIST register. REQBIST bits persist until a new BIST is conducted.

[2] VDD\_UVOV fault bit is not set at power up. If VDD is shorted at power up, a VDD\_UVOV fault is not reported and the MCU infers a VDD fault from other behaviors.

[3] VREF fault bit is not set at power up. If VREF is shorted at power up, a VREF fault is not reported and the MCU infers a VREF fault from other behaviors.

### 11.14.16 MSK2 register (ADDR = 0x0F)

The MSK2 register determines bit-for-bit the faults to be reported to INTB or INTA from the STATUS2 register. The GD3160 must be in CONFIG mode for the mask settings to be changed. Not all faults may be masked (such as BIST\_FAIL and VDD\_UVOV).

Table 54. MSK2 register bit readout

|                             | Rb/W | ADDR<br>[4:0] | DATA9 | DATA8 | DATA7  | DATA6   | DATA5       | DATA4      | DATA3     | DATA2   | DATA1 | DATA0    | CRC   |
|-----------------------------|------|---------------|-------|-------|--------|---------|-------------|------------|-----------|---------|-------|----------|-------|
| Bit #                       | [23] | [22:18]       | [17]  | [16]  | [15]   | [14]    | [13]        | [12]       | [11]      | [10]    | [9]   | [8]      | [7:0] |
| Name/Value                  | 0/1  | 0x0F          | —     | —     | DTFLTM | SPIERRM | CONFRCRERRM | RTMON_FLTM | WDOG_FLTM | COMERRM | —     | VEE_OORM | —     |
| Write locked in normal mode | —    | —             | —     | —     | yes    | yes     | yes         | yes        | yes       | yes     | —     | yes      | —     |
| Default                     | —    | —             | 0     | 0     | 1      | 1       | 1           | 0          | 1         | 1       | 0     | 0        | —     |

Table 55. MSK2 register description

| Bit    | Bit function         | Logic 0   | Logic 1      |
|--------|----------------------|---|--------------|
| DTFLTM | Deadtime fault mask. | PWMing remains enabled, fault not latched or reported, programmed PWM deadtime is enforced. | PWM enabled. |

Table 55. MSK2 register description...continued

| Bit                      | Bit function                                  | Logic 0   | Logic 1                                   |
|--------------------------|---|---|---|
| SPIERRM                  | SPI CRC or framing error fault mask.          | PWMing remains enabled, fault not latched or reported.                            | PWM enabled.                              |
| CONFRCRERM               | LV or HV domain CONF register CRC error mask. | PWMing remains enabled, fault not latched or reported.                            | PWM disabled. GL = 1, AMC = 1 if enabled. |
| RTMON_FLTM               | RTMON error mask.                             | PWMing remains enabled, fault not latched or reported.                            | PWM disabled. GL = 1, AMC = 1 if enabled. |
| WDOG_FLTM <sup>[1]</sup> | Watchdog fault mask.                          | PWMing remains enabled, fault not latched or reported, periodic REQADC continues. | PWM disabled. GL = 1, AMC = 1 if enabled. |
| COMERRM                  | Internal communications fault mask.           | PWMing remains enabled, fault not latched or reported.                            | PWM disabled. GL = 1, AMC = 1 if enabled. |
| VEE_OORM                 | VEE out of range fault mask.                  | PWMing remains enabled, fault not latched or reported.                            | PWM disabled. GL = 1, AMC = 1 if enabled. |

[1] WDOG\_FLT indicates LV domain received NO message in response to one of the periodic LV domain DATA messages. This bit should be used only for debug purposes. This bit defaults to "unmasked" at power up.

11.14.17 RMSK2 register (ADDR = 0x10)

The RMSK2 register values determine which interrupt pin (either INTB or INTA) an unmasked fault is to be reported. Not all STATUS2 faults can be reported at INTA (such as BIST\_FAIL, VDD\_UVOV, and so on.). A value of '0' reports the fault to INTB, and a value of '1' reports the fault to INTA. Recall that for INTA to be configured as a fault pin, the RTRPT bit must be set accordingly in the MODE2 register.

Table 56. RMSK2 register bit readout

|                             | Rb/W | ADDR<br>[4:0] | DATA9 | DATA8 | DATA7  | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1    | DATA0    | CRC   |
|-----------------------------|------|---------------|-------|-------|--------|-------|-------|-------|-------|-------|----------|----------|-------|
| Bit #                       | [23] | [22:18]       | [17]  | [16]  | [15]   | [14]  | [13]  | [12]  | [11]  | [10]  | [9]      | [8]      | [7:0] |
| Name/Value                  | 0/1  | 0x10          | —     | —     | DTFLTA | —     | —     | —     | —     | —     | VREF_UVA | VEE_OORA | —     |
| Write locked in normal mode | —    | —             | —     | —     | yes    | —     | —     | —     | —     | —     | yes      | yes      | —     |
| Default                     | —    | —             | 0     | 0     | 0      | 0     | 0     | 0     | 0     | 0     | 1        | 0        | —     |

| Bit      | Bit function                               | Logic 0                             | Logic 1                             |
|----------|--|-------------------------------------|-------------------------------------|
| DTFLTA   | Select INTx pin to report DTFLT fault to   | Report fault on INTB <sup>[1]</sup> | Report fault on INTA                |
| VREF_UVA | Select INTx pin to report VREF_UV fault to | Report fault on INTB                | Report fault on INTA <sup>[1]</sup> |
| VEE_OORA | Select INTx pin to report VEE_OOR fault to | Report fault on INTB <sup>[1]</sup> | Report fault on INTA                |

[1] Default value

#### 11.14.18 STATUS3 register (ADDR = 0x11)

The STATUS3 pin reports critical GD3160 control and status pin states, after deglitch. The MCU can monitor pin state bits (i.e. PWM, PWMALT, FSSTATE, FSENB) to check circuit integrity. A change in the deglitched logic pin state is reflected in the corresponding bit within 1  $\mu$ s. The POR recovery bits (POR\_1, POR\_2) will only read '1' following a POR event or after BIST operation; they will read '0' following a software reset command or after writing a '1' to these bits. If INTA is configured to report faults, the INTA and VRTMON may report different values.

Table 57. STATUS3 register

|            | Rb/W | ADDR<br>[4:0] | DATA9 | DATA8 | DATA7 | DATA6 | DATA5  | DATA4   | DATA3 | DATA2 | DATA1 | DATA0  | CRC   |
|------------|------|---------------|-------|-------|-------|-------|--------|---------|-------|-------|-------|--------|-------|
| Bit #      | [23] | [22:18]       | [17]  | [16]  | [15]  | [14]  | [13]   | [12]    | [11]  | [10]  | [9]   | [8]    | [7:0] |
| Name/Value | 0/1  | 0x11          | POR_1 | POR_2 | FSISO | PWM   | PWMALT | FSSTATE | FSENB | INTB  | INTA  | VRTMON | —     |
| Default    | —    | —             | 1     | 1     | —     | —     | —      | —       | —     | —     | —     | —      | —     |

Table 58. STATUS3 register description

| Bit     | Bit function   | Logic 0   | Logic 1   |
|---------|--|---|---|
| POR_1   | Report LV die recovery from POR  | LV die POR recovery bit has been cleared  | Notification of LV die recovery from POR                                      |
| POR_2   | Report HV die recovery from POR  | HV die POR recovery bit has been cleared  | Notification of HV die recovery from POR                                      |
| FSISO   | Report FSISO pin state   | FSISO pin is logic low  | FSISO pin is logic high   |
| PWM     | Report PWM pin state   | PWM pin is logic low  | PWM pin is logic high   |
| PWMALT  | Report PWMALT pin state  | PWMALT pin is logic low   | PWMALT pin is logic high  |
| FSSTATE | Report FSSTATE pin state   | FSSTATE pin is logic low  | FSSTATE pin is logic high   |
| FSENB   | Report FSENB pin state   | FSENB pin is logic low  | FSENB pin is logic high   |
| INTB    | Report INTB pin state  | INTB pin is logic low   | INTB pin is logic high  |
| INTA    | Report INTA pin state  | INTA pin is logic low   | INTA pin is logic high  |
| VRTMON  | Report the state of the quantity under real-time monitoring/reporting (VGE) or reporting (VCE): <ul style="list-style-type: none"> <li>When RTMON_CFG = 0: VGE</li> <li>When RTMON_CFG = 1: VCE</li> </ul> <sup>[1]</sup> <sup>[2]</sup> | VGE: VGE is low (power device is OFF)<br>VCE: VCE is high (power device is OFF) | VGE: VGE is high (power device is ON)<br>VCE: VCE is low (power device is ON) |

[1] By default, VRTMON reports the VGE state. This is due to the default RTMON\_CFG = 0 in the MODE2 register.

[2] The RTMON\_CFG bit in MODE2 determines the quantity to report to the VTRMON. This must be changed during CONFIG mode.

### 11.14.19 CONFIGAOUT register (ADDR = 0x12)

The CONFIGAOUT register determines the second quantity reported on AOUT, the magnitude of temperature-sense current, and sets the ADC offset and range for the AMUXIN and TSENSEA inputs. The CONFIGAOUT register is permanently unlocked; CONFIG mode is not required to modify the CONFIGAOUT register values. These values are configurable on-the-fly and may be changed according to system or application demands.

**Table 59. CONFIGAOUT register bit readout**

|                                | Rb/W | ADDR<br>[4:0] | DATA9    | DATA8    | DATA7    | DATA6    | DATA5 | DATA4     | DATA3       | DATA2       | DATA1            | DATA0            | CRC   |
|--------------------------------|------|---------------|----------|----------|----------|----------|-------|-----------|-------------|-------------|------------------|------------------|-------|
| Bit #                          | [23] | [22:18]       | [17]     | [16]     | [15]     | [14]     | [13]  | [12]      | [11]        | [10]        | [9]              | [8]              | [7:0] |
| Name/Value                     | 0/1  | 0x12          | ITSNS[1] | ITSNS[0] | TOFST[1] | TOFST[0] | TRNG  | AMUXINRNG | AMUXINOS[1] | AMUXINOS[0] | AOUT_<br>SEL [1] | AOUT_<br>SEL [0] | —     |
| Write locked in<br>normal mode | —    | —             | no       | no       | no       | no       | no    | no        | no          | no          | no               | no               | —     |
| Default                        | —    | —             | 1        | 1        | 0        | 0        | 0     | 0         | 0           | 0           | 0                | 0                | —     |

**Table 60. CONFIGAOUT bit description**

| Bits          | Bit function   |
|---------------|--|
| ITSNS[1:0]    | TSENSEA current source magnitude. See <a href="#">Table 61</a> for values.   |
| TOFST[1:0]    | TSENSEA offset selection. See <a href="#">Table 61</a> for values.   |
| TRNG          | Select the full-scale range for TSENSEA ADC: <ul style="list-style-type: none"> <li>TRNG = 0: full-scale range = 5 V [1]</li> <li>TRNG = 1: full-scale range = 1 V</li> </ul>          |
| AMUXRNG       | Select the full-scale range for the AMUXIN ADC: <ul style="list-style-type: none"> <li>AMUXRNG = 0: full-scale range = 5 V [1]</li> <li>AMUXRNG = 1: full-scale range = 1 V</li> </ul> |
| AMUXINOS[1:0] | AMUXIN offset selection. See <a href="#">Table 61</a> for values.  |
| AOUT_SEL[1:0] | Select the 2nd quantity reported to the AOUT pin. See <a href="#">Table 61</a> for selections.   |

[1] Default value

Table 61. CONFIGAOUT parametric ranges

| Bit value [1:0] | ITSNS[1:0]             | TOFST[1:0]           | AMUXINOS[1]          | AOUT_SEL[1:0] |
|-----------------|------------------------|----------------------|----------------------|---------------|
| 0x00            | 0.25 mA                | 0.0 V <sup>[1]</sup> | 0.0 V <sup>[1]</sup> | VCCREG        |
| 0x01            | 0.50 mA                | 0.5 V                | 0.5 V                | AMUXIN        |
| 0x02            | 0.75 mA                | 1.0 V                | 1.0 V                | VCC           |
| 0x03            | 1.00 mA <sup>[1]</sup> | 1.5 V                | 1.5 V                | VEE           |

[1] Default value

#### 11.14.20 ADC request and response (ADDR = 0x13)

The REQADC command will convert the requested quantity and respond with the result over SPI. The REQADC request is delivered as a "read" command (leading MSB = 0), with the four LSBs indicating the quantity to be read, given in [Table 63](#). A REQADC command/request delivered as a write (leading MSB = 1) is an invalid command and ignored. The REQADC response includes the identical address as the command (ADDR[4:0] = 0x13) followed by the 10-bit data.

Table 62. REQADC request and response bit readout

|                      | Rb/W | ADDR<br>[4:0] | DATA9         | DATA8         | DATA7         | DATA6         | DATA5         | DATA4         | DATA3            | DATA2            | DATA1            | DATA0            | CRC   |
|----------------------|------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|------------------|------------------|------------------|------------------|-------|
| Bit #                | [23] | [22:18]       | [17]          | [16]          | [15]          | [14]          | [13]          | [12]          | [11]             | [10]             | [9]              | [8]              | [7:0] |
| REQADC<br>(request)  | 0    | 0x13          | —             | —             | —             | —             | —             | —             | AMUX_<br>SEL [3] | AMUX_<br>SEL [2] | AMUX_<br>SEL [1] | AMUX_<br>SEL [0] | —     |
| REQADC<br>(response) | 0    | 0x13          | ADCVAL<br>[9] | ADCVAL<br>[8] | ADCVAL<br>[7] | ADCVAL<br>[6] | ADCVAL<br>[5] | ADCVAL<br>[4] | ADCVAL<br>[3]    | ADCVAL<br>[2]    | ADCVAL<br>[1]    | ADCVAL<br>[0]    | —     |

Table 63. REQADC request selections

| AMUX_SEL[3:0] | AMUX selection reported in REQADC response | Other relevant settings  |
|---------------|--|--|
| 0x00          | VCCREG                                     | —  |
| 0x01          | AMUXIN                                     | <ul style="list-style-type: none"> <li>AMUXINOS[1:0]</li> <li>AMUXINRNG</li> </ul>             |
| 0x02          | VCC  | —  |
| 0x03          | VEE  | —  |
| 0x04          | Power device temperature                   | <ul style="list-style-type: none"> <li>ITSNS[1:0]</li> <li>TRNG</li> <li>TOFST[1:0]</li> </ul> |
| 0x05          | Die temperature (GH)                       | —  |
| 0x06 – 0x0F   | Not used                                   | —  |

See [Section 11.12.2](#) for further information interpreting post-converted results.

#### 11.14.21 BIST request and response (ADDR = 0x14)

The REQBIST command reads and reports the results of the latest built-in self-test (BIST) critical for safety-critical, high ASIL-level applications. After completing BIST, send a REQBIST command to elaborate on the result. A circuit passing BIST receives a REQBIST = 0 bit value, a failed circuit is indicated by a REQBIST = 1 bit value. Unlike the BIST itself, the REQBIST request does not need to be initiated while the GD3160 is in configuration mode. REQBIST bits persist until a new BIST is conducted or POR occurs. SPI is inactive while the BIST is running.

For other details on the BIST operation, see [Section 11.16](#). For a recommended BIST procedure, see [Section 12.2](#).

Table 64. REQBIST request and response bit readout

|                            | Rb/W | ADDR<br>[4:0] | DATA9          | DATA8          | DATA7          | DATA6          | DATA5          | DATA4          | DATA3          | DATA2          | DATA1          | DATA0          | CRC   |
|----------------------------|------|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-------|
| Bit #                      | [23] | [22:18]       | [17]           | [16]           | [15]           | [14]           | [13]           | [12]           | [11]           | [10]           | [9]            | [8]            | [7:0] |
| REQUEST BIST<br>(command)  | 0    | 0x14          | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              | —     |
| REQUEST BIST<br>(response) | 0    | 0x14          | REQBIST<br>[9] | REQBIST<br>[8] | REQBIST<br>[7] | REQBIST<br>[6] | REQBIST<br>[5] | REQBIST<br>[4] | REQBIST<br>[3] | REQBIST<br>[2] | REQBIST<br>[1] | REQBIST<br>[0] | —     |

Table 65. REQBIST bit descriptions

| Bit        | Logic 1 indicates BIST failure in:                                    |
|------------|---|
| REQBIST[9] | DATA_IN, DATA_OUT communications link.                                |
| REQBIST[8] | LV domain LBIST, logic state machine, timers, or combinational logic. |
| REQBIST[7] | HV domain LBIST, logic state machine, timers, or combinational logic. |
| REQBIST[6] | Oscillator failure (LV or HV domain).                                 |
| REQBIST[5] | DESAT and/or SEGDRV comparators.                                      |
| REQBIST[4] | ISENSE short-circuit, overcurrent comparators.                        |
| REQBIST[3] | LV or HV domain overtemperature protection.                           |
| REQBIST[2] | ADC failure (HV domain).  |
| REQBIST[1] | LV domain power management, diagnostics, UV/OV monitors.              |
| REQBIST[0] | HV domain power management, diagnostics, UV/OV monitors.              |

#### 11.14.22 Device ID (ADDR = 0x15)

The ID registers provides revision and version information on the LV and HV domain die each.

Table 66. ID register bit readout

|            | Rb/W | ADDR<br>[4:0] | DATA9 | DATA8 | DATA7 | DATA6   | DATA5   | DATA4   | DATA3 | DATA2   | DATA1   | DATA0   | CRC   |
|------------|------|---------------|-------|-------|-------|---------|---------|---------|-------|---------|---------|---------|-------|
| Bit #      | [23] | [22:18]       | [17]  | [16]  | [15]  | [14]    | [13]    | [12]    | [11]  | [10]    | [9]     | [8]     | [7:0] |
| Name/Value | 0    | 0x15          | —     | —     | VDD3  | LVDC[2] | LVDC[1] | LVDC[0] | FS3ST | HVDC[2] | HVDC[1] | HVDC[0] | —     |
| Default    | 0    | —             | 0     | 0     | —     | —       | —       | —       | —     | —       | —       | —       | —     |

Table 67. ID bit description

| Bits      | Bit description  |
|-----------|--|
| VDD3      | VDD selection:<br>VDD3 = 1 VDD = 5 V<br>VDD3 = 0 VDD = 3 V                                       |
| LVDC[2:0] | Low-voltage (LV) domain die revision number<br>LVDC[2:0] = '011'                                 |
| FS3ST     | FSISO Tristate selection:<br>FS3ST = 0 On state selected (default)<br>FS3ST = 1 3-state selected |
| HVDC[2:0] | High-voltage (HV) domain die revision number<br>HVDC[2:0] = '011'                                |

11.15 Low-voltage domain to high-voltage domain communications

11.15.1 Introduction

The GD3160 integrates communications channels between the low-voltage (LV) domain connected to the MCU, and the high-voltage (HV) domain connected to the IGBT/SiC power device. These channels are mostly transparent to the user, but enable critical controls, configurability, as well as fault and status reporting.

All LV/HV domain communications are protected by 8-bit CRC (checked on both domains). These domain communications are initiated with regularity and supervised by a watchdog, again on both domains. This contributes to the ASIL level of the GD3160 and system.

11.15.2 Overview of low-voltage (LV) communications

The LV domain receives inputs from the MCU and originates communication messages to the HV domain. The LV domain also receives a real-time status from the HV domain and might react to it according to the GD3160's configuration.

The LV domain retrieves converted ADC data from the HV domain on a regular basis using the watchdog routine. The LV domain stores the most recently acquired data and provides this to the AOUT pin. If the user requests the same data over a REQADC SPI command, a new LV/HV domain command is not initiated and the stored data is reported.

The GD3160 uses dynamic scheduling of watchdog and other LV/HV domain communications to try to avoid PWM edges (frequently the most electrically disruptive activity in the gate driver IC) and execute precision operations during idle PWM times. The GD3160 will attempt to schedule the next LV/HV communications during the longest idle time of the PWM cycle – or if the frequency is too fast, it prefers to schedule after PWM edges.

| Duty cycle condition | Scheduling      |
|----------------------|-----------------|
| d < 50 %             | During PWM low  |
| d > 50 %             | During PWM high |
| Very fast frequency  | After PWM high  |

The GD3160 will also manage interruptions to the LV/HV communications and retry message transmission after the PWM is idle. For example, if a PWM edge is received during a SPI command, the GD3160 will suspend internal LV/HV communications, throw out the command, and retry transmission. There is no internal error (COMERR) reported for this case.

No command is sent to the HV domain in the case of a SPI error (SPIERR) or invalid address request. Transitions in CSB that are not accompanied by SCLK activity do not result in an LV/HV message being sent, and no SPIERR or COMERR is reported.

11.15.3 Overview of high-voltage (HV) communications

The HV domain continuously relays real-time status of the HV domain and power device to the LV domain. Otherwise, the HV domain behaves as a communications responder, only replying to commands originating from the LV domain.

If the HV domain does not see a command from the LV domain within the watchdog timeout period, the HV domain will latch a fault, notify the LV domain, and latch off the gate outputs.

### 11.15.4 Managing LV/HV domain communication errors

There are several types of communications errors that can occur between the SPI master and the GD3160 or between the low-voltage and high-voltage domains on the GD3160. [Table 68](#) lists the errors that can occur with each message type and how the GD3160 responds to each error.

**Table 68. SPI and LV/HV domain communication error management**

| Message type  | From      | To        | Error   | Response  |
|---|-----------|-----------|---|---|
| SPI command   | MCU       | LV domain | The low-voltage domain detects error or framing error                                     | The low-voltage domain returns data from last valid command, ignores message, sets SPIERR bit in STATUS 2, latches fault and reports fault at INTB. IGBT state is not changed.  |
| SPI command   | LV domain | HV domain | The high-voltage domain detects CRC or framing error                                      | The high-voltage domain returns data from last valid command and increments its COMERR counter. If count is exceeded: <ul style="list-style-type: none"> <li>• Sets COMERR bit in STATUS 2</li> <li>• Latches fault and reports fault at INTB</li> <li>• Turns off IGBT</li> </ul>                    |
| SPI command   | HV domain | LV domain | The low-voltage domain detects no response from the high-voltage domain                   | When the WD timer expires, the low-voltage domain latches a WDOG_FLT, reports the fault at INTB, sets WDOG_FLT bit in STATUS 2 and instructs the high-voltage domain to turn off IGBT   |
| SPI command   | HV domain | LV domain | The low-voltage domain detects CRC or framing error, or last valid data                   | The low-voltage domain returns data from last valid command and increments its COMERR counter. If count is exceeded: <ul style="list-style-type: none"> <li>• Sets COMERR bit in STATUS 2</li> <li>• Latches fault and reports fault at INTB</li> <li>• Turns off IGBT</li> </ul>                     |
| SPI command   | MCU       | LV domain | SPI message delay time is too brief (< 19 µs)   | The low-voltage domain returns data from last valid command and ignores message. Condition is reported as SPIERR  |
| Low-voltage domain to high-voltage domain request ADC command | LV domain | HV domain | The high-voltage domain does not receive any message within the watchdog timeout interval | The high-voltage domain sets WDOG_FLT bit in its STATUS 2, latches fault, reports fault at INTB and turns off IGBT  |
| Low-voltage domain to high-voltage domain request ADC command | LV domain | HV domain | The high-voltage domain detects CRC or framing error                                      | The high-voltage domain returns data from last valid message and increments its error counter. If count is exceeded: <ul style="list-style-type: none"> <li>• Sets COMERR bit in STATUS 2</li> <li>• Latches fault and reports fault at INTB</li> <li>• Turns off IGBT</li> </ul>                     |
| Low-voltage domain to high-voltage domain request ADC command | HV domain | LV domain | The low-voltage domain detects no response from the high-voltage domain                   | When the WD timer expires, the low-voltage domain latches a WDOG_FLT, reports the fault at INTB, sets WDOG_FLT bit in STATUS 2 and instructs the high-voltage domain to turn off IGBT   |
| Low-voltage domain to high-voltage domain request ADC command | HV domain | LV domain | The low-voltage domain detects CRC or framing error                                       | The low-voltage domain ignores returned data and increments its error counter. If count is exceeded: <ul style="list-style-type: none"> <li>• Sets COMERR bit in STATUS 2</li> <li>• Latches fault and reports fault at INTB</li> <li>• Instructs the high-voltage domain to turn off IGBT</li> </ul> |

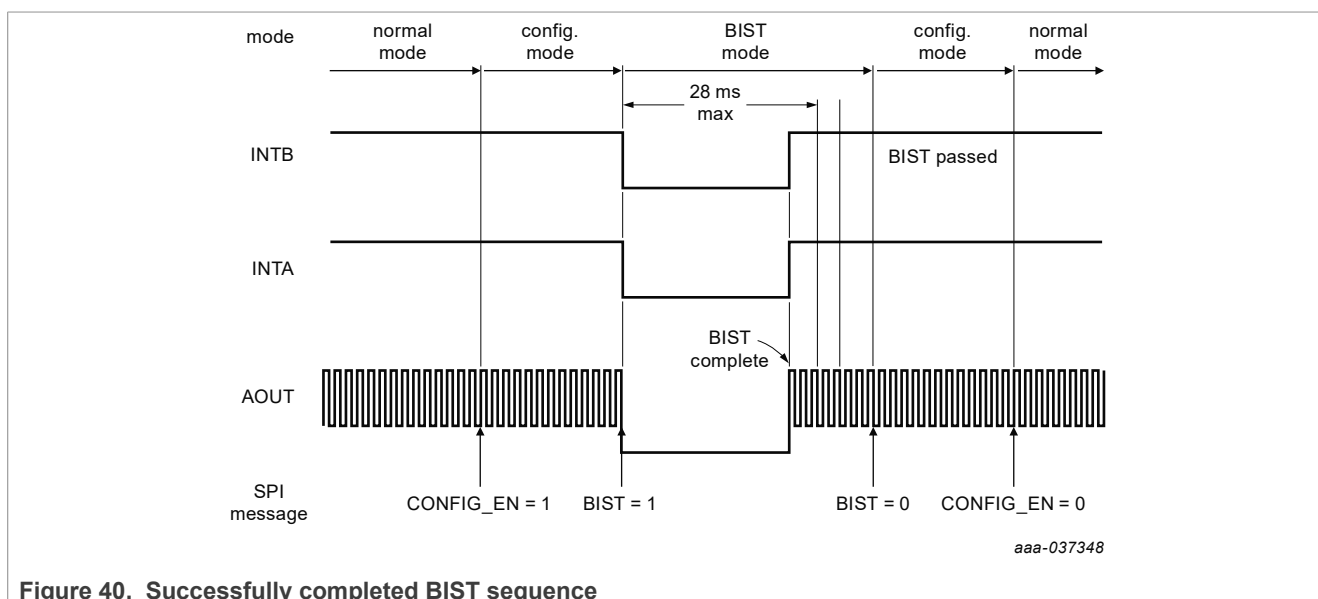
## 11.16 Built-in self-test

### 11.16.1 BIST overview

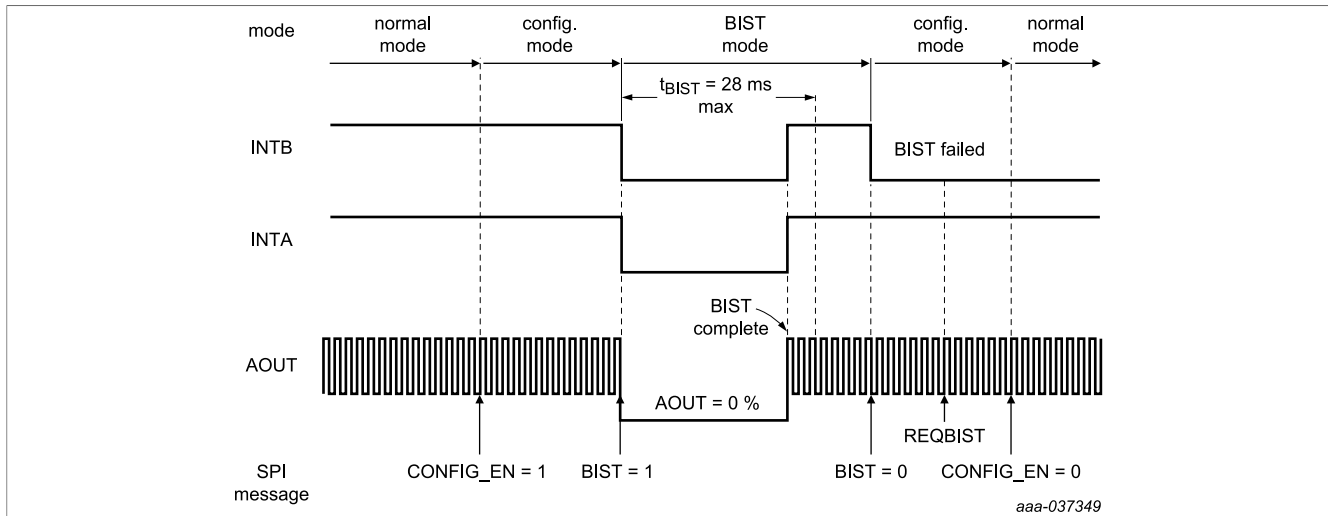
The GD3160's built-in self-test (BIST) is critical in helping meet its ASIL/SIL safety metrics. The BIST, including logic BIST/LBIST and analog BIST/ABIST, checks all key safety mechanisms and other circuits used in general operation:

- LV domain power management, diagnostics, UV/OV monitors (VSUP, VDD)
- HV domain power management, diagnostics, UV/OV monitors (VCC, VCCREG, VREF, VEE out of range)
- ISENSE short-circuit (SC) and overcurrent (OC) comparators
- LV and HV overtemperature comparators
- Clock loss/oscillator failure
- ADC conversion failure
- Desaturation fault and segmented drive comparators
- Logic block BIST, on both LV and HV domains
- LV/HV domain communications

The BIST process is described in [Section 11.16.2](#). [Figure 40](#) and [Figure 41](#) show the INTB, INTA, and AOUT output pin states. One important note on configuring VEEM before running the BIST is given in [Section 11.16.3](#).



The BIST result is reported on INTB when the BIST bit is set to '0' by a SPI command to exit BIST mode. If any portion of the low-voltage domain or high-voltage domain BIST sequence fails, the INTB pin behaves as shown in [Figure 41](#). In this case, INTB is pulled low when the device enters Configuration mode, the BIST\_FAIL bit in STATUS2 register is latched to Logic 1, the circuit that failed BIST is identified in the REQBIST register, and the IGBT gate drive output is forced to the OFF state. The BIST fault bit reported by the SPI is a logic OR of the BIST faults of both low-voltage domain and high-voltage domain.



If the GD3160 fails the BIST test, it can be queried to determine the source of the failure. To accomplish this, the MCU sends a REQBIST command, whereupon it receives a response indicating which of 10 sub-circuits reported the failure.

Power cycling only one domain resets the logic and BIST result of that domain only; the other domain is preserved, and the ORed BIST result of the whole device (seen at the BIST\_FAIL bit) is refreshed.

BIST relies on the VEE\_OORM mask setting to determine whether it should test VEE monitoring circuitry or not. The GD3160 interprets a VEE\_OORM = 0 as a system without a negative supply, and not check VEE monitor circuits. Setting VEE\_OORM = 1 confirms a negative supply is expected, and VEE monitor circuits are checked.

BIST configuration and use are described in [Section 12](#).

### 11.16.2 BIST process

The GD3160 can only enter BIST from Configuration mode (in MODE2 register, CONFIG\_EN = 1). Any other BIST request initiated while the device is not in Configuration mode is ignored. BIST starts once a Logic 1 is written to the BIST bit in the MODE2 register, while the device was already in Configuration mode.

The GD3160 output pins INTB, INTA, and AOUT provide a way for the MCU to monitor BIST progress, as well as validate pin connections and ensure proper functionality of INTB, INTA, and AOUT features. Upon starting BIST, INTB, INTA are pulled low, and AOUT reports 0 % duty cycle (pulled low). During BIST, the gate is latched off and the PWM control is disabled (until BIST = 0 and the device is no longer in Configuration mode). Allow 28 ms for BIST completion.

Upon completion of the BIST tasks, INTB and INTA go to Logic 1 and AOUT returns a 10 % fixed duty cycle. The GD3160 remains in Configuration mode (CONFIG\_EN = 1) and returns all configuration register contents to their default states. Refer to [Section 11.14](#) for information on default register states. The BIST results are loaded to the REQBIST register, and results are ORed into the BIST\_FAIL bit (STATUS2 register) bit. Upon exit of the BIST mode (set BIST = 0), the BIST\_FAIL result is loaded to the INTB pin state.

The BIST results are stored in the REQBIST register after BIST completes (setting BIST = 0 is not required) and may be read anytime, until a POR occurs or BIST is run again. Cycling power on the LV die resets LV die logic, but not HV die or the ORed response of all BIST faults.

### 11.16.3 Configure VEE\_OORM before running BIST

BIST uses the VEE\_OORM mask setting, before BIST has started, to determine whether it should test VEE monitoring circuitry or not, as part of the BIST.

The GD3160 interprets a VEE\_OORM = 0 as a system without a negative supply, and does not check VEE monitoring circuits during BIST. Setting VEE\_OORM = 1 going into BIST indicates a negative supply will be present and causes the GD3160 to test VEE monitoring circuits.

For this reason, if the system includes a negative supply, it is recommended to set VEE\_OORM = 1 before running BIST, even if VEE\_OORM = 0 (the VEE out of range fault will be masked) during normal operation. BIST may cover this anyway. Configuring mask values before BIST is therefore part of the recommended BIST operation procedure given in [Section 12.2 "Perform BIST upon initialization"](#).

## 12 Operation

Get the GD3160 up and running in an application using the steps given in this section:

1. Power up the GD3160 safely into a zero-fault state per [Section 12.1](#).
2. Run BIST upon initialization per [Section 12.2](#).
  - If BIST is run on power down, skip this step.
3. The GD3160 now may be safely used in the default configuration now, as detailed in [Section 12.3](#).
4. Configure the GD3160 for an application using SPI and return to normal operation, according to [Section 12.4](#).
5. Exceptions to normal operation are given by fault reactions described in [Section 12.5](#).
6. Manage the system safe state with fail-safe controls and modes given to [Section 12.6](#).

### 12.1 GD3160 power-up sequence

The following sequence can be used as a guideline for powering up the GD3160.

1. Bring up VSUP/VDD to power up the LV domain properly. Passive pullup/pulldown on input pins ensure a safe state.
2. Configure all MCU I/O connected to the GD3160.
  - a. Set CSB, FSENB = Logic 1.
  - b. Set MOSI, PWM, FSSTATE = Logic 0.
  - c. Set MCU pins seeing GD3160's INTB, INTA, and AOUT pins to be inputs.
3. Confirm LV domain is working properly without faults, while HV domain is still unpowered.
  - a. Verify the following to confirm GD3160 is in the right state (WAIT state) and working properly:
    - i. INTB = Logic 0
    - ii. AOUT duty cycle is  $d = 5\%$  (before HV domain is powered up)
    - iii. AOUT period is  $4\text{ kHz} \pm 3\%$  (verifies GD3160 internal clock)
  - b. Read SPI registers to ensure no faults on LV domain:
    - i. Check STATUS2 register to ensure VDD is properly powered up (no VDD\_UVOV fault) and that there are no errors in SPI communication (no SPIERR fault).
    - ii. Check for LV die OTSD\_IC fault by reading STATUS1
    - iii. A watchdog fault (WDOG\_FLT) is acceptable at this point, since we have not powered the HV domain, the LV/HV domain communications will not yet work.
  - c. Confirm correct pin states on LV domain I/O pins:
    - Read STATUS3 register to confirm PWM, PWMALT, FSENB, FSSTATE, and INTB pins are in the correct states.
4. Enable the DC-DC converter that powers the HV domain (VCC) to complete the power-up sequence, and clear/diagnose any faults upon completing power up.
  - a. Enable the power supply supplying VCC, and wait for the supply/regulators to stabilize.
  - b. Output pins indicate when HV domain is powered and working properly (GD3160 is in NORMAL mode):
    - i. AOUT reports the voltage on TSENSEA, duty cycle is between  $10\%$  and  $90\%$  (no longer reporting  $5\%$ ).
    - ii. INTB = Logic 1 indicates there are no faults present.
    - iii. If INTB = 0 still at this step, there are faults to clear.
  - c. Read SPI status registers to ensure no faults persist after full power up. INTB = 1 indicates there are no faults or all faults were cleared.
    - i. Check STATUS2 register and clear any latched watchdog faults (WDOG\_FLT) remaining from power up.

- ii. Check STATUS1 register for any fault with incorrect gate supply (no VCCOV or VCCREGUV faults), load (no DESAT, etc.) or temperature element (no OTSD or OTW faults) and clear as needed.
- iii. A REQADC command of the TSENSEA should confirm the reading seen on AOUT.
- d. Confirm correct expected states on HV domain connections:
  - Read STATUS3 register to ensure FSISO and power device gate (VGE) are in the expected state.

The GD3160 is now ready for BIST, configuration, or operation with default settings.

## 12.2 Perform BIST upon initialization

Upon initial configuration, perform a BIST with the relevant GD3160 settings configured.

1. If not already done, enter Configuration mode by writing a '1' to the CONFIG\_EN bit in the MODE2 register.
2. Configure protections for BIST to check.
  - a. If operating in a system with a negative gate voltage, set the VEE\_OORM mask bit (in MSK2 register) to 1 so that BIST checks the comparator monitoring for VEE out of range (OOR) Failure mode. Even if VEE\_OORM will be masked in the application, this is one setting the BIST looks at to determine what to check. The VEE\_OORM mask bit can be set later to any value.
  - b. If operating a system without a negative gate voltage (minimum gate-emitter voltage = 0 V), VEE\_OORM may be left at 0, the default value.
3. Write a 1 to the BIST bit in the MODE2 register. This initializes the BIST process. See [Section 11.16](#) for additional information.
4. Following BIST completion, write BIST = 0 to end the BIST mode and deliver the result to the INTB pin.
  - For block-level elaboration on the BIST result, send a REQBIST command and view the response. See [Section 11.16](#) for additional information.
5. Because PWM is disabled by configuration mode (CONFIG\_EN = 1), after passing BIST the MCU can verify the system path to various pins, if not already done.
  - a. Verify paths to input pins PWM, PWMALT, FSSTATE, FSENB, and FSISO pins by toggling the state from the MCU and reading pin state (as seen by the GD3160) back over STATUS3 register.
  - b. The INTA and INTB output states can also be verified by STATUS3, the MCU can compare its own pin state to the state reported by the GD3160 STATUS3 bit state. This can be done during a BIST fail or pass state.
6. Write desired fault mask settings back to all mask registers (MSK1, MSK2, RMSK1, RMSK2) per application settings. This enables desired fault and protections reporting now that BIST has been completed with as many circuits as desired active.
7. At this point, BIST and verification measures are complete. There are two ways to proceed:
  - a. Write CONFIG\_EN = 0 to leave CONFIG mode and enable PWMing with default settings. Continue to [Section 12.3](#).
  - b. Leave CONFIG\_EN = 1 for now to continue configuring the device. Bearing the default configuration in mind, skip to [Section 12.5](#) for configure the G3160 best for an application.
8. Clear bits POR\_1 and POR\_2 in STATUS 3 register.

## 12.3 Default functionality

The GD3160 takes default functionality settings upon initial power up, POR recovery, software reset command by SPI (RESET bit), or after completing the BIST sequence. The default settings are optimal for SiC MOSFETs or very fast IGBTs. Default functionality is given below, along with the associated bit setting.

### 12.3.1 Default configuration

Without additional configuration via the SPI, GD3160 will take the following functionality by default.

- PWM activity on the gate is not disabled or restricted once power supplies are in full regulation and LV/HV domain supplies are working. CONFIG = BIST = RESET = 0.
- The VCCREG gate supply regulator is enabled (VCC level and hardware connections permitting) and initializes at 15 V. VCCREG[2:0] = 0b001.
- INTA is configured as a second fault pin and real-time report is disabled. RTRPT = RTMON\_CFG = 0.
  - INTA and INTB will report faults per the RMSK1 and RMSK2 registers.
- The mandatory PWM deadtime is initialized to 3.24  $\mu$ s (includes div. by 2 factor by TIME\_2 = 1). DEADT = 0b1111, TIME\_2 = 1.
- AMC is enabled and will hold the gate low after turn-off is complete. AMC = 1.
- TSENSEA current source is enabled. TISNS\_EN = 1.
  - The value TSENSEA current source is 1 mA. ITSNS = 0b11.
  - Power device overtemperature fault and warning are masked by default, so the device will not initialize into a faulted state. OTSDM = OTWM = 0.
- AOUT reports the voltage at the TSENSEA pin. AOUT = 0.
- The FSISO pin is enabled and can turn on the gate. FSISOEN = 1.
- Upon gate supply (VCCREG) undervoltage recovery, PWM activity is allowed. UV\_LATCH = 0.
  - The VCCREG undervoltage threshold is 11.5 V. UV\_TH[2:0] = 0b011.
- The real-time monitor delay (RTMONDLY) is configured for 1000 ns time (includes div. by 2 factor for TIME\_2). RTMONDLY = 0b1010, TIME\_2 = 1.

### 12.3.2 Default protections

The enabled protections have the following settings, by default:

- DESAT protection (interface with power device collector/drain) is enabled. DESAT = 1.
  - The internal DESAT pin current source is 500  $\mu$ A. IDESAT[1:0] = 0b01.
  - The DESAT threshold voltage is 6.0 V. DESAT\_TH = 0b1010.
  - The DESAT detection filter time is 80 ns. DESAT\_FLT[1:0] = 0b01.
  - The DESAT leading edge blanking time is 240 ns. DESAT\_LEB[2:0] = 0b011.
- 2LTO is enabled and will engage the gate while verifying a fault. 2LTO = 1.
  - The 2LTO voltage is 7.26 V. 2LTOV = 0b011.
  - The duration of 2LTO is 500 ns (includes default faster behavior by SCFF bit). SCFILT = 0b100, SCFF = 1.
- SSD is enabled and will engage during a faulted shutdown. SSD = 1.
  - The SSD current is 0.541 A. SSD\_CUR = 0b100.
  - The default SSD time is 3000 ns (including div. by 2 factor from the default TIME\_2 setting). SSDT = 0b100, TIME\_2 = 1.
- Deadtime fault protection is not masked and will be reported by default. DTFLTM = 1.
- The SPI message error (SPIERR) will be reported by default. SPIERRM = 1.
  - If the GD3160 SPI response is not updating, and INTB goes low upon sending a SPI message, this could indicate a SPIERR fault occurred due to problems with the SPI message.

- The watchdog fault will be reported, indicating when LV/HV domain communications are not occurring. WDOG\_FLTM = 1.
- Internal domain communications errors and unintended configuration register flips will be reported. CONFCRCERRM = COMERRM = 1.
- A VREF undervoltage condition will be reported and latch off gate outputs.

### 12.3.3 Default mask settings

The following functions are disabled or masked by default and will not be reported:

- ISENSE protection (interface with a current mirror) is disabled.
  - Short-circuit detection by the ISENSE pin is disabled. SCSNS = 0.
  - Overcurrent sense by the ISENSE pin is disabled. OCSNS = 0.
- Segmented drive mode is disabled. SEGDRV = 0.
- Active VCE clamp is disabled. ACTCLMP = 0.
- VEE supply out of range is masked and not reported. VEE\_OORM = 0.
- Power device overtemperature/warning reporting is masked by default and not reported. OTSDM = OTWM = 0.
- PWM-to-gate-output coherency check is masked by default, and will not be reported. RTMON\_FLTM = 0.

## 12.4 Register initialization in CONFIG mode

To configure the GD3160 operating modes and reporting scheme, first place the device into configuration mode by a SPI message.

1. Write a '1' to the CONFIG\_EN bit in the MODE2 register. No other register will retain written data until this is done. Entering Configuration mode also disables PWMing and prevents unwanted bit flips.
2. Read back the MODE2 register and confirm CONFIG\_EN bit = 1 before writing the remaining registers. If CONFIG\_EN is not set to '1' or INTB is low, the SPI communication is invalid.
3. When CONFIG\_EN = 1, the GD3160 is in Configuration mode and all MODE, CONFIG registers, and interrupt MSK and RMSK registers can be written to. The registers do not need to be read back in order for the bit settings to be retained. The bits are finalized upon rising edge of CSB.

## 12.5 Summary of faults and GD3160 responses

[Table 69](#) lists the GD3160's faults bits, the mode, and mask bits associated with each fault, and the response to the fault based on the state of the mode and mask bits.

All faults are reported at the INTB or INTA and the SPI unless the fault is masked. If the fault is no longer present, latched fault bits can be cleared by POR, Reset, BIST, or by writing a Logic 1 to the faulted SPI bit.

**Table 69. GD3160 fault response and mask settings**

| Fault bit description<br>(Symbol) | Mode bit and function |                                 | Mask bit and functional response |  |  |   | Power device faulted turnoff |                   |
|-----------------------------------|-----------------------|---------------------------------|----------------------------------|--|--|---|------------------------------|-------------------|
|                                   | Mode bit              | Function<br>(When Mode bit = 1) | Mask bit                         | Response when masked (Mask bit = 0)                    | Unmasked response (Mask bit = 1) with fault present                    | Unmasked response (Mask bit = 1) after fault is no longer present | SSD (if enabled)             | TLTO (if enabled) |
| VCC overvoltage (VCCOV)           | —                     | —                               | VCCOVM                           | PWMing remains enabled, fault not latched or reported. | PWM disabled. GL on. AMC on, if enabled.                               | PWM disabled. GL on. AMC on, if enabled.                          | No                           | No                |
| VCCREG undervoltage (VCCREGUV)    | —                     | —                               | VCCREGUVM                        | PWMing remains enabled, fault not latched or reported. | PWM gated by UV comparator if UV_LATCH = 0. GL on. AMC on, if enabled. | PWM disabled if UV_LATCH bit = 1 (in CONFIG1)                     | No                           | No                |
| VSUP overvoltage (VSUPOV)         | —                     | —                               | VSUPOVM                          | PWMing remains enabled, fault not latched or reported. | PWM disabled. GL on. AMC on, if enabled.                               | PWM disabled. GL on. AMC on, if enabled.                          | NA                           | NA                |

Table 69. GD3160 fault response and mask settings...continued

| Fault bit description<br>(Symbol)   | Mode bit and function |   | Mask bit and functional response |  |  |   | Power device faulted turnoff |                   |
|---|-----------------------|---|----------------------------------|--|--|---|------------------------------|-------------------|
|   | Mode bit              | Function<br>(When Mode bit = 1)   | Mask bit                         | Response when masked (Mask bit = 0)  | Unmasked response (Mask bit = 1) with fault present                              | Unmasked response (Mask bit = 1) after fault is no longer present           | SSD (if enabled)             | TLTO (if enabled) |
| VDD regulator overtemperature shutdown (OTSD_IC)  | —                     | —   | —                                | Not maskable.  | PWM disabled.<br>GL on. AMC on, if enabled. VDD remains ON.                      | PWM disabled.<br>GL on. AMC on, if enabled. VDD remains ON.                 | No                           | No                |
| VCCREG regulator and GH transistor overtemperature shutdown (OTSD_IC)                             | —                     | —   | —                                | Not maskable.  | PWM disabled.<br>VCCREG and GH = off GL on. AMC on, if enabled. VREF = off.      | PWM disabled.<br>VCCREG and GH = off GL on. AMC on, if enabled. VREF = off. | No                           | No                |
| GL transistor overtemperature shutdown (OTSD_IC)  | —                     | —   | —                                | Not maskable.  | PWM disabled.<br>VCCREG and GH = off GL on. AMC on, if enabled. VREF = off.      | PWM disabled.<br>VCCREG and GH = off GL on. AMC on, if enabled. VREF = off. | No                           | No                |
| Overtemperature shutdown of IGBT (OTSD)   | —                     | —   | OTSDM                            | PWMing remains enabled, fault not latched or reported. Temp reported in ADCVAL and AOUT.     | PWM disabled.<br>GL on. AMC on, if enabled.                                      | PWM disabled.<br>GL on. AMC on, if enabled.                                 | No                           | No                |
| Overtemperature warning of IGBT (OTW)   | —                     | —   | OTWM                             | PWMing remains enabled, fault not latched or reported. Temp reported in ADCVAL.              | PWM enabled.   | PWM enabled.  | NA                           | NA                |
| V <sub>CE</sub> clamp activation (CLAMP)  | ACTCLMP               | Enables clamp comparator, protection, fault reporting.                  | CLAMPM                           | PWMing remains enabled, fault not latched or reported.                                       | PWM disabled. SSD is engaged for the intervention time.                          | PWM enabled.  | Yes, min SSD (100 mA)        | NA                |
| Power device desaturation, by DESAT detection (DESAT)   | DESAT                 | Enables DESAT comparator, current sources, protection, fault reporting. | —                                | Not maskable.  | PWM disabled.<br>GL on. AMC on, if enabled.                                      | PWM disabled.<br>GL on. AMC on, if enabled.                                 | Yes                          | Yes               |
| Power device short-circuit, by current-sense (SC)   | SCSNS                 | Enables SC comparator, protection, fault reporting.                     | —                                | Not maskable.  | PWM disabled.<br>GL on. AMC on, if enabled.                                      | PWM disabled.<br>GL on. AMC on, if enabled.                                 | Yes                          | Yes               |
| Power device overcurrent, by current-sense (OC)   | OCSNS                 | Enables OC comparator, protection, fault reporting.                     | OCM                              | PWM remains enabled, fault not latched or reported.  | PWM enabled.   | PWM enabled.  | Yes, max SSD (1 A)           | No                |
| BIST failure (BIST_FAIL)  | BIST                  | Enables BIST sequence.  | —                                | Not maskable.  | PWM disabled.<br>GL on. AMC on, if enabled.                                      | PWM disabled.<br>GL on. AMC on, if enabled.                                 | NA                           | NA                |
| VDD out of range (VDD_UVOV)   | —                     | —   | —                                | Not maskable.  | PWM disabled.<br>GL on. AMC on, if enabled.                                      | PWM disabled.<br>GL on. AMC on, if enabled.                                 | No                           | No                |
| PWM deadtime violation (DTFLT)  | —                     | —   | DTFLTM                           | PWMing remains enabled, fault not latched or reported, programmed deadtime remains enforced. | PWM enabled additional deadtime inserted via settings, INTA or INTB is reported. | PWM enabled, INTB remains latched.  | NA                           | NA                |
| SPI framing or CRC error (SPIERR)   | —                     | —   | SPIERRM                          | PWMing remains enabled, fault not latched or reported.                                       | PWM enabled.   | PWM enabled.  | NA                           | NA                |
| LV or HV domain detected a use reading issue or a CRC change in its CONFIG registers (CONFCRCERR) | —                     | —   | CONFCRCERRM                      | PWMing remains enabled, fault not latched or reported.                                       | PWM disabled.<br>GL on. AMC on, if enabled.                                      | PWM disabled.<br>GL on. AMC on, if enabled.                                 | No                           | No                |
| Gate not tracking PWM commanded state (RTMON_FLT)   | —                     | —   | RTMON_FLTM                       | PWMing remains enabled, fault not latched or reported.                                       | PWM disabled.<br>GL on. AMC on, if enabled.                                      | PWM disabled.<br>GL on. AMC on, if enabled.                                 | No                           | No                |
| Loss of LV/HV domain communication (WDOG_FLT)   | —                     | —   | WDOG_FLTM                        | PWMing remains enabled, fault not latched or reported.                                       | PWM disabled.<br>GL on. AMC on, if enabled.                                      | PWM disabled.<br>GL on. AMC on, if enabled.                                 | No                           | No                |
| Error in HV/LV domain communications (COMERR)   | —                     | —   | COMERRM                          | PWMing remains enabled, fault not latched or reported.                                       | PWM disabled.<br>GL on. AMC on, if enabled.                                      | PWM disabled.<br>GL on. AMC on, if enabled.                                 | No                           | No                |

Table 69. GD3160 fault response and mask settings...continued

| Fault bit description<br>(Symbol) | Mode bit and function |                                    | Mask bit and functional response |  |   |  | Power device faulted turnoff |                      |
|-----------------------------------|-----------------------|------------------------------------|----------------------------------|--|---|--|------------------------------|----------------------|
|                                   | Mode bit              | Function<br>(When Mode<br>bit = 1) | Mask bit                         | Response when<br>masked (Mask bit =<br>0)                    | Unmasked response<br>(Mask bit = 1) with<br>fault present | Unmasked response<br>(Mask bit = 1) after<br>fault is no longer<br>present | SSD (if<br>enabled)          | TLTO (if<br>enabled) |
| VREF out of range<br>(VREF_UV)    | —                     | —                                  | —                                | Not maskable.  | PWM disabled.<br>GL on. AMC on, if<br>enabled.            | PWM disabled.<br>GL on. AMC on, if<br>enabled.                             | No                           | No                   |
| VEE out of range<br>(VEE_OOR)     | —                     | —                                  | VEE_OORM                         | PWMing remains<br>enabled, fault not<br>latched or reported. | PWM disabled.<br>GL on. AMC on, if<br>enabled.            | PWM disabled.<br>GL on. AMC on, if<br>enabled.                             | No                           | No                   |

## 12.6 Fail-safe transitions

Upon realization of a fault, the system must move into a Safe state. The exact architecture and implementation varies by design but the GD3160 clearly implements fail-safe and fault responses per [Table 70](#).

Table 70. G3160 control priority: Normal, Fault, and Fail-safe modes

| Priority | Signal <sup>[1]</sup> | Origin     | Type <sup>[2]</sup>      | Maskable <sup>[3]</sup> |
|----------|-----------------------|------------|--------------------------|-------------------------|
| 1        | FSISO                 | Die 2 (HV) | Pin                      | N                       |
| 2        | OSC_LOSS/WD_FLT       | Die 2 (HV) | Fault                    | Y                       |
| 3        | RESET                 | SPI        | Register                 | N                       |
| 4        | BIST                  | SPI        | Register                 | N                       |
| 5        | VCCOV                 | Die 2 (HV) | Fault                    | Y                       |
| 5        | VCCREGUV              | Die 2 (HV) | Gated (UV_LATCH)         | Y                       |
| 5        | VCCREGUV              | Die 2 (HV) | Fault                    | Y                       |
| 5        | OTSD_IC               | Die 2 (HV) | Fault                    | N                       |
| 5        | OTSD                  | Die 2 (HV) | Fault                    | Y                       |
| 5        | BIST fault            | Die 2 (HV) | Fault                    | N                       |
| 5        | CONFRCRERR            | Die 2 (HV) | Fault                    | Y                       |
| 5        | WD_FLT                | Die 2 (HV) | Fault                    | Y                       |
| 5        | COMERR                | Die 2 (HV) | Fault                    | Y                       |
| 5        | VREF_UV               | Die 2 (HV) | Fault                    | N                       |
| 5        | VEE_OOR               | Die 2 (HV) | Fault                    | Y                       |
| 6        | DESAT                 | Die 2 (HV) | Fault                    | N                       |
| 6        | SC                    | Die 2 (HV) | Fault                    | N                       |
| 7        | SEG_DRV               | Die 2 (HV) | SD Mod                   | N                       |
| 8        | CLAMP                 | Die 2 (HV) | Fault (not masked)       | Y                       |
| 8        | CLAMP                 | Die 2 (HV) | SD Mod (masked)          | Y                       |
| 9        | OC                    | Die 2 (HV) | SD Mod/Warn (not masked) | Y                       |
| 9        | OC                    | Die 2 (HV) | SD Mod (masked)          | Y                       |
| 10       | FSENBFSSATE           | SPI        | Register                 | N                       |
| 11       | CONFIG_EN             | Die 1 (LV) | Pin                      | N                       |
| 12       | VSUPOV                | Die 1 (LV) | Fault                    | Y                       |
| 12       | OTSD_IC               | Die 1 (LV) | Fault                    | N                       |
| 12       | VDD_UV                | Die 1 (LV) | Fault (VDD_UVOV)         | N                       |
| 12       | VDD_OV                | Die 1 (LV) | Fault (VDD_UVOV)         | N                       |
| 12       | RTMON_FLT             | Die 1 (LV) | Fault                    | Y                       |
| 12       | BIST fault            | Die 1 (LV) | Fault                    | N                       |
| 12       | CONFRCRERR            | Die 1 (LV) | Fault                    | Y                       |
| 12       | WD_FLT                | Die 1 (LV) | Fault                    | Y                       |

Table 70. G3160 control priority: Normal, Fault, and Fail-safe modes...continued

| Priority | Signal <sup>[1]</sup> | Origin     | Type <sup>[2]</sup>          | Maskable <sup>[3]</sup> |
|----------|-----------------------|------------|------------------------------|-------------------------|
| 12       | COMERR                | Die 1 (LV) | Fault                        | Y                       |
| 13       | DTFLT/DEADT           | Die 1 (LV) | TO PWM Mod/Warn (not masked) | Y                       |
| 13       | DTFLT/DEADT           | Die 1 (LV) | TO PWM Mod (masked)          | Y                       |
| 14       | PWM                   | Die 1 (LV) | Pin                          | N                       |
| NA       | OTW                   | Die 2 (HV) | Warn                         | Y                       |
| NA       | POR_2                 | Die 2 (HV) | Warn                         | N                       |
| NA       | POR_1                 | Die 1 (LV) | Warn                         | N                       |
| NA       | SPIERR                | Die 1 (LV) | Warn                         | Y                       |

[1] Signals are repeated when Origin or configuration changes the type.

[2] Types are:

- Pin = An external voltage level input
- Register = A SPI register mode bit
- Fault = A detected and latched fault resulting in Gate OFF
- Gated = A fault response that is not latched and only holds the Gate OFF during the Fault condition
- Mod = A Gate transition modifier:
  - SD: Shutdown
  - TO PWM: Turn-ON PWM
- Warn = A latched-status response that does not change Gate operation; cleared same as a Fault

[3] Maskable signals are not latched and action is not taken when masked, unless the signals show a type change.

The GD3160 fault response and action taken (on the gate) varies between Normal and Fail-safe modes. Fail-safe can be used following a fault to place the gate into a Safe state while the fault is addressed, before the fault is cleared.

[Table 71](#) details fail-safe response following various faults on the GD3160. The fault/fail-safe response is identical whether the fault occurred before fail-safe, or whether the Fail-safe state preceded the fault.

Table 71. GD3160 fault priority and responses

| Reported fault<br>Fault description                                     | Fault latched               | Gate follows PWM/<br>PWMALT following<br>fault?<br>(Normal mode) | Gate follows<br>FSSTATE following<br>fault?<br>(Fail-safe mode) | Gate follows FSISO<br>following fault?<br>(Fail-safe mode) | Notes/Rationale  |
|---|-----------------------------|--|---|--|--|
|   |                             | PWM/PWMALT = X<br>FSEN B = 1<br>FSISO = 0                        | PWM/PWMALT = X<br>FSEN B = 0<br>FSISO = 0                       | PWM/PWMALT = X<br>FSEN B = X<br>FSISO = 1                  |  |
| STATUS1 register  |                             |  |   |  |  |
| <b>VCCOV</b><br>VCC overvoltage   | Yes                         | No   | No  | Yes  | Control by PWM and FSSTATE is disabled during gate-facing HV domain fault.   |
| <b>VCCREGUV</b><br>VCCREG undervoltage                                  | Per UV_<br>LATCH<br>setting | No   | No  | Yes  | Control by PWM and FSSTATE is disabled during the VCCREG undervoltage condition. Response upon VCCREG UV recovery is determined by UV_LATCH configuration bit. |
| <b>VSUPOV</b><br>VSUP overvoltage                                       | Yes                         | No   | Yes   | Yes  | VSUP overvoltage is an LV domain fault, which does not impact fail-safe functionality.   |
| <b>OTSD_IC</b><br>Overtemperature shutdown<br>on GD3160 LV or HV domain | Yes                         | No   | No  | Yes  | IC overtemperature disables PWM and FSSTATE control. The safe state is gate latched off.   |
| <b>OTSD</b><br>Overtemperature shutdown<br>on IGBT                      | Yes                         | No   | No  | Yes  | Power device overtemperature disables PWM and FSSTATE control to prevent overheating. Safe state is gate latched off.  |
| <b>OTW</b><br>IGBT overtemperature<br>warning                           | Yes                         | Yes  | Yes   | Yes  | OTW has no impact on gate control.   |
| <b>CLAMP</b><br>VCE overvoltage fault, clamp<br>activated               | Per CLAMP<br>setting        | No   | No  | Yes  | VCE overvoltage clamp disables PWM and FSSTATE, and safely shuts down and latches the gate off.  |
| <b>DESAT</b><br>Desaturation fault                                      | Yes                         | No   | No  | Yes  | A desaturation fault disables PWM and FSSTATE, and safely shuts down and latches off the gate.   |

Table 71. GD3160 fault priority and responses...continued

| Reported fault<br>Fault description   | Fault latched      | Gate follows PWM/<br>PWMALT following<br>fault?<br>(Normal mode) | Gate follows<br>FSSTATE following<br>fault?<br>(Fail-safe mode) | Gate follows FSISO<br>following fault?<br>(Fail-safe mode) | Notes/Rationale  |
|---|--------------------|--|---|--|--|
|   |                    | PWM/PWMALT = X<br>FSENb = 1<br>FSISO = 0                         | PWM/PWMALT = X<br>FSENb = 0<br>FSISO = 0                        | PWM/PWMALT = X<br>FSENb = X<br>FSISO = 1                   |  |
| <b>SC</b><br>Short-circuit fault  | Yes                | No   | No  | Yes  | A short-circuit fault disables PWM and FSSTATE, and safely shuts down and latches off the gate.  |
| <b>OC</b><br>Overcurrent fault  | Per OCM<br>setting | Yes  | Yes   | Yes  | SSD utilized upon OC fault under PWM and FSSTATE transitions. OC and SSD are not active under FSISO.   |
| <b>STATUS2 register</b>   |                    |  |   |  |  |
| <b>BIST_FAIL</b><br>BIST failure on LV domain<br>(facing MCU)   | Yes                | No   | Yes   | Yes  | If the LV domain fails BIST, the gate follows FSSTATE in Fail-safe mode. All BIST failures on both LV/HV domains are ORed and reported to one BIST_FAIL bit.   |
| <b>BIST_FAIL</b><br>BIST failure on HV domain<br>(facing gate)  | Yes                | No   | No  | Yes  | If the HV domain fails BIST, gate control by FSSTATE is disabled. All BIST failures on both LV/HV domains are ORed and reported to one BIST_FAIL bit.  |
| <b>VDD_UVOV</b><br>VDD out of range   | Yes                | No   | Yes   | Yes  | If VDD UV/OV is temporary and recovers, then no fault is latched.  |
| <b>DTFLT</b><br>Deadtime violation in PWM<br>command  | Yes                | Yes  | Yes   | Yes  | A deadtime fault will result in delayed turn-on by PWM, but does not disable normal PWM control. Deadtime protection is unavailable while in Fail-safe modes. Functional deadtime must be provided by the safety logic providing FSSTATE.  |
| <b>SPIERR</b><br>SPI communication, framing,<br>or CRC error  | Yes                | Yes  | Yes   | Yes  | SPIERR has no effect on gate control, and does not disable control by PWM or FSSTATE.  |
| <b>CONFRCRERR</b><br>CONFIG register CRC value<br>mismatch or bit flip on LV<br>domain (facing MCU)         | Yes                | No   | Yes   | Yes  | A CONFRCRERR fault on the LV domain will not disable gate control by FSSTATE in Fail-safe mode. All LV or HV domain CONFRCRERR faults are ORed to the CONFRCRERR fault bit.  |
| <b>CONFRCRERR</b><br>CONFIG register CRC value<br>mismatch or bit flip on HV<br>domain (facing gate)        | Yes                | No   | No  | Yes  | A CONFRCRERR fault on the HV domain will disable gate control by FSSTATE. All LV or HV domain CONFRCRERR faults are ORed to the CONFRCRERR fault bit.  |
| <b>RTMON_FLT</b><br>Power device not tracking<br>PWM command  | Yes                | No   | Yes   | Yes  | Real-time power device monitoring fault does not disable control by FSSTATE in Fail-safe mode.   |
| <b>WDOG_FLT</b><br>Loss of watchdog<br>communication, seen by LV<br>domain (HV domain does not<br>respond). | Yes                | No   | Yes   | Yes  | If LV die latches WDOG_FLT (HV die does not respond), FSSTATE is not disabled during Fail-safe mode. If WDOG_FLT is due to unpowered HV domain, the gate is automatically held off. Normal PWM is always disabled by WDOG_FLT.   |
| <b>WDOG_FLT</b><br>Loss of watchdog<br>communication, seen by HV<br>domain (LV domain does not<br>respond). | Yes                | No   | No  | Yes  | If HV die latches fault (LV domain does not respond), FSSTATE is disabled. If LV domain is unpowered, there is no transmission of PWM or FSSTATE commands to the HV domain. Normal PWM is always disabled by WDOG_FLT.   |
| <b>COMERR</b><br>Inter-domain communications<br>error (CRC, framing, and so<br>on.)                         | Yes                | No   | No  | Yes  | COMERR fault latches gate off safely and disables all gate commands from the LV domain.  |
| <b>VREF_UV</b><br>VREF undervoltage   | Yes                | No   | No  | Yes  | VREF undervoltage fault disables control by PWM and FSSTATE, but not FSISO. During VREF undervoltage, the ADC, OC, DESAT, VCC overvoltage fault, and VCE real-time monitor are disabled, and the WD_FLT is set. While the ADC is disabled, the OT_TH and OTW_TH cannot be tripped. |
| <b>VEE_OOR</b><br>VEE negative gate supply out<br>of range  | Yes                | No   | No  | Yes  | Loss of negative gate supply disables control by PWM and FSSTATE.  |

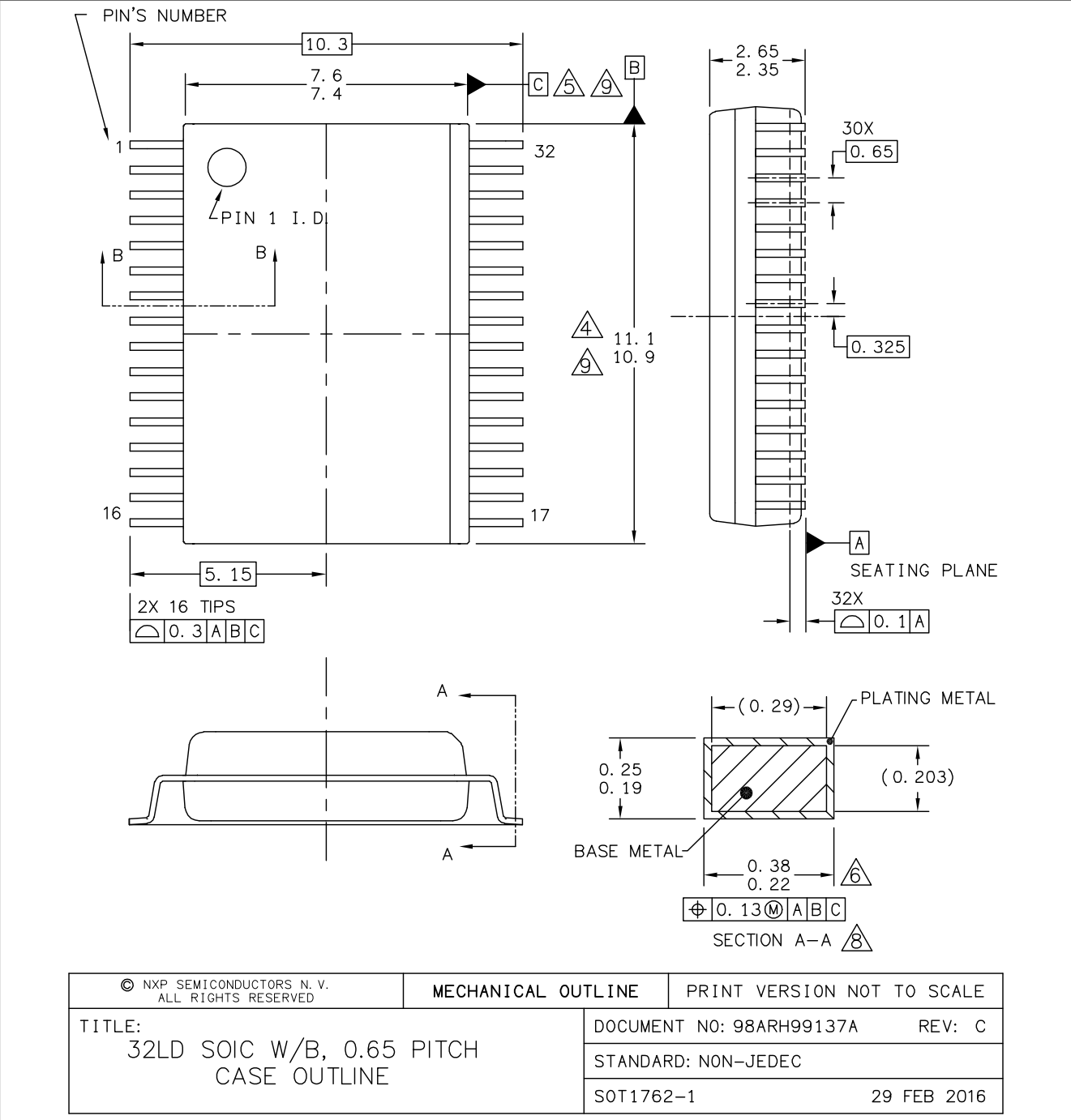
13 Packaging

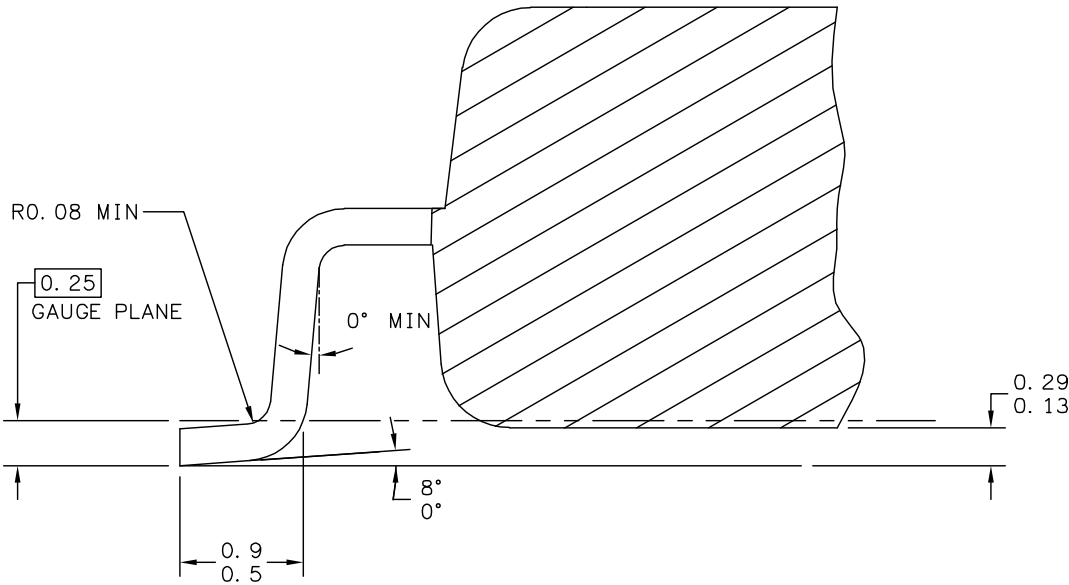
13.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to [www.nxp.com](http://www.nxp.com) and perform a keyword search for the drawing's document number.

Table 72. Package outline

| Package               | Suffix | Package outline drawing number |
|-----------------------|--------|--------------------------------|
| 32-pin wide body SOIC | EK     | 98ARH99137A                    |





|   |                                      |                            |
|---|--------------------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V.<br>ALL RIGHTS RESERVED    | MECHANICAL OUTLINE                   | PRINT VERSION NOT TO SCALE |
| TITLE:<br>32LD SOIC W/B, 0.65 PITCH<br>CASE OUTLINE | DOCUMENT NO: 98ARH99137A      REV: C |                            |
|   | STANDARD: NON-JEDEC                  |                            |
|   | SOT1762-1                            | 29 FEB 2016                |

NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
- 3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- 4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- 5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- 6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
- 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
- 9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

|  |                          |                            |
|--|--------------------------|----------------------------|
| © NXP SEMICONDUCTORS N. V.<br>ALL RIGHTS RESERVED    | MECHANICAL OUTLINE       | PRINT VERSION NOT TO SCALE |
| TITLE:<br>32LD SOIC W/B, 0.65 PITCH,<br>CASE OUTLINE | DOCUMENT NO: 98ARH99137A | REV: C                     |
|  | STANDARD: NON–JEDEC      |                            |
|  | SOT1762–1                | 29 FEB 2016                |

## 14 Revision history

Table 73. Revision history

| Document ID  | Release date      | Description  |
|--------------|-------------------|--|
| GD3160 v.13  | 06 May 2024       | <ul style="list-style-type: none"> <li>Product</li> <li>CIN 202404008I</li> <li>Global editing for style and grammar throughout.</li> <li>Updated <a href="#">Section 14</a> to conform with NXP's document content standard.</li> <li><a href="#">Table 8</a>: Changed "<math>V_{IOWM}</math>" Value to "1060" and Unit to "<math>V_{RMS}</math>"</li> <li><a href="#">Section 9.5</a>: Updated Min and Max values for "<math>I_{DESAT}</math>" and "<math>V_{DESAT\_TH}</math>"</li> <li><a href="#">Section 9.7</a>: Updated Min and Max values for "<math>T_{OSET}</math>"</li> <li><a href="#">Table 20</a>: Updated "<math>V_{OS}</math>" Min and Max values</li> <li><a href="#">Section 10.1</a>: Removed "is monitored and" from <a href="#">list</a> item 3.</li> <li><a href="#">Section 11.1.6</a>: Changed text of third paragraph from "... DESAT, VCC_OV faults and VCE RTMON ..." to "... DESAT, and VCC_OV faults ...".</li> <li><a href="#">Section 11.7.3</a>: Changed "(e.g. during SPI or if CSB is kept low, etc.)" to "(for example, during SPI)."</li> <li><a href="#">Section 11.9.3</a>: Changed "... delay of <math>t_{fittedly}</math> ..." to "... delay of <math>t_{RTRPT\_DLY}</math> ...".</li> <li><a href="#">Table 50</a>: Removed "Fault will be latched as VCCREGUV fault in STATUS1 register and reported on INTA or INTB." under "Logic 0 = masked" from Bit "VCCREGUVM".</li> <li>Updated <a href="#">Figure 30</a> and <a href="#">Figure 40</a></li> </ul> |
| GD3160 v.12  | 16 November 2023  | <ul style="list-style-type: none"> <li>Product</li> <li>CIN 202311012I</li> </ul>  |
| GD3160 v.11  | 21 April 2023     | <ul style="list-style-type: none"> <li>Product</li> <li>CIN 202302043I</li> </ul>  |
| GD3160 v.10  | 27 February 2023  | <ul style="list-style-type: none"> <li>Product</li> <li>CIN 202302043I</li> </ul>  |
| GD3160 v.9.0 | 21 November 2022  | <ul style="list-style-type: none"> <li>Product</li> <li>CIN 202209020I</li> </ul>  |
| GD3160 v.8.0 | 14 March 2022     | <ul style="list-style-type: none"> <li>Product</li> <li>CIN 202203016I</li> </ul>  |
| GD3160 v.7.0 | 23 November 2021  | Product  |
| GD3160 v.6.1 | 05 November 2021  | Objective  |
| GD3160 v.6.0 | 11 August 2021    | Objective  |
| GD3160 v.5.0 | 22 June 2021      | Objective  |
| GD3160 v.4.0 | 14 April 2021     | Objective  |
| GD3160 v.3.0 | 12 February 2021  | Objective  |
| GD3160 v.2.0 | 02 September 2020 | Objective  |
| GD3160 v.1.0 | 01 July 2020      | Initial version  |

Legal information

Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.  
[2] The term 'short data sheet' is explained in section "Definitions".  
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

Definitions

**Draft** — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Suitability for use in automotive applications** — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as “Critical Applications”), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys’ fees) that NXP may incur related to customer’s incorporation of any product in a Critical Application.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

**Security** — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at [PSIRT@nxp.com](mailto:PSIRT@nxp.com)) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

**NXP B.V.** — NXP B.V. is not an operating company and it does not distribute or sell products.

## Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

**NXP** — wordmark and logo are trademarks of NXP B.V.

## Tables

|          |   |    |          |   |     |
|----------|---|----|----------|---|-----|
| Tab. 1.  | Orderable part variations .....   | 5  | Tab. 36. | CONFIG3 parameter ranges .....                                      | 78  |
| Tab. 2.  | Pin definitions .....   | 7  | Tab. 37. | CONFIG4 register bit readout .....                                  | 79  |
| Tab. 3.  | Range of functionality .....  | 9  | Tab. 38. | CONFIG4 parameter ranges .....                                      | 79  |
| Tab. 4.  | Absolute maximum ratings .....  | 9  | Tab. 39. | CONFIG5 register .....  | 79  |
| Tab. 5.  | Thermal ratings .....   | 11 | Tab. 40. | CONFIG5 parameter ranges .....                                      | 79  |
| Tab. 6.  | Thermal resistance characteristics .....                                | 11 | Tab. 41. | CONFIG6 register bit readout .....                                  | 80  |
| Tab. 7.  | Insulation specifications .....   | 12 | Tab. 42. | CONFIG6 parameter ranges .....                                      | 80  |
| Tab. 8.  | DIN V VDE 0884-10 (VDE V 0884-10)<br>insulation characteristics .....   | 12 | Tab. 43. | CONFIG7 register bit readout .....                                  | 81  |
| Tab. 9.  | Regulatory information .....  | 13 | Tab. 44. | CONFIG7 parameter ranges .....                                      | 81  |
| Tab. 10. | Power management electrical<br>characteristics .....                    | 14 | Tab. 45. | OT_TH register bit readout .....                                    | 82  |
| Tab. 11. | Low-voltage digital I/O electrical<br>characteristics .....             | 16 | Tab. 46. | OTW_TH (IGBT overtemperature warning<br>threshold register) .....   | 82  |
| Tab. 12. | SPI timing .....  | 17 | Tab. 47. | STATUS1 register bit readout .....                                  | 83  |
| Tab. 13. | FSISO pin electrical characteristics .....                              | 18 | Tab. 48. | STATUS1 register description .....                                  | 83  |
| Tab. 14. | Gate drive output stage electrical<br>characteristics .....             | 18 | Tab. 49. | MSK1 register bit readout .....                                     | 83  |
| Tab. 15. | Short-circuit and overcurrent fault electrical<br>characteristics ..... | 21 | Tab. 50. | MSK1 register description .....                                     | 83  |
| Tab. 16. | Desaturation fault management .....                                     | 23 | Tab. 51. | RMSK1 register bit readout .....                                    | 84  |
| Tab. 17. | Active VCE clamping electrical<br>characteristics .....                 | 24 | Tab. 52. | STATUS2 register bit readout .....                                  | 85  |
| Tab. 18. | Power device overtemperature electrical<br>characteristics .....        | 25 | Tab. 53. | STATUS2 register description .....                                  | 85  |
| Tab. 19. | IC overtemperature electrical<br>characteristics .....                  | 25 | Tab. 54. | MSK2 register bit readout .....                                     | 85  |
| Tab. 20. | AMUX and ADC electrical characteristics .....                           | 26 | Tab. 55. | MSK2 register description .....                                     | 85  |
| Tab. 21. | LV/HV domain communications .....                                       | 26 | Tab. 56. | RMSK2 register bit readout .....                                    | 86  |
| Tab. 22. | Power supplies and their functions .....                                | 31 | Tab. 57. | STATUS3 register .....  | 87  |
| Tab. 23. | Recommended external capacitors .....                                   | 32 | Tab. 58. | STATUS3 register description .....                                  | 87  |
| Tab. 24. | INTA configuration options .....  | 63 | Tab. 59. | CONFIGAOUT register bit readout .....                               | 88  |
| Tab. 25. | SPI registers .....   | 74 | Tab. 60. | CONFIGAOUT bit description .....                                    | 88  |
| Tab. 26. | MODE1 register bit readout .....  | 74 | Tab. 61. | CONFIGAOUT parametric ranges .....                                  | 89  |
| Tab. 27. | MODE1 register description .....  | 75 | Tab. 62. | REQADC request and response bit readout .....                       | 89  |
| Tab. 28. | Mode2 register bit readout .....  | 75 | Tab. 63. | REQADC request selections .....                                     | 89  |
| Tab. 29. | Mode2 register description .....  | 75 | Tab. 64. | REQBIST request and response bit<br>readout .....                   | 90  |
| Tab. 30. | CONFIG1 register bit readout .....                                      | 76 | Tab. 65. | REQBIST bit descriptions .....                                      | 90  |
| Tab. 31. | CONFIG1 bit description .....   | 76 | Tab. 66. | ID register bit readout .....                                       | 90  |
| Tab. 32. | CONFIG1 parameter ranges .....  | 76 | Tab. 67. | ID bit description .....  | 90  |
| Tab. 33. | CONFIG2 register bit readout .....                                      | 77 | Tab. 68. | SPI and LV/HV domain communication<br>error management .....        | 92  |
| Tab. 34. | CONFIG3 register bit readout .....                                      | 78 | Tab. 69. | GD3160 fault response and mask settings .....                       | 99  |
| Tab. 35. | CONFIG3 bit descriptions .....  | 78 | Tab. 70. | G3160 control priority: Normal, Fault, and<br>Fail-safe modes ..... | 101 |
|          |   |    | Tab. 71. | GD3160 fault priority and responses .....                           | 102 |
|          |   |    | Tab. 72. | Package outline .....   | 104 |
|          |   |    | Tab. 73. | Revision history .....  | 108 |

## Figures

|          |  |    |          |   |    |
|----------|--|----|----------|---|----|
| Fig. 1.  | Simplified application diagram .....                             | 3  | Fig. 19. | Overcurrent fault timing (OCM = 0, SSD = 1) .....   | 51 |
| Fig. 2.  | Internal block diagram .....                                     | 6  | Fig. 20. | Desaturation fault detection block .....  | 52 |
| Fig. 3.  | Pinout diagram .....   | 7  | Fig. 21. | DESAT fault timing (2LTO = 0, SSD = 1), RTMON_CFG = 1 .....   | 53 |
| Fig. 4.  | Main domain operating modes .....                                | 30 | Fig. 22. | DESAT fault timing (2LTO = 1, SSD = 1), RTMON_CFG = 1 .....   | 54 |
| Fig. 5.  | Definitions of over and undervoltage hysteresis .....            | 33 | Fig. 23. | DESAT fault timing (2LTO = 1, SSD = 1), RTMON_CFG = 0 .....   | 55 |
| Fig. 6.  | Power supply sequencing at power up, low-voltage domain .....    | 34 | Fig. 24. | VCE active clamping timing .....  | 57 |
| Fig. 7.  | Power supply sequencing at power down, low-voltage domain .....  | 35 | Fig. 25. | Segmented drive detection circuitry .....   | 58 |
| Fig. 8.  | Power supply sequencing at power-up, high-voltage domain .....   | 36 | Fig. 26. | Segmented drive timing .....  | 59 |
| Fig. 9.  | Power supply sequencing at power-down, high-voltage domain ..... | 37 | Fig. 27. | AOUT % duty cycle vs. ADC value .....   | 61 |
| Fig. 10. | HV domain power supplies, regulation, and monitoring .....       | 38 | Fig. 28. | AOUT signal with interleaved pattern .....  | 61 |
| Fig. 11. | Control and status reporting I/O .....                           | 40 | Fig. 29. | Low voltage domain monitoring of IGBT's VGE, RTMON_CFG = 0 (Vge state monitored at the AMC pin) ..... | 62 |
| Fig. 12. | FSEN and FSSTATE filtering when entering a Fail-safe state ..... | 42 | Fig. 30. | INTA as a real-time VCE reporter .....  | 64 |
| Fig. 13. | FSEN and FSSTATE filtering when exiting a fail-safe state .....  | 43 | Fig. 31. | INTA as a real-time VGE reporter .....  | 65 |
| Fig. 14. | PWM and PWMALT with deadtime enforcement .....                   | 44 | Fig. 32. | Overtemperature monitoring circuitry .....  | 66 |
| Fig. 15. | Gate drive output stage block diagram .....                      | 45 | Fig. 33. | GD3160 overtemperature block diagram .....  | 67 |
| Fig. 16. | Active Miller clamp operation .....                              | 47 | Fig. 34. | AMUX and ADC block diagram .....  | 68 |
| Fig. 17. | Short-circuit and overcurrent detection block diagram .....      | 49 | Fig. 35. | SPI timing .....  | 70 |
| Fig. 18. | Short-circuit fault timing (2LTO = 1, SSD = 1) .....             | 50 | Fig. 36. | Single-device SPI message breakdown .....   | 71 |
|          |  |    | Fig. 37. | CRC Polynomial .....  | 71 |
|          |  |    | Fig. 38. | Daisy chain connection .....  | 73 |
|          |  |    | Fig. 39. | Daisy chain data transmission .....   | 73 |
|          |  |    | Fig. 40. | Successfully completed BIST sequence .....  | 93 |
|          |  |    | Fig. 41. | BIST sequence with failure .....  | 94 |

## Contents

|           |   |           |          |  |    |
|-----------|---|-----------|----------|--|----|
| <b>1</b>  | <b>General description</b>  | <b>1</b>  | 11.2.4   | SPI pins (CSB, SCLK, MOSI, MISO)                     | 44 |
| <b>2</b>  | <b>Features and benefits</b>  | <b>2</b>  | 11.2.5   | PWM and PWMALT pins                                  | 44 |
| 2.1       | Key features  | 2         | 11.3     | Gate drive output stage and diagnostics              | 45 |
| 2.2       | Safety features   | 2         | 11.3.1   | Introduction   | 45 |
| 2.3       | Safety and regulatory approvals   | 2         | 11.3.2   | Functional block diagram                             | 45 |
| <b>3</b>  | <b>Simplified application diagram</b>   | <b>3</b>  | 11.3.3   | Types of gate drive                                  | 46 |
| <b>4</b>  | <b>Applications</b>   | <b>4</b>  | 11.3.3.1 | Normal mode turn on and turn off                     | 46 |
| <b>5</b>  | <b>Ordering information</b>   | <b>5</b>  | 11.3.3.2 | Soft shutdown  | 46 |
| <b>6</b>  | <b>Internal block diagram</b>   | <b>6</b>  | 11.3.3.3 | Two-level turn-off                                   | 46 |
| <b>7</b>  | <b>Pinning information</b>  | <b>7</b>  | 11.3.3.4 | Active Miller clamp and holdoff                      | 47 |
| 7.1       | Pinning   | 7         | 11.4     | Current sense protection                             | 48 |
| 7.2       | Pin description   | 7         | 11.4.1   | Introduction   | 48 |
| <b>8</b>  | <b>Product characteristics</b>  | <b>9</b>  | 11.4.2   | Short-circuit fault management via the<br>ISENSE pin | 48 |
| 8.1       | Range of functionality  | 9         | 11.4.3   | Overcurrent fault management with the<br>ISENSE pin  | 50 |
| 8.2       | Absolute maximum ratings  | 9         | 11.5     | Desaturation fault protection                        | 51 |
| 8.3       | Thermal characteristics   | 11        | 11.5.1   | Introduction   | 51 |
| 8.4       | Isolation and safety related specifications   | 12        | 11.5.2   | Features   | 51 |
| <b>9</b>  | <b>Electrical characteristics</b>   | <b>14</b> | 11.5.3   | Protection and diagnostic features                   | 52 |
| 9.1       | Power management  | 14        | 11.6     | VCE overvoltage protection                           | 55 |
| 9.2       | Digital inputs and outputs  | 15        | 11.6.1   | Introduction   | 55 |
| 9.3       | Gate drive outputs  | 18        | 11.6.2   | VCE advanced active clamp                            | 56 |
| 9.4       | Current sense protection  | 21        | 11.6.3   | Segmented drive operation                            | 58 |
| 9.5       | Desaturation protection   | 23        | 11.7     | Fault status and analog reporting                    | 60 |
| 9.6       | VCE overvoltage protection  | 24        | 11.7.1   | Introduction   | 60 |
| 9.7       | Power device overtemperature  | 25        | 11.7.2   | INTB pin   | 60 |
| 9.8       | IC overtemperature  | 25        | 11.7.3   | AOUT pin   | 61 |
| 9.9       | AMUX and ADC electrical characteristics   | 26        | 11.8     | VGE real-time monitoring (RTMON)                     | 62 |
| 9.10      | LV/HV domain communications   | 26        | 11.9     | INTA fault reporting and real-time reporting         | 63 |
| <b>10</b> | <b>Functional description</b>   | <b>28</b> | 11.9.1   | INTA overview  | 63 |
| 10.1      | Device overview   | 28        | 11.9.2   | INTA fault reporting                                 | 63 |
| 10.2      | State diagram   | 30        | 11.9.3   | INTA real-time VCE reporting                         | 63 |
| 10.2.1    | Main domain state diagram   | 30        | 11.9.4   | INTA real-time VGE reporting                         | 64 |
| <b>11</b> | <b>Functional block operation</b>   | <b>31</b> | 11.10    | Power device overtemperature detection<br>circuitry  | 65 |
| 11.1      | Power management  | 31        | 11.10.1  | Introduction   | 65 |
| 11.1.1    | Introduction  | 31        | 11.10.2  | Features   | 65 |
| 11.1.2    | Power sources and regulators  | 31        | 11.11    | Overtemperature detection of the GD3160              | 66 |
| 11.1.3    | Recommended external capacitance  | 32        | 11.11.1  | Introduction   | 66 |
| 11.1.4    | OV and UV threshold description   | 33        | 11.11.2  | Features   | 67 |
| 11.1.5    | Power supply sequencing of the low-<br>voltage domain   | 33        | 11.12    | AMUX and analog-to-digital converter                 | 68 |
| 11.1.6    | Power supply sequencing of the high-<br>voltage domain  | 35        | 11.12.1  | Introduction   | 68 |
| 11.1.7    | Fault management at power up  | 37        | 11.12.2  | AMUX and ADC features                                | 68 |
| 11.1.8    | High-voltage domain supplies and monitors   | 38        | 11.13    | 24-bit serial peripheral interface                   | 69 |
| 11.2      | Digital I/Os for control and configuration  | 39        | 11.13.1  | Introduction   | 69 |
| 11.2.1    | Introduction  | 39        | 11.13.2  | SPI CRC  | 71 |
| 11.2.2    | Functional block diagram  | 39        | 11.13.3  | Protection of register configuration                 | 71 |
| 11.2.3    | Safing logic pins   | 41        | 11.13.4  | Clearing fault bits                                  | 72 |
| 11.2.3.1  | FSENb and FSSTATE pins  | 41        | 11.13.5  | Daisy chain operation                                | 72 |
| 11.2.3.2  | FSISO pin - Gate ON (MGD3160AM515EK,<br>MGD3160AM518EK, MGD3160AM315EK,<br>or MGD3160AM318EK)         | 43        | 11.14    | SPI registers  | 74 |
| 11.2.3.3  | FSISO pin - Gate 3-state<br>(MGD3160AM535EK, MGD3160AM538EK,<br>MGD3160AM335EK, or<br>MGD3160AM338EK) | 43        | 11.14.1  | MODE1 register (ADDR = 0x00)                         | 74 |
|           |   |           | 11.14.2  | MODE2 register (ADDR = 0x01)                         | 75 |
|           |   |           | 11.14.3  | CONFIG1 register (ADDR = 0x02)                       | 76 |
|           |   |           | 11.14.4  | CONFIG2 register (ADDR = 0x03)                       | 77 |
|           |   |           | 11.14.5  | CONFIG3 register (ADDR = 0x04)                       | 78 |

|           |   |            |
|-----------|---|------------|
| 11.14.6   | CONFIG4 register (ADDR = 0x05) .....                              | 78         |
| 11.14.7   | CONFIG5 register (ADDR = 0x06) .....                              | 79         |
| 11.14.8   | CONFIG6 register (ADDR = 0x07) .....                              | 80         |
| 11.14.9   | CONFIG7 register (ADDR = 0x08) .....                              | 81         |
| 11.14.10  | OT_TH register (ADDR = 0x09) .....                                | 82         |
| 11.14.11  | OTW_TH register (ADDR = 0x0A) .....                               | 82         |
| 11.14.12  | STATUS1 register (ADDR = 0x0B) .....                              | 82         |
| 11.14.13  | MSK1 register (ADDR = 0x0C) .....                                 | 83         |
| 11.14.14  | RMSK1 register (ADDR = 0x0D) .....                                | 84         |
| 11.14.15  | STATUS2 register (ADDR = 0x0E) .....                              | 84         |
| 11.14.16  | MSK2 register (ADDR = 0x0F) .....                                 | 85         |
| 11.14.17  | RMSK2 register (ADDR = 0x10) .....                                | 86         |
| 11.14.18  | STATUS3 register (ADDR = 0x11) .....                              | 87         |
| 11.14.19  | CONFIGAOUT register (ADDR = 0x12) .....                           | 88         |
| 11.14.20  | ADC request and response (ADDR = 0x13) ....                       | 89         |
| 11.14.21  | BIST request and response (ADDR = 0x14) ....                      | 89         |
| 11.14.22  | Device ID (ADDR = 0x15) .....                                     | 90         |
| 11.15     | Low-voltage domain to high-voltage domain<br>communications ..... | 91         |
| 11.15.1   | Introduction .....  | 91         |
| 11.15.2   | Overview of low-voltage (LV)<br>communications .....              | 91         |
| 11.15.3   | Overview of high-voltage (HV)<br>communications .....             | 91         |
| 11.15.4   | Managing LV/HV domain communication<br>errors .....               | 92         |
| 11.16     | Built-in self-test .....  | 93         |
| 11.16.1   | BIST overview .....   | 93         |
| 11.16.2   | BIST process .....  | 94         |
| 11.16.3   | Configure VEE_OORM before running<br>BIST .....                   | 95         |
| <b>12</b> | <b>Operation .....</b>  | <b>96</b>  |
| 12.1      | GD3160 power-up sequence .....                                    | 96         |
| 12.2      | Perform BIST upon initialization .....                            | 97         |
| 12.3      | Default functionality .....                                       | 98         |
| 12.3.1    | Default configuration .....                                       | 98         |
| 12.3.2    | Default protections .....   | 98         |
| 12.3.3    | Default mask settings .....                                       | 99         |
| 12.4      | Register initialization in CONFIG mode .....                      | 99         |
| 12.5      | Summary of faults and GD3160 responses ....                       | 99         |
| 12.6      | Fail-safe transitions .....                                       | 101        |
| <b>13</b> | <b>Packaging .....</b>  | <b>104</b> |
| 13.1      | Package mechanical dimensions .....                               | 104        |
| <b>14</b> | <b>Revision history .....</b>                                     | <b>108</b> |
|           | <b>Legal information .....</b>                                    | <b>109</b> |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.