# GigaDevice Semiconductor Inc.

# GD30BC2502x
# Multi-Cell Battery Charger

Datasheet

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# 3 General description

The GD30BC2502x is a highly integrated low quiescent current switching battery charger control IC for 2/3/5 series cell Li-ion battery packs. It drives an external N-MOSFET that can output a charge current up to 5A through a sensing resistor and has a very high efficiency up to 90%. The battery voltage is regulated to very high precision (less than +/- 1%). The device operates with wide input range up to 32V. It has peak-current-mode control for fast loop response and easy compensation.

Two control loops, constant current (CC) and constant voltage (CV) are implemented in the GD30BC2502x. The constant current is programmable up to 5A and regulated using a sense resistor. The constant voltage is precisely regulated internally.

The device includes multiple protection features such as cycle-by-cycle current limiting, under voltage lockout and thermal shutdown. Other protection features include battery temperature monitoring and protection, charge status indication and internal timer to stop the charging cycle.

The GD30BC2502x has a small footprint of QFN16 (4mmx4mm) and requires a minimal number of external components allowing for it to best used in clean robots, drones or any 2/3/5 cell Li-ion battery chargers.

# 4 Device overview

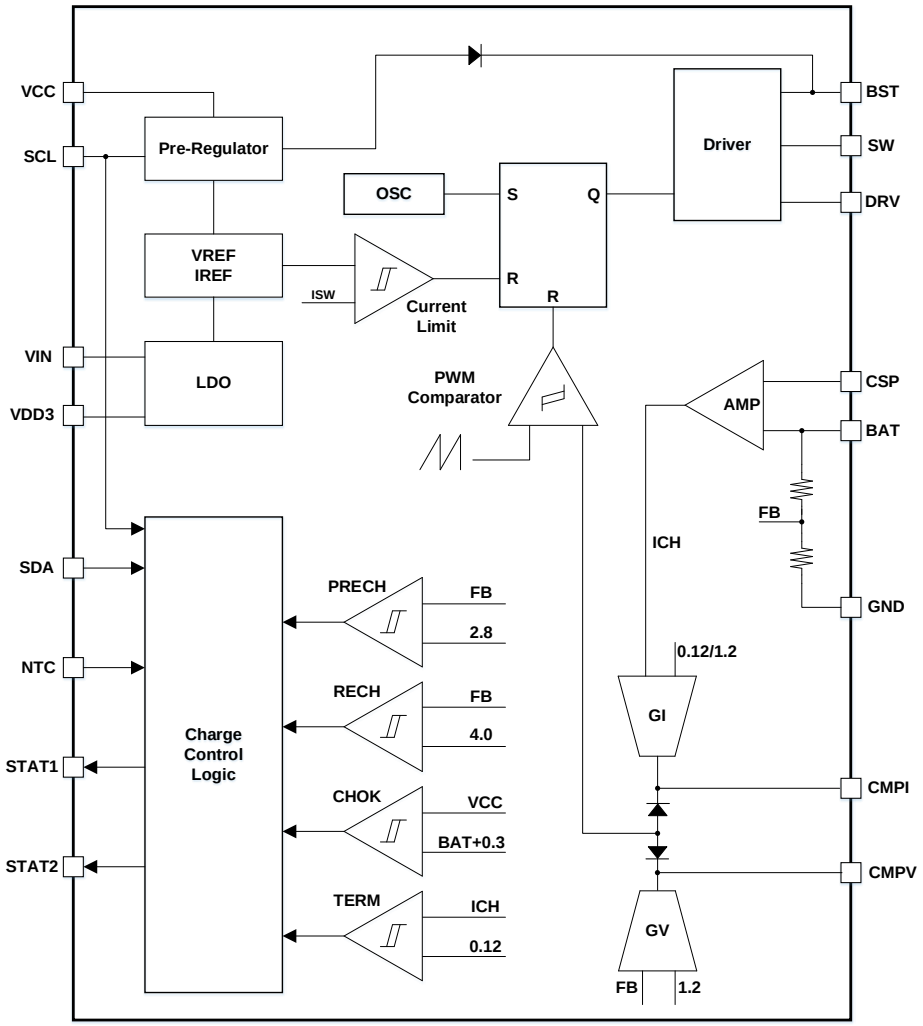
## 4.1 Device information

**Table 4-1 Device information for GD30BC2502x**

| Part Number | Package | Function | Description |
|---|---|---|---|
| GD30BC2502x | QFN16(4X4) | With I²C Interface | Cooperate with MCU solution, 2/3/5 cells |

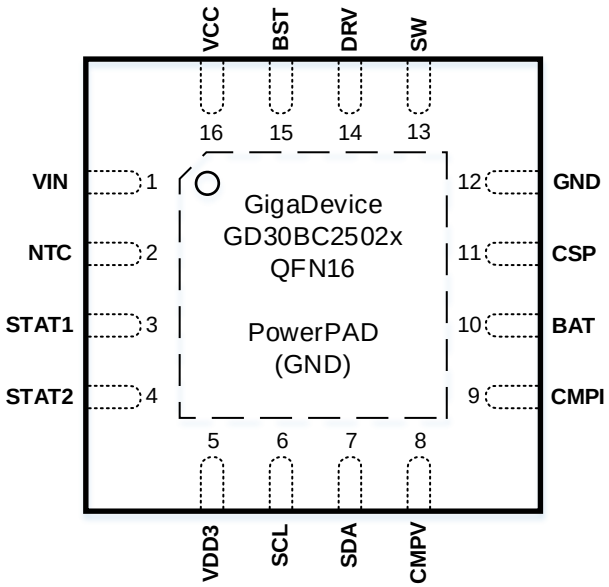
## 4.2 Block diagram

**Figure 4-1 Block diagram for GD30BC2502x**



## 4.3 Pinout and pin assignment

**Figure 4-2 GD30BC2502x QFN16 pinouts**




## 4.4 Pin definitions

**Table 4-2 GD30BC2502x pin definitions**

| Pin Name | Pins | Pin Type | Functions description |
|---|---|---|---|
| VIN | 1 | P | Input voltage, bypass to ground with a 4.7uF capacitor. |
| NTC | 2 | I | Thermistor terminal voltage for battery. |
| STAT1 | 3 | OD | Open drain charging status indication 1. |
| STAT2 | 4 | OD | Open drain charging status indication 2. |
| VDD3 | 5 | O | 3.3V LDO output, connect a 1uF capacitor to ground. |
| SCL | 6 | I/O | SCL for I2C communication. |
| SDA | 7 | I/O | SDA for I2C communication. |
| CMPV | 8 | O | Compensation for constant voltage charge control. |
| CMPI | 9 | O | Compensation for constant current charge control. |
| BAT | 10 | I | Connect to positive battery node for voltage/current sensing. |
| CSP | 11 | I/O | Connect to sensor resistor as current sense positive input. |
| GND | 12 | G | Ground. |
| SW | 13 | O | Switching node, connecting to CSP by an inductor. |
| DRV | 14 | P | Drive the gate of the external N-MOSFET. |

| Pin Name | Pins | Pin Type | Functions description |
|---|---|---|---|
| BST | 15 | P | Bootstrap voltage, connect to SW with a 0.1uF capacitor. |
| VCC | 16 | P | Supply voltage, connect a capacitor to ground; could connect to VIN with diode. |
| PGND | EPAD | G | Device power ground. |

**Notes:**

1. Type: I = input, O = output, I/O = input or output, P = power, G = Ground, OD = Open Drain.

# 5 Functional description

## 5.1 Operation

When power is ready ($V_{CC}$/ $V_{IN}$ above the UVLO threshold and $V_{CC}$-$V_{BAT}$ > 0.3V), the GD30BC2502x pulls the DRV high to turn on the external N-MOSFET, connecting SW and inductor to power supply and begins the charging process. If $V_{CC}$/ $V_{IN}$ is above UVLO, but $V_{CC}$-$V_{BAT}$ is less than 0.3V, the IC enters sleep mode.

As the inductor current increases and reaches the current limit, the RS flip-flop resets the driver and DRV is pulled low and the external N-MOSFET is turned off. An external Schottky diode then conducts the inductor current.

Depending on the BAT voltage, the IC enters different charging status respectively: pre-charge, constant current charge and constant voltage charge. Pre-charge and constant current charge share one current control loop which is compensated with an external RC network at CMPI. A constant voltage charge control takes over when the battery voltage is charged up to the reference voltage. It also requires a compensation circuit at CMPV. The normal charge process will be stopped if the charge current falls below an internally-set current level ($I_{TER}$) during constant voltage charge.

The charging process will be terminated if a fault condition is triggered. The fault conditions include: battery under/over temperature; supply under voltage lockout; battery over charge; thermal shutdown; charging timer out.

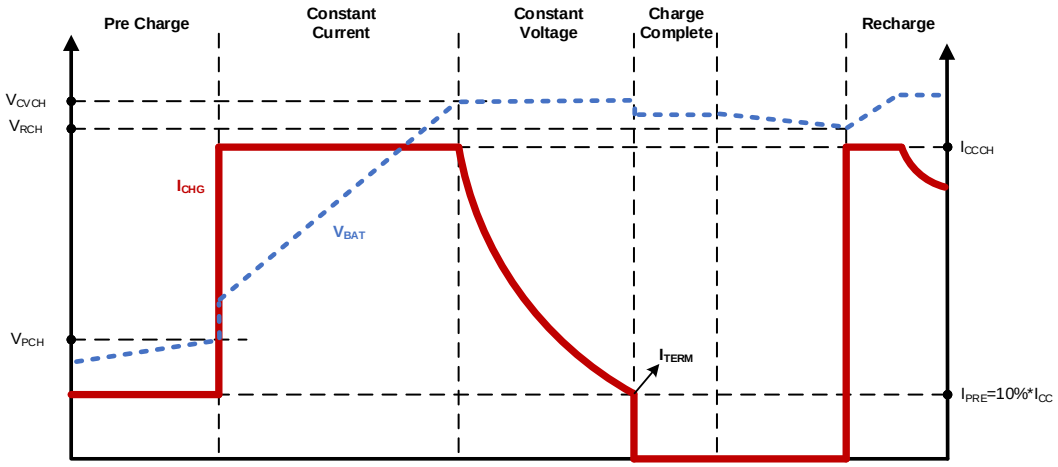
## 5.2 Charging Control

### 5.2.1 Charge cycle

The GD30BC2502x is a switching charger that allows the battery to be charged with a programmable charge current up to 5A. The regulation voltage can be programmed to 8.4V(2-cell)/12.6V (3-cell) /21V (5-cell) through I2C interface. A complete charge cycle shown in Figure 5-1 is implemented in the device.

When $V_{BAT}$ is lower than $V_{PCH}$, charge starts from pre-charge. Pre-charge current $I_{PCH}$ is set to the 1/10 of the current $I_{CCCH}$ which is determined by the sense resistor $R_{SEN}$. After $V_{BAT}$ is charged to be above $V_{PCH}$, a constant current control loop takes over and the charging current is set to $I_{CCCH}$. Constant current charge lasts until $V_{BAT}$ reaches the regulated voltage $V_{CVCH}$. By then a constant voltage control takes over and the charge current gradually decreases while the output voltage is fixed at $V_{CVCH}$. The charge process stops when the charge current is reduced to a termination current $I_{TER}$, which is set to equal to $I_{PCH}$ in the device. When the battery voltage drops to $V_{RCH}$, the whole charge process will resume.

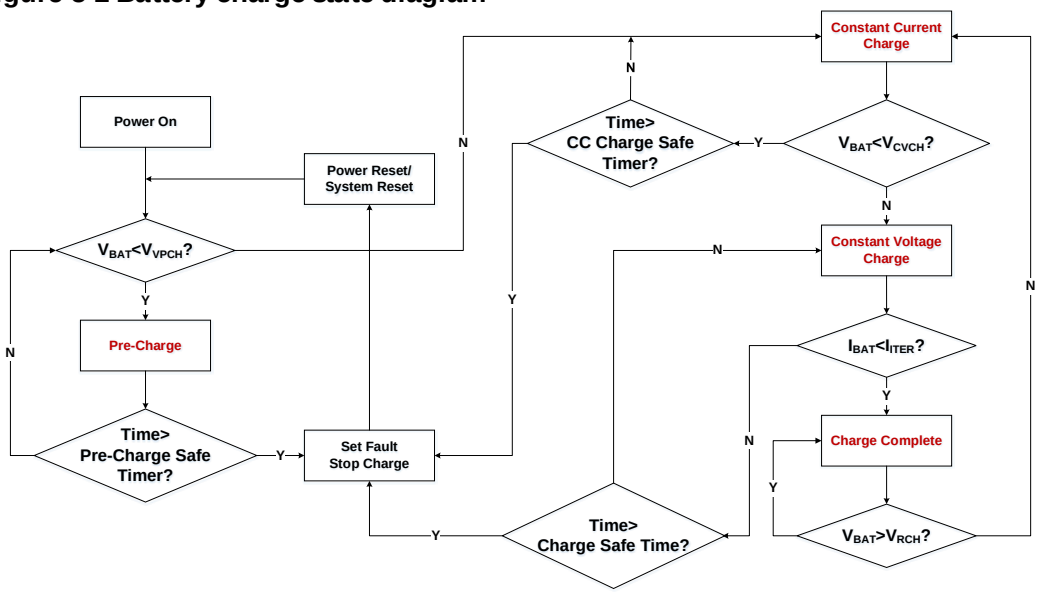
**Figure 5-1 Battery charge cycle**




## 5.2.2 Charge state diagram

The normal charge state diagram is shown in Figure 5-2. The fault conditions besides timer out include thermal shutdown, battery temperature through NTC monitoring, and supply under voltage lockout. All fault conditions are always monitored in the charging process. Any fault will halt the charging process and can only be reset by power-on.

**Figure 5-2 Battery charge state diagram**




## 5.2.3 Charge parameters

The maximum charge current through the external N-MOSFET is programmed by a sense resistor connected from the CSP to BAT. The resistor value and the maximum current are related by:

$$R_{SEN} \times I_{CCCH} = 200\ mV$$

Where $I_{CCCH}$ is the targeted maximum charge current in A and $R_{SEN}$ is the sense resistor. And the pre-charge current and termination charge current is determined internally by:

$$I_{PCH} = I_{TER} = \frac{1}{10} I_{CCCH}$$

## 5.3 LDO 3.3V

The GD30BC2502x has an internal 3.3V LDO VDD3 to power the internal circuitry. VDD3 can also provide up to 3.3V/ 25mA current for external circuitry. Connect a 1uF bypass capacitor from VDD3 to GND to ensure stability.

## 5.4 NTC battery temperature

A built-in NTC resistance window comparator that allows the GD30BC2502x to sense the battery temperature through the thermistor included in the battery pack. Connect a resistor with an appropriate value from VDD3 to NTC and connect the thermistor from NTC to GND. A resistor divider determines the voltage on NTC as a function of the battery temperature. Charging will stop or resume when the voltage is within or out of the NTC window.

## 5.5 STAT1/STAT2

STAT1/STAT2 are two open-drain status output which are used to indicate the charging status. Table 5-1 shows the charging status indications.

**Table 5-1 LED state for GD30BC2502x**

| STAT1 | STAT2 | Charging Indication |
|---|---|---|
| LOW | LOW | In Charging |
| LOW | HIGH | End of Charge, or NTC Fault, or Timer Out, or Thermal Shutdown |
| HIGH | HIGH | VCC-VBAT < 0.3V, or VIN < UVLO, or VBAT < 4.8V |

## 5.6 Thermal shutdown

If the die temperature exceeds the trip point of the thermal shutdown limit ($T_{SD}$), the charge process will be terminated and the external N-MOSFET are disabled. The fault condition will be shown in STAT1/STAT2. The charging cycle will be resumed when the die temperature is reduced below the thermal shutdown limit (with a hysteresis).

## 5.7 Recommended device selection

### 5.7.1 Inductor selection

During normal operation, the transient inductor current changes periodically. During the turn-on period of the N-MOS field effect transistor, the input voltage charges the inductor and the inductor current increases; during the turn-off period of the N-MOS field effect transistor, the inductor discharges to the battery and the inductor current decreases. The ripple current of the inductor increases with the decrease of the inductance value and increases with the increase of the input voltage. Larger inductor ripple current will cause larger ripple charging current and magnetic loss. Therefore, the ripple current of the inductor should be limited within a reasonable range. The inductor value can be calculated:

$$L = \frac{V_{BAT}}{f_{sw} \times I_{PP}} \times \left(1 - \frac{V_{BAT}}{V_{IN(MAX)}}\right)$$

Where

- $f_{SW}$ is the switching frequency, fixed value $f_{SW}$ = 500kHz, unit KHz.
- $I_{PP}$ is the maximum ripple current, unit A.
- $V_{IN}$ is the maximum input voltage, unit V.
- $V_{BAT}$ is the battery voltage, unit V.

When selecting the inductor value, the inductor ripple current can be limited to 40 percent of charging current. For the selection of inductor value when VIN = 24V, VBAT = 12V, refer to Table 5-2.

**Table 5-2 Inductor recommended selection**

| Charging Current | Inductor value |
|---|---|
| 1A | 36uH |
| 2A | 27uH |
| 3A | 20uH |
| 4A | 15uH |
| 5A | 12uH |

### 5.7.2 Input VCC capacitor selection

With the increase of charging current, the input current fluctuation of power supply is also increasing. In order to ensure the stability of VCC power supply, the capacitance of VCC filter capacitor also needs to be increased. For the selection of capacitor value when VIN = 24V, VBAT = 12V, refer to Table 5-3.

**Table 5-3 VCC capacitor recommended selection**

| Charging Current | Capacitor selection |
|---|---|
| 1A | 4.7uF |
| 2A | 10uF |

| | |
|---|---|
| 3A | 22uF |
| 4A | 33uF |
| 5A | 47uF |

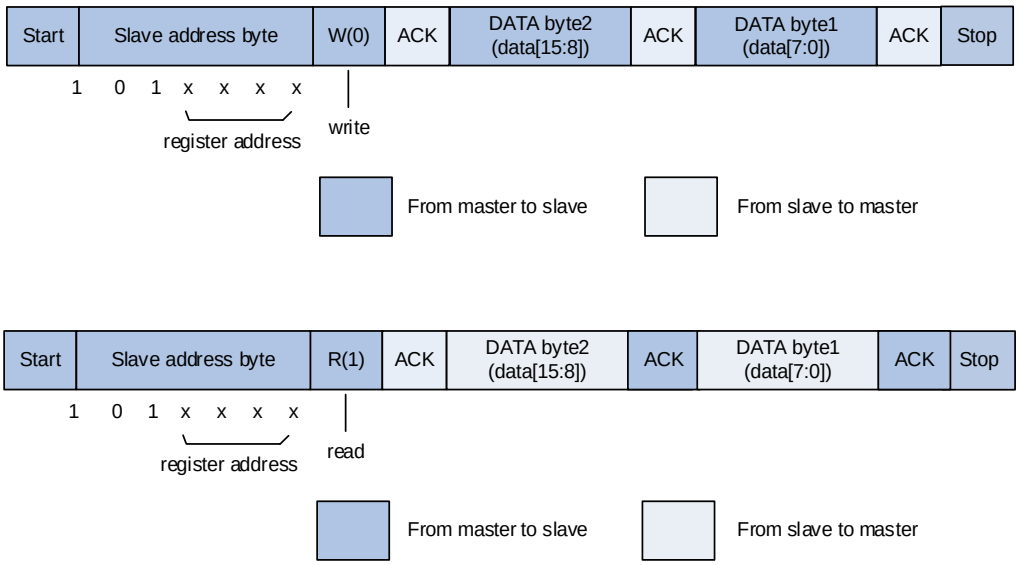
## 5.8 I2C interface

I2C interface is included only in GD30BC2502x.

The I2C (inter-integrated circuit) module provides an I2C interface which is an industry standard two-line serial interface for MCU to communicate with external I2C interface. I2C bus uses two serial lines: a serial data line, SDA, and a serial clock line, SCL.

The I2C interface implements standard I2C protocol with standard-mode (up to 100 kHz) and fast-mode (up to 400 kHz). The I2C interface only supports Slave-mode. The I2C interface receive data on rising SCL and transmit data on falling SCL.

**Figure 5-3 I2C communication flow**




The data format is fixed:

8bit function (3'b101 + 4bit(register address), +1bit(1'b0-write, 1'b1-read))

+ 8bit data[15:8]

+8bit data[7:0].

## 5.9 Register Map

### 5.9.1 Fault Register

Address：0b 0000

| Bits | R/W | fields | default | Description |
|---|---|---|---|---|
| 15:7 | R | Reserved | 0b0 | Must be kept at reset value. |

| Bits | R/W | fields | default | Description |
|---|---|---|---|---|
| 6 | R | VBAT_OV _FAULT | 0b0 | VBAT overvoltage fault event indicator.<br>0: normal<br>1: VBAT over voltage fault is detected |
| 5 | R | TO_FAULT | 0b0 | Full charge TIME_OUT fault event indicator. (Can be Cleared by writing control register ENB_REG = 0).<br>0: normal<br>1: Time out fault is detected |
| 4 | R | TO_PCH_FAULT | 0b0 | Pre-charge TIME OUT. (Can be Cleared by writing control register ENB_REG = 0).<br>0: normal<br>1: Pre-charge time out fault is detected |
| 3 | R | Reserved | 0b0 | Must be kept at reset value. |
| 2 | R | NTC_HOT_FAULT | 0b0 | NTC high temperature fault event indicator.<br>0: normal<br>1: NTC high temperature fault is detected |
| 1 | R | NTC_COLD_FAULT | 0b0 | NTC low temperature fault event indicator.<br>0: normal<br>1: NTC low temperature fault is detected |
| 0 | R | TEMP_FAULT | 0b0 | Battery over temperature fault event indicator.<br>0: normal<br>1: Over temperature fault is detected |

### 5.9.2 Control Register

Address：0b 0001

| Bits | R/W | fields | default | Description |
|---|---|---|---|---|
| 15:14 | RW | CELLSEL_CF | 0b0 | Battery cell count selection configuration.<br>10: 2 Cell Li-ion Batteries<br>00: 3 Cell Li-ion Batteries(Default)<br>01: 5 Cell Li-ion Batteries<br>1x: Reserved |
| 13:12 | RW | ACOKSEL | 0b0 | The minimum difference between VCC and VBAT during charging.<br>00: 300mV<br>01: 600mV<br>10: 1.2V<br>11: 2.4V |
| 11:8 | R | Reserved | 0b0 | Must be kept at reset value. |
| 7 | RW | ENB_REG | 0b1 | IC enable configuration register.<br>0: Sleep mode<br>1: Normal working mode |
| 6 | RW | RST_ALL | 0b0 | Reset all registers to default values. |

| Bits | R/W | fields | default | Description |
|---|---|---|---|---|
| | | | | 0: No effect<br>1: Reset all chip |
| 5 | RW | RST_OTHS | 0b0 | Reset registers to default values except I2C.<br>0: No effect<br>1: Reset all chip but I2C itself |
| 4 | R | Reserved | 0b0 | Must be kept at reset value. |
| 3:2 | RW | TIMEOUT_SEL | 0b0 | Charge status timeout time select.<br>00: 30min(Pre-charge)/ 180min(All time)<br>01: 20min(Pre-charge)/ 120min(All time)<br>10: 40min(Pre-charge)/ 240min(All time)<br>11: 30min(Pre-charge)/ 180min(All time) |
| 1:0 | RW | VBATREG_CF | 0b0 | Constant current charge terminate voltage configuration.<br>00: 4.2V<br>01: 4.1V<br>10: 4.3V<br>11: 4.35V |

### 5.9.3 User configure Register

Address：0b 0011

| Bits | R/W | fields | default | Description |
|---|---|---|---|---|
| 15 | RW | VBATREG_EN | 0b0 | VBATREG calibration signal enable.<br>0: VBATREG_CF disable<br>1: VBATREG_CF enable |
| 14 | RW | CELLSEL_EN | 0b0 | Cellsel enable.<br>0: CELLSEL_CF disable<br>1: CELLSEL_CF enable |
| 13:0 | R | Reserved | 0b0 | Must be kept at reset value. |

# 6 Electrical characteristics

## 6.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 6-1 Absolute maximum ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Power supply from adaptor (VIN, VCC) | -0.3 | 40 | V |
| $V_{BAT}$ | Battery voltage (BAT) | -0.3 | 40 | V |
| $V_{CSP}$ | Current sense voltage | -0.3 | 40 | V |
| $V_{DRV}$ | Drive node to external N-MOSFET gate | -0.3 | 40 | V |
| $V_{VDD3}$ | LDO output voltage | -0.3 | 5 | V |
| $V_{BST}$ | Bootstrap voltage | -0.3 | 40 | V |
| $V_{SW}$ | Switching node voltage (SW) | -1 | 40 | V |
| $V_{IO}$ | I/O pin voltage (NTC, SCL, SDA, CMPI, CMPV) | -0.3 | 7 | V |
| $V_{STAT}$ | Open drain output STAT1, STAT2 | -0.3 | 40 | V |
| **Thermal characteristics** | | | | |
| $T_J$ | Operating junction temperature | -40 | 125 | °C |
| $T_{stg}$ | Storage temperature | -65 | 150 | °C |

## 6.2 Recommended operation conditions

**Table 6-2 Recommended operation conditions**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Power supply from adaptor (VIN, VCC) | 9 | 32 | V |
| $V_{BAT}$ | Battery voltage (BAT) | 5 | — | V |
| $V_{IO}$ | I/O pin voltage (NTC, SCL, SDA, CMPI, CMPV) | -0.3 | 5.5 | V |
| $V_{STAT}$ | Open drain output STAT1，STAT2 | -0.3 | 32 | V |
| **Thermal characteristics** | | | | |
| $T_A$ | Operating ambient temperature | -40 | 85 | °C |

## 6.3 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample.

**Table 6-3 Electrostatic Discharge characteristics**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $V_{ESD(HBM)}$ | human body model | $T_A$ = 25 °C; JS-001-2017 | ±1000 | V |
| $V_{ESD(CDM)}$ | charge device model | $T_A$ = 25 °C; JS-002-2018 | ±1000 | V |

## 6.4 Power supplies voltage and current

**Table 6-4 Power supplies voltages and currents**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_Q$ | Sleep mode quiescent current | $T_A$ = 25°C | — | — | 100 | µA |
| $I_{CC}$ | Operation current | $T_A$ = 25°C | — | 2 | — | mA |
| $t_{WAKE}$ | Turn-on time | $V_{USB}$ > $V_{UVLO}$ to outputs ready | 1 | — | — | ms |
| $V_{VDD3}$ | LDO regulator voltage | $I_{VDD3}$ = 0 to 30 mA | 3 | 3.3 | 3.6 | V |
| $V_{UVLO}$ | Under voltage lockout | $T_A$ = 25°C | — | 3.25 | — | V |
| $V_{CC}$-$V_{BAT}$ | — | VCC rise, ACOKSEL = 00 | — | 0.3 | — | V |
| $V_{CC}$-$V_{BAT}$ | hysteresis | VCC fall | — | 0.15 | — | V |

## 6.5 Logic input and open drain output characteristics

**Table 6-5 Logic input and open drain output characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input logic low voltage | — | 0 | — | 0.8 | V |
| $V_{IH}$ | Input logic high voltage | — | 1.5 | — | 5.5 | V |
| $V_{HYS}$ | Input logic hysteresis | — | 100 | — | — | mV |
| $I_{IL}$ | Input logic low current | $V_{IO}$ = 0 V | -5 | — | 5 | µA |
| $I_{IH}$ | Input logic high current | $V_{IO}$ = 3.3 V | — | — | 5 | µA |
| $R_{PD}$ | Pull down resistance | To GND | — | 1 | — | MΩ |
| $V_{OD}$ | Output logic low voltage | $I_{OD}$ = 10 mA | — | — | 0.1 | V |
| $I_{LK\_SDA}$ | SDA leakage | $V_{SDA}$ = 3.3 V | — | — | 2 | µA |
| $I_{LK\_STAT}$ | STAT1/2 leakage | $V_{STAT}$ = 32 V | — | — | 2 | µA |

## 6.6 Switching control characteristics

**Table 6-6 Linear charger characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CVCH}$ | Regulated battery voltage | Per cell (2-cell, x2;3-Cell,x3;5-Cell,x5) | 4.16 | 4.20 | 4.24 | V |
| $V_{PCH}$ | Pre-Charge to charge transition | Per cell (2-cell, x2;3-Cell,x3;5- | — | 3.0 | — | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | Cell,x5) | | | | |
| $V_{RCH}$ | Re-Charge threshold | Per cell (2-cell, x2;3-Cell,x3;5-Cell,x5) | — | 4.0 | — | V |
| | Re-Charge hysteresis | — | — | 2% | — | $V_{RCH}$ |
| $V_{SEN}$ | Current sense $V_{CSP}$ - $V_{BAT}$ | CC-CV charge | 180 | 200 | 220 | mV |
| | | Pre-charge | 18 | 20 | 22 | mV |
| $I_{CCCH}$ | Charge current | $R_{SEN}$=100mΩ | 1.80 | 2.00 | 2.20 | A |
| $I_{PCH}$ | Pre-Charge/Termination current | — | — | 10% | — | $I_{CCCH}$ |
| $I_{LK\_SW}$ | SW leakage current | $V_{SW}$=32V | — | — | 2 | μA |
| $f_{SW}$ | Switching frequency | — | 450 | 500 | 550 | KHz |
| $D_{MAX}$ | Maximum duty cycle | — | — | 95 | — | % |
| $V_{PU}$ | Pull up voltage | $V_{DRV}$ - $V_{SW}$ | 5.4 | 6 | 6.6 | V |
| $T_R$ | Pull up rise time | $C_L$ = 2nF, $V_{DRV}$ from 10% to 90% | — | 40 | — | ns |
| $T_F$ | Pull down fall time | $C_L$ = 2nF, $V_{DRV}$ from 90% to 10% | — | 40 | — | ns |

## 6.7 NTC characteristics and thermal protection

**Table 6-7 NTC characteristics and thermal protection**

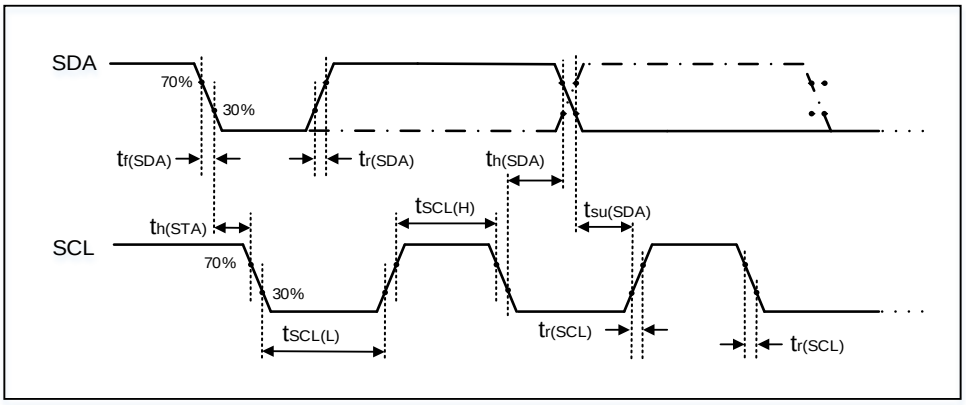
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{TL}$ | NTC low-temp rising threshold | As percentage of VDD3 | 64 | 65 | 66 | % |
| $V_{TH}$ | NTC high-temp falling threshold | As percentage of VDD3 | 34 | 35 | 36 | % |
| $T_{SD}$ | Thermal shutdown temperature | — | — | 150 | — | ℃ |
| $T_{SDHYS}$ | Thermal shutdown hysteresis | — | — | 25 | — | ℃ |

## 6.8 I2C characteristics

**Table 6-8 I2C characteristics**

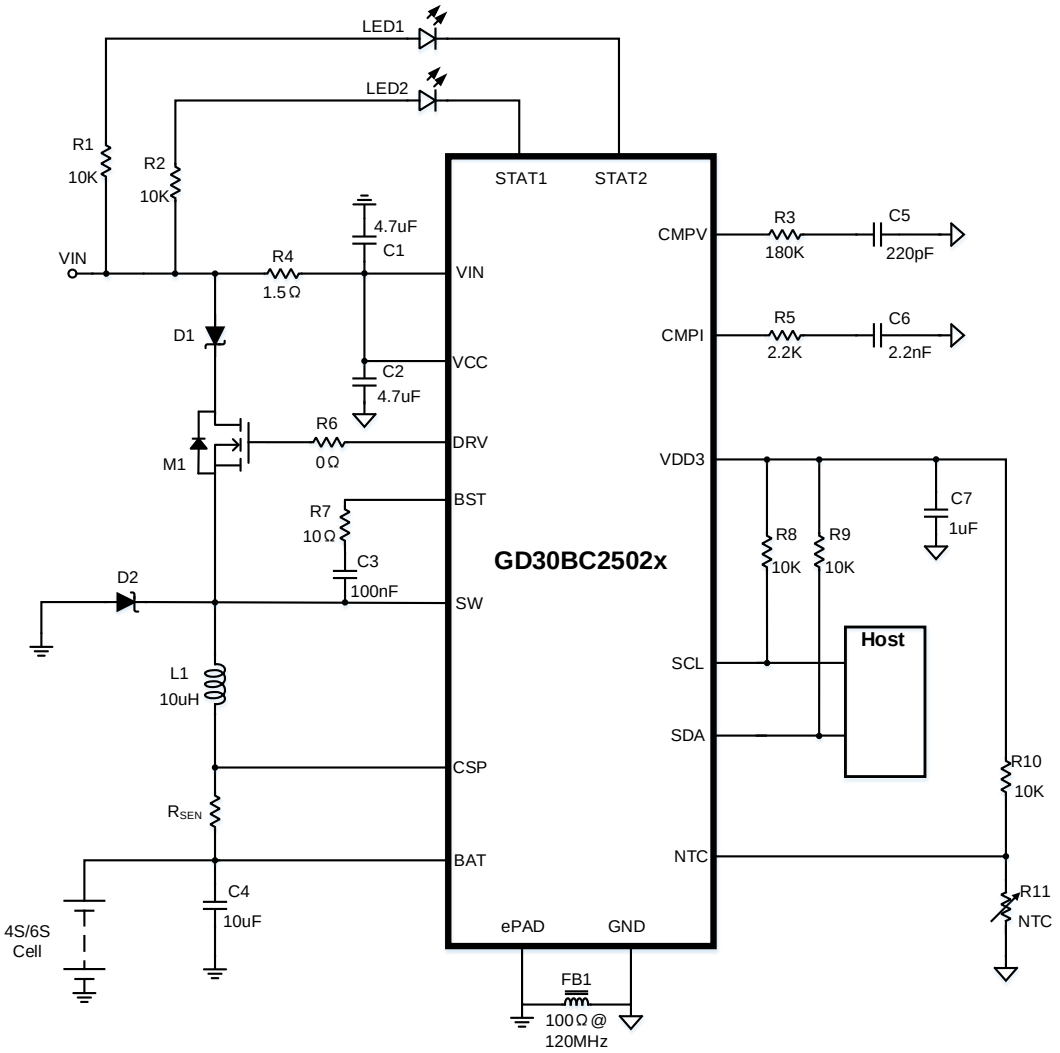
| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{SCL(H)}$ | SCL clock high time | — | 4.0 | — | 0.6 | — | μs |
| $t_{SCL(L)}$ | SCL clock low time | — | 4.7 | — | 1.3 | — | μs |
| $t_{su(SDA)}$ | SDA setup time | — | 250 | — | 100 | — | ns |
| $t_{h(SDA)}$ | SDA data hold time | — | 0 | 3450 | 0 | 900 | ns |
| $t_{r(SDA/SCL)}$ | SDA and SCL rise time | — | — | 1000 | — | 300 | ns |
| $t_{f(SDA/SCL)}$ | SDA and SCL fall time | — | — | 300 | 3 | 300 | ns |
| $t_{h(STA)}$ | Start condition hold time | — | 4.0 | — | 0.6 | — | μs |

**Figure 6-1. I2C bus timing diagram**



# 7 Typical application circuit

**Figure 7-1 Typical GD30BC2502x application circuit**

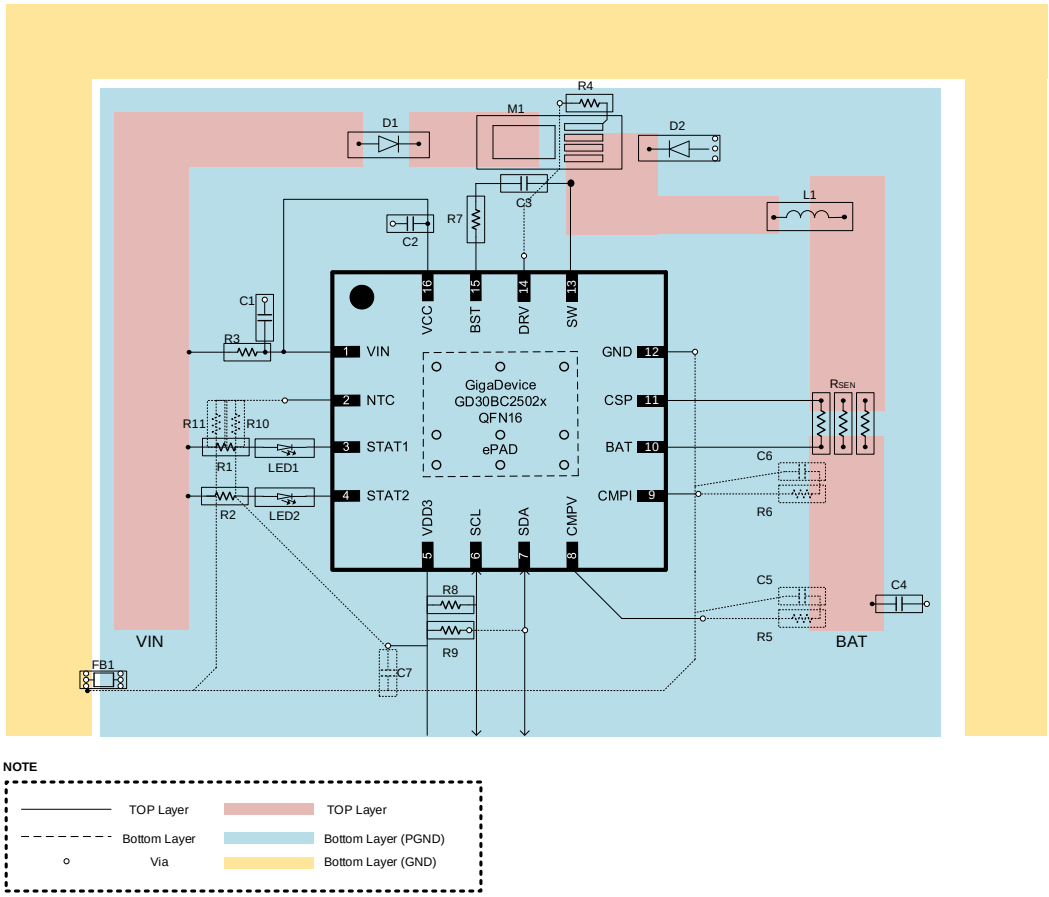



**Notes:**

1. The values of C2, L1 and $R_{SEN}$ will change according to the change of constant current charging current. Please refer to section 5.7 for specific calculation method. Figure 7-1 shows a typical application circuit with 2/3/5 batteries.
2. Resistor R4 and capacitor C1 should be close to VIN pin.

# 8 Layout guideline

**Figure 8-1 Typical GD30BC2502x layout guideline**




**Notes:**

1. In buck regulator, the loop area should be minimized as far as possible, which can reduce stray inductance and minimize noise.
2. The MOSFET should be close to the chip as far as possible to reduce the routing length of the driver and SW, so as to reduce the noise.
3. $R_{SEN}$ should be close to the chip to ensure the accuracy of charging current. $R_{SEN}$ suggests that multiple resistors should be connected in parallel to reduce the heat loss of a single resistor.
4. The capacitor C3 should be placed on the top layer to reduce parasitic parameters.

# 9 Package information

## 9.1 QFN16 package outline and dimensions

**Figure 9-1 QFN16 package outline**

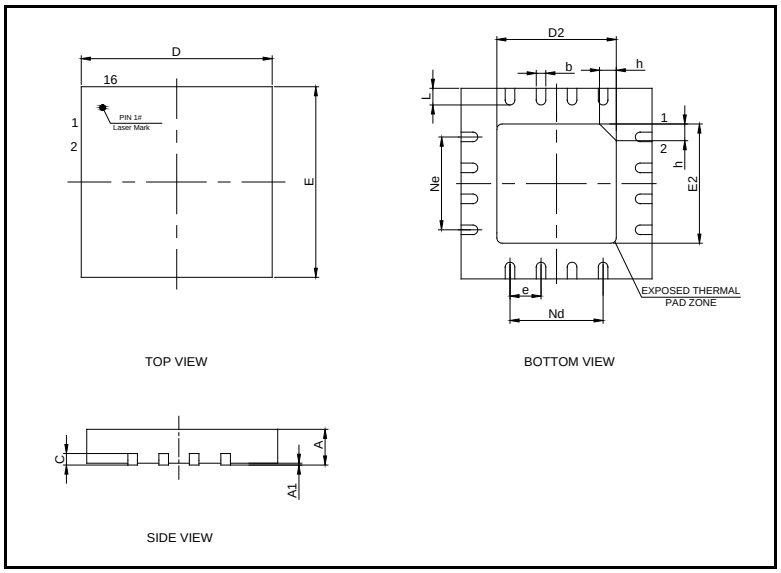
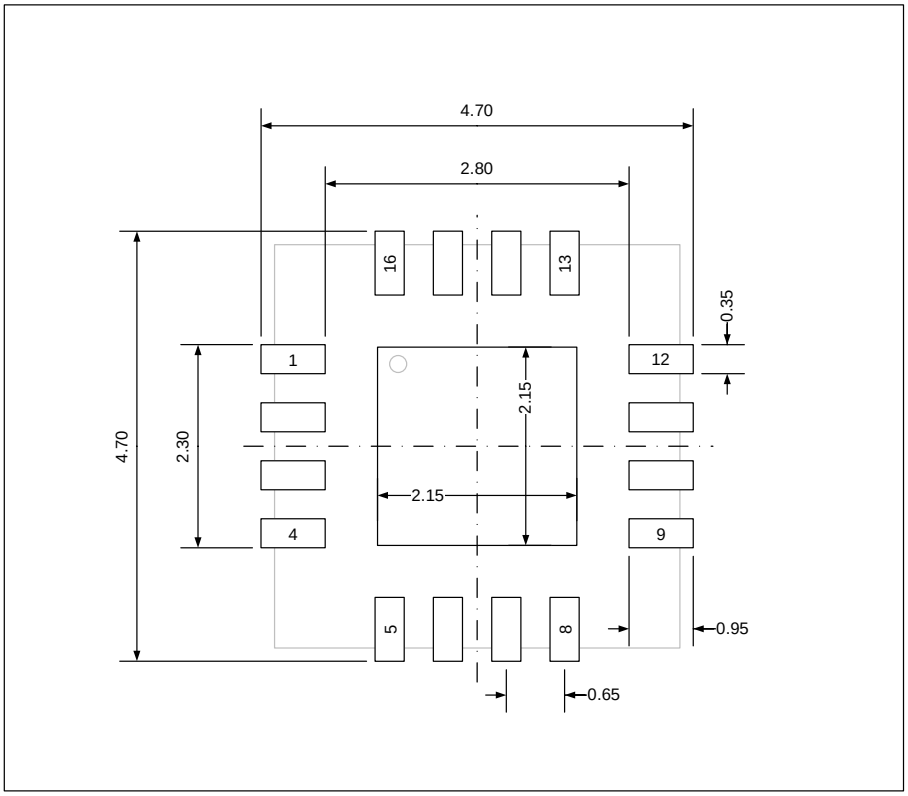



**Table 9-1 QFN16 package dimensions**

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | — | 0.02 | 0.05 |
| b | 0.25 | 0.30 | 0.35 |
| c | 0.18 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.10 | 2.20 | 2.30 |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.10 | 2.20 | 2.30 |
| e | — | 0.65 | — |
| h | 0.30 | 0.35 | 0.40 |
| L | 0.45 | 0.55 | 0.65 |
| Nd | — | 1.95 | — |
| Ne | — | 1.95 | — |

(Original dimensions are in millimeters)

**Figure 9-2 QFN16 recommend footprint**




(All dimensions are in millimeters)

## 9.2 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "Θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

$\Theta_{JA}$: Thermal resistance, junction-to-ambient.

$\Theta_{JB}$: Thermal resistance, junction-to-board.

$\Theta_{JC}$: Thermal resistance, junction-to-case.

$\Psi_{JB}$: Thermal characterization parameter, junction-to-board.

$\Psi_{JT}$: Thermal characterization parameter, junction-to-top center.

$\Theta_{JA} = (T_J - T_A)/P_D$

$\Theta_{JB} = (T_J - T_B)/P_D$

$\Theta_{JC} = (T_J - T_C)/P_D$

Where, $T_J$ = Junction temperature.

$T_A$ = Ambient temperature

$T_B$ = Board temperature

$T_C$ = Case temperature which is monitoring on package surface

$P_D$ = Total power dissipation

$\Theta_{JA}$ represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower $\Theta_{JA}$ can be considerate as better overall thermal performance. $\Theta_{JA}$ is generally used to estimate junction temperature.

$\Theta_{JB}$ is used to measure the heat flow resistance between the chip surface and the PCB board.

$\Theta_{JC}$ represents the thermal resistance between the chip surface and the package top case. $\Theta_{JC}$ is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

**Table 9-2 Package thermal characteristics(1)**

| Symbol | Condition | Package | Value | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Natural convection, 2S2P PCB | QFN16 | 51.23 | °C/W |
| $\Theta_{JB}$ | Cold plate, 2S2P PCB | QFN16 | 17.44 | °C/W |
| $\Theta_{JC}$ | Cold plate, 2S2P PCB | QFN16 | 23.22 | °C/W |
| $\Psi_{JB}$ | Natural convection, 2S2P PCB | QFN16 | 17.61 | °C/W |
| $\Psi_{JT}$ | Natural convection, 2S2P PCB | QFN16 | 1.17 | °C/W |

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

# 10 Ordering information

**Table 10-1 Part order code for GD30BC2502x**

| Ordering Code | Package | Package Type | Packing Type | MOQ | Temperature Operating Range |
|---|---|---|---|---|---|
| GD30BC2502LRTR | QFN16(4X4) | Green | Tape&Reel | 3000 | Industrial -40°C to +85°C |

# 11 Revision history

**Table 11-1 Revision history**

| Revision No. | Description | Date |
|---|---|---|
| 1.0 | Initial Release | Aug.25, 2022 |

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