GC9C01

a-Si TFT LCD Single Chip Driver
360RGBx360 Resolution

Data Sheet

Rev.1.0

2020-09-15

GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	PREPARED BY
1.0	2020-09-15	New Created	Kelly

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1. Introduction

GC9C01 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 360RGBx360 dots, comprising a 540-channel source driver, a 32-channel gate driver, 291,600 bytes GRAM for graphic display data of 360RGBx360 dots, and power supply circuit.

GC9C01 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface , 3-/4-line serial peripheral interface (SPI) and Quad serial peripheral interface . The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

GC9C01 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9C01 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Dual gate TFT LCD driver with 0D 0C
- Display resolution: [360RGB](H) x 360(V)
- Output:
  - 540 source outputs
  - 32 gate outputs
- Resolution:
  240x240：S91-S450
  320x320：S31-S510
  320x360：S31-S510
  360x360：S1-S540
  320x390：S31-S510
- a-TFT LCD driver with on-chip full display RAM: 291,600 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-I /8080-II series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 8-bits, 9-bits Serial Peripheral Interface (SPI) and 2 data lane SPI
  - Quad Serial Peripheral Interface
  - MIPI（1 lane）
- Display mode:
  - Full color mode (Idle mode OFF): 16.7M-color（with dither in QSPI interface only）
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- Frame rate
  -Normal mode（20Hz~65Hz）
  -Idle mode （1Hz~60Hz）
- On chip functions:
  - Timing generator
  - Oscillator
  - DC/DC converter
  - column ， dot inversion
- Low -power consumption architecture
  - Low operating power supplies:
    - VDDI = 1.65V ~ 3.3V (logic)
    - VDDB = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source/Gamma power supply voltage
    - Vreg1A ~ vreg2A = 6.5V ~-4.4V
  - Gate driver output voltage
    - VGH - GND = 8.0V ~ 15.0V

- VGL - GND = -12.0V ~ -7.0V

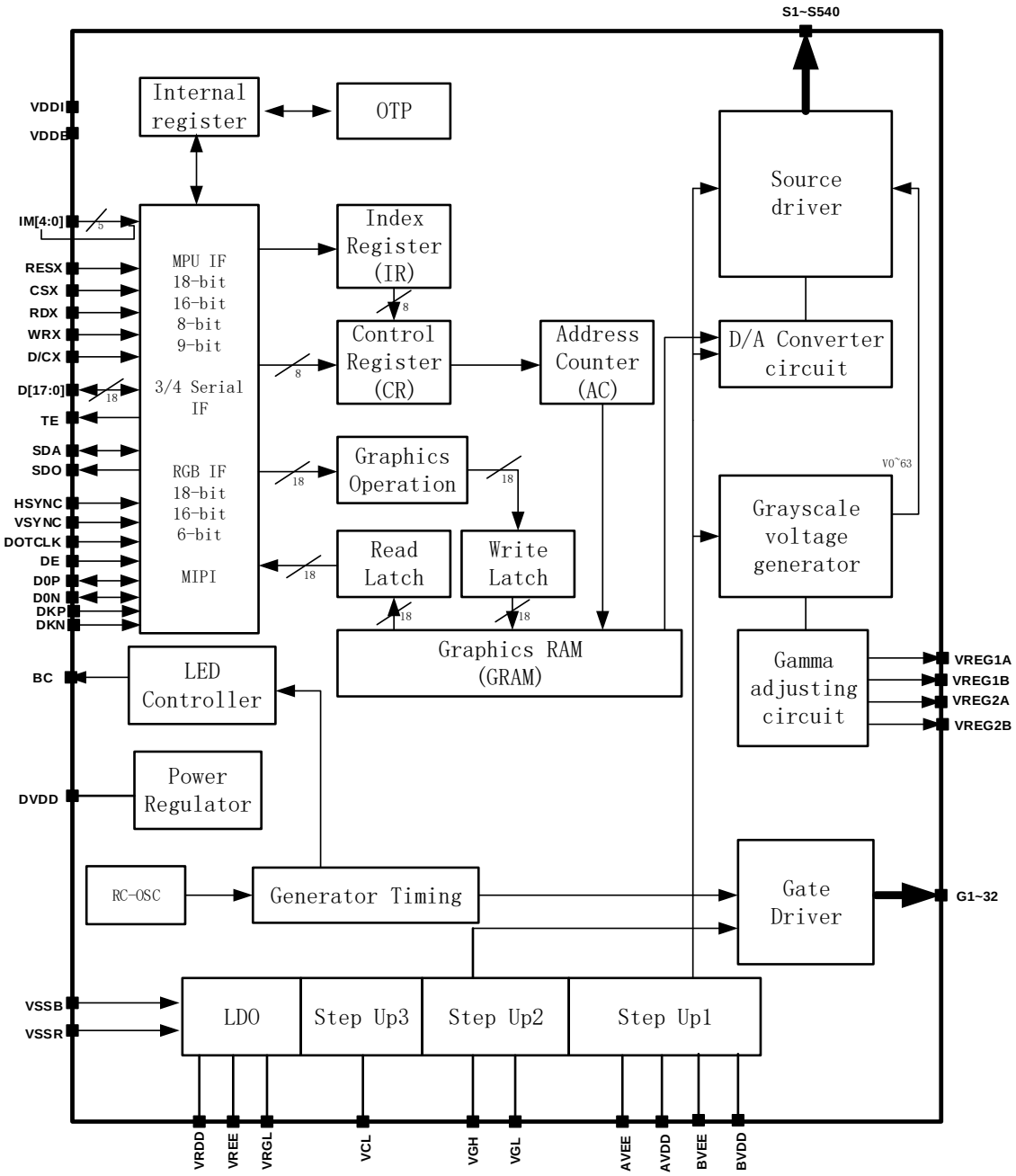
- VCOM connect to GND

◆ Operate temperature range: -40℃to 80℃

3. Block Diagram

3.1. Block diagram

Figure1



3.2. Pin Description

Table 1.

Power Supply Pins			
Pin Name	I/O	Connect Pin	Descriptions
VDDI(IOVCC)	I	VDDI	Low voltage power supply for interface logic circuits(1.65~3.3V)
VDDB(VCI)	I	VDDB	High voltage power supply for analog circuit blocks(2.5~3.3V)
VSSB/VSSR	I	GND	System ground level

Table 2

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Connect Pin</th><th>Descriptions</th></tr>
<tr><td>IM[4]=1
IM[3:0]</td><td>I</td><td>(VDDI/ GND)</td><td>-Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080- MCU 8bit interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080- MCU 9bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080-MCU16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10]
D[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8080- MCU 8bit interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>8080- MCU 9bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>8080- MCU 16bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8080- MCU 18bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td>SDA
SDO</td><td>SDA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface II</td><td>SDA
SDO</td><td>SDA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Q_SPI</td><td>SDA</td><td>SDA,
D[3:1]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td>SDA</td><td>SDA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>MIPI</td><td></td><td></td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface I</td><td>SDA</td><td>SDA</td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.
Fix this pin at VDDI or GND.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU
(VDDI/GND)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU
(VDDI/GND)</td><td>Chip select input pin("Low" enable).
This pin can be permanently fixed "Low" in MPU interface mode only.</td></tr>
</table>

D/CX (SCL)	I	MCU (VDDI/ GND)	This pin is used to select "Data or Command" in the parallel interface When DCX='1', data is selected. When DCX='0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit /QSPI serial interface. If not used, this pin should be connected to VDDI or GND.
RDX	I	MCU (VDDI/ GND)	8080-I/8080-II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use
WRX (D/CX)	I	MCU (VDDI/ GND)	8080-I/8080-II system (WRX): Serves as a write signal and writes data at the rising edge. 4-wire system (D/CX): Serves as command or parameter select. 3-wire 2data mode：Serves as second data pin Fix to VDDI level when not in use.
D[17:0]	I/O	MCU (VDDI/ GND)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode QSPI 4wire mode D[3:1] Server as SDA[3:1] Fix to GND level when not in use
SDA	I/O	MCU (VDDI/ GND)	When IM[2]: High, Serial in/out signal in 3-wire 9-bit/4-wire 8-bit serial data interface. When IM[2]: Low, Serial input signal in 3-wire 9-bit/4-wire 8-bit serial data interface. When IM[4:0]=11100, Serial input signal in QSPI serial data interface. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or GND.
SDO	O	MCU (VDDI/GND)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (VDDI/ GND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (VDDI/GND)	Dot clock signal for RGB interface operation. Fix to VDDI or GND level when not in use.
VSYNC	I	MCU (VDDI/GND)	Frame synchronizing signal for RGB interface operation. Fix to VDDI or GND level when not in use.
HSYNC	I	MCU (VDDI/ GND)	Line synchronizing signal for RGB interface operation. Fix to VDDI or GND level when not in use.
DE	I	MCU (VDDI/ GND)	Data enable signal for RGB interface operation. Fix to VDDI or GND level when not in use.
DKP/ Clock_P	I	MIPI	- Positive polarity of low voltage differential clock signal If MIPI are not used, they should be connected to GND.
DKN/ Clock_N	I	MIPI	- Negative polarity of low voltage differential clock signal If MIPI are not used, they should be connected to GND.

D0P/ Data_P	I/O	MIPI	- Positive polarity of low voltage differential data signal If MIPI are not used, they should be connected to GND
D0N/ Data_N	I/O	MIPI	- Negative polarity of low voltage differential data signal If MIPI are not used, they should be connected to GND
PSWAP	I	MCU(VDDI/ GND)	Differential clock polarity swap For MIPI DSI interface 0: D0P->D0P, D0N->D0N; DKP->DKP, DKN->DKN, 1: D0P->D0N, D0N->D0P; DKP->DKN, DKN->DKP,
VCOM	I	GND	Fix to GND

Note:

1. If CSX is connected to GND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Further more there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

Table 3

LCD Driver Input/Output Pins			
Pin Name	I/O	Connect Pin	Descriptions
S540~S1	O	LCD	Source output signals. Leave the pin to open when not in use.
G1~G32	O	LCD	Gate output signals. Leave the pin to open when not in use.
VCOM	O	GND	Connect to GND.
VRDD	O	Power	Power supply for AVDD.
VREE	O	Power	Power supply for AVEE.
DVDD	O	Power	Regulated Low voltage level for interface circuits Don't apply any external power to this pin
VRGL	O	Power	Power supply for VCL.
AVDD	O	Power	Analog power for Source.
AVEE	O	Power	Analog power for Source.
VGH	O	Power	Power supply for the gate driver(Positive).
VGL	O	Power	Power supply for the gate driver(Negative).
VREG1A	O	Ref	VREG1A is the highest positive grayscale reference voltage of source driver.
VREG1B	O	Ref	VREG1B is the lowest positive grayscale reference voltage of source driver. test by VREGP pin
VREG2B	O	Ref	VREG2B is the lowest negative grayscale reference voltage of source driver, test by VREGP pin
VREG2A	O	Ref	VREG2A is the highest negative grayscale reference voltage of source driver , test VREGN pin
BC	O	Dig IO	Output pin for PWM (Pulse width Modulation) signal of LED driving. If not used, open this pin.

Table 4

Test Pins			
Pin Name	I/O	Connect Pin	Descriptions
OSC_IN	I/O	Open	Test pin
OSC_TEST	I/O	Open	Test pin
VPP	I/O	Open	Test pin
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation ,leave these pads open.

Liquid crystal power supply specifications Table

Table 5

No.	Item		Description
1	TFT Source Driver		support 360*RGB（max）
2	TFT Gate Driver		32 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S540	V0~V63 grayscales
		G1~G32	VGH-VGL
5	Input Voltage	VDDI	1.65~3.30V
		VDDB	2.50~3.30V
6	Liquid Crystal Drive Voltages	AVDD	6.5~7.5V
		AVEE	-5.5V~-4.5V
		VGH	8.0~15.0V
		VGL	-11.0~-7.0V
		VCL	-3.0~-1.5V
7	Internal Step-up Circuits	AVDD	VDDB*3
		AVEE	VDDB*-2
		VGH	VDDB*5
		VGL	VDDB*-5
		VCL	VDDB*-1

3.3.PAD coordinates

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	DUMMY	-5973	-437	51	VSSB	-3449	-437	101	DUMMY	150	-437
2	DUMMY	-5928	-437	52	VSSB	-3399	-437	102	DUMMY	250	-437
3	DUMMY	-5883	-437	53	VSSB	-3349	-437	103	DUMMY	350	-437
4	DUMMY	-5838	-437	54	VDDB	-3299	-437	104	DUMMY	450	-437
5	DUMMY	-5793	-437	55	VDDB	-3249	-437	105	DUMMY	549.98	-437
6	DUMMY	-5748	-437	56	VDDB	-3200	-437	106	DUMMY	649.96	-437
7	DUMMY	-5703	-437	57	VDDB	-3150	-437	107	DUMMY	749.94	-437
8	DUMMY	-5658	-437	58	VDDB	-3100	-437	108	DUMMY	849.92	-437
9	DUMMY	-5613	-437	59	DUMMY	-3000	-437	109	DUMMY	949.9	-437
10	DUMMY	-5568	-437	60	DUMMY	-2900	-437	110	DUMMY	1049.9	-437
11	DUMMY	-5523	-437	61	DUMMY	-2800	-437	111	VSSB	1149.9	-437
12	DUMMY	-5478	-437	62	DUMMY	-2700	-437	112	VSSB	1199.9	-437
13	DUMMY	-5433	-437	63	BVEE	-2600	-437	113	VSSB	1249.8	-437
14	DUMMY	-5388	-437	64	BVEE	-2550	-437	114	VSSB	1299.8	-437
15	DUMMY	-5343	-437	65	BVEE	-2500	-437	115	VSSB	1349.8	-437
16	DUMMY	-5298	-437	66	BVDD	-2450	-437	116	VSSR	1399.8	-437
17	DUMMY	-5253	-437	67	BVDD	-2400	-437	117	VSSR	1449.8	-437
18	DUMMY	-5208	-437	68	BVDD	-2350	-437	118	VSSR	1499.8	-437
19	DUMMY	-5163	-437	69	DUMMY	-2250	-437	119	VSSR	1549.8	-437
20	DUMMY	-5118	-437	70	DUMMY	-2150	-437	120	VSSR	1599.8	-437
21	DUMMY	-5073	-437	71	DUMMY	-2050	-437	121	VPP	1649.8	-437
22	DUMMY	-5028	-437	72	DUMMY	-1950	-437	122	VREG1A	1699.8	-437
23	DUMMY	-4983	-437	73	DUMMY	-1850	-437	123	VREG1A	1749.8	-437
24	DUMMY	-4938	-437	74	DUMMY	-1750	-437	124	VREGP	1799.8	-437
25	VCOM	-4781	-437	75	DUMMY	-1650	-437	125	VREGP	1849.7	-437
26	VCOM	-4731	-437	76	DUMMY	-1550	-437	126	VREG_VREF	1899.7	-437
27	VCOM	-4681	-437	77	DUMMY	-1450	-437	127	VREG_VREF	1949.7	-437
28	VCOM	-4631	-437	78	DUMMY	-1350	-437	128	AVDD	1999.7	-437
29	VCOM	-4581	-437	79	DVDD	-1250	-437	129	AVDD	2049.7	-437
30	VGL	-4531	-437	80	DVDD	-1200	-437	130	AVDD	2099.7	-437
31	VGL	-4481	-437	81	DVDD	-1150	-437	131	VDDB	2149.7	-437
32	VGL	-4431	-437	82	VDDSF	-1100	-437	132	VDDB	2199.7	-437
33	VGL	-4381	-437	83	VDDSF	-1050	-437	133	VDDB	2249.7	-437
34	VGL	-4331	-437	84	VDDSF	-999.9	-437	134	VDDB	2299.7	-437
35	VRGL	-4281	-437	85	VSSB	-949.9	-437	135	VDDB	2349.7	-437
36	VRGL	-4231	-437	86	VSSB	-899.9	-437	136	VSSB	2399.6	-437
37	VRGL	-4181	-437	87	VSSB	-849.9	-437	137	VSSB	2449.6	-437
38	VCL	-4131	-437	88	VSSB	-799.9	-437	138	VSSB	2499.6	-437
39	VCL	-4081	-437	89	VSSB	-749.9	-437	139	VSSB	2549.6	-437
40	VCL	-4031	-437	90	VDDB	-699.9	-437	140	VSSB	2599.6	-437
41	VDH	-3949	-437	91	VDDB	-650	-437	141	AVEE	2649.6	-437
42	VDH	-3899	-437	92	VDDB	-600	-437	142	AVEE	2699.6	-437
43	VDH	-3849	-437	93	VDDB	-550	-437	143	AVEE	2749.6	-437
44	VGH	-3799	-437	94	VDDB	-500	-437	144	VREGN	2799.6	-437
45	VGH	-3749	-437	95	VDDGM	-450	-437	145	VREGN	2849.6	-437
46	VGH	-3699	-437	96	DUMMY	-350	-437	146	IM<4>	2985.5	-437
47	VGH	-3649	-437	97	DUMMY	-250	-437	147	OSC_OUT	3049.5	-437
48	VGH	-3599	-437	98	DUMMY	-150	-437	148	OSC_IN	3149.5	-437
49	VSSB	-3549	-437	99	DUMMY	-50	-437	149	VDDI	3199.5	-437
50	VSSB	-3499	-437	100	DUMMY	50	-437	150	VDDI	3249.5	-437

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
151	VDDI	3299.5	-437	201	VSSB	5973.1	402	251	S<8>	4070.3	417
152	VDDI	3349.5	-437	202	VSSB	5883.1	402	252	S<9>	4056.3	307
153	VDDI	3399.5	-437	203	VDDB	5838.1	402	253	S<10>	4042.3	417
154	IM<3>	3449.5	-437	204	VDDB	5793.1	402	254	S<11>	4028.4	307
155	HSYNC	3502.4	-437	205	VDDB	5748.1	402	255	S<12>	4014.4	417
156	VSYNC	3562.4	-437	206	VDDI	5703.1	402	256	S<13>	4000.4	307
157	ENABLE	3622.4	-437	207	VDDI	5658.1	402	257	S<14>	3986.4	417
158	DOTCLK	3682.4	-437	208	TE	5613.1	402	258	S<15>	3972.4	307
159	SDO	3742.4	-437	209	RD	5568.1	402	259	S<16>	3958.4	417
160	SDA	3802.4	-437	210	DC	5523.1	402	260	S<17>	3944.4	307
161	DB<17>	3868.4	-437	211	CS	5478.1	402	261	S<18>	3930.4	417
162	DB<16>	3940.4	-437	212	WR	5433.2	402	262	S<19>	3916.4	307
163	DB<15>	4012.4	-437	213	BC	5388.2	402	263	S<20>	3902.4	417
164	DB<14>	4084.3	-437	214	DB<0>	5343.2	402	264	S<21>	3888.4	307
165	DB<13>	4156.3	-437	215	DB<1>	5298.2	402	265	S<22>	3874.4	417
166	DB<12>	4228.3	-437	216	DB<2>	5253.2	402	266	S<23>	3860.4	307
167	DB<11>	4300.3	-437	217	DB<3>	5208.2	402	267	S<24>	3846.4	417
168	DB<10>	4372.3	-437	218	DB<4>	5163.2	402	268	S<25>	3832.4	307
169	DB<9>	4444.3	-437	219	DB<5>	5118.2	402	269	S<26>	3818.4	417
170	DB<8>	4516.3	-437	220	DB<6>	5073.2	402	270	S<27>	3804.4	307
171	VCOM	4580.8	-437	221	DB<7>	5028.2	402	271	S<28>	3790.4	417
172	VCOM	4630.8	-437	222	TESTP	4983.2	402	272	S<29>	3776.4	307
173	VCOM	4680.7	-437	223	TESTN	4938.2	402	273	S<30>	3762.4	417
174	VCOM	4730.7	-437	224	Aling_mark	4861	374	274	S<31>	3748.4	307
175	VCOM	4780.7	-437	225	GOUT<32>	4789.7	402	275	S<32>	3734.4	417
176	DUMMY	4938.2	-437	226	GOUT<31>	4757.7	402	276	S<33>	3720.4	307
177	DUMMY	4983.2	-437	227	GOUT<30>	4725.7	402	277	S<34>	3706.4	417
178	DUMMY	5028.2	-437	228	GOUT<29>	4693.7	402	278	S<35>	3692.4	307
179	DUMMY	5073.2	-437	229	GOUT<28>	4661.7	402	279	S<36>	3678.4	417
180	DUMMY	5118.2	-437	230	GOUT<27>	4629.8	402	280	S<37>	3664.4	307
181	DUMMY	5163.2	-437	231	GOUT<26>	4597.8	402	281	S<38>	3650.4	417
182	DUMMY	5208.2	-437	232	GOUT<25>	4565.8	402	282	S<39>	3636.4	307
183	DUMMY	5253.2	-437	233	GOUT<24>	4533.8	402	283	S<40>	3622.4	417
184	DUMMY	5298.2	-437	234	GOUT<23>	4501.8	402	284	S<41>	3608.4	307
185	DUMMY	5343.2	-437	235	GOUT<22>	4469.8	402	285	S<42>	3594.4	417
186	DUMMY	5388.2	-437	236	GOUT<21>	4437.8	402	286	S<43>	3580.4	307
187	DUMMY	5433.2	-437	237	GOUT<20>	4405.8	402	287	S<44>	3566.4	417
188	DUMMY	5478.1	-437	238	GOUT<19>	4373.8	402	288	S<45>	3552.4	307
189	DUMMY	5523.1	-437	239	GOUT<18>	4341.8	402	289	S<46>	3538.4	417
190	DUMMY	5568.1	-437	240	GOUT<17>	4309.8	402	290	S<47>	3524.4	307
191	DUMMY	5613.1	-437	241	DUM	4210.3	417	291	S<48>	3510.4	417
192	DUMMY	5658.1	-437	242	DUM	4196.3	307	292	S<49>	3496.4	307
193	DUMMY	5703.1	-437	243	DUM	4182.3	417	293	S<50>	3482.4	417
194	DUMMY	5748.1	-437	244	S<1>	4168.3	307	294	S<51>	3468.5	307
195	DUMMY	5793.1	-437	245	S<2>	4154.3	417	295	S<52>	3454.5	417
196	DUMMY	5838.1	-437	246	S<3>	4140.3	307	296	S<53>	3440.5	307
197	DUMMY	5883.1	-437	247	S<4>	4126.3	417	297	S<54>	3426.5	417
198	DUMMY	5928.1	-437	248	S<5>	4112.3	307	298	S<55>	3412.5	307
199	DUMMY	5973.1	-437	249	S<6>	4098.3	417	299	S<56>	3398.5	417
200	VSSB	5928.1	402	250	S<7>	4084.3	307	300	S<57>	3384.5	307

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
301	S<58>	3370.5	417	351	S<108>	2670.6	417	401	S<158>	1970.7	417
302	S<59>	3356.5	307	352	S<109>	2656.6	307	402	S<159>	1956.7	307
303	S<60>	3342.5	417	353	S<110>	2642.6	417	403	S<160>	1942.7	417
304	S<61>	3328.5	307	354	S<111>	2628.6	307	404	S<161>	1928.7	307
305	S<62>	3314.5	417	355	S<112>	2614.6	417	405	S<162>	1914.7	417
306	S<63>	3300.5	307	356	S<113>	2600.6	307	406	S<163>	1900.7	307
307	S<64>	3286.5	417	357	S<114>	2586.6	417	407	S<164>	1886.7	417
308	S<65>	3272.5	307	358	S<115>	2572.6	307	408	S<165>	1872.7	307
309	S<66>	3258.5	417	359	S<116>	2558.6	417	409	S<166>	1858.7	417
310	S<67>	3244.5	307	360	S<117>	2544.6	307	410	S<167>	1844.7	307
311	S<68>	3230.5	417	361	S<118>	2530.6	417	411	S<168>	1830.7	417
312	S<69>	3216.5	307	362	S<119>	2516.6	307	412	S<169>	1816.7	307
313	S<70>	3202.5	417	363	S<120>	2502.6	417	413	S<170>	1802.7	417
314	S<71>	3188.5	307	364	S<121>	2488.6	307	414	S<171>	1788.8	307
315	S<72>	3174.5	417	365	S<122>	2474.6	417	415	S<172>	1774.8	417
316	S<73>	3160.5	307	366	S<123>	2460.6	307	416	S<173>	1760.8	307
317	S<74>	3146.5	417	367	S<124>	2446.6	417	417	S<174>	1746.8	417
318	S<75>	3132.5	307	368	S<125>	2432.6	307	418	S<175>	1732.8	307
319	S<76>	3118.5	417	369	S<126>	2418.6	417	419	S<176>	1718.8	417
320	S<77>	3104.5	307	370	S<127>	2404.6	307	420	S<177>	1704.8	307
321	S<78>	3090.5	417	371	S<128>	2390.6	417	421	S<178>	1690.8	417
322	S<79>	3076.5	307	372	S<129>	2376.6	307	422	S<179>	1676.8	307
323	S<80>	3062.5	417	373	S<130>	2362.6	417	423	S<180>	1662.8	417
324	S<81>	3048.5	307	374	S<131>	2348.7	307	424	S<181>	1648.8	307
325	S<82>	3034.5	417	375	S<132>	2334.7	417	425	S<182>	1634.8	417
326	S<83>	3020.5	307	376	S<133>	2320.7	307	426	S<183>	1620.8	307
327	S<84>	3006.5	417	377	S<134>	2306.7	417	427	S<184>	1606.8	417
328	S<85>	2992.5	307	378	S<135>	2292.7	307	428	S<185>	1592.8	307
329	S<86>	2978.5	417	379	S<136>	2278.7	417	429	S<186>	1578.8	417
330	S<87>	2964.5	307	380	S<137>	2264.7	307	430	S<187>	1564.8	307
331	S<88>	2950.5	417	381	S<138>	2250.7	417	431	S<188>	1550.8	417
332	S<89>	2936.5	307	382	S<139>	2236.7	307	432	S<189>	1536.8	307
333	S<90>	2922.5	417	383	S<140>	2222.7	417	433	S<190>	1522.8	417
334	S<91>	2908.6	307	384	S<141>	2208.7	307	434	S<191>	1508.8	307
335	S<92>	2894.6	417	385	S<142>	2194.7	417	435	S<192>	1494.8	417
336	S<93>	2880.6	307	386	S<143>	2180.7	307	436	S<193>	1480.8	307
337	S<94>	2866.6	417	387	S<144>	2166.7	417	437	S<194>	1466.8	417
338	S<95>	2852.6	307	388	S<145>	2152.7	307	438	S<195>	1452.8	307
339	S<96>	2838.6	417	389	S<146>	2138.7	417	439	S<196>	1438.8	417
340	S<97>	2824.6	307	390	S<147>	2124.7	307	440	S<197>	1424.8	307
341	S<98>	2810.6	417	391	S<148>	2110.7	417	441	S<198>	1410.8	417
342	S<99>	2796.6	307	392	S<149>	2096.7	307	442	S<199>	1396.8	307
343	S<100>	2782.6	417	393	S<150>	2082.7	417	443	S<200>	1382.8	417
344	S<101>	2768.6	307	394	S<151>	2068.7	307	444	S<201>	1368.8	307
345	S<102>	2754.6	417	395	S<152>	2054.7	417	445	S<202>	1354.8	417
346	S<103>	2740.6	307	396	S<153>	2040.7	307	446	S<203>	1340.8	307
347	S<104>	2726.6	417	397	S<154>	2026.7	417	447	S<204>	1326.8	417
348	S<105>	2712.6	307	398	S<155>	2012.7	307	448	S<205>	1312.8	307
349	S<106>	2698.6	417	399	S<156>	1998.7	417	449	S<206>	1298.8	417
350	S<107>	2684.6	307	400	S<157>	1984.7	307	450	S<207>	1284.8	307

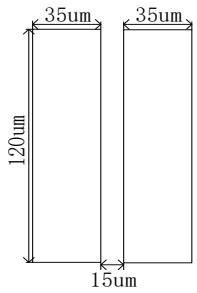
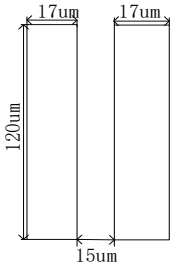
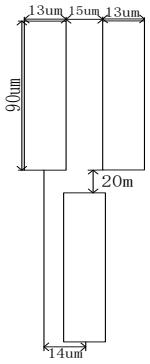
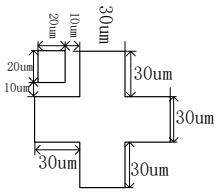
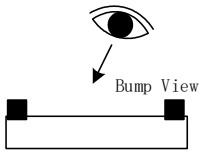
No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
451	S<208>	1270.8	417	501	S<258>	570.97	417	551	S<298>	-780.9	307
452	S<209>	1256.8	307	502	S<259>	556.97	307	552	S<299>	-794.9	417
453	S<210>	1242.8	417	503	S<260>	542.97	417	553	S<300>	-808.9	307
454	S<211>	1228.9	307	504	S<261>	528.98	307	554	S<301>	-822.9	417
455	S<212>	1214.9	417	505	S<262>	514.98	417	555	S<302>	-836.9	307
456	S<213>	1200.9	307	506	S<263>	500.98	307	556	S<303>	-850.9	417
457	S<214>	1186.9	417	507	S<264>	486.98	417	557	S<304>	-864.9	307
458	S<215>	1172.9	307	508	S<265>	472.99	307	558	S<305>	-878.9	417
459	S<216>	1158.9	417	509	S<266>	458.99	417	559	S<306>	-892.9	307
460	S<217>	1144.9	307	510	S<267>	444.99	307	560	S<307>	-906.9	417
461	S<218>	1130.9	417	511	S<268>	430.99	417	561	S<308>	-920.9	307
462	S<219>	1116.9	307	512	S<269>	417	307	562	S<309>	-934.9	417
463	S<220>	1102.9	417	513	S<270>	403	417	563	S<310>	-948.9	307
464	S<221>	1088.9	307	514	DUM	389	307	564	S<311>	-962.9	417
465	S<222>	1074.9	417	515	DUM	375	417	565	S<312>	-976.9	307
466	S<223>	1060.9	307	516	DUM	349	417	566	S<313>	-990.9	417
467	S<224>	1046.9	417	517	DUM	323	417	567	S<314>	-1005	307
468	S<225>	1032.9	307	518	DUM	297	417	568	S<315>	-1019	417
469	S<226>	1018.9	417	519	DUM	-297	417	569	S<316>	-1033	307
470	S<227>	1004.9	307	520	DUM	-323	417	570	S<317>	-1047	417
471	S<228>	990.89	417	521	DUM	-349	417	571	S<318>	-1061	307
472	S<229>	976.9	307	522	DUM	-375	417	572	S<319>	-1075	417
473	S<230>	962.9	417	523	DUM	-389	307	573	S<320>	-1089	307
474	S<231>	948.9	307	524	S<271>	-403	417	574	S<321>	-1103	417
475	S<232>	934.9	417	525	S<272>	-417	307	575	S<322>	-1117	307
476	S<233>	920.91	307	526	S<273>	-431	417	576	S<323>	-1131	417
477	S<234>	906.91	417	527	S<274>	-445	307	577	S<324>	-1145	307
478	S<235>	892.91	307	528	S<275>	-459	417	578	S<325>	-1159	417
479	S<236>	878.91	417	529	S<276>	-473	307	579	S<326>	-1173	307
480	S<237>	864.92	307	530	S<277>	-487	417	580	S<327>	-1187	417
481	S<238>	850.92	417	531	S<278>	-501	307	581	S<328>	-1201	307
482	S<239>	836.92	307	532	S<279>	-515	417	582	S<329>	-1215	417
483	S<240>	822.92	417	533	S<280>	-529	307	583	S<330>	-1229	307
484	S<241>	808.93	307	534	S<281>	-543	417	584	S<331>	-1243	417
485	S<242>	794.93	417	535	S<282>	-557	307	585	S<332>	-1257	307
486	S<243>	780.93	307	536	S<283>	-571	417	586	S<333>	-1271	417
487	S<244>	766.93	417	537	S<284>	-585	307	587	S<334>	-1285	307
488	S<245>	752.94	307	538	S<285>	-599	417	588	S<335>	-1299	417
489	S<246>	738.94	417	539	S<286>	-613	307	589	S<336>	-1313	307
490	S<247>	724.94	307	540	S<287>	-627	417	590	S<337>	-1327	417
491	S<248>	710.94	417	541	S<288>	-641	307	591	S<338>	-1341	307
492	S<249>	696.95	307	542	S<289>	-655	417	592	S<339>	-1355	417
493	S<250>	682.95	417	543	S<290>	-669	307	593	S<340>	-1369	307
494	S<251>	668.95	307	544	S<291>	-682.9	417	594	S<341>	-1383	417
495	S<252>	654.95	417	545	S<292>	-696.9	307	595	S<342>	-1397	307
496	S<253>	640.96	307	546	S<293>	-710.9	417	596	S<343>	-1411	417
497	S<254>	626.96	417	547	S<294>	-724.9	307	597	S<344>	-1425	307
498	S<255>	612.96	307	548	S<295>	-738.9	417	598	S<345>	-1439	417
499	S<256>	598.96	417	549	S<296>	-752.9	307	599	S<346>	-1453	307
500	S<257>	584.97	307	550	S<297>	-766.9	417	600	S<347>	-1467	417

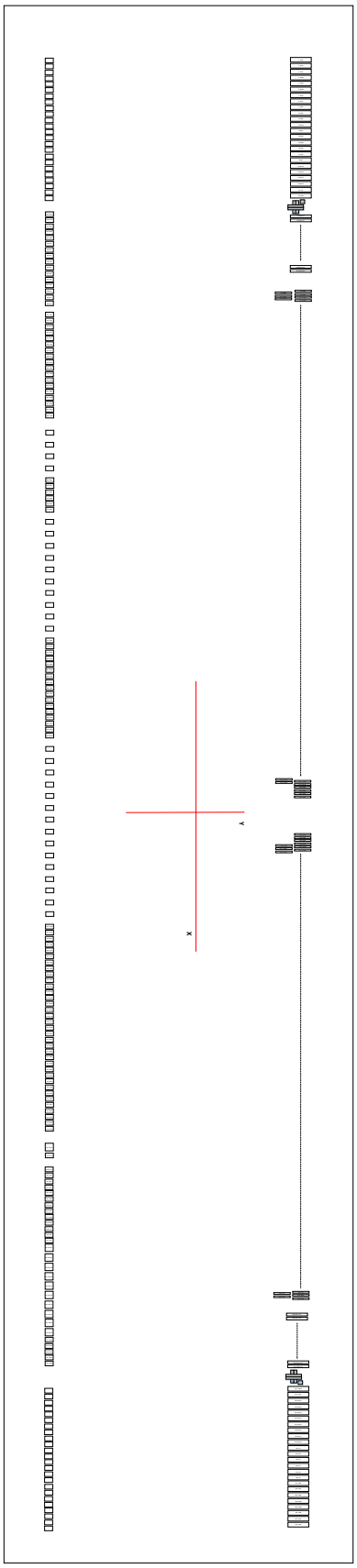
No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
601	S<348>	-1481	307	651	S<398>	-2181	307	701	S<448>	-2881	307
602	S<349>	-1495	417	652	S<399>	-2195	417	702	S<449>	-2895	417
603	S<350>	-1509	307	653	S<400>	-2209	307	703	S<450>	-2909	307
604	S<351>	-1523	417	654	S<401>	-2223	417	704	S<451>	-2923	417
605	S<352>	-1537	307	655	S<402>	-2237	307	705	S<452>	-2937	307
606	S<353>	-1551	417	656	S<403>	-2251	417	706	S<453>	-2951	417
607	S<354>	-1565	307	657	S<404>	-2265	307	707	S<454>	-2965	307
608	S<355>	-1579	417	658	S<405>	-2279	417	708	S<455>	-2979	417
609	S<356>	-1593	307	659	S<406>	-2293	307	709	S<456>	-2993	307
610	S<357>	-1607	417	660	S<407>	-2307	417	710	S<457>	-3007	417
611	S<358>	-1621	307	661	S<408>	-2321	307	711	S<458>	-3021	307
612	S<359>	-1635	417	662	S<409>	-2335	417	712	S<459>	-3035	417
613	S<360>	-1649	307	663	S<410>	-2349	307	713	S<460>	-3049	307
614	S<361>	-1663	417	664	S<411>	-2363	417	714	S<461>	-3063	417
615	S<362>	-1677	307	665	S<412>	-2377	307	715	S<462>	-3077	307
616	S<363>	-1691	417	666	S<413>	-2391	417	716	S<463>	-3091	417
617	S<364>	-1705	307	667	S<414>	-2405	307	717	S<464>	-3105	307
618	S<365>	-1719	417	668	S<415>	-2419	417	718	S<465>	-3119	417
619	S<366>	-1733	307	669	S<416>	-2433	307	719	S<466>	-3133	307
620	S<367>	-1747	417	670	S<417>	-2447	417	720	S<467>	-3147	417
621	S<368>	-1761	307	671	S<418>	-2461	307	721	S<468>	-3161	307
622	S<369>	-1775	417	672	S<419>	-2475	417	722	S<469>	-3175	417
623	S<370>	-1789	307	673	S<420>	-2489	307	723	S<470>	-3189	307
624	S<371>	-1803	417	674	S<421>	-2503	417	724	S<471>	-3202	417
625	S<372>	-1817	307	675	S<422>	-2517	307	725	S<472>	-3216	307
626	S<373>	-1831	417	676	S<423>	-2531	417	726	S<473>	-3230	417
627	S<374>	-1845	307	677	S<424>	-2545	307	727	S<474>	-3244	307
628	S<375>	-1859	417	678	S<425>	-2559	417	728	S<475>	-3258	417
629	S<376>	-1873	307	679	S<426>	-2573	307	729	S<476>	-3272	307
630	S<377>	-1887	417	680	S<427>	-2587	417	730	S<477>	-3286	417
631	S<378>	-1901	307	681	S<428>	-2601	307	731	S<478>	-3300	307
632	S<379>	-1915	417	682	S<429>	-2615	417	732	S<479>	-3314	417
633	S<380>	-1929	307	683	S<430>	-2629	307	733	S<480>	-3328	307
634	S<381>	-1943	417	684	S<431>	-2643	417	734	S<481>	-3342	417
635	S<382>	-1957	307	685	S<432>	-2657	307	735	S<482>	-3356	307
636	S<383>	-1971	417	686	S<433>	-2671	417	736	S<483>	-3370	417
637	S<384>	-1985	307	687	S<434>	-2685	307	737	S<484>	-3384	307
638	S<385>	-1999	417	688	S<435>	-2699	417	738	S<485>	-3398	417
639	S<386>	-2013	307	689	S<436>	-2713	307	739	S<486>	-3412	307
640	S<387>	-2027	417	690	S<437>	-2727	417	740	S<487>	-3426	417
641	S<388>	-2041	307	691	S<438>	-2741	307	741	S<488>	-3440	307
642	S<389>	-2055	417	692	S<439>	-2755	417	742	S<489>	-3454	417
643	S<390>	-2069	307	693	S<440>	-2769	307	743	S<490>	-3468	307
644	S<391>	-2083	417	694	S<441>	-2783	417	744	S<491>	-3482	417
645	S<392>	-2097	307	695	S<442>	-2797	307	745	S<492>	-3496	307
646	S<393>	-2111	417	696	S<443>	-2811	417	746	S<493>	-3510	417
647	S<394>	-2125	307	697	S<444>	-2825	307	747	S<494>	-3524	307
648	S<395>	-2139	417	698	S<445>	-2839	417	748	S<495>	-3538	417
649	S<396>	-2153	307	699	S<446>	-2853	307	749	S<496>	-3552	307
650	S<397>	-2167	417	700	S<447>	-2867	417	750	S<497>	-3566	417

No.	Pad name	X	Y
751	S<498>	-3580	307
752	S<499>	-3594	417
753	S<500>	-3608	307
754	S<501>	-3622	417
755	S<502>	-3636	307
756	S<503>	-3650	417
757	S<504>	-3664	307
758	S<505>	-3678	417
759	S<506>	-3692	307
760	S<507>	-3706	417
761	S<508>	-3720	307
762	S<509>	-3734	417
763	S<510>	-3748	307
764	S<511>	-3762	417
765	S<512>	-3776	307
766	S<513>	-3790	417
767	S<514>	-3804	307
768	S<515>	-3818	417
769	S<516>	-3832	307
770	S<517>	-3846	417
771	S<518>	-3860	307
772	S<519>	-3874	417
773	S<520>	-3888	307
774	S<521>	-3902	417
775	S<522>	-3916	307
776	S<523>	-3930	417
777	S<524>	-3944	307
778	S<525>	-3958	417
779	S<526>	-3972	307
780	S<527>	-3986	417
781	S<528>	-4000	307
782	S<529>	-4014	417
783	S<530>	-4028	307
784	S<531>	-4042	417
785	S<532>	-4056	307
786	S<533>	-4070	417
787	S<534>	-4084	307
788	S<535>	-4098	417
789	S<536>	-4112	307
790	S<537>	-4126	417
791	S<538>	-4140	307
792	S<539>	-4154	417
793	S<540>	-4168	307
794	DUM	-4182	417
795	DUM	-4196	307
796	DUM	-4210	417
797	GOUT<16>	-4310	402
798	GOUT<15>	-4342	402
799	GOUT<14>	-4374	402
800	GOUT<13>	-4406	402

No.	Pad name	X	Y
801	GOUT<12>	-4438	402
802	GOUT<11>	-4470	402
803	GOUT<10>	-4502	402
804	GOUT<9>	-4534	402
805	GOUT<8>	-4566	402
806	GOUT<7>	-4598	402
807	GOUT<6>	-4630	402
808	GOUT<5>	-4662	402
809	GOUT<4>	-4694	402
810	GOUT<3>	-4726	402
811	GOUT<2>	-4758	402
812	GOUT<1>	-4790	402
813	Aling_mark	-4861	374
814	VGLO	-4938	402
815	VGL	-4983	402
816	IM<2>	-5028	402
817	IM<1>	-5073	402
818	IM<0>	-5118	402
819	PSWAP	-5163	402
820	RST	-5208	402
821	VGH	-5253	402
822	VDDI	-5298	402
823	VSSB	-5343	402
824	D0N	-5388	402
825	D0P	-5433	402
826	VSSB	-5478	402
827	DKN	-5523	402
828	DKP	-5568	402
829	VSSB	-5613	402
830	VSSR	-5658	402
831	VSSR	-5703	402
832	VDDB	-5748	402
833	VDDB	-5793	402
834	VDDB	-5838	402
835	VSSB	-5883	402
836	VSSB	-5973	402
837	VSSB	-5928	402

Name	X-axis	Y-axis
left mark	-4861	374
right mark	4861	374

Chip Size (without scribe line): 12250um x 950um	
Chip thickness: 250um	
Bump height: 9um	
Input Pads 1~24、611~634、752~756： 120um x 30um pitch：45um 635~726、728~741： 50um x 35um pitch：50um 742~751：50um x 50um pitch：72um	 pad：635~726
Gout Pads 25~40、595~610：120um x 17um pitch：32um	 pad：25~40
Source Pads 41~594：90um x 13um pitch：28um	 pad：41~594
Mark The left is symmetrical to the right	
View	



4. Interface setting

4.1. MCU interfaces

GC9C01 provides the 8-/9-/16-/18-bit parallel system interface for 8080-I /8080- II series, and 3-/4-line serial system interface for serial data input, QSPI and MIPI interface. The input system interface is selected by external pins IM [4:0] and the bit formal per pixel color order is selected by DBI [2:0] 3-bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [4:0] as shown in the following table.

Table 6

IM4	IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
						Register/Content	GRAM
1	0	0	0	0	8080- MCU 8bit bus interface II	D[7:10]	D[17:10] ,WRX,RDX,CSX,D/CX
1	0	0	0	1	8080- MCU 9bit bus interface II	D[7:10]	D[17: 9],WRX,RDX,CSX,D/CX
1	0	0	1	0	8080- MCU 16bit bus interface II	D[8: 1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	1	8080- MCU 18bit bus interface II	D[8: 1]	D[17: 0], WRX,RDX,CSX,D/CX
1	0	1	0	0	8080- MCU 8bit bus interface I	D[7: 0]	D[7: 0] , WRX,RDX,CSX,D/CX
1	0	1	0	1	8080- MCU 9bit bus interface I	D[7: 0]	D[8: 0] , WRX,RDX,CSX,D/CX
1	0	1	1	0	8080- MCU 16bit bus interface I	D[7: 0]	D[15: 0] , WRX,RDX,CSX,D/CX
1	0	1	1	1	8080- MCU 18bit bus interface I	D[7: 0]	D[17: 0] , WRX,RDX,CSX,D/CX
1	1	0	0	0	X	X	X
1	1	0	0	1	3-wire 9-bit data serial interface II	SDA/SDO	SCL, SDA, CSX
1	1	0	1	0	X	X	X
1	1	0	1	1	4-wire 8-bit data serial interface II	SDA/SDO	SCL, SDA, D/CX, CSX
1	1	1	0	0	Quad serial interface	SDA	SDA, D[3:1],CLK,CSX
1	1	1	0	1	3-wire 9-bit data serial interface I	SDA	SCL, SDA, CSX
1	1	1	1	0	MIPI	D0P, D0N, DKP, DKN	
1	1	1	1	1	4-wire 8-bit data serial interface I	SDA	SCL, SDA, D/CX, CSX

4.1.2. 8080-I Series Parallel Interface

GC9C01 can be accessed via 8-/9-/16-/18-bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable GC9C01 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9C01 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX=’1’, D [17:0] bits are display RAM data or command’s parameters. When D/CX=’0’, D[17:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The selection of 8080-I series parallel interface is shown as the table in the following.

Table 7

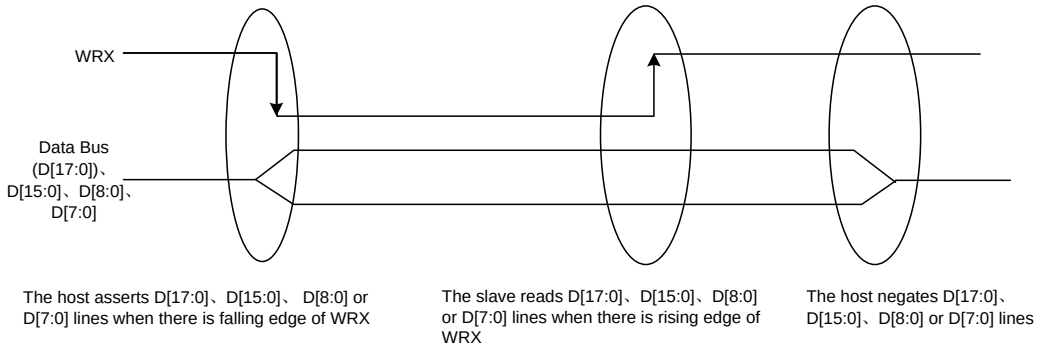
IM4	IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
1	0	1	0	0	8080 MCU 8-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
						“L”	“H”	↑	“H”	Read internal status.
						“L”	↑	“H”	“H”	Write parameter or display data.
						“L”	“H”	↑	“H”	Reads parameter or display data.
1	0	1	1	0	8080 MCU 16-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
						“L”	“H”	↑	“H”	Read internal status.
						“L”	↑	“H”	“H”	Write parameter or display data.
						“L”	“H”	↑	“H”	Reads parameter or display data.
1	0	1	0	1	8080 MCU 9-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
						“L”	“H”	↑	“H”	Read internal status.
						“L”	↑	“H”	“H”	Write parameter or display data.
						“L”	“H”	↑	“H”	Reads parameter or display data.
1	0	1	1	1	8080 MCU 18-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
						“L”	“H”	↑	“H”	Read internal status.
						“L”	↑	“H”	“H”	Write parameter or display data.
						“L”	“H”	↑	“H”	Reads parameter or display data.

4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is SRAM data or command's parameter.

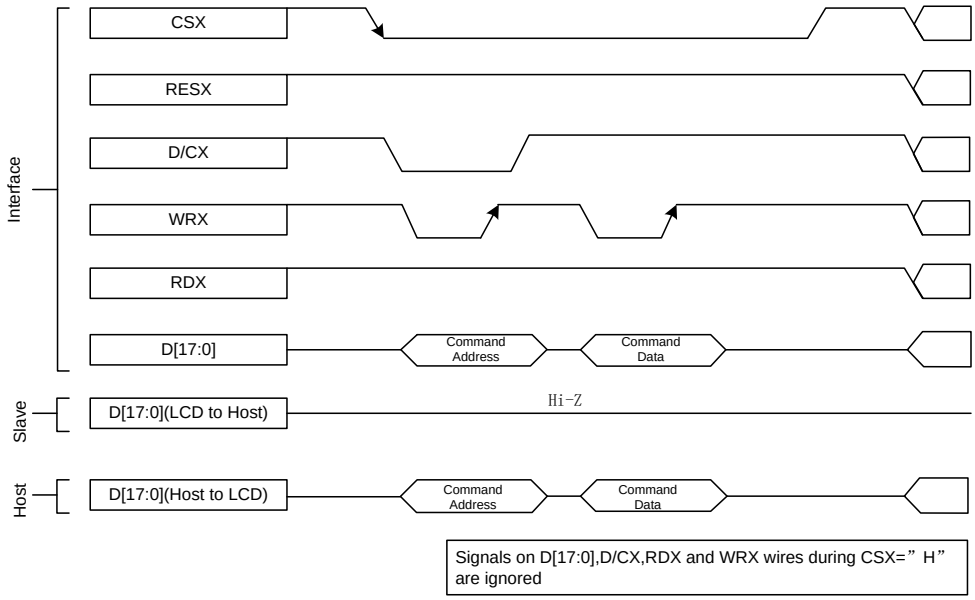
The following figure shows a write cycle for the 8080-I MCU interface.

Figure 2.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 3.

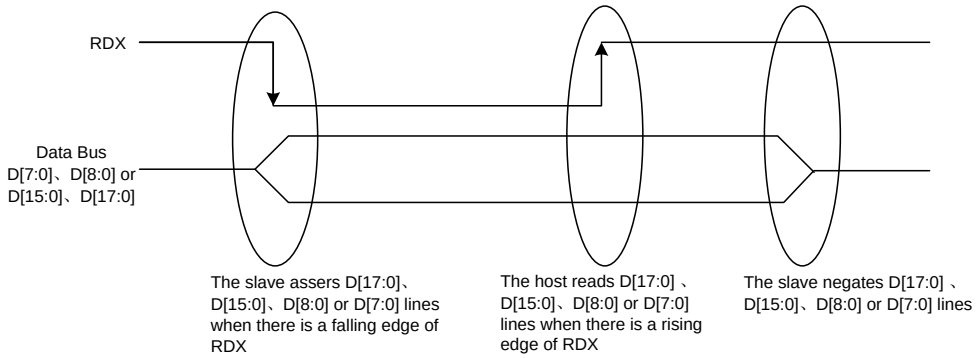


4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

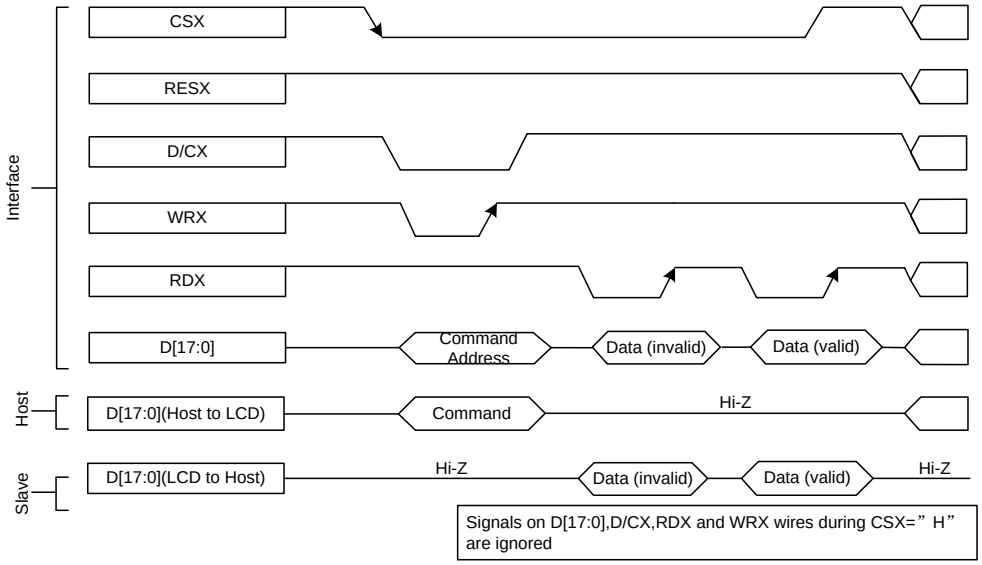
The following figure shows the read cycle for the 8080-I MCU interface.

Figure 4.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 5.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.5. 8080-Ⅱ Series Parallel Interface

GC9C01 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip select CSX (active low) is used to enable or disable GC9C01 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9C01 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX=’1’, D [17:0] bits are display RAM data or command’s parameters. When D/CX=’0’, D[17:0] bits are commands.
The 8080-II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip.
The selection of 8080-II series parallel interface is shown as the table in the following.

Table 8

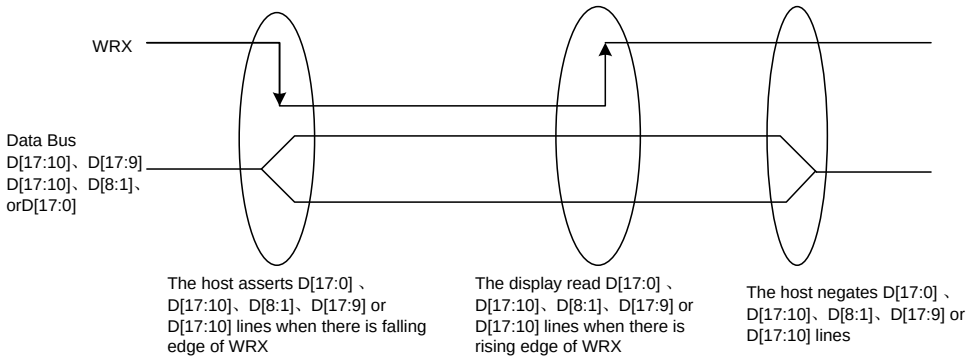
IM4	IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
1	0	0	1	0	8080 MCU 16-bit bus interface II	“L”	↑	“H”	“L”	Write command code.
						“L”	“H”	↑	“H”	Read internal status.
						“L”	↑	“H”	“H”	Write parameter or display data.
						“L”	“H”	↑	“H”	Reads parameter or display data.
1	0	0	0	0	8080 MCU 8-bit bus interface II	“L”	↑	“H”	“L”	Write command code.
						“L”	“H”	↑	“H”	Read internal status.
						“L”	↑	“H”	“H”	Write parameter or display data.
						“L”	“H”	↑	“H”	Reads parameter or display data.
1	0	0	1	1	8080 MCU 18-bit bus interface II	“L”	↑	“H”	“L”	Write command code.
						“L”	“H”	↑	“H”	Read internal status.
						“L”	↑	“H”	“H”	Write parameter or display data.
						“L”	“H”	↑	“H”	Reads parameter or display data.
1	0	0	0	1	8080 MCU 9-bit bus interface II	“L”	↑	“H”	“L”	Write command code.
						“L”	“H”	↑	“H”	Read internal status.
						“L”	↑	“H”	“H”	Write parameter or display data.
						“L”	“H”	↑	“H”	Reads parameter or display data.

4.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

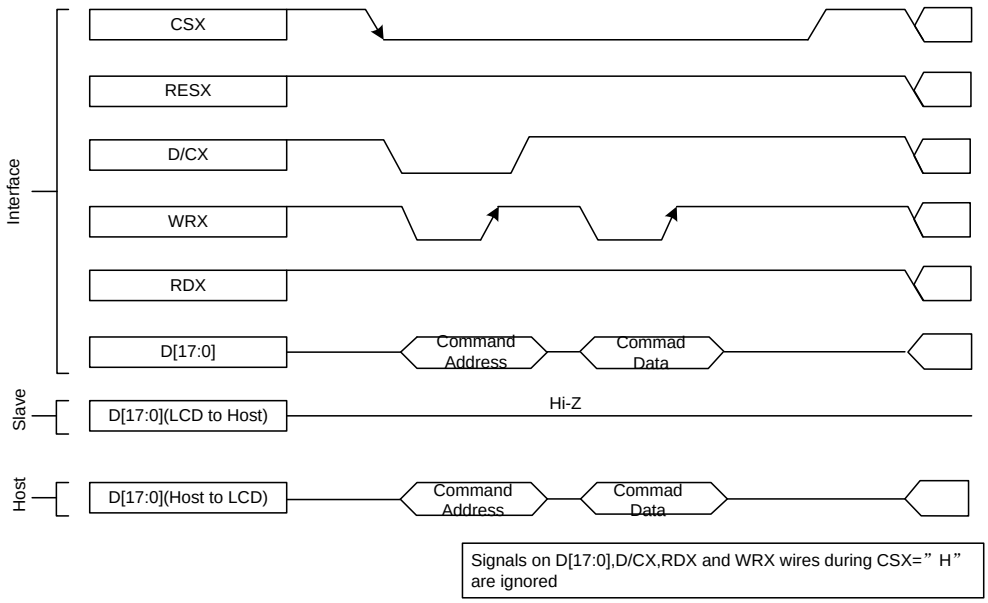
The following figure shows a write cycle for the 8080-II MCU interface.

Figure 6.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 7.

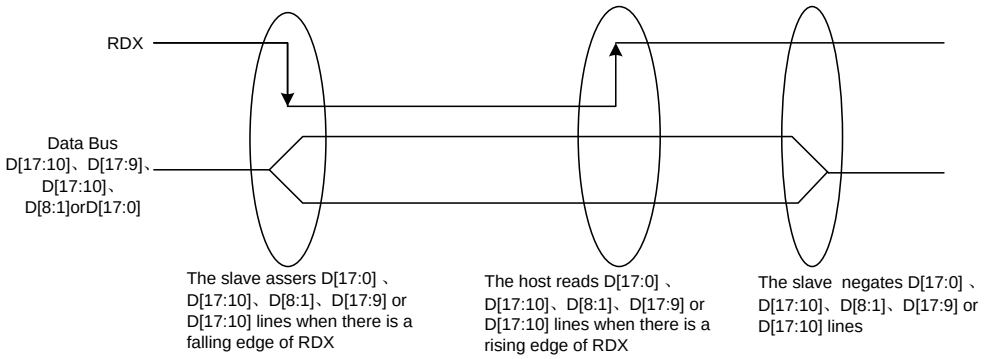


4.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

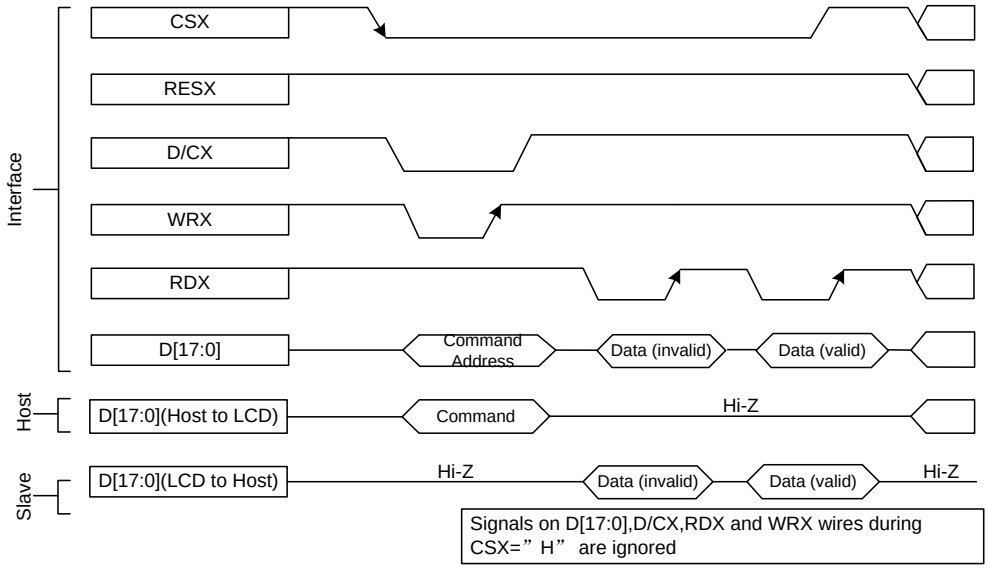
The following figure shows the read cycle for the 8080-II MCU interface.

Figure 8.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 9.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.8. Serial Interface

The selection of interface is done by IM [4:0] bits. Please refer to the Table in the following.

Table 8.

IM4	IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
1	1	1	0	1	3-line serial interface I	“L”	-	↑	Read/Write command, parameter or display data.
1	1	1	1	1	4-line serial interface I	“L”	"H/L"	↑	Read/Write command, parameter or display data.
1	1	0	0	1	3-line serial interface II	“L”	-	↑	Read/Write command, parameter or display data.
1	1	0	1	1	4-line serial interface II	“L”	"H/L"	↑	Read/Write command, parameter or display data.

GC9C01 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9C01. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to GC9C01. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to GC9C01 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Figure 10.

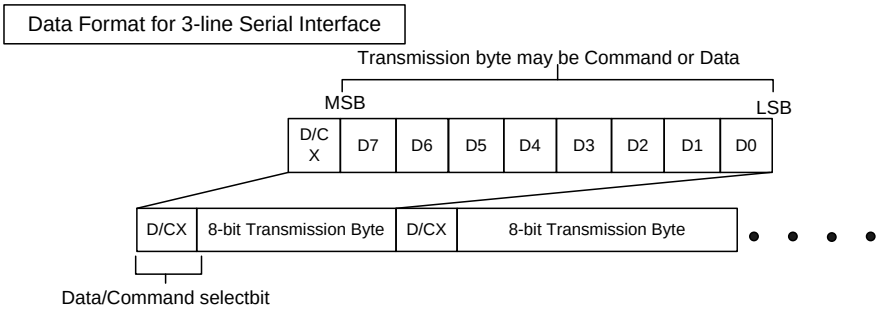
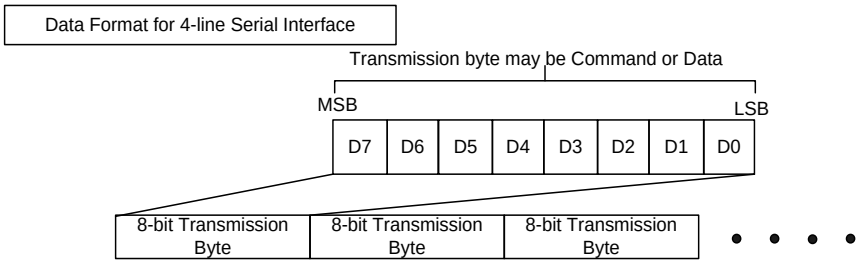


Figure11.



Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9C01 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

Figure 12.

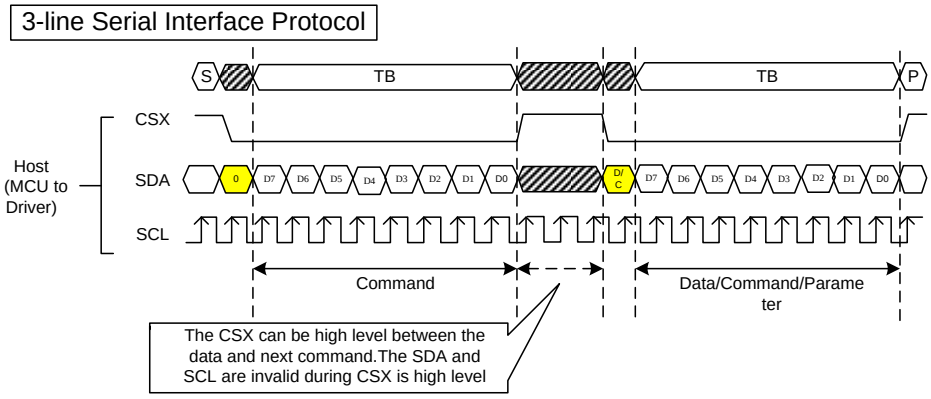
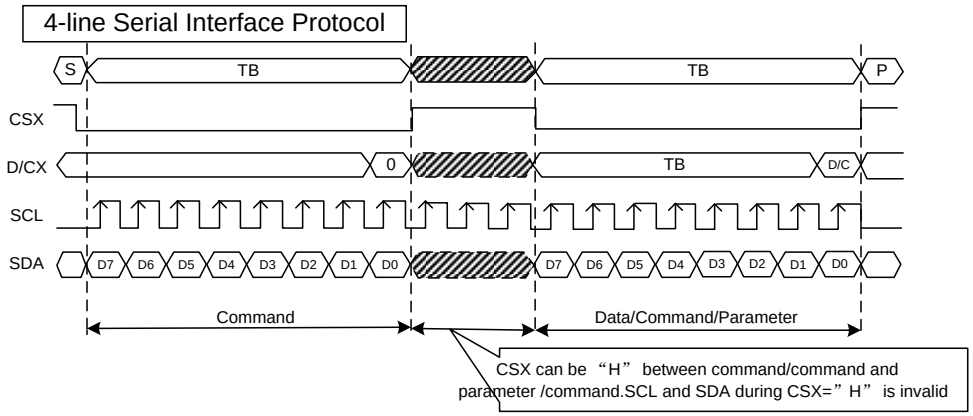


Figure 13.



4.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter from GC9C01. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9C01 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

Figure 14.

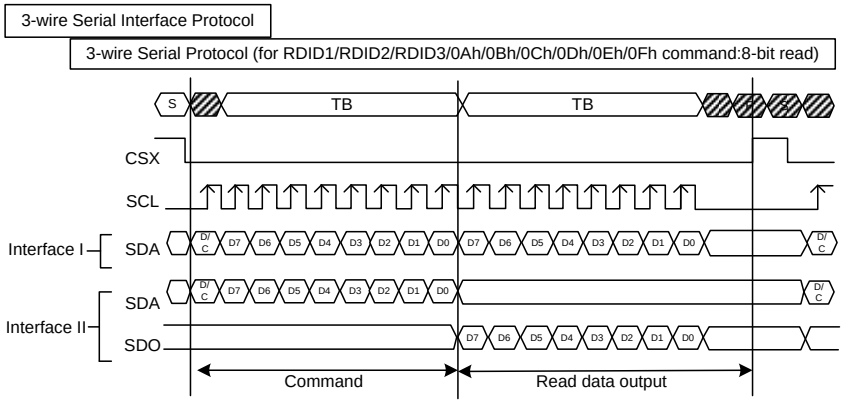


Figure 15.

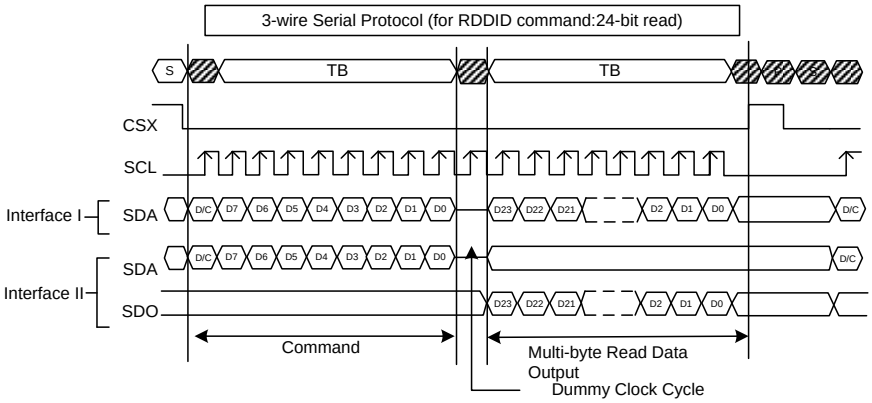


Figure 16.

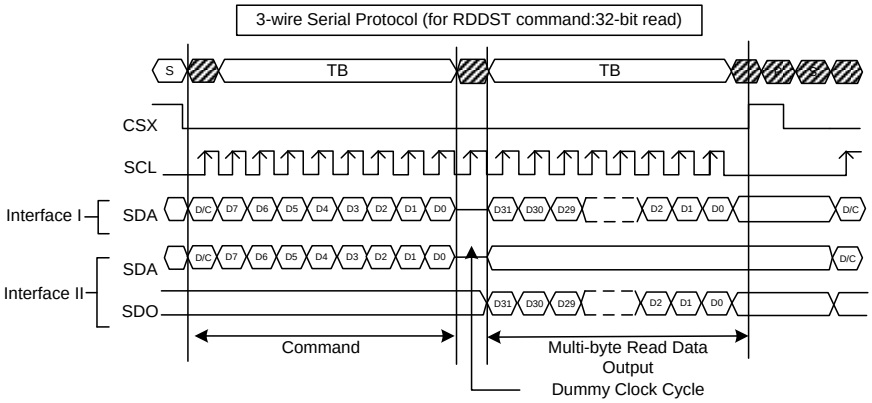


Figure 17.

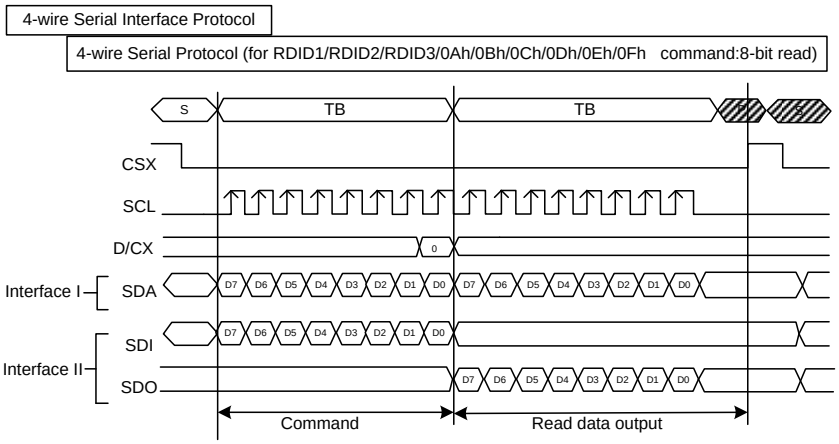


Figure 18.

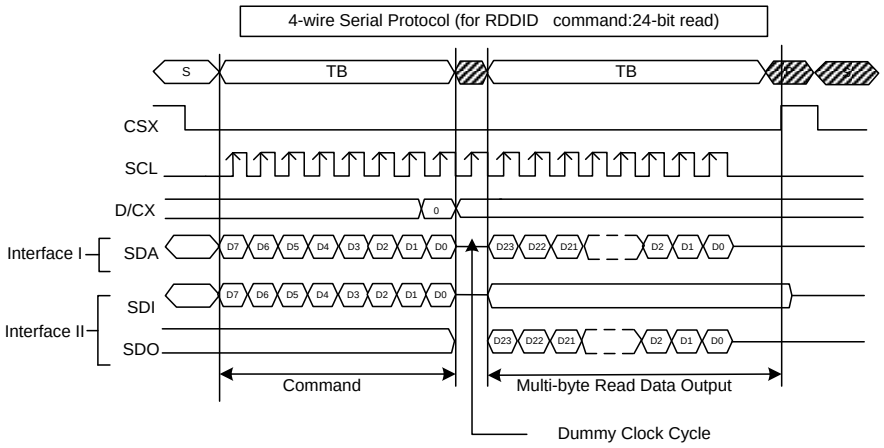
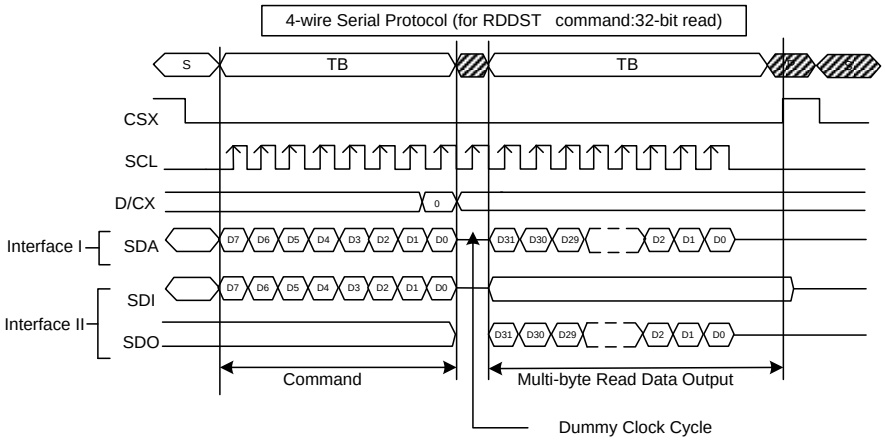


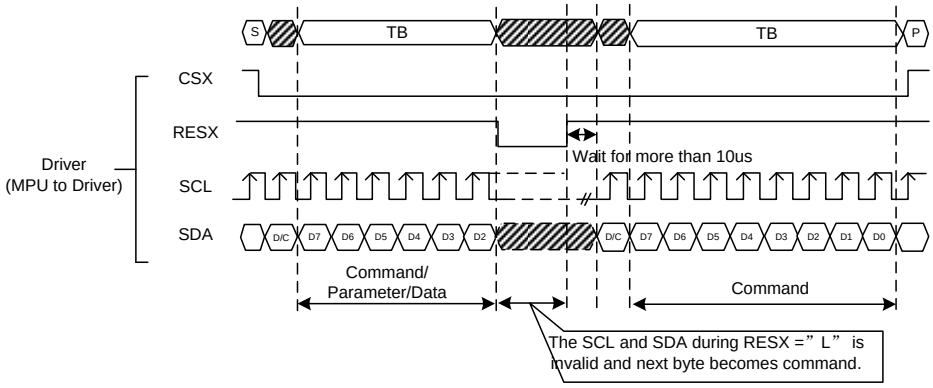
Figure 19.



4.1.11. Data Transfer Break and Recovery

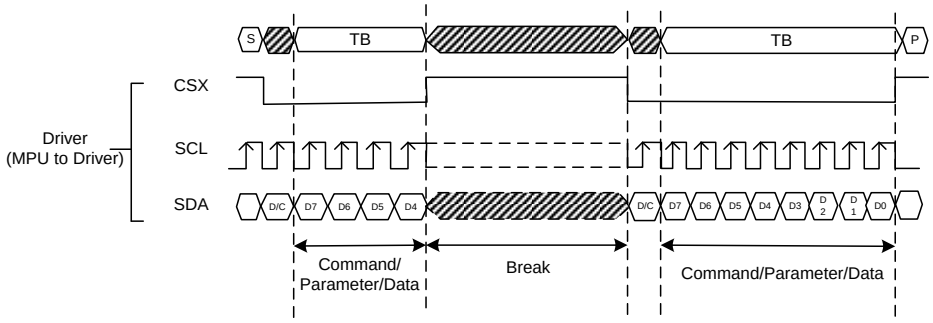
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

Figure 20.



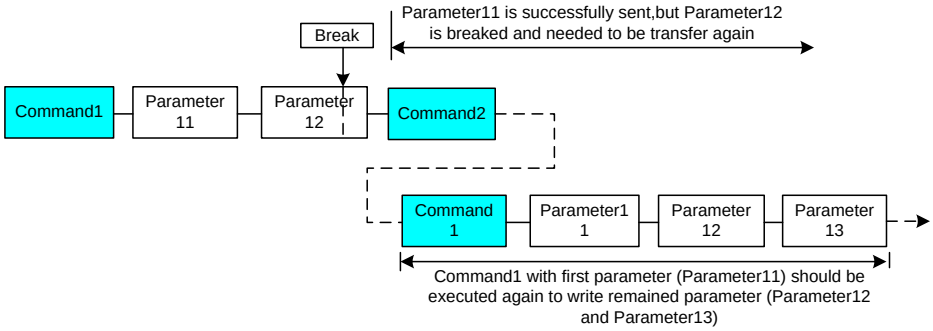
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

Figure 21.



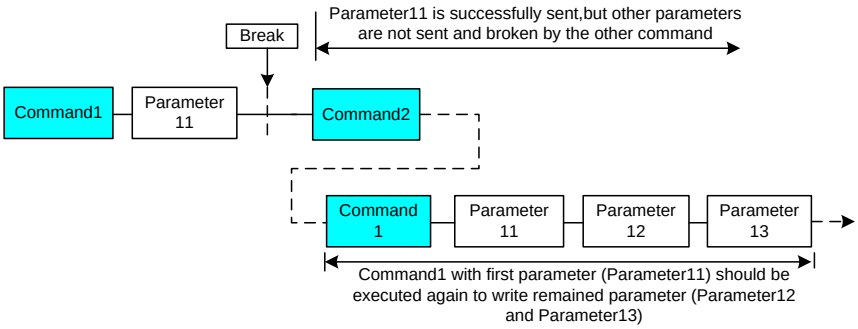
If two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

Figure 22.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

Figure 23.

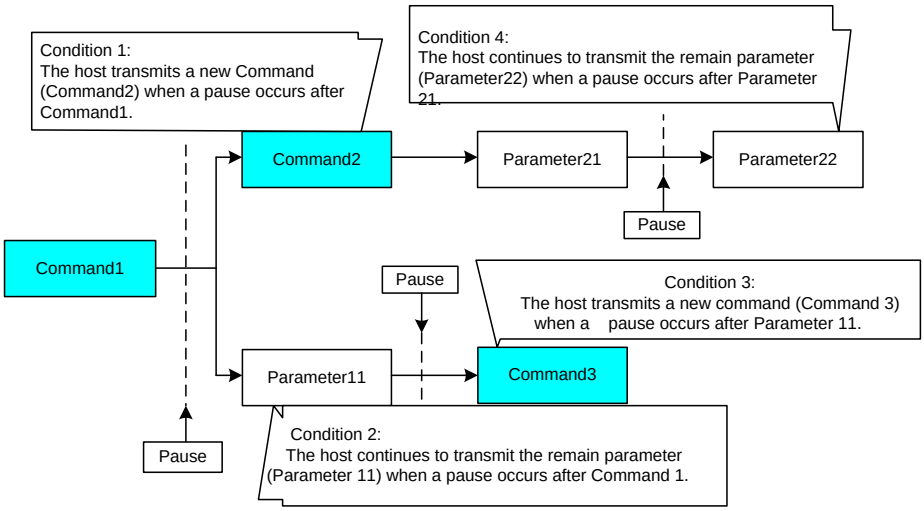


4.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9C01 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

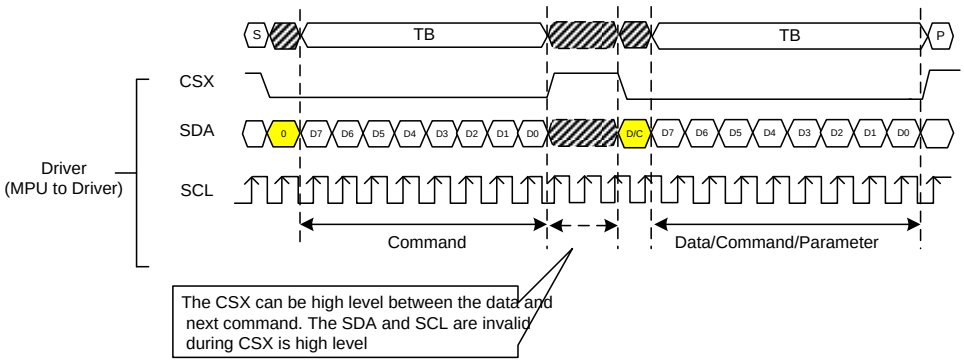
This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Figure 24.



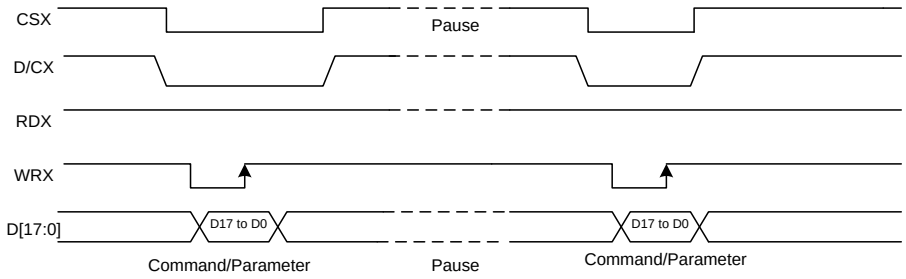
4.1.13. Serial Interface Pause (3_wire)

Figure 25.



4.1.14. Parallel Interface Pause

Figure 26.



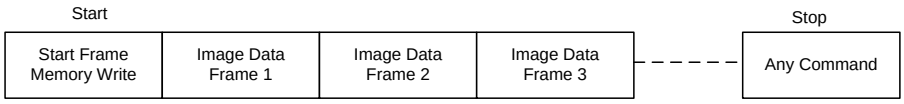
4.1.15. Data Transfer Mode

GC9C01 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

4.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.

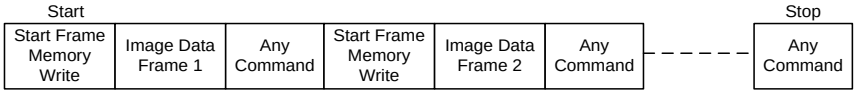
Figure 27.



4.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.

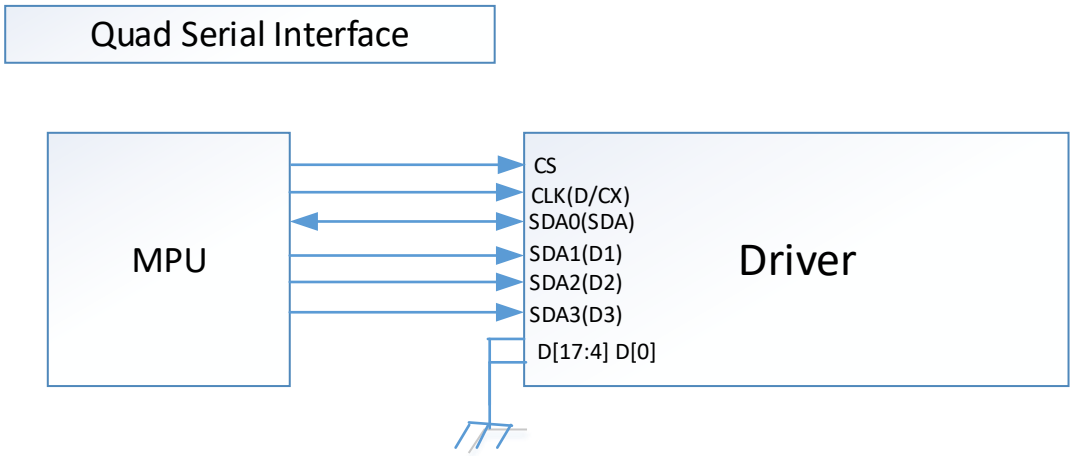
Figure 28.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

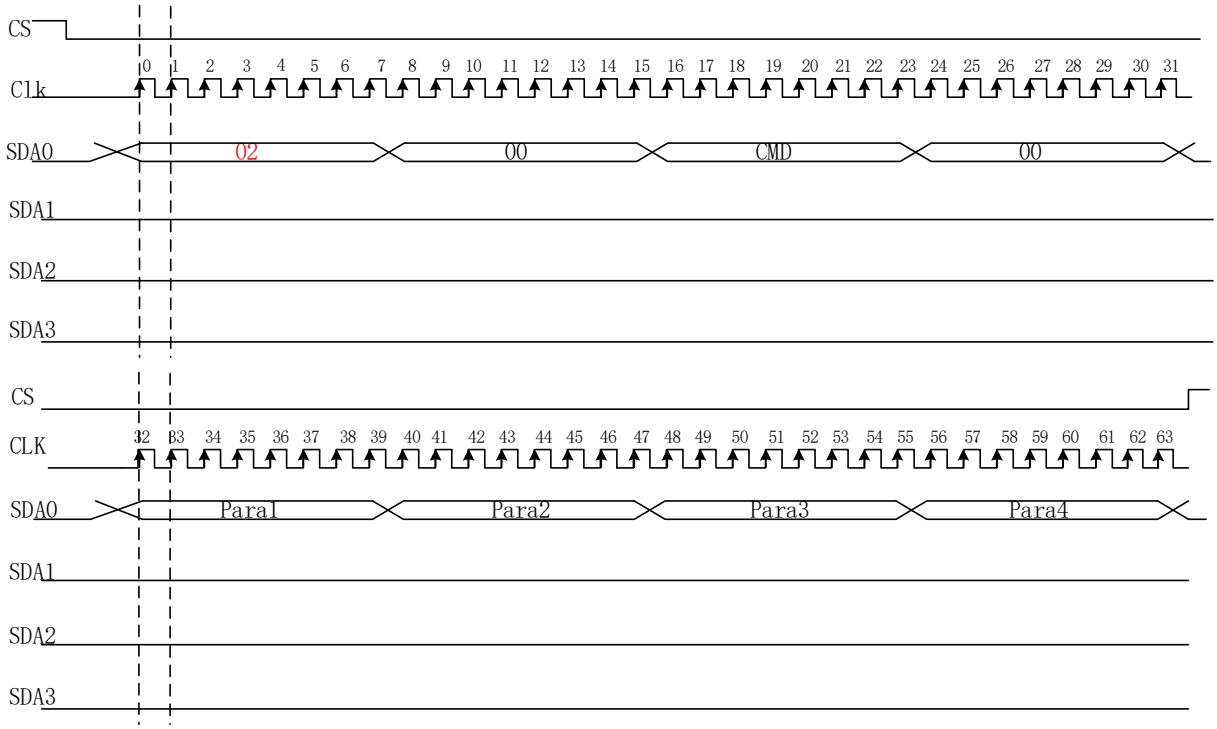
4.1.18. Quad Serial Peripheral Interface

The Quad Serial Peripheral Interface of GC9C01 can be selected by setting hardware pin IM [4:0] to “11100”. The following shown figure is the example of interface with Quad Serial Peripheral Interface.

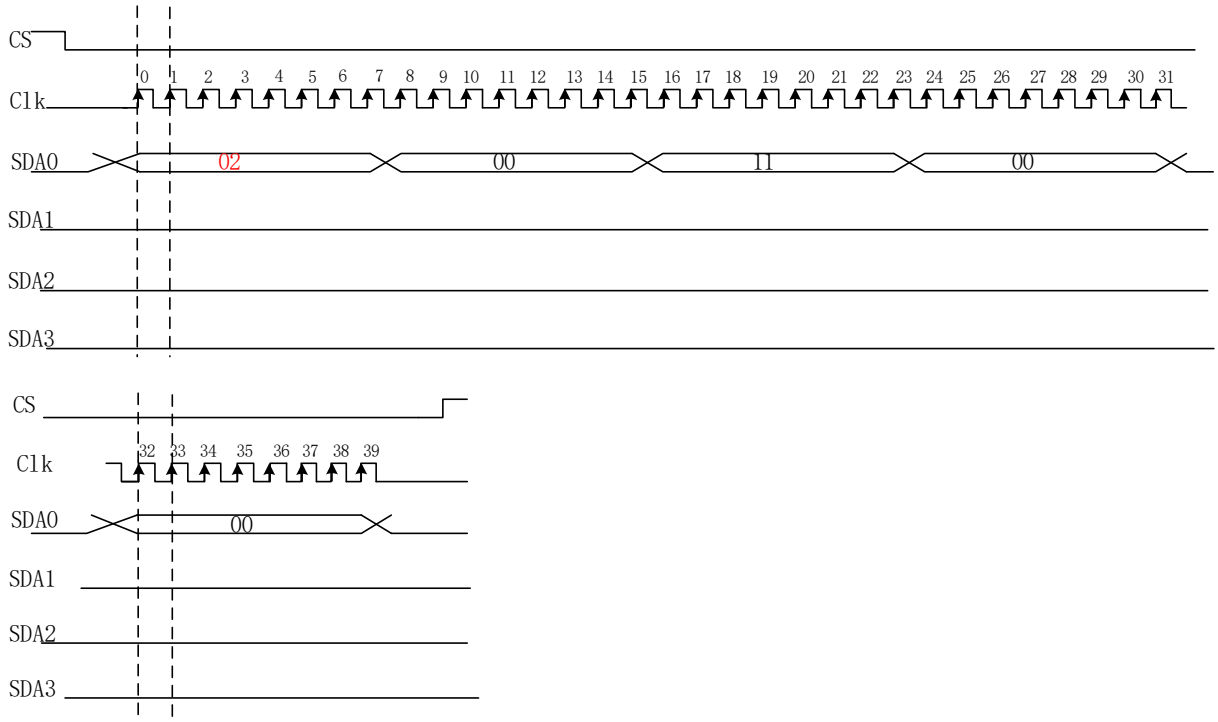


4.1.19. Write Cycle Sequence

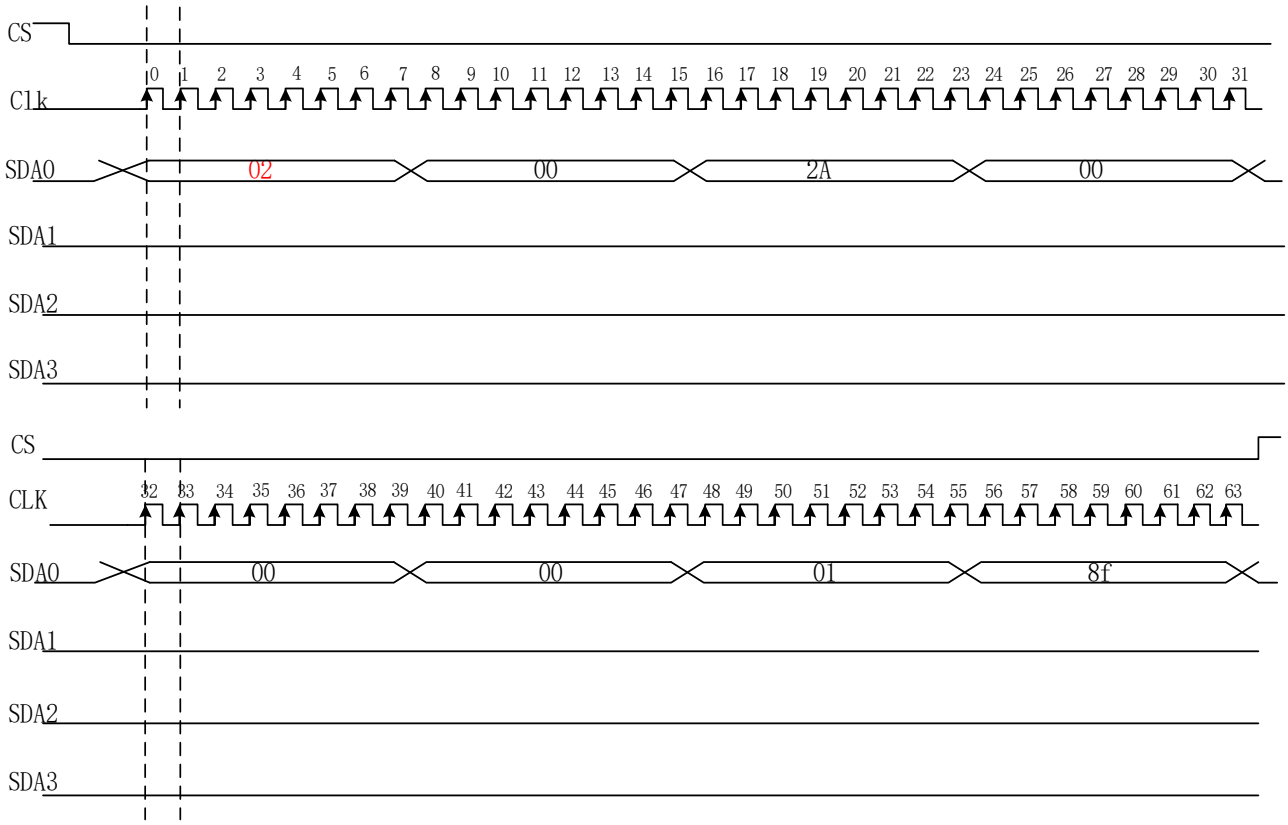
The GC9C01 reads the data at the rising edge of SCL signal.
The timing of Write Cycle Sequence is shown as below
CMD_WR only use SDA, first byte=0x02



Eg:11



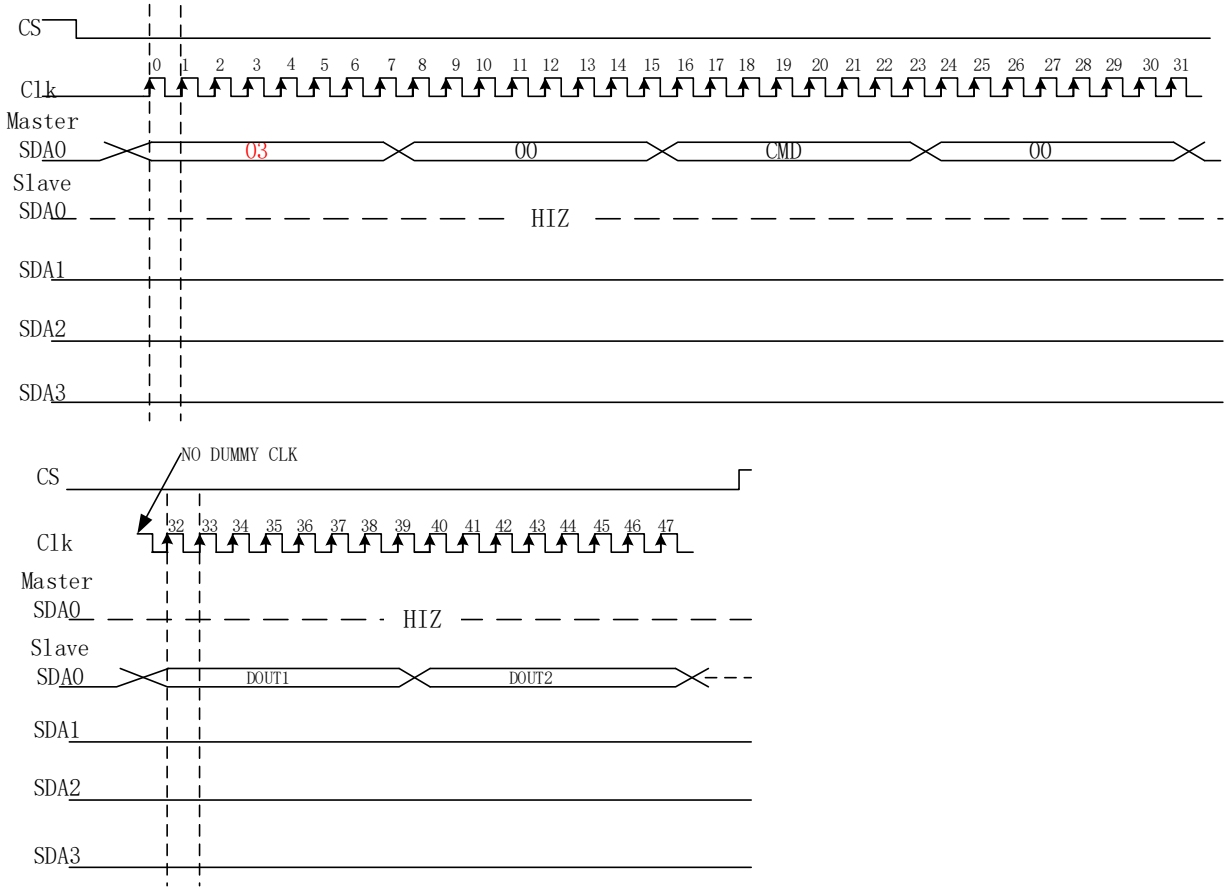
Eg:2A=00,00,01,8f



4.1.20. Read Cycle Sequence

The timing of Read Cycle Sequence is shown as below

CMD_RD: Only Use SDA0, First Byte=0x03



4.2. RGB Interface

4.2.1. RGB Interface Selection

GC9C01 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC,DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.
GC9C01 supports several pixel formats that can be selected by RIM bit of F6h command. The selection of a given interfaces is done by setting RCM [1:0] as show in the following table.

Table 9

RCM[1:0]		RIM	DPI[1:0]			RGB interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	DE Mode Valid data is determined by the DE signal	VSYNC,HSYNC,DE,DOTCLK,D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DE,DOTCLK,D[17:13] & D[11:1]
1	0	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DE,DOTCLK,D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	SYNC Mode In SYNC mode, DE signal is ignored;blanking porch is determined by B5h command	VSYNC,HSYNC,DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DOTCLK, D[17:13] & D[11:1]
1	1	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DOTCLK, D[5:0]

18-bit data bus interface (D[17:0] is used) , RIM=0

Figure 29.

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

Figure 30.

	D17	D16	D15	D14	D13	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red/blue color are same as MSB data.

6-bit data bus interface (D[5:0] is used) , RIM=1

Figure 31.

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D[17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of DOTCLK). D [17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.

Figure32.

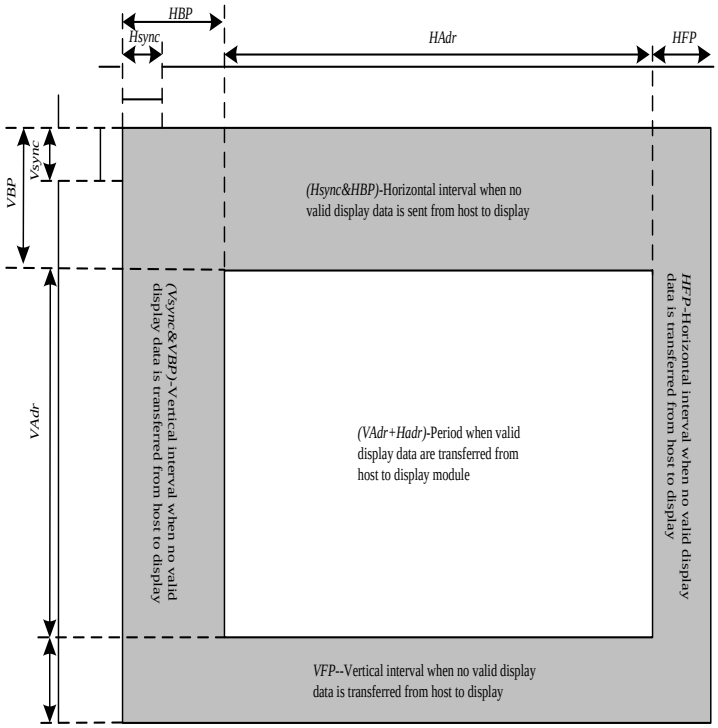


Table 10.

Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	360	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line

Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	360	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Notes:

1. Vertical period (one frame) shall be equal to the sum of VBP + VAdr + VFP.

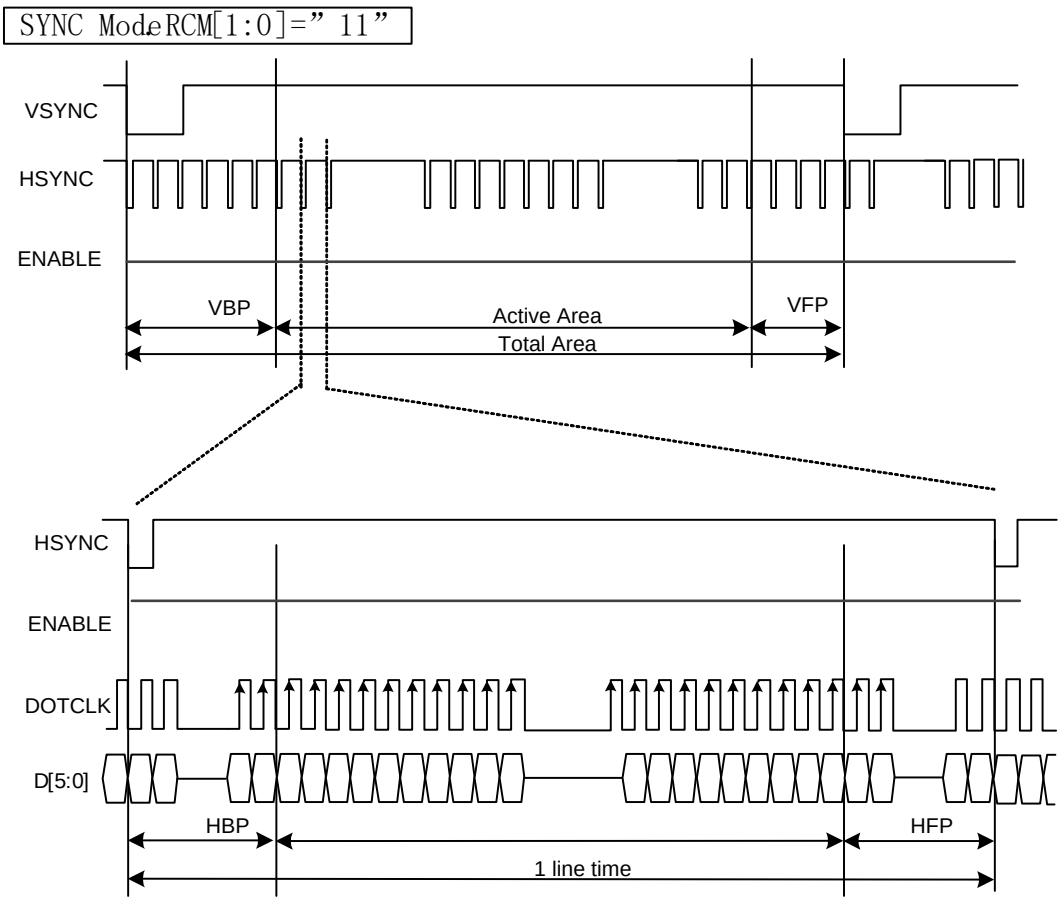
2. Horizontal period (one line) shall be equal to the sum of HBP + HAdr + HFP.

3. Control signals Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

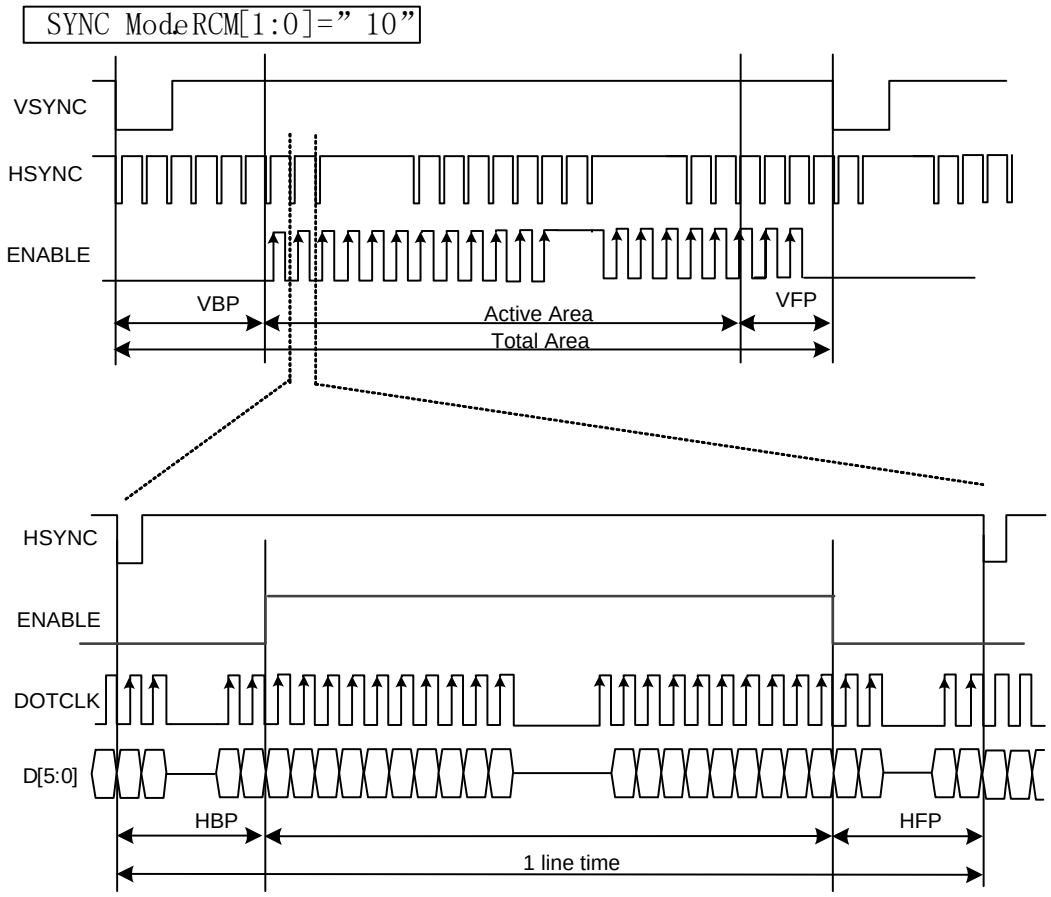
4.2.2. RGB Interface Timing

The timing chart of 18/16-bit RGB interface mode1 and mode 2 is shown as below.

Figure33.



Mode1 RGB SYNC mode



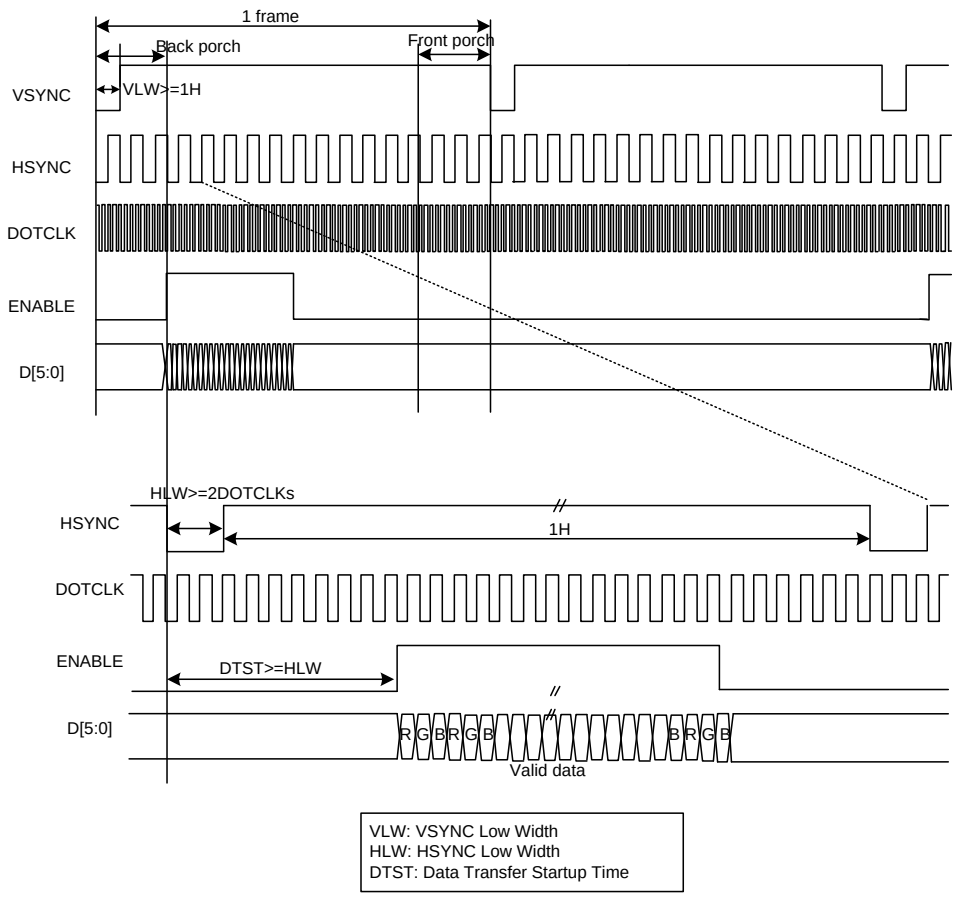
Mode2 RGB SYNC+DE mode

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:

Figure34.



Note 1: 6-bit RGB interface mode only used in the DE interface.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

4.3. Display Data RAM (DDRAM)

GC9C01 has an integrated 360x360x18-bit graphic type static RAM. This 291,600 -bytes memory allows storing a 36xRGBx360 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

4.4. Display Data Format

GC9C01 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [4:0] and RGB interface mode can be selected by software command parameters

RCM[1:0].

4.4.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9C01 can be used by setting external pin as IM [4:0] to “11101” for serial interface. The shown figure is the example of 3-line SPI interface.

Figure39.

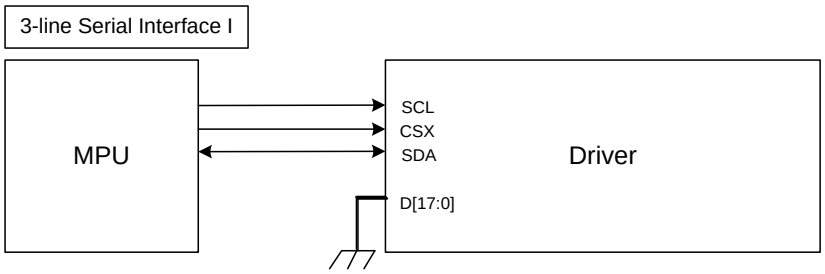
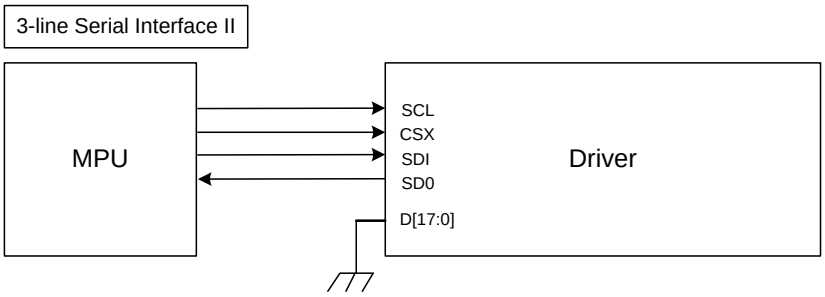


Figure40.



In 3-line serial interface, different display data format is available for three color depths supported by the LCM listed below.

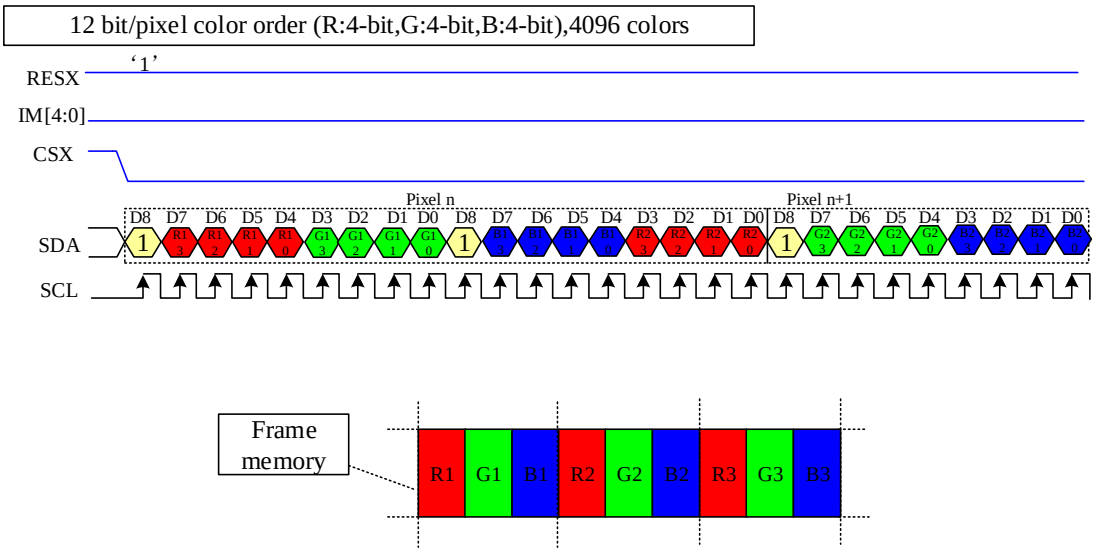
-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

1)4K-Colors:12-bit/pixel(RGB 4, 4, 4 -bits input).

Figure41.



Note 1: The pixel data with 12-bit color depth information.

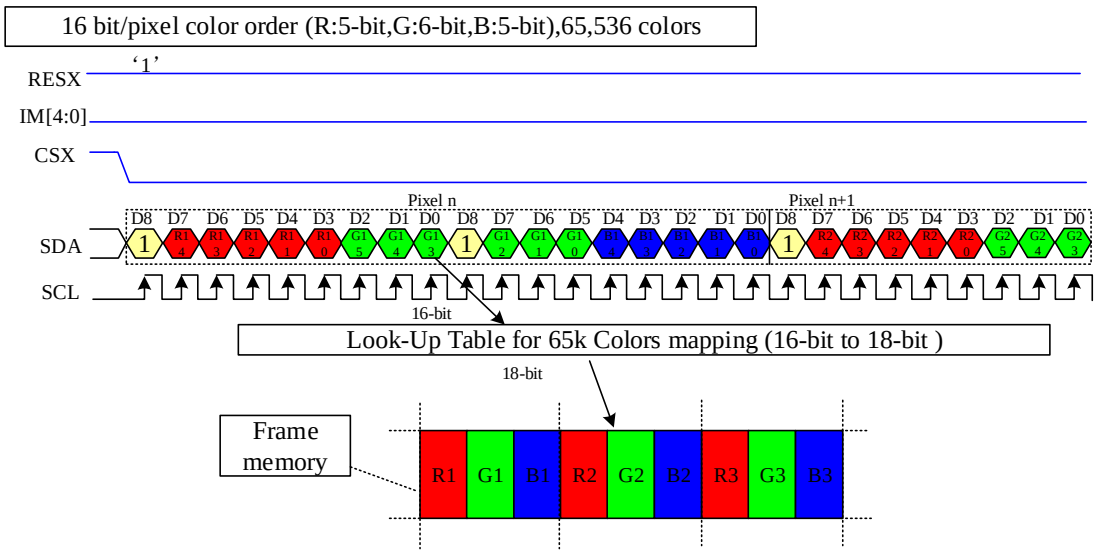
Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

2)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

Figure41.



Note 1: The pixel data with 16-bit color depth information.

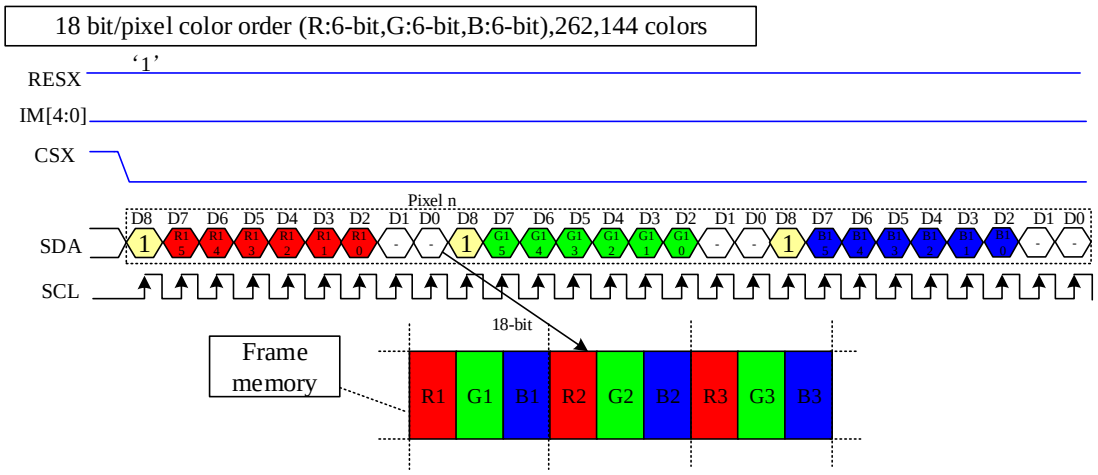
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

3)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure42.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

4.4.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9C01 can be used by setting external pin as IM [4:0] to “11111” for serial interface . The shown figure is the example of 4-line SPI interface.

Figure43.

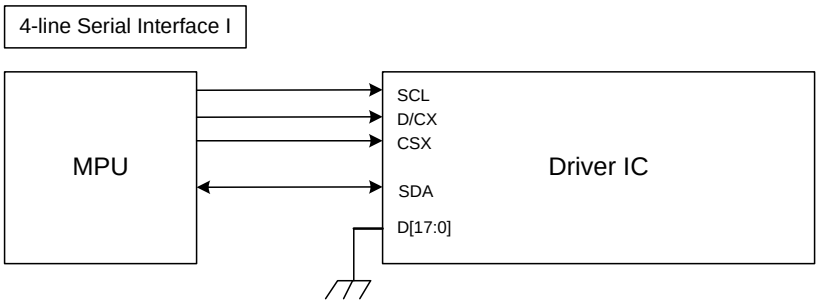
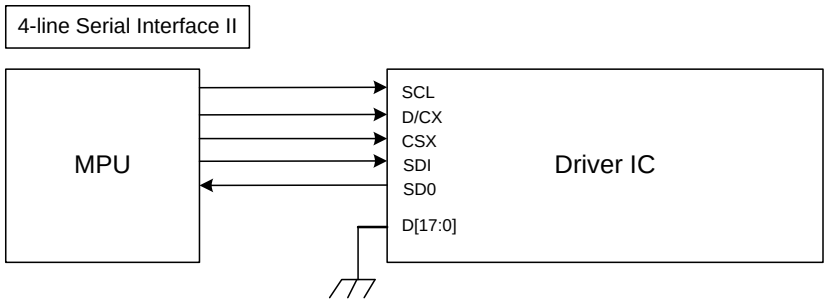


Figure44.



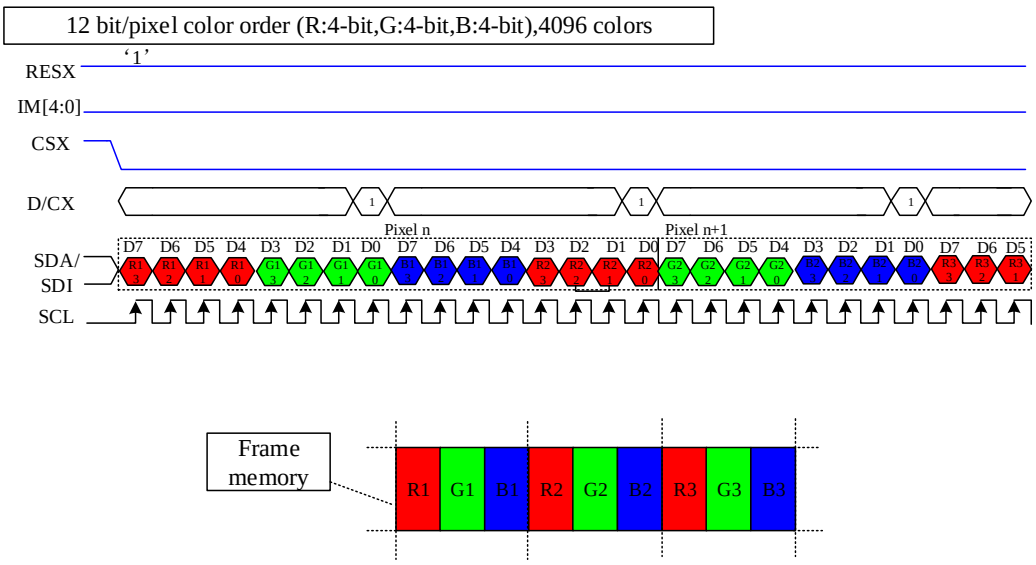
In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

Figure44.



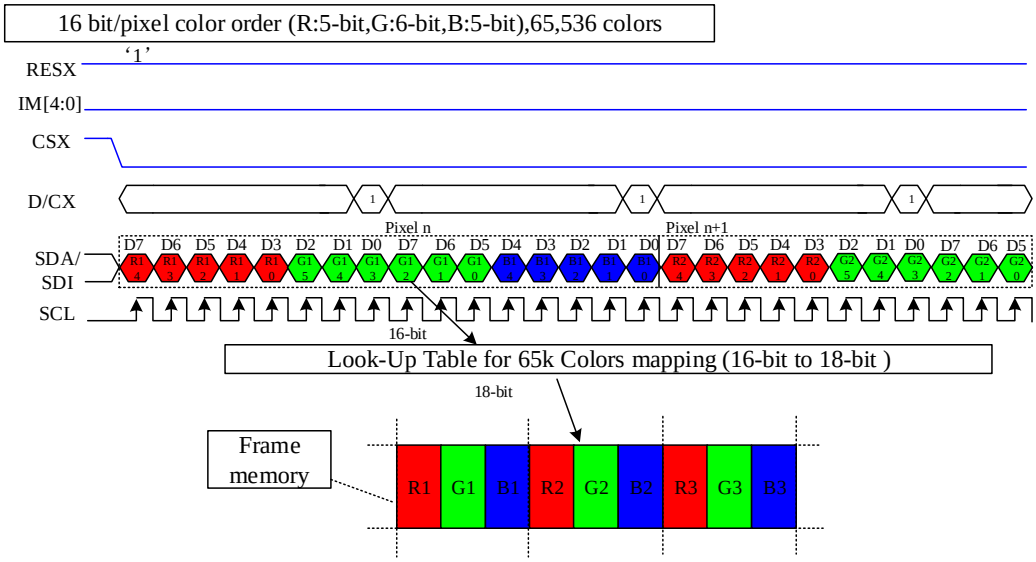
Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure45.



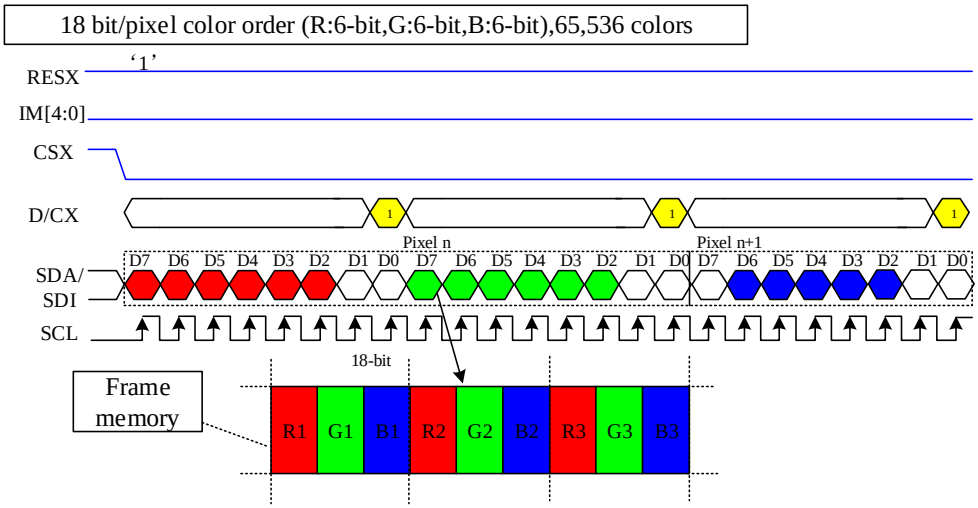
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure46.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

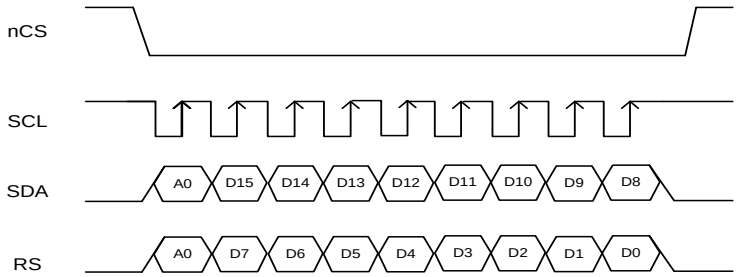
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

4.4.3. 2-data-line mode

This mode is active when 2data_en (B1h[3]) set to “1” in 3-wire. Only frame pixel data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire.
The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and DCX are serial data lines.
Serial data must be input to SDA in the sequence A0, D15 to D10 and DCX in the sequence A0, D7 to D0. The GC9C01 reads the data at the rising edge of SCL signal. The first bit of serial data A0 is data/command flag. It must be set to "1", D15 to D0 bits are display RAM data.

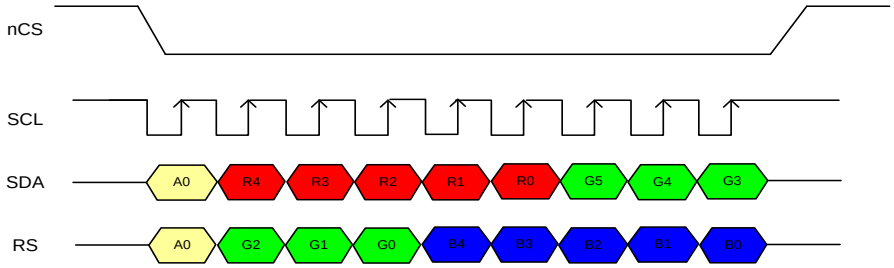
Figure47.



Five data formats are supported in 2-data-line mode, which is indicated by 2data_mdt (B1h[2:0]) .

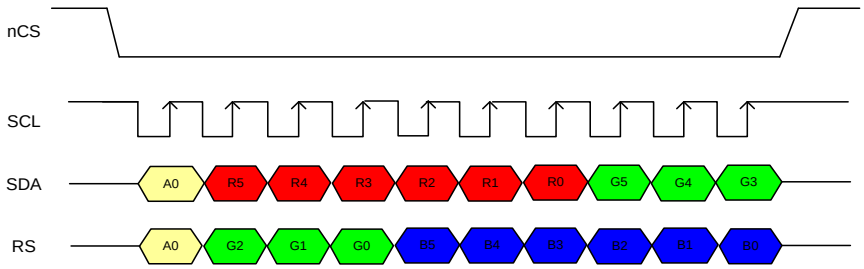
1)RGB565 1pixel/transition(65K color,2data_mdt[2:0]=’000’)

Figure48.



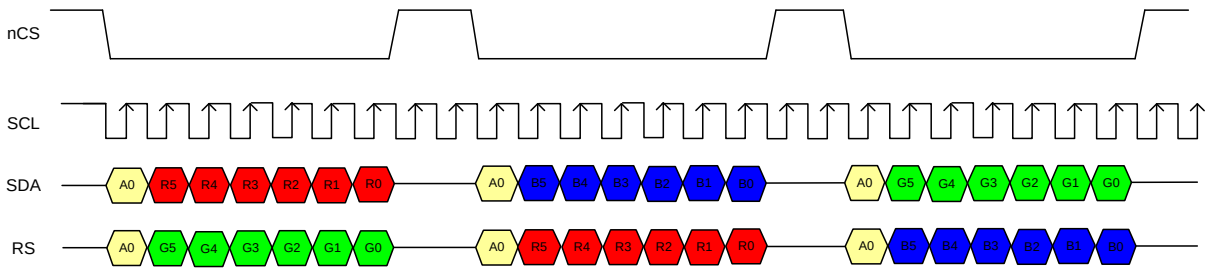
2)RGB666 1pixel/transition(262K color,2data_mdt[2:0]=’001’)

Figure49.



3)RGB666 2/3pixel/transition(262K color,2data_mdt[2:0]=’010’)

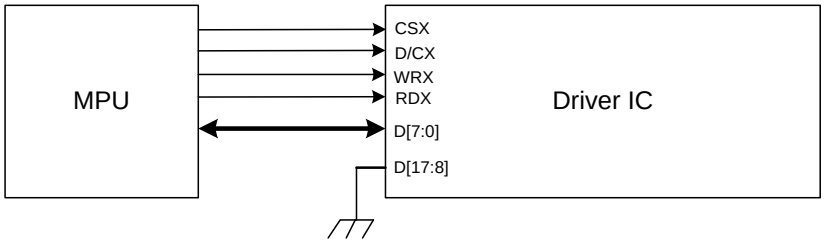
Figure50.


nCS
SCL
SDA
RS
A0 R5 R4 R3 R2 R1 R0
A0 B5 B4 B3 B2 B1 B0
A0 G5 G4 G3 G2 G1 G0
A0 G5 G4 G3 G2 G1 G0
A0 R5 R4 R3 R2 R1 R0
A0 B5 B4 B3 B2 B1 B0

4.4.4. 8-bit Parallel MCU Interface

The 8080-Ⅰsystem 8-bit parallel bus interface of GC9C01 can be used by setting external pin as IM [4:0] to“10100”.The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure53.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table 11.

Count	0	1	2	3	4	…	717	718	719	720
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	358R4	358G2	359R4	359G2
D6	C6	0R3	0G1	1R3	1G1	…	358R3	358G1	359R3	359G1
D5	C5	0R2	0G0	1R2	1G0	…	358R2	358G0	359R2	359G0
D4	C4	0R1	0B4	1R1	1B4	…	358R1	358B4	359R1	359B4
D3	C3	0R0	0B3	1R0	1B3	…	358R0	358B3	359R0	359B3
D2	C2	0G5	0B2	1G5	1B2	…	357G5	358B2	358G5	359B2
D1	C1	0G4	0B1	1G4	1B1	…	357G4	358B1	358G4	359B1
D0	C0	0G3	0B0	1G3	1B0	…	357G3	358B0	358G3	359B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

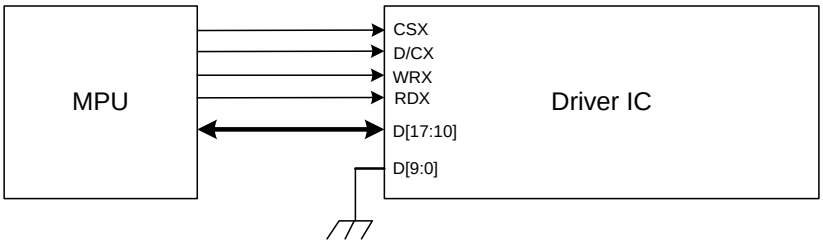
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table12.

Count	0	1	2	3	…	1078	1079	1080
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	359R5	359G5	359B5
D6	C6	0R4	0G4	0B4	…	359R4	359G4	359B4
D5	C5	0R3	0G3	0B3	…	359R3	359G3	359B3
D4	C4	0R2	0G2	0B2	…	359R2	359G2	359B2
D3	C3	0R1	0G1	0B1	…	359R1	359G1	359B1
D2	C2	0R0	0G0	0B0	…	359R0	359G0	359B0
D1	C1				…			
D0	C0				…			

The 8080-II system 8-bit parallel bus interface of GC9C01 can be used by settings as IM [4:0] =”10000”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.

Figure54.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table13.

Count	0	1	2	3	4	…	717	718	719	720
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	358R4	358G2	359R4	359G2
D16	C6	0R3	0G1	1R3	1G1	…	358R3	358G1	359R3	359G1
D15	C5	0R2	0G0	1R2	1G0	…	358R2	358G0	359R2	359G0
D14	C4	0R1	0B4	1R1	1B4	…	358R1	358B4	359R1	359B4
D13	C3	0R0	0B3	1R0	1B3	…	358R0	358B3	359R0	359B3
D12	C2	0G5	0B2	1G5	1B2	…	358G5	358B2	358G5	359B2
D11	C1	0G4	0B1	1G4	1B1	…	358G4	358B1	358G4	359B1
D10	C0	0G3	0B0	1G3	1B0	…	358G3	358B0	358G3	359B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to“110”.

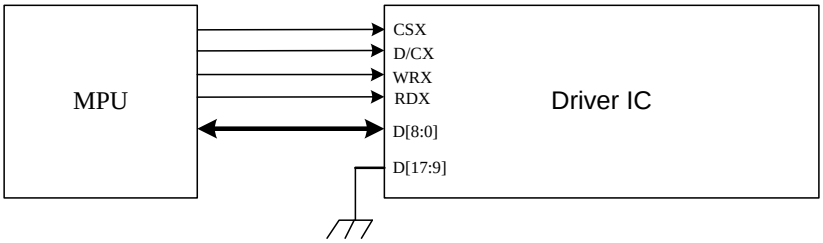
Table14.

Count	0	1	2	3	…	1078	1079	1080
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	359R5	359G5	359B5
D16	C6	0R4	0G4	0B4	…	359R4	359G4	359B4
D15	C5	0R3	0G3	0B3	…	359R3	359G3	359B3
D14	C4	0R2	0G2	0B2	…	359R2	359G2	359B2
D13	C3	0R1	0G1	0B1	…	359R1	359G1	359B1
D12	C2	0R0	0G0	0B0	…	359R0	359G0	359B0
D11	C1				…			
D10	C0				…			

4.4.5. 9-bit Parallel MCU Interface

The 8080-I system 9-bit parallel bus interface of GC9C01 can be selected by setting hardware pin IM [4:0] to "10101". The following shown figure is the example of interface with 8080- Ⅰ MCU system interface.

Figure55.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

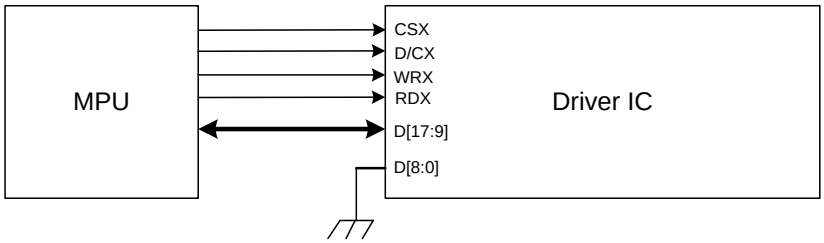
There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

Table15.

Count	0	1	2	3	4	…	717	718	719	720
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2	…	358R5	358G2	359R5	359G2
D7	C7	0R4	0G1	1R4	1G1	…	358R4	358G1	359R4	359G1
D6	C6	0R3	0G0	1R3	1G0	…	358R3	358G0	359R3	359G0
D5	C5	0R2	0B5	1R2	1B5	…	358R2	358B5	359R2	359B5
D4	C4	0R1	0B4	1R1	1B4	…	358R1	358B4	359R1	359B4
D3	C3	0R0	0B3	1R0	1B3	…	358R0	358B3	359R0	359B3
D2	C2	0G5	0B2	1G5	1B2	…	358G5	358B2	359G5	359B2
D1	C1	0G4	0B1	1G4	1B1	…	358G4	358B1	359G4	359B1
D0	C0	0G3	0B0	1G3	1B0	…	358G3	358B0	359G3	359B0

The 8080- Ⅱ system 9-bit parallel bus interface of GC9C01 can be selected by setting hardware pin IM [4:0] to “10001”. The following shown figure is the example of interface with 8080- MCU system interface.

Figure56.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to “110”.

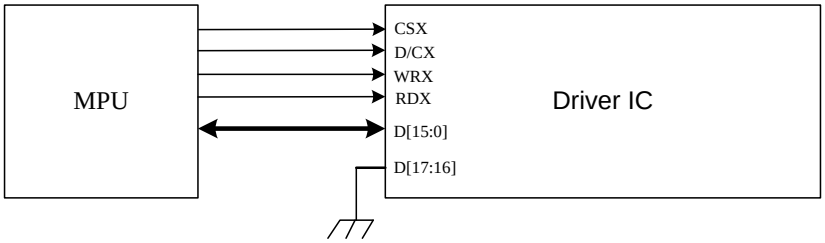
Table16.

Count	0	1	2	3	4	…	717	718	719	720
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	…	358R5	358G2	359R5	359G2
D16	C6	0R4	0G1	1R4	1G1	…	358R4	358G1	359R4	359G1
D15	C5	0R3	0G0	1R3	1G0	…	358R3	358G0	359R3	359G0
D14	C4	0R2	0B5	1R2	1B5	…	358R2	358B5	359R2	359B5
D13	C3	0R1	0B4	1R1	1B4	…	358R1	358B4	359R1	359B4
D12	C2	0R0	0B3	1R0	1B3	…	358R0	358B3	359R0	359B3
D11	C1	0G5	0B2	1G5	1B2	…	358G5	358B2	358G5	359B2
D10	C0	0G4	0B1	1G4	1B1	…	358G4	358B1	358G4	359B1
D9		0G3	0B0	1G3	1B0	…	358G3	358B0	358G3	359B0

4.4.6. 16-bit Parallel MCU Interface

The 8080-Ⅰ system 16-bit parallel bus interface of GC9C01 can be selected by setting hardware pin IM4:0] to "10110".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure57.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Table17.

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	357R4	358R4	359R4
D14		0R3	1R3	2R3	…	357R3	358R3	359R3
D13		0R2	1R2	2R2	…	357R2	358R2	359R2
D12		0R1	1R1	2R1	…	357R1	358R1	359R1
D11		0R0	1R0	2R0	…	357R0	358R0	359R0
D10		0G5	1G5	2G5	…	357G5	358G5	359G5
D9		0G4	1G4	2G4	…	357G4	358G4	359G4
D8		0G3	1G3	2G3	…	357G3	358G3	359G3
D7	C7	0G2	1G2	2G2	…	357G2	358G2	359G2
D6	C6	0G1	1G1	2G1	…	357G1	358G1	359G1
D5	C5	0G0	1G0	2G0	…	357G0	358G0	359G0
D4	C4	0B4	1B4	2B4	…	357B4	358B4	359B4
D3	C3	0B3	1B3	2B3	…	357B3	358B3	359B3
D2	C2	0B2	1B2	2B2	…	357B2	358B2	359B2
D1	C1	0B1	1B1	2B1	…	357B1	358B1	359B1
D0	C0	0B0	1B0	2B0	…	357B0	358B0	359B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

1)MDT[1:0]="00"

Table18.

Count	0	1	2	3	…	538	539	540
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	358R5	358B5	359G5
D14		0R4	0B4	1G4	…	358R4	358B4	359G4
D13		0R3	0B3	1G3	…	358R3	358B3	359G3
D12		0R2	0B2	1G2	…	358R2	358B2	359G2
D11		0R1	0B1	1G1	…	358R1	358B1	359G1
D10		0R0	0B0	1G0	…	358R0	358B0	359G0
D9								
D8								
D7	C7	0G5	1R5	1B5	…	358G5	359R5	359B5
D6	C6	0G4	1R4	1B4	…	358G4	359R4	359B4
D5	C5	0G3	1R3	1B3	…	358G3	359R3	359B3
D4	C4	0G2	1R2	1B2	…	358G2	359R2	359B2
D3	C3	0G1	1R1	1B1	…	358G1	359R1	359B1
D2	C2	0G0	1R0	1B0	…	358G0	359R0	359B0
D1	C1							
D0	C0							

2)MDT[1:0]="01"

Table19.

Count	0	1	2	3		…	717	718	719	720
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B5	1R5	1B5	…	358R5	358B5	359R5	359B5
D14		0R4	0B4	1R4	1B4	…	358R4	358B4	359R4	359B4
D13		0R3	0B3	1R3	1B3	…	358R3	358B3	359R3	359B3
D12		0R2	0B2	1R2	1B2	…	358R2	358B2	359R2	359B2
D11		0R1	0B1	1R1	1B1	…	358R1	358B1	359R1	359B1
D10		0R0	0B0	1R0	1B0	…	358R0	358B0	359R0	359B0
D9						…				
D8						…				
D7	C7	0G5		1G5		…	358G5		359G5	
D6	C6	0G4		1G4		…	358G4		359G4	
D5	C5	0G3		1G3		…	358G3		359G3	
D4	C4	0G2		1G2		…	358G2		359G2	
D3	C3	0G1		1G1		…	358G1		359G1	
D2	C2	0G0		1G0		…	358G0		359G0	
D1	C1					…				
D0	C0					…				

3)MDT[1:0]="10"

Table20.

Count	0	1	2	3		…	717	718	719	720
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B1	1R5	1B1	…	358R5	358B1	359R5	359B1
D14		0R4	0B0	1R4	1B0	…	358R4	358B0	359R4	359B0
D13		0R3		1R3		…	358R3		359R3	
D12		0R2		1R2		…	358R2		359R2	
D11		0R1		1R1		…	358R1		359R1	
D10		0R0		1R0		…	358R0		359R0	
D9		0G5		1G5		…	358G5		359G5	
D8		0G4		1G4		…	358G4		359G4	
D7	C7	0G3		1G3		…	358G3		359G3	
D6	C6	0G2		1G2		…	358G2		359G2	
D5	C5	0G1		1G1		…	358G1		359G1	
D4	C4	0G0		1G0		…	358G0		359G0	
D3	C3	0B5		1B5		…	358B5		359B5	
D2	C2	0B4		1B4		…	358B4		359B4	
D1	C1	0B3		1B3		…	358B3		359B3	
D0	C0	0B2		1B2		…	358B2		359B2	

4)MDT[1:0]="11"

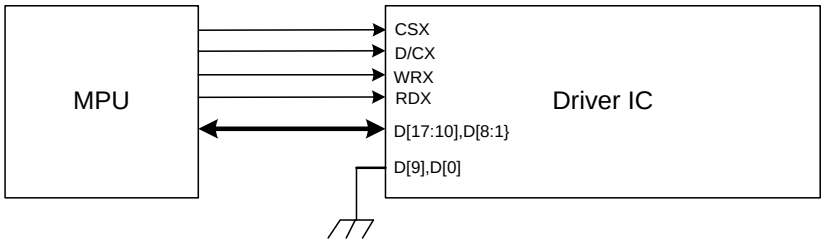
Table21.

Count	0	1	2	3		…	717	718	719	720
D/CX	0	1	1	1		…	1	1	1	1
D15			0R3		1R3	…		358R3		359R3
D14			0R2		1R2	…		358R2		359R2
D13			0R1		1R1	…		358R1		359R1
D12			0R0		1R0	…		358R0		359R0
D11			0G5		1G5	…		358G5		359G5
D10			0G4		1G4	…		358G4		359G4
D9			0G3		1G3	…		358G3		359G3
D8			0G2		1G2	…		358G2		359G2
D7	C7		0G1		1G1	…		358G1		359G1
D6	C6		0G0		1G0	…		358G0		359G0
D5	C5		0B5		1B5	…		358B5		359B5
D4	C4		0B4		1B4	…		358B4		359B4
D3	C3		0B3		1B3	…		358B3		359B3
D2	C2		0B2		1B2	…		358B2		359B2
D1	C1	0R5	0B1	1R5	1B1	…	358R5	358B1	359R5	359B1
D0	C0	0R4	0B0	1R4	1B0	…	358R4	358B0	359R4	359B0

The 8080-II system 16-bit parallel bus interface of GC9C01 can be selected by settings IM [4:0] ="10010".

The following shown figure is the example of interface with 8080- MCU system interface.

Figure58.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table22.

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17		0R4	1R4	2R4	…	357R4	358R4	359R4
D16		0R3	1R3	2R3	…	357R3	358R3	359R3
D15		0R2	1R2	2R2	…	357R2	358R2	359R2
D14		0R1	1R1	2R1	…	357R1	358R1	359R1
D13		0R0	1R0	2R0	…	357R0	358R0	359R0
D12		0G5	1G5	2G5	…	357G5	358G5	359G5
D11		0G4	1G4	2G4	…	357G4	358G4	359G4
D10		0G3	1G3	2G3	…	357G3	358G3	359G3
D8	C7	0G2	1G2	2G2	…	357G2	358G2	359G2
D7	C6	0G1	1G1	2G1	…	357G1	358G1	359G1
D6	C5	0G0	1G0	2G0	…	357G0	358G0	359G0
D5	C4	0B4	1B4	2B4	…	357B4	358B4	359B4
D4	C3	0B3	1B3	2B3	…	357B3	358B3	359B3
D3	C2	0B2	1B2	2B2	…	357B2	358B2	359B2
D2	C1	0B1	1B1	2B1	…	357B1	358B1	359B1
D1	C0	0B0	1B0	2B0	…	357B0	358B0	359B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

1)MDT[1:0]=00

Table23.

Count	0	1	2	3	…	538	539	540
D/CX	0	1	1	1	…	1	1	1
D17		0R5	0B5	1G5	…	358R5	358B5	359G5
D16		0R4	0B4	1G4	…	358R4	358B4	359G4
D15		0R3	0B3	1G3	…	358R3	358B3	359G3
D14		0R2	0B2	1G2	…	358R2	358B2	359G2

D13		0R1	0B1	1G1	…	358R1	358B1	359G1
D12		0R0	0B0	1G0	…	358R0	358B0	359G0
D11								
D10								
D8	C7	0G5	1R5	1B5	…	358G5	359R5	359B5
D7	C6	0G4	1R4	1B4	…	358G4	359R4	359B4
D6	C5	0G3	1R3	1B3	…	358G3	359R3	359B3
D5	C4	0G2	1R2	1B2	…	358G2	359R2	359B2
D4	C3	0G1	1R1	1B1	…	358G1	359R1	359B1
D3	C2	0G0	1R0	1B0	…	358G0	359R0	359B0
D2	C1							
D1	C0							

2)MDT[1:0]=01

Table24.

Count	0	1	2	3		…	717	718	719	720
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B5	1R5	1B5	…	358R5	358B5	359R5	359B5
D16		0R4	0B4	1R4	1B4	…	358R4	358B4	359R4	359B4
D15		0R3	0B3	1R3	1B3	…	358R3	358B3	359R3	359B3
D14		0R2	0B2	1R2	1B2	…	358R2	358B2	359R2	359B2
D13		0R1	0B1	1R1	1B1	…	358R1	358B1	359R1	359B1
D12		0R0	0B0	1R0	1B0	…	358R0	358B0	359R0	359B0
D11						…				
D10						…				
D8	C7	0G5		1G5		…	358G5		359G5	
D7	C6	0G4		1G4		…	358G4		359G4	
D6	C5	0G3		1G3		…	358G3		359G3	
D5	C4	0G2		1G2		…	358G2		359G2	
D4	C3	0G1		1G1		…	358G1		359G1	
D3	C2	0G0		1G0		…	358G0		359G0	
D2	C1					…				
D1	C0					…				

3)MDT[1:0]=10

Table25.

Count	0	1	2	3		…	717	718	719	720
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B1	1R5	1B1	…	358R5	358B1	359R5	359B1
D16		0R4	0B0	1R4	1B0	…	358R4	358B0	359R4	359B0
D15		0R3		1R3		…	358R3		359R3	
D14		0R2		1R2		…	358R2		359R2	
D13		0R1		1R1		…	358R1		359R1	
D12		0R0		1R0		…	358R0		359R0	
D11		0G5		1G5		…	358G5		359G5	
D10		0G4		1G4		…	358G4		359G4	
D8	C7	0G3		1G3		…	358G3		359G3	
D7	C6	0G2		1G2		…	358G2		359G2	
D6	C5	0G1		1G1		…	358G1		359G1	
D5	C4	0G0		1G0		…	358G0		359G0	
D4	C3	0B5		1B5		…	358B5		359B5	
D3	C2	0B4		1B4		…	358B4		359B4	
D2	C1	0B3		1B3		…	358B3		359B3	
D1	C0	0B2		1B2		…	358B2		359B2	

4)MDT[1:0]=11

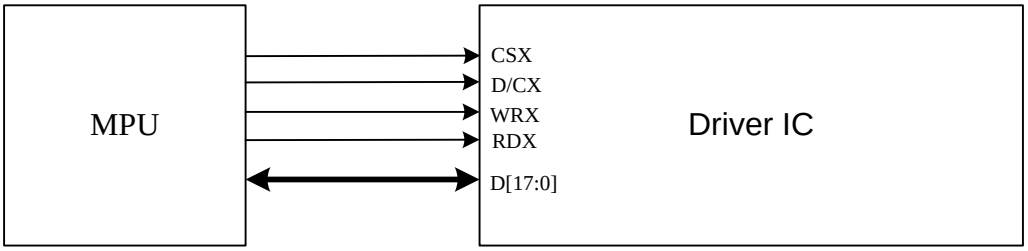
Table26.

Count	0	1	2	3		…	717	718	719	720
D/CX	0	1	1	1		…	1	1	1	1
D17			0R3		1R3	…		358R3		359R3
D16			0R2		1R2	…		358R2		359R2
D15			0R1		1R1	…		358R1		359R1
D14			0R0		1R0	…		358R0		359R0
D13			0G5		1G5	…		358G5		359G5
D12			0G4		1G4	…		358G4		359G4
D11			0G3		1G3	…		358G3		359G3
D10			0G2		1G2	…		358G2		359G2
D8	C7		0G1		1G1	…		358G1		359G1
D7	C6		0G0		1G0	…		358G0		359G0
D6	C5		0B5		1B5	…		358B5		359B5
D5	C4		0B4		1B4	…		358B4		359B4
D4	C3		0B3		1B3	…		358B3		359B3
D3	C2		0B2		1B2	…		358B2		359B2
D2	C1	0R5	0B1	1R5	1B1	…	358R5	358B1	359R5	359B1
D1	C0	0R4	0B0	1R4	1B0	…	358R4	358B0	359R4	359B0

4.4.7. 18-bit Parallel MCU Interface

The 8080-I system 18-bit parallel bus interface I of GC9C01 can be selected by setting hardware pin IM[4:0] to “10111”.The following shown figure is the example of interface with 8080-I MCU system interface.

Figure58.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table27.

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	357R4	358R4	359R4
D14		0R3	1R3	2R3	…	357R3	358R3	359R3
D13		0R2	1R2	2R2	…	357R2	358R2	359R2
D12		0R1	1R1	2R1	…	357R1	358R1	359R1
D11		0R0	1R0	2R0	…	357R0	358R0	359R0
D10		0G5	1G5	2G5	…	357G5	358G5	359G5
D9		0G4	1G4	2G4	…	357G4	358G4	359G4
D8		0G3	1G3	2G3	…	357G3	358G3	359G3
D7	C7	0G2	1G2	2G2	…	357G2	358G2	359G2
D6	C6	0G1	1G1	2G1	…	357G1	358G1	359G1
D5	C5	0G0	1G0	2G0	…	357G0	358G0	359G0
D4	C4	0B4	1B4	2B4	…	357B4	358B4	359B4
D3	C3	0B3	1B3	2B3	…	357B3	358B3	359B3
D2	C2	0B2	1B2	2B2	…	357B2	358B2	359B2
D1	C1	0B1	1B1	2B1	…	357B1	358B1	359B1
D0	C0	0B0	1B0	2B0	…	357B0	358B0	359B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

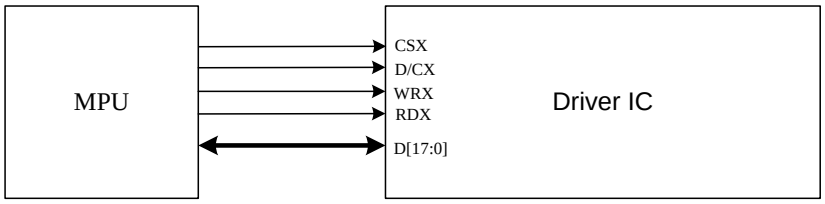
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table28.

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	357R5	358R5	359R5
D16		0R4	1R4	2R4	…	357R4	358R4	359R4
D15		0R3	1R3	2R3	…	357R3	358R3	359R3
D14		0R2	1R2	2R2	…	357R2	358R2	359R2
D13		0R1	1R1	2R1	…	357R1	358R1	359R1
D12		0R0	1R0	2R0	…	357R0	358R0	359R0
D11		0G5	1G5	2G5	…	357G5	358G5	359G5
D10		0G4	1G4	2G4	…	357G4	358G4	359G4
D9		0G3	1G3	2G3	…	357G3	358G3	359G3
D8		0G2	1G2	2G2	…	357G2	358G2	359G2
D7	C7	0G1	1G1	2G1	…	357G1	358G1	359G1
D6	C6	0G0	1G0	2G0	…	357G0	358G0	359G0
D5	C5	0B5	1B5	2B5	…	357B5	358B5	359B5
D4	C4	0B4	1B4	2B4	…	357B4	358B4	359B4
D3	C3	0B3	1B3	2B3	…	357B3	358B3	359B3
D2	C2	0B2	1B2	2B2	…	357B2	358B2	359B2
D1	C1	0B1	1B1	2B1	…	357B1	358B1	359B1
D0	C0	0B0	1B0	2B0	…	357B0	358B0	359B0

The 8080-II system 18-bit parallel bus interface mode can be selected by settings IM [4:0] =”10011”. The following shown figure is the example of interface with 8080- MCU system interface.

Figure59.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table29.

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	357R5	358R4	359R4
D14		0R3	1R3	2R3	…	357R4	358R3	359R3
D13		0R2	1R2	2R2	…	357R3	358R2	359R2
D12		0R1	1R1	2R1	…	357R2	358R1	359R1
D11		0R0	1R0	2R0	…	357R1	358R0	359R0
D10		0G5	1G5	2G5	…	357G5	358G5	359G5
D9		0G4	1G4	2G4	…	357G4	358G4	359G4
D8	C7	0G3	1G3	2G3	…	357G3	358G3	359G3
D7	C6	0G2	1G2	2G2	…	357G2	358G2	359G2
D6	C5	0G1	1G1	2G1	…	357G1	358G1	359G1
D5	C4	0G0	1G0	2G0	…	357G0	358G0	359G0
D4	C3	0B4	1B4	2B4	…	357B4	358B4	359B4
D3	C2	0B3	1B3	2B3	…	357B3	358B3	359B3
D2	C1	0B2	1B2	2B2	…	357B2	358B2	359B2
D1	C0	0B1	1B1	2B1	…	357B1	358B1	359B1
D0		0B0	1B0	2B0	…	357B0	358B0	359B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table30.

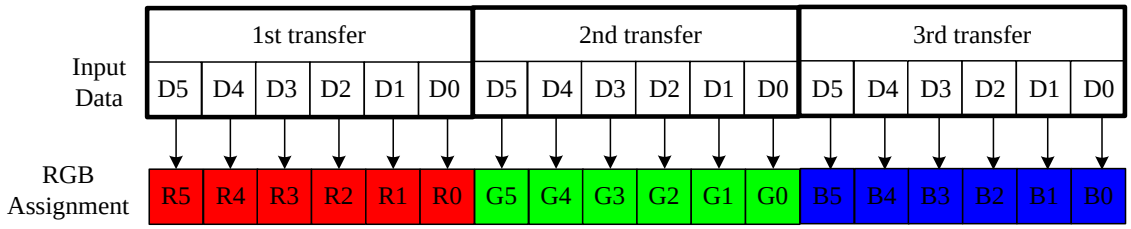
Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	357R5	358R5	359R5
D16		0R4	1R4	2R4	…	357R4	358R4	359R4
D15		0R3	1R3	2R3	…	357R3	358R3	359R3
D14		0R2	1R2	2R2	…	357R2	358R2	359R2
D13		0R1	1R1	2R1	…	357R1	358R1	359R1
D12		0R0	1R0	2R0	…	357R0	358R0	359R0
D11		0G5	1G5	2G5	…	357G5	358G5	359G5
D10		0G4	1G4	2G4	…	357G4	358G4	359G4
D9		0G3	1G3	2G3	…	357G3	358G3	359G3
D8	C7	0G2	1G2	2G2	…	357G2	358G2	359G2
D7	C6	0G1	1G1	2G1	…	357G1	358G1	359G1
D6	C5	0G0	1G0	2G0	…	357G0	358G0	359G0
D5	C4	0B5	1B5	2B5	…	357B5	358B5	359B5

D4	**C3**	**0B4**	**1B4**	**2B4**	**…**	**357B4**	**358B4**	**359B4**
D3	**C2**	**0B3**	**1B3**	**2B3**	**…**	**357B3**	**358B3**	**359B3**
D2	**C1**	**0B2**	**1B2**	**2B2**	**…**	**357B2**	**358B2**	**359B2**
D1	**C0**	**0B1**	**1B1**	**2B1**	**…**	**357B1**	**358B1**	**359B1**
D0		**0B0**	**1B0**	**2B0**	**…**	**357B0**	**358B0**	**359B0**

4.4.8. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the RIM bit to “1”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

1)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).
Figure60.



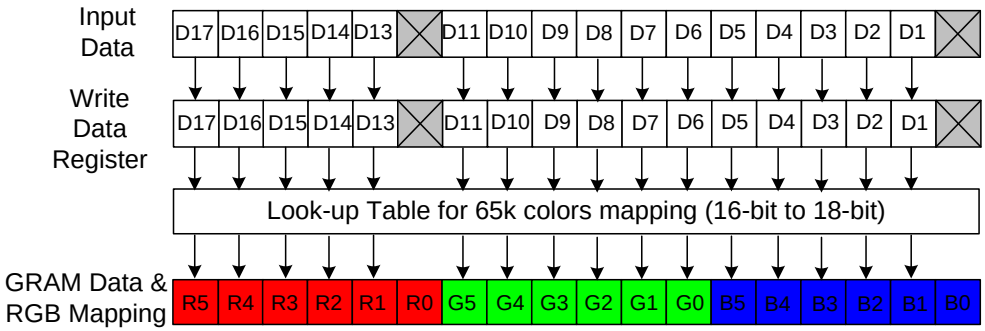
GC9C01 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK).Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

4.4.9. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D[17:13] & D[11:0]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:13] & D[11:0] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.

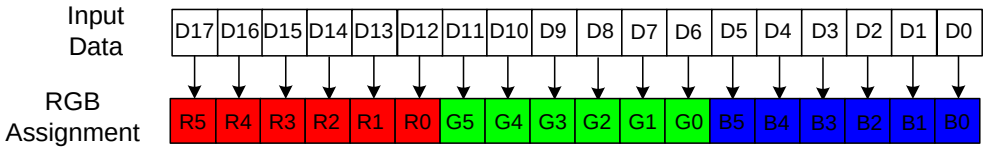
Figure62.



4.4.10. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.

Figure63.



4.4.11. Quad Serial Peripheral Interface

In quad serial Peripheral interface, different display data format is available for three color depths supported by the LCM listed below.

-16.7M colors RGB 8, 8, 8-bits input with dither on by setting DBI[2:0]=7(3Ah) and DTR_EN=1 (B1h)

-262k colors, RGB 6, 6, 6 -bits input.

-65k colors, RGB 5, 6, 5 -bits input

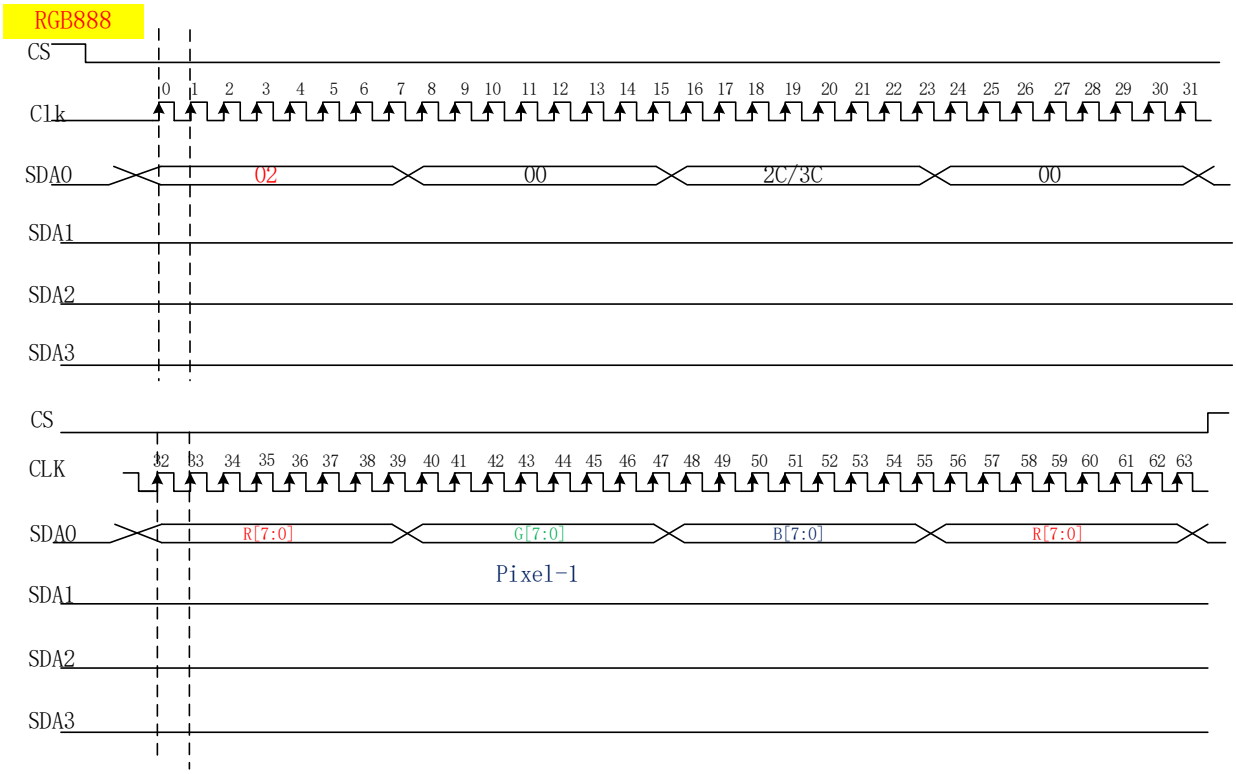
-256 colors, RGB 3, 3, 2 -bits input

-8 colors，RGB 1, 1, 1-bits input

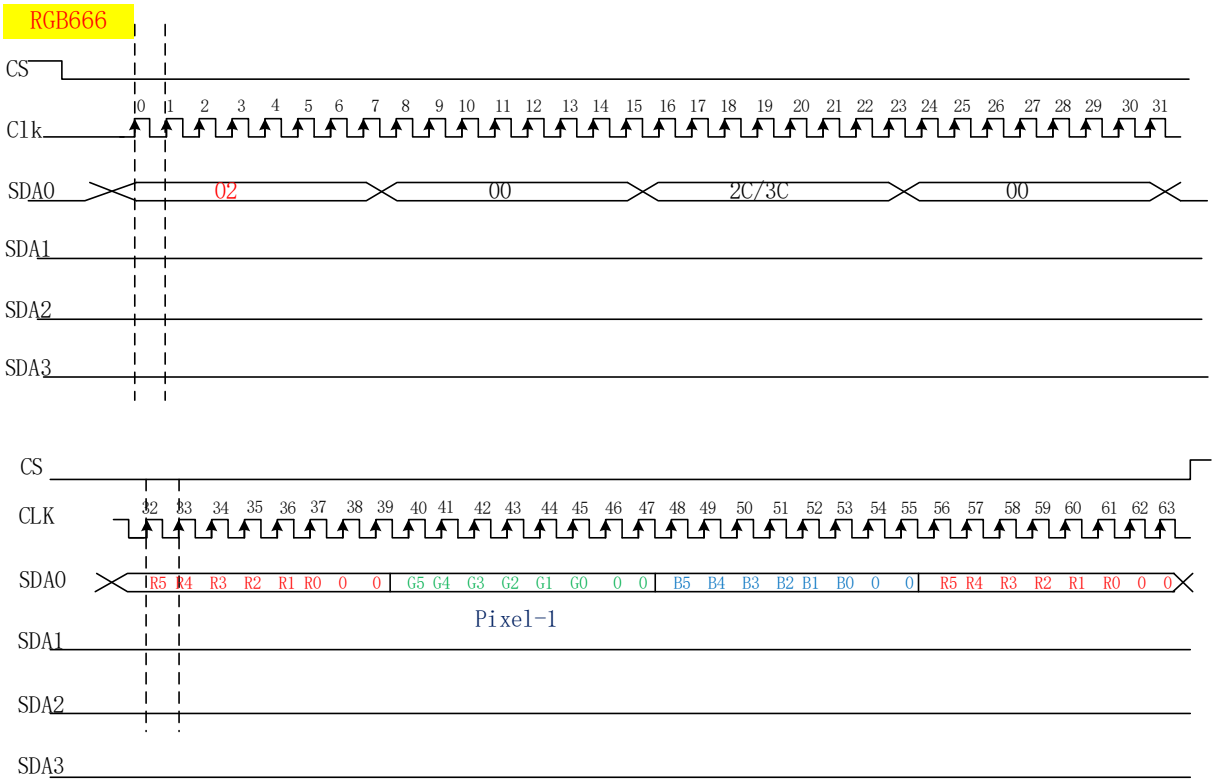
-256 gray，data：BIN00000000~BIN11111111

1wire data: only use SDA, first byte=0x02

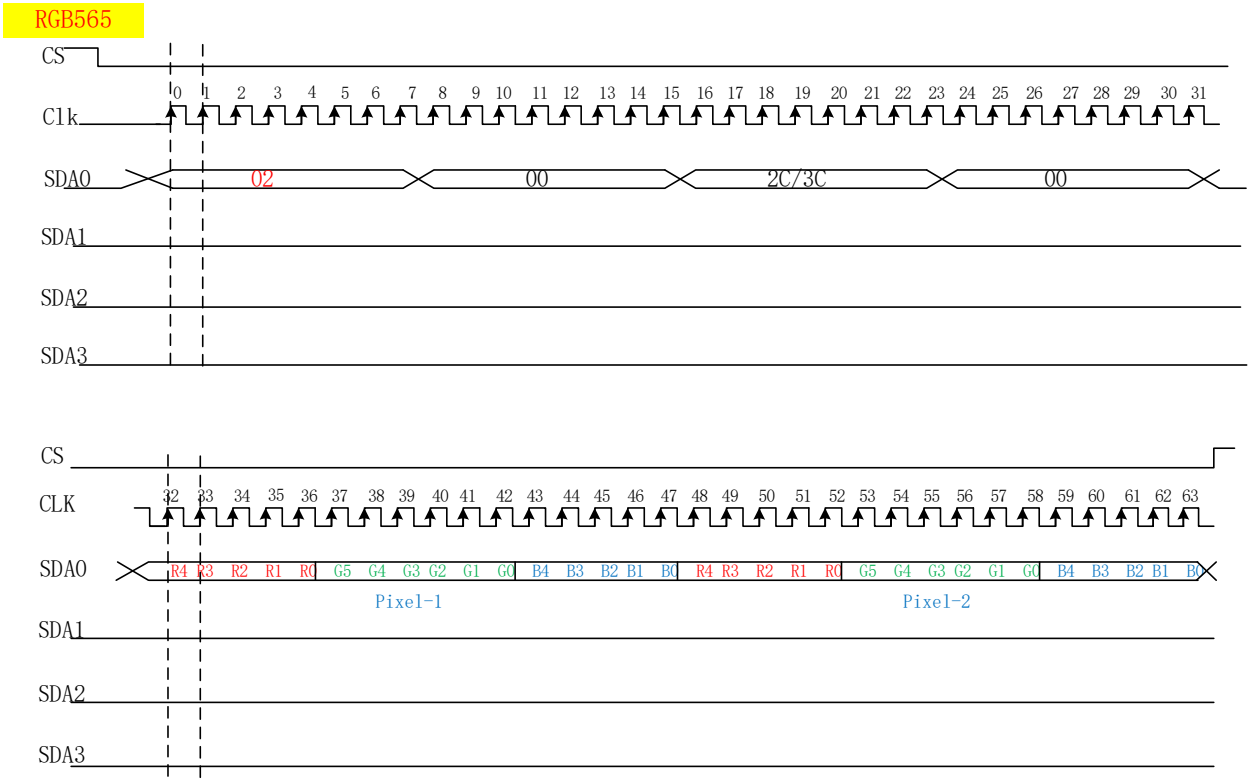
1） 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input).



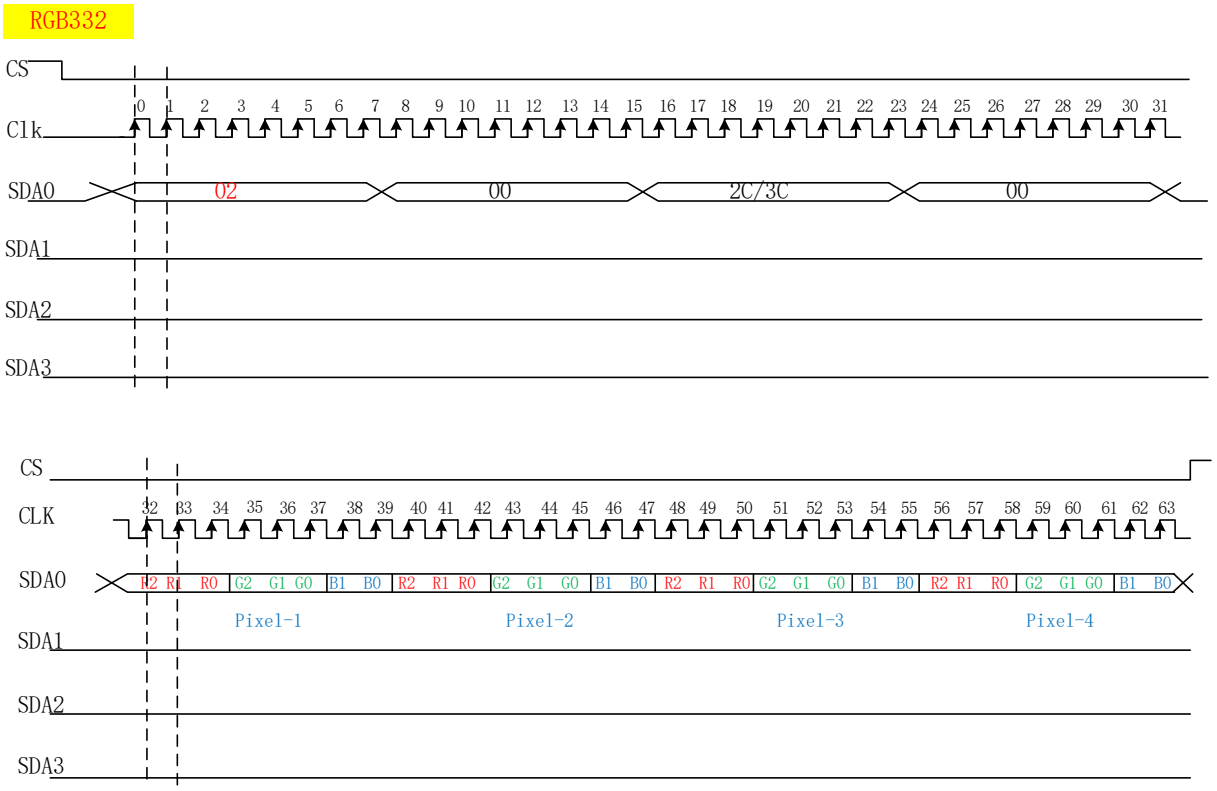
2） 262k-Colors:18-bit/pixel (RGB 6, 6, 6-bits input).



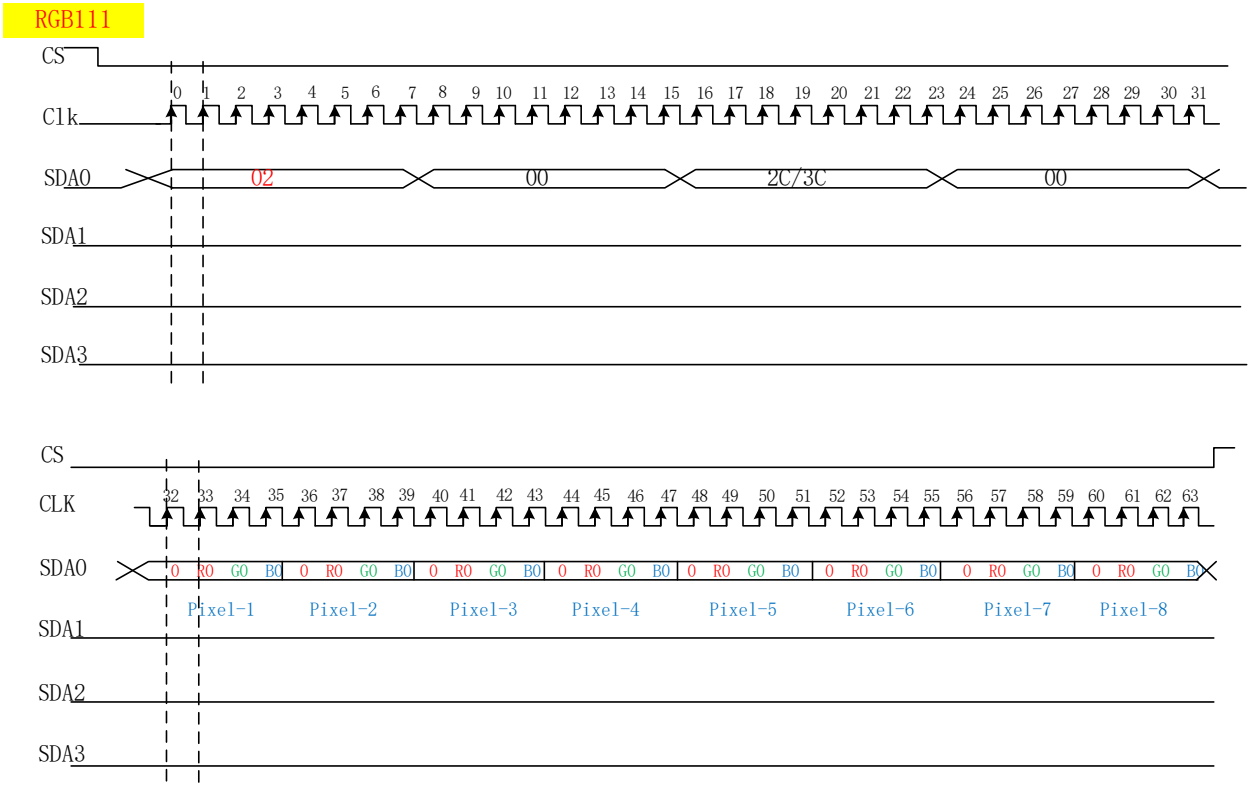
3） 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input).



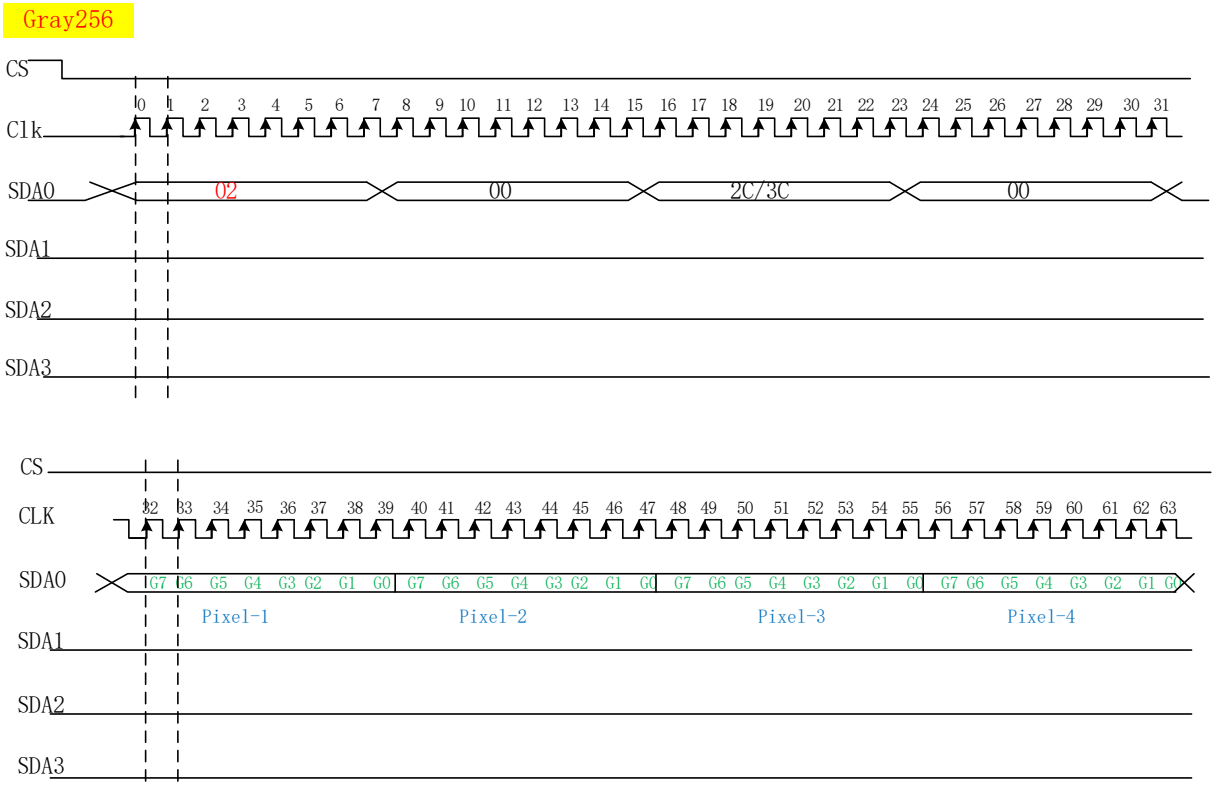
4） 256-Colors:8-bit/pixel (RGB 3, 3, 2 -bits input).



5） **8-Colors:3-bit/pixel (RGB 1, 1, 1 -bits input).**

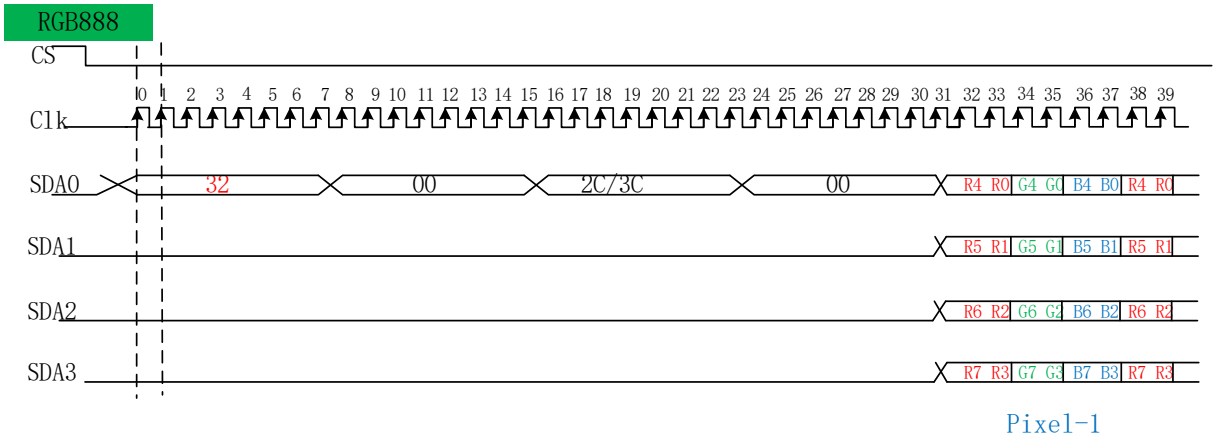


6） **256gray (data：bin0~bin11111111).**

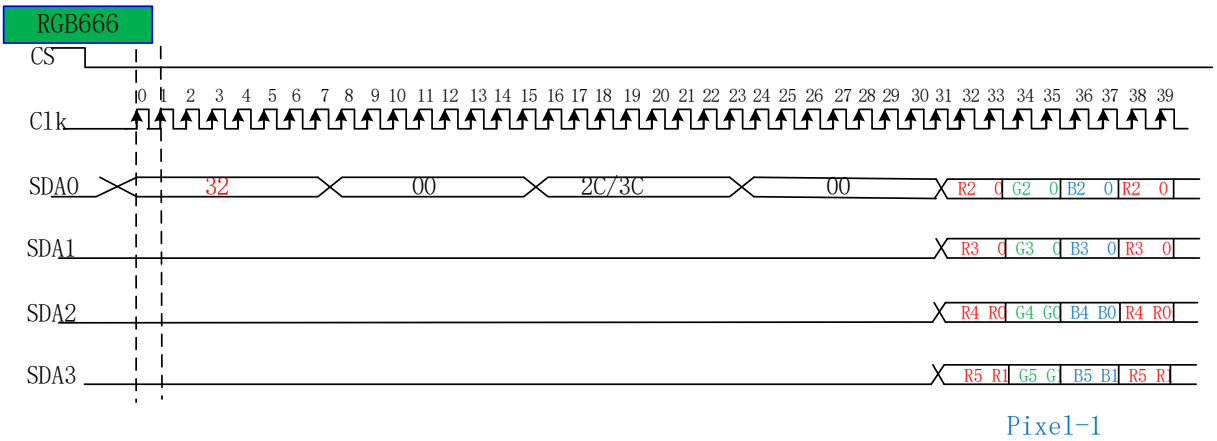


4wire data 1wire Addr: first byte=0x32

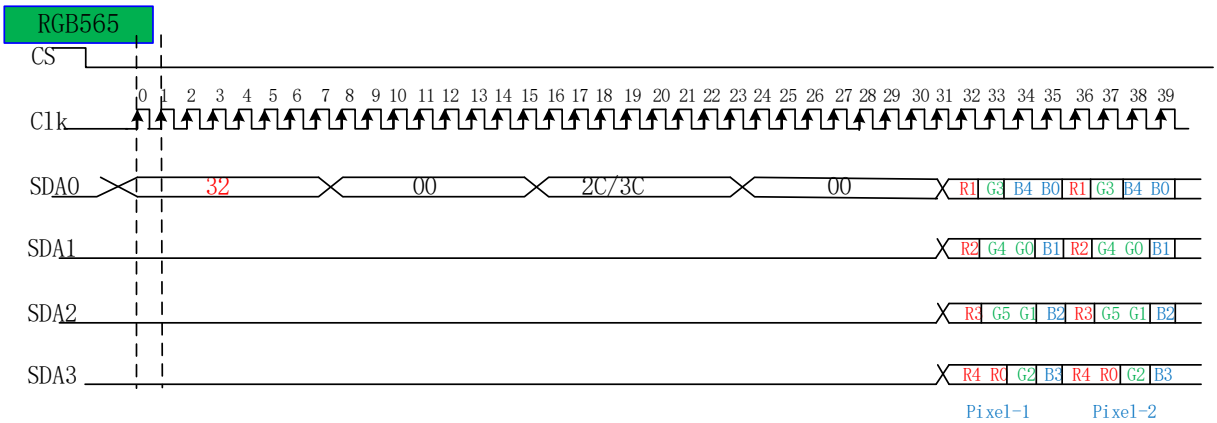
1） 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input).



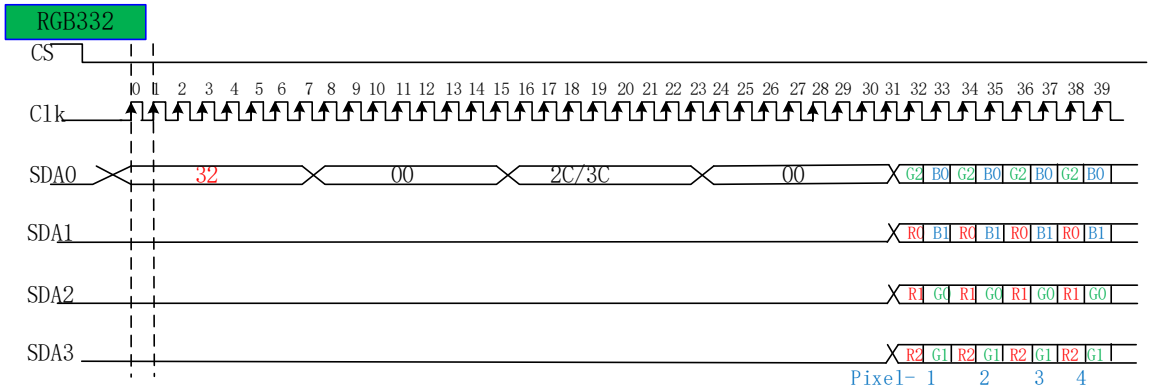
2） 262k-Colors:18-bit/pixel (RGB 6, 6, 6 -bits input).



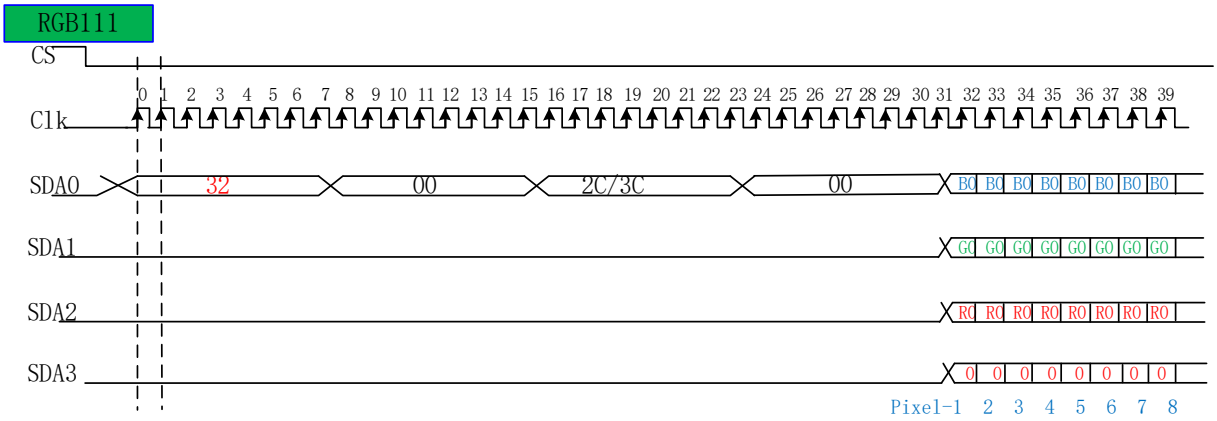
3） 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input).



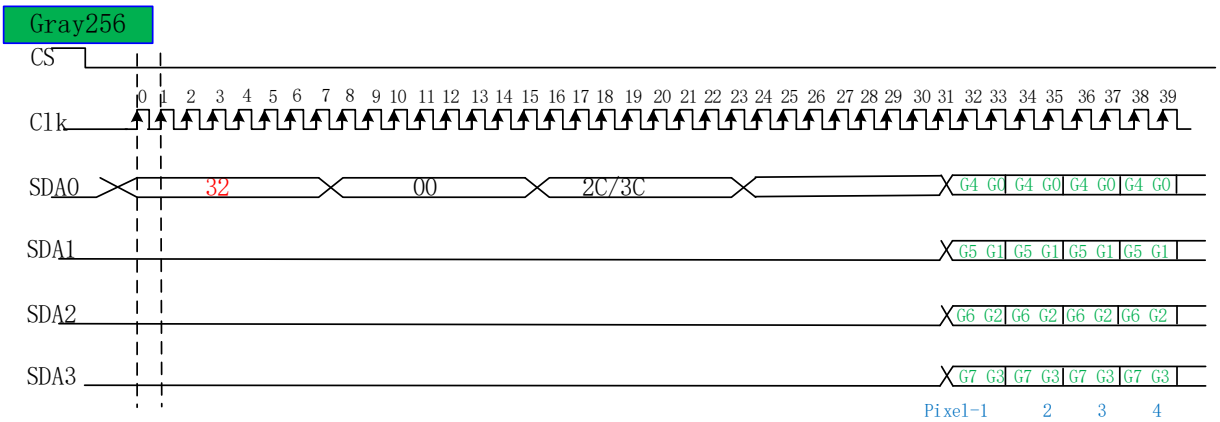
4） 256-Colors:8-bit/pixel (RGB 3, 3, 2 -bits input).



5） 8-Colors:3-bit/pixel (RGB 1, 1, 1 -bits input).

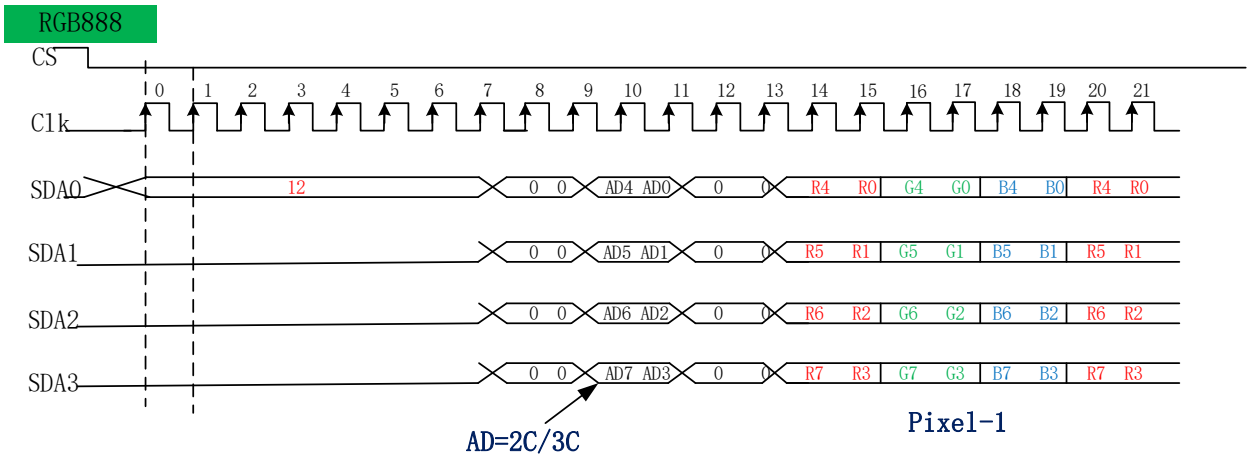


6） 256gray (data：bin0~bin11111111).

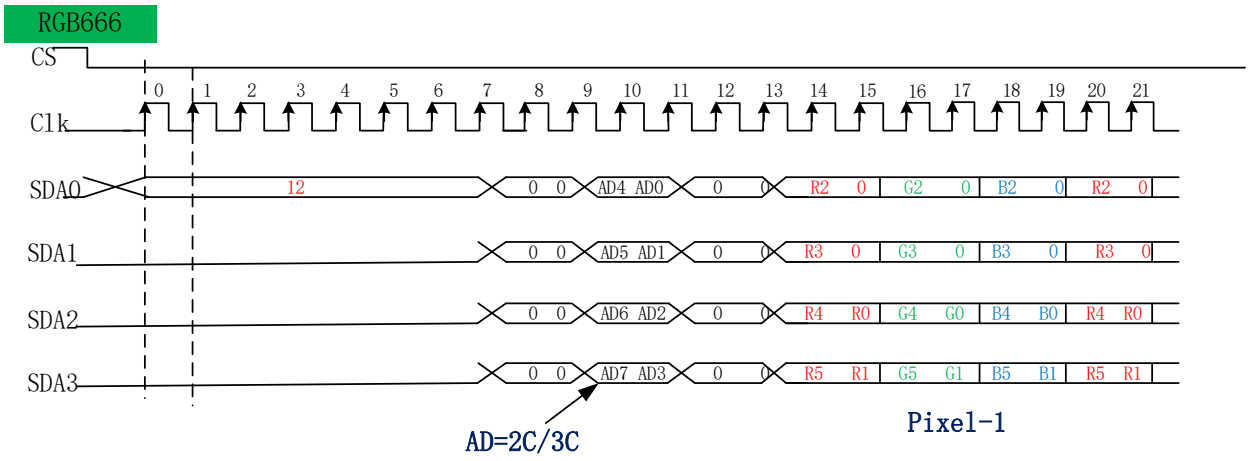


4wire data 4wire Addr: first byte=0x12

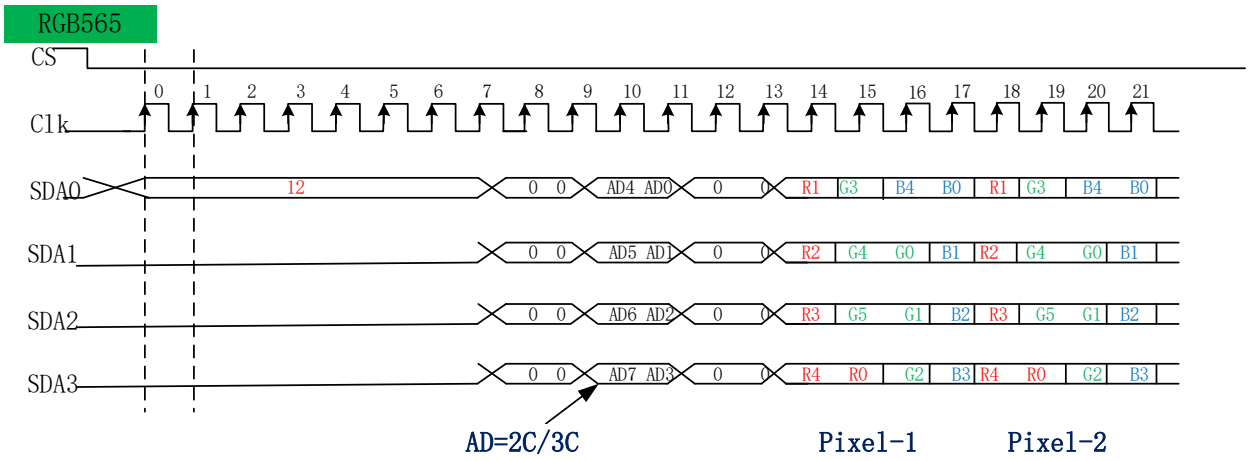
1）16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input).



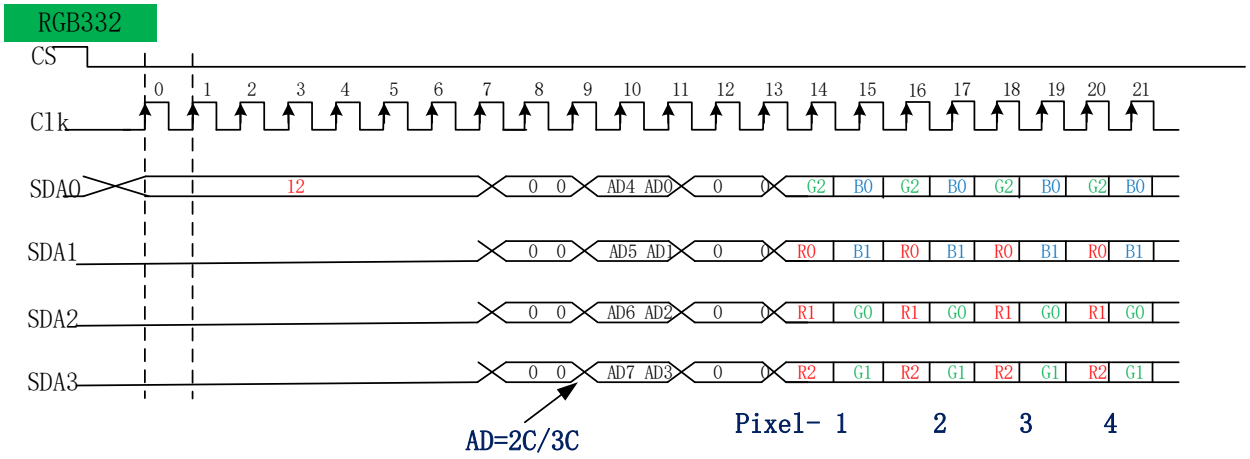
2）262k-Colors:18-bit/pixel (RGB 6, 6, 6-bits input).



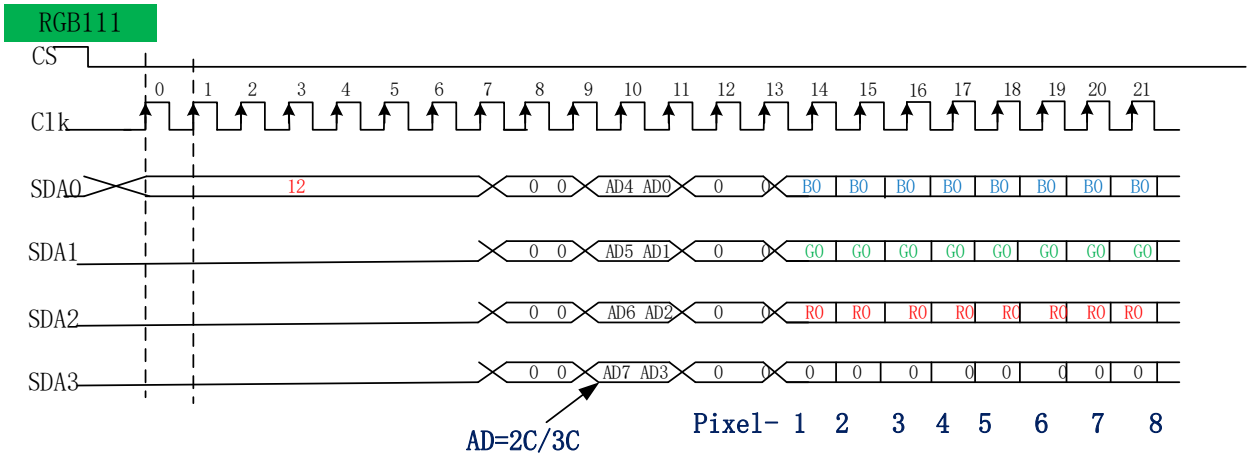
3）65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input).



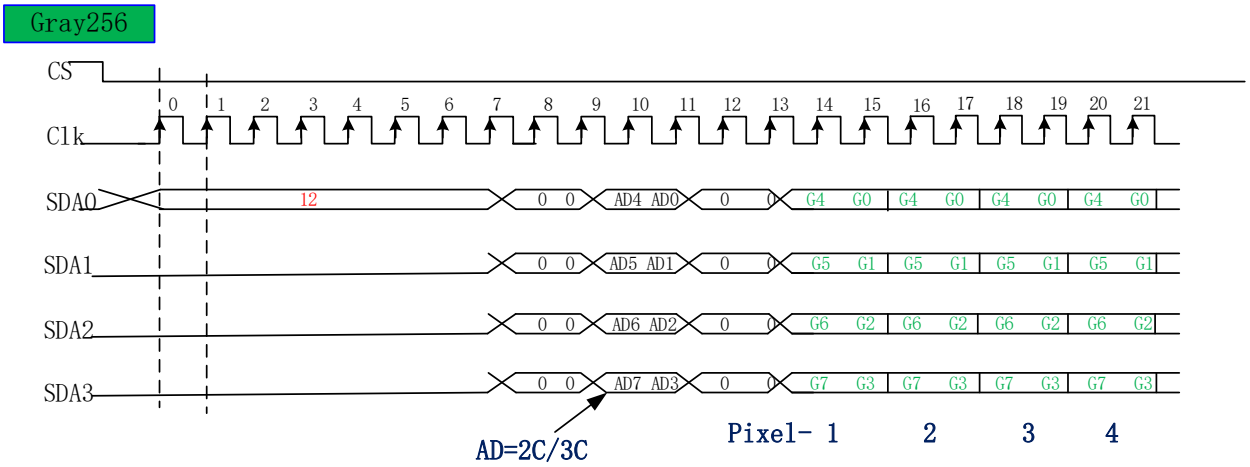
4）256-Colors:8-bit/pixel (RGB 3, 3, 2 -bits input).



5）8-Colors:3-bit/pixel (RGB 1, 1, 1 -bits input).



6）256gray (data：bin0~bin11111111).

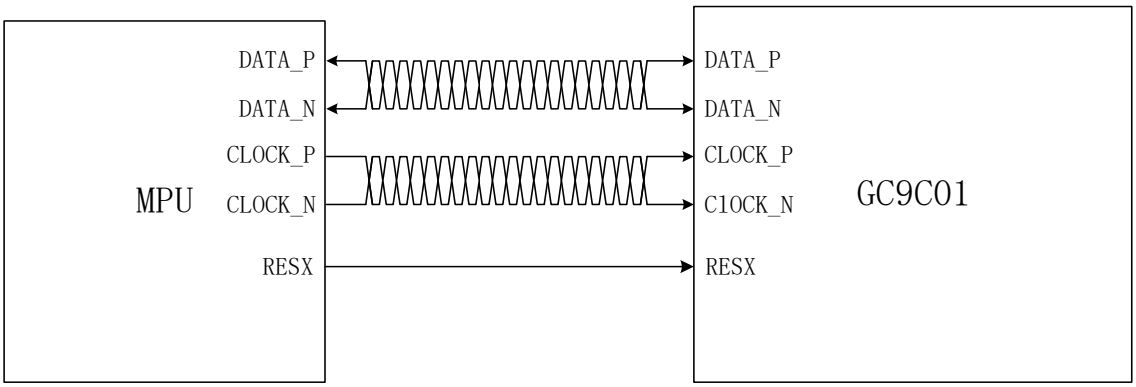


4.5. MIPI (Mobile Industry Processor Interface)

GC9C01supports MIPI DSI which can be enabled or disabled by external IM [4:0] pin. GC9C01can be accessed through one PHY lane module which communicates via two lines to a complementary part at the other side of the lane interconnects. The communication can be separated two different levels between the MCU and GC9C01:

- Low level communication what is done on the interface level.
- High level communication what is done on the packet level.

GC9C01 uses data and clock lane differential pairs for DSI, The data lane (D0P and D0N) is used for data communication and clock lane (DKP and DKN) is used to transmit the clock signal. The Mobile Industry Processor Interface (MIPI) can be used for communication between the processor and DSI-compliant LCD driver chip. The selection of this interface is done when IM [4:0] =11110.



Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to GC9C01 and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane pair state code	Line DC Voltage Levels		High Speed	Low Power	
	D0_P	D0_N	Burst mode	DK_P	DK_N
HS-0	Low(HS)	High(HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low(LP)	Low(LP)	Not define	Bridge	Space
LP-01	Low(LP)	High(LP)	Not define	HS-Request	Mark-0
LP-10	High(LP)	Low(LP)	Not define	LP-Request	Mark-1
LP-11	High(LP)	High(LP)	Not define	Stop	Note 2

Notes: (1) Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane

Pair is in the High Speed (HS) mode.

(2) If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

4.5.1. Interface Level Communication – Clock Lanes

DK_P/N lanes can be driven into three different power modes:

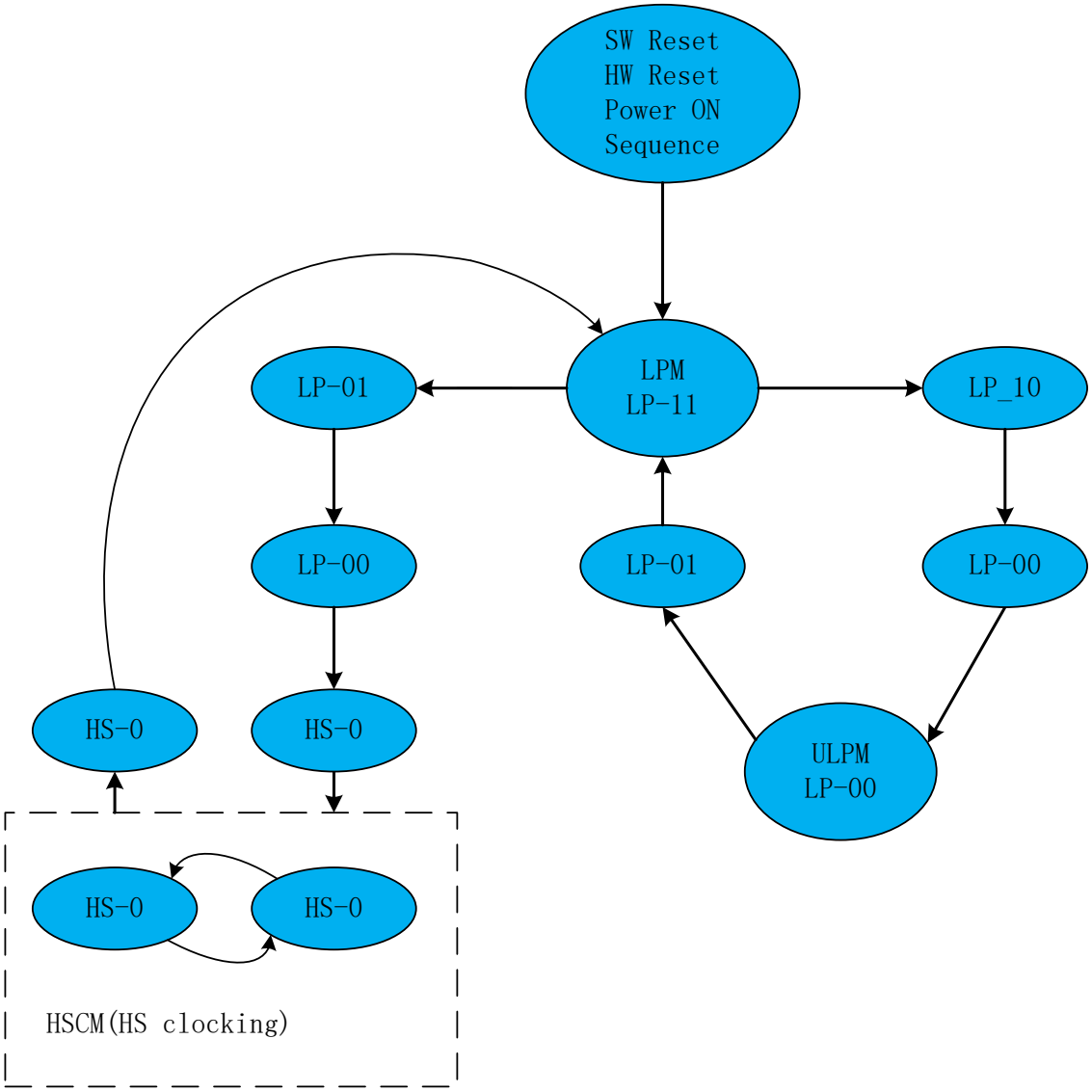
- Low Power Mode (LPM)
- Ultra Low Power Mode (ULPM)
- High Speed Clock Mode (HSCM)

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

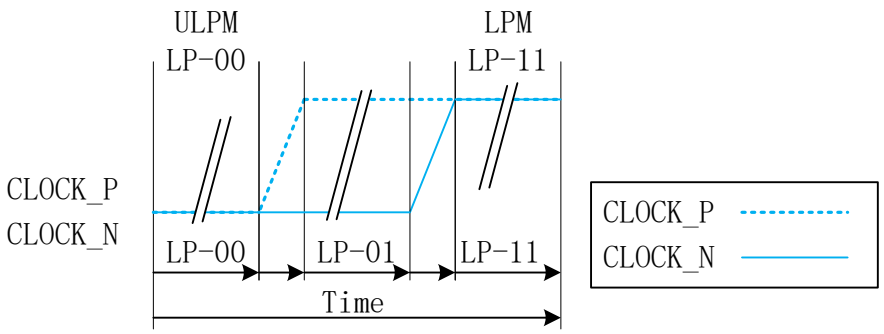


4.6.1.1. Low Power Mode (LPM)

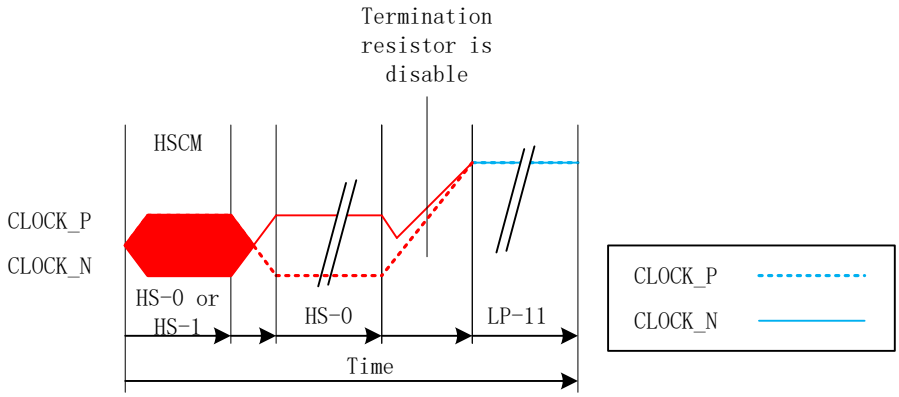
DK_P/N lanes can be driven to the Low Power Mode (LPM), when DK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

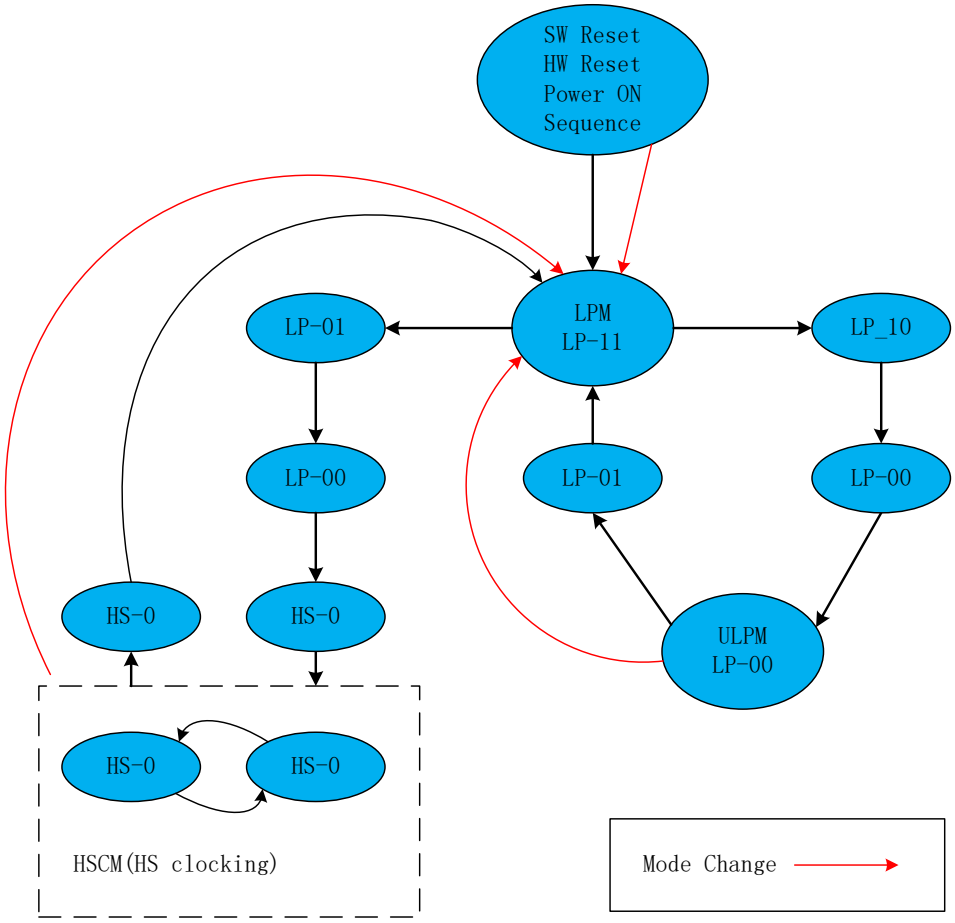
2) After DK_P/N lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.



3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.



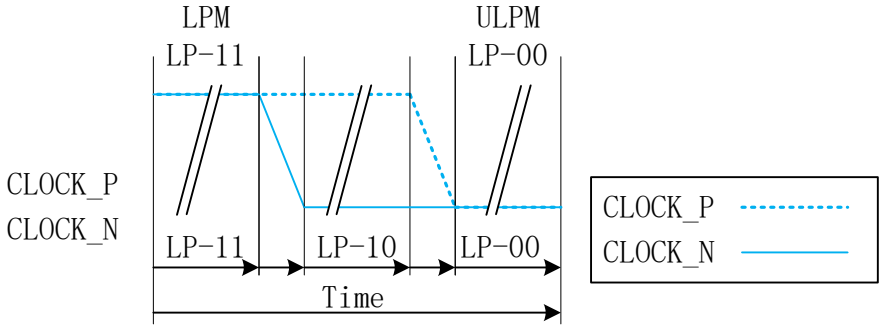
All three mode changes are illustrated a flow chart below.



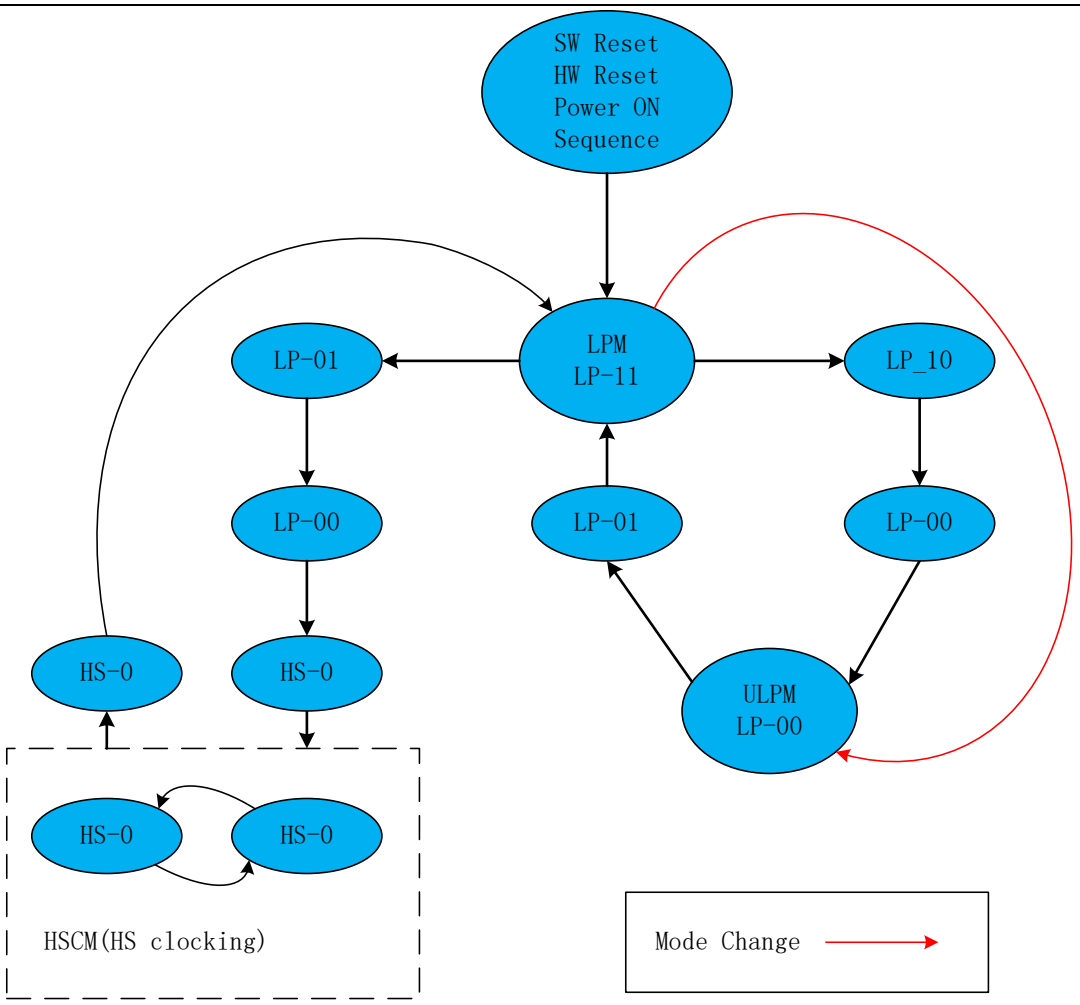
4.6.1.2. Ultra Low Power Mode (ULPM)

DK_P/N lanes can be driven to the Ultra Low power Mode (ULPM), when DK lanes are entering LP-00 State Code.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below



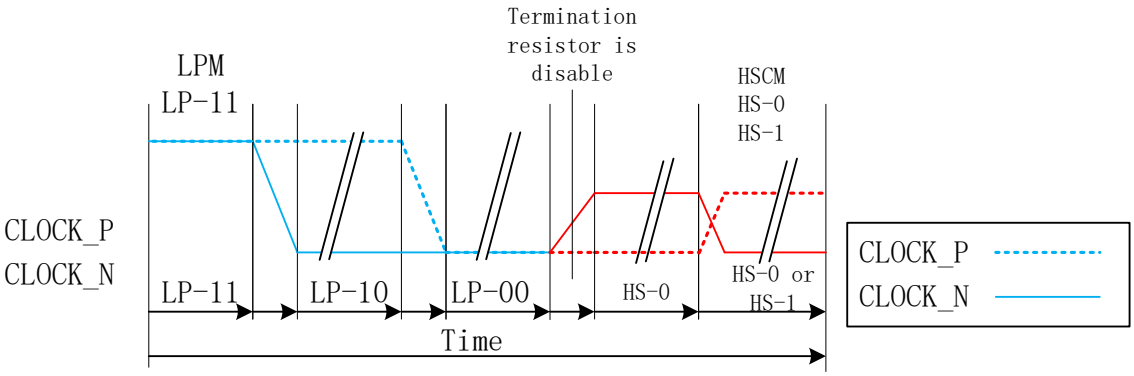
The mode change is also illustrated below.



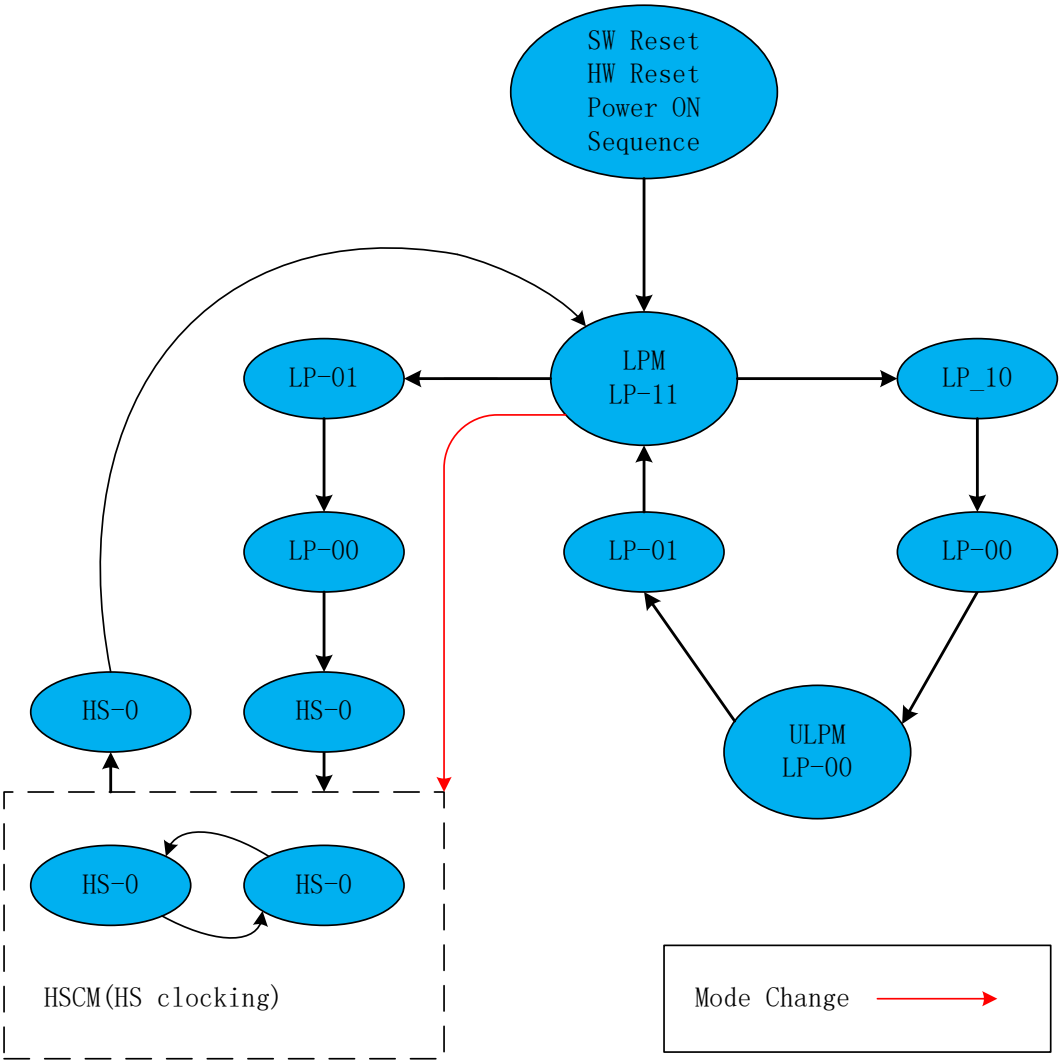
4.6.1.3. High-Speed Clocked Mode (HSCM)

DK_P/N lanes can be driven to the High Speed Clock Mode (HSCM), when DK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

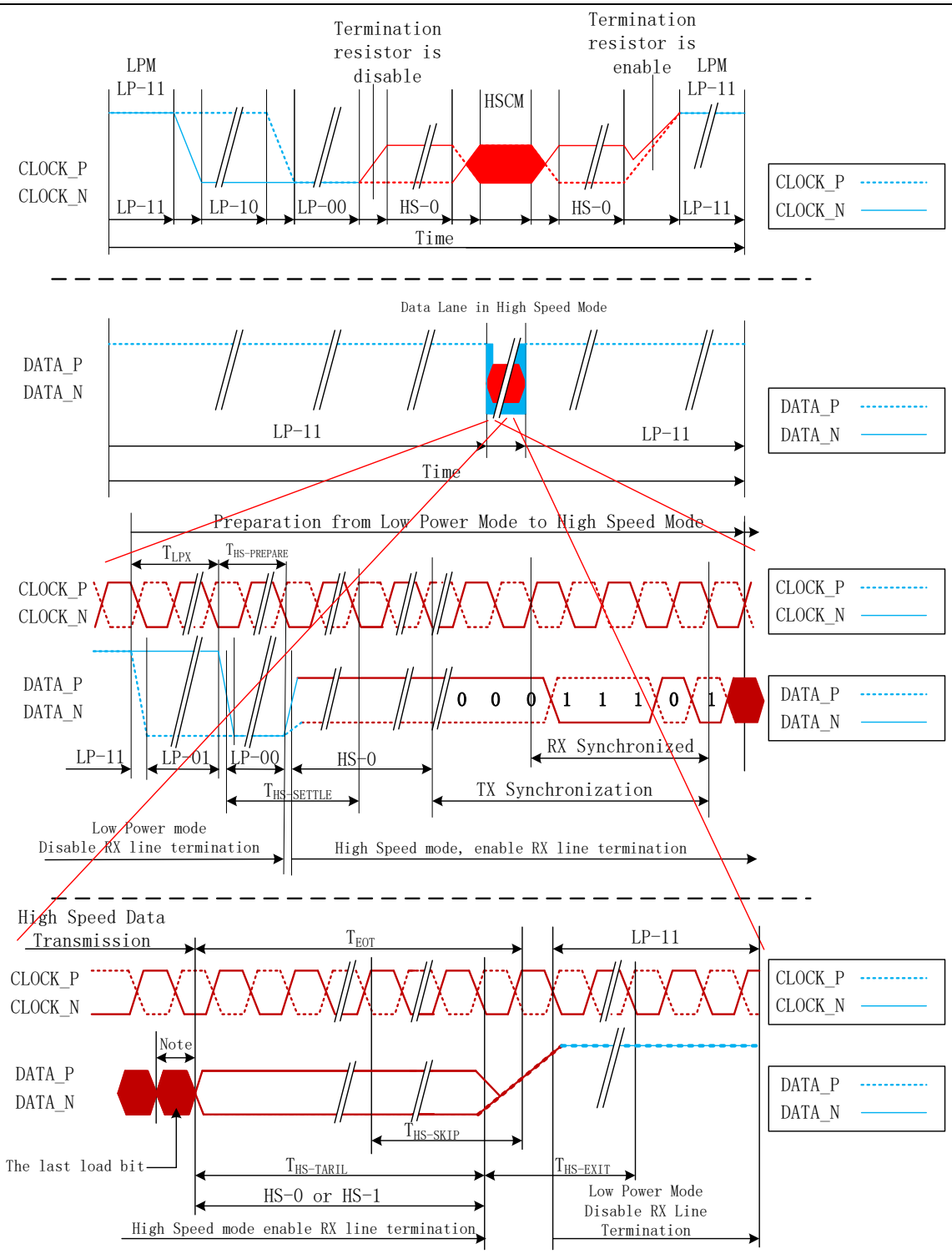


The mode change is also illustrated below.



The high speed clock (DK_P/N) is started before high speed data is sent via DK_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped. The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



Notes: 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.5.2. Interface Level Communication – Data Lanes

D0_P/N Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 →LP-01 →LP-00	LP-00 →LP-10 →LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 →LP-01 →LP-00 →HS-0	(HS-0 or HS-1) →LP-11
Bus Turnaround Request	LP-11 →LP-10 →LP-00 →LP-10 →LP-00	Hi-Z

4.6.2.1 Escape Modes

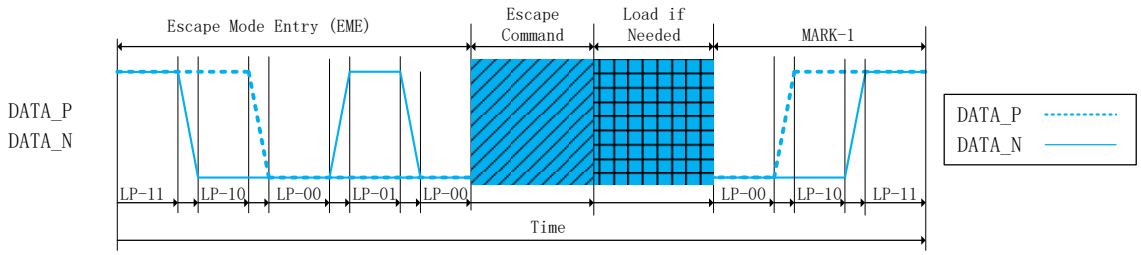
Data lanes (D0_P/N) can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to GC9C01,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which is resetting GC9C01,
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from GC9C01 to the MCU,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from GC9C01 to the MCU

The basic sequence of the Escape Mode is as follow:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-DATA_P = 1, DSI-DATA_N- = 0) e.g. When DSI-DATA_N is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



There are a total of eight Escape Command(EC) divided into two types, Modes and Triggers(see below table).
An example of a Mode type Escape Command is "Ultra-Low Power Mode" where the MCU instructs the display module to enter it's Ultra-Low Power Mode.
An example of Trigger type Escape Command is 'Tearing Effect'. In this case the MCU has already instructed .The display module to provide this trigger and is waiting for the response. The display module then sends a TE Trigger(TEE) on the next V-sync event.

Escape commands are defined on the next table.

Escape command	Command Type Mode / Trigger	Entry command Pattern (First to Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001
Ultra-Low Power Mode	Mode	0001 1110
Undefined-1, Note	Mode	1001 1111
Undefined-2, Note	Mode	1101 1110
Remote Application Reset	Trigger	0110 0010
Tearing Effect	Trigger	0101 1101
Acknowledge	Trigger	0010 0001
Uknown-5, Note	Trigger	1010 0000

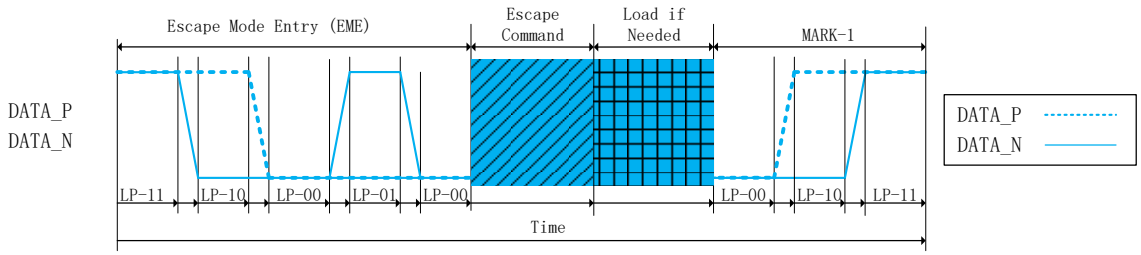
Note: This Escape command support has not been implemented on GC9C01.

4.6.2.1.1. Low-Power Data Transmission (LPDT)

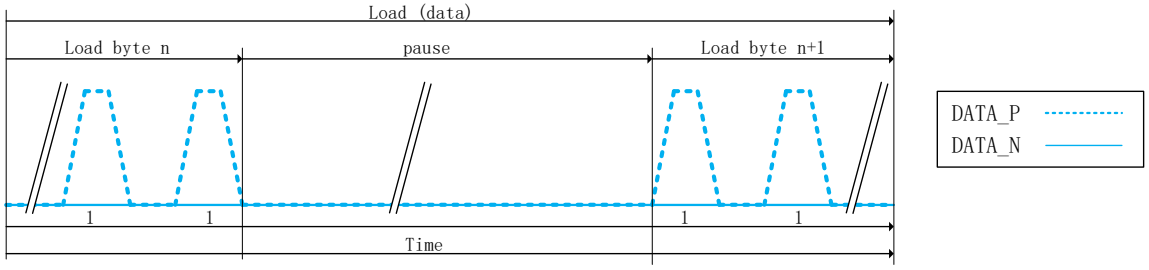
The MCU can send data to GC9C01 in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to GC9C01. GC9C01 is also using the same sequence when it is sending data to the MCU.
The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
  - One or more bytes (8 bit)
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note: Load (Data) is presenting that the first bit is logical '1' in this example.



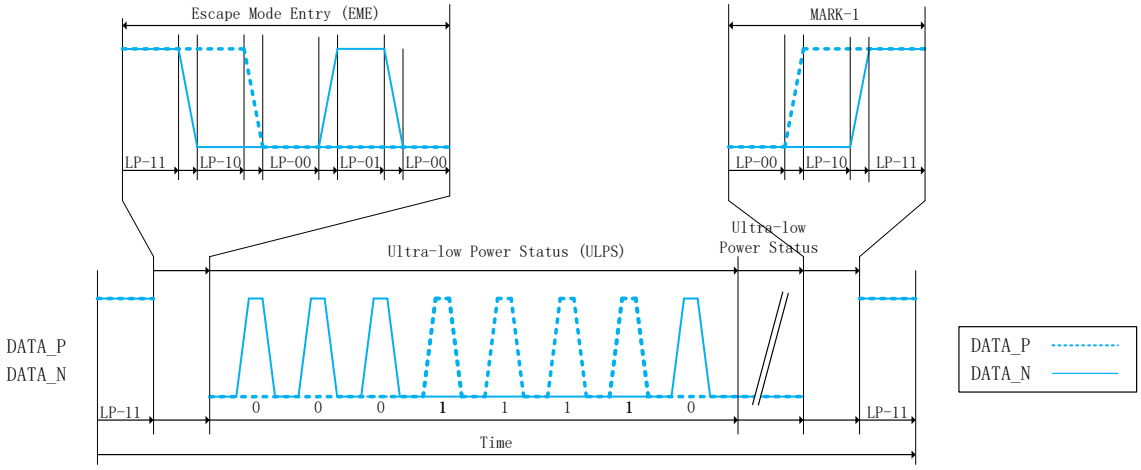
4.6.2.1.2. Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



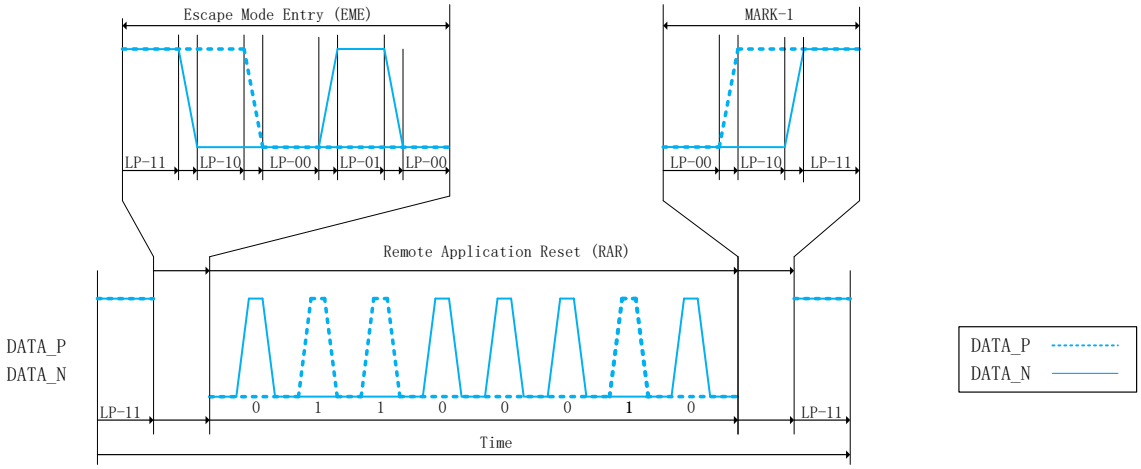
4.6.2.1.3. Remote Application Reset (RAR)

The MCU can inform to GC9C01 that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.
The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

- This sequence is illustrated for reference purposes below:



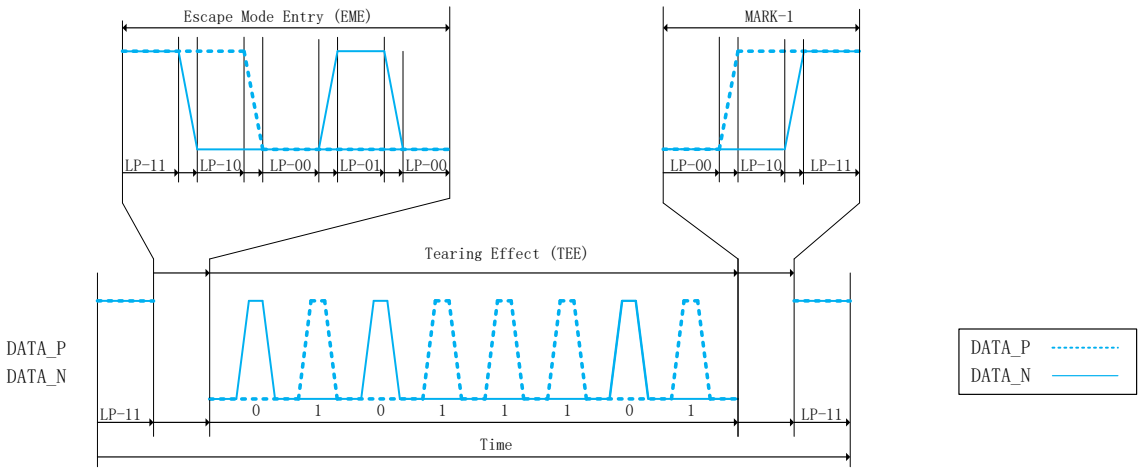
4.6.2.1.4. Tearing Effect (TEE)

GC9C01 can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



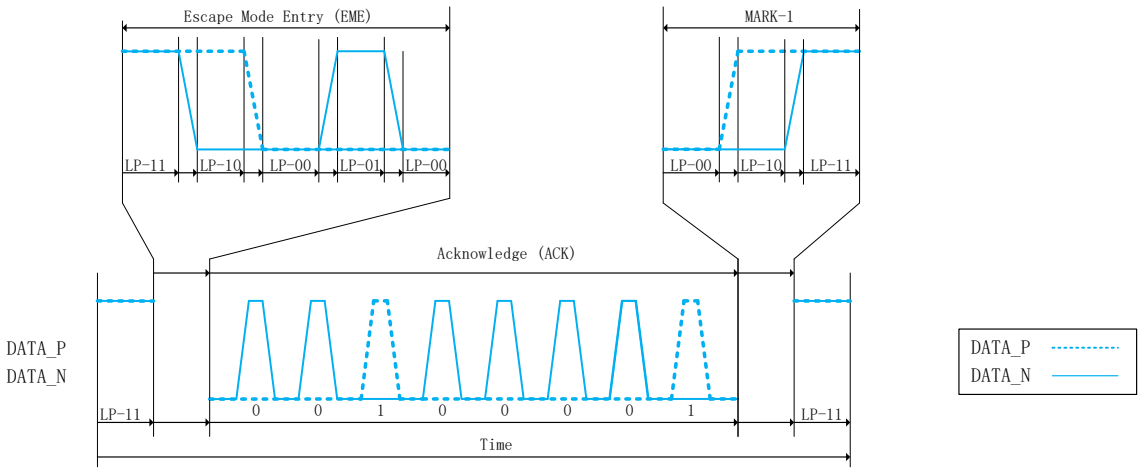
4.6.2.1.5. Acknowledge (ACK)

GC9C01 can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



4.6.2.2.High-Speed Data Transmission (HSDT)

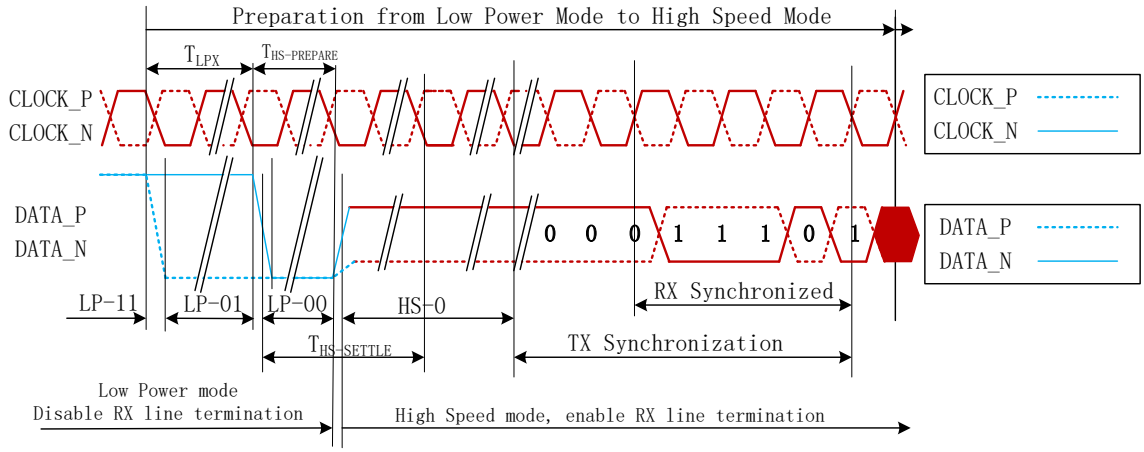
4.6.2.2.1. Entering High-Speed Data Transmission (TSOT of HSDT)

GC9C01 is entering High-Speed Data Transmission (HSDT) when Clock lanes DK_P/N have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes DSI-DATA_P/N of GC9C01 are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below:



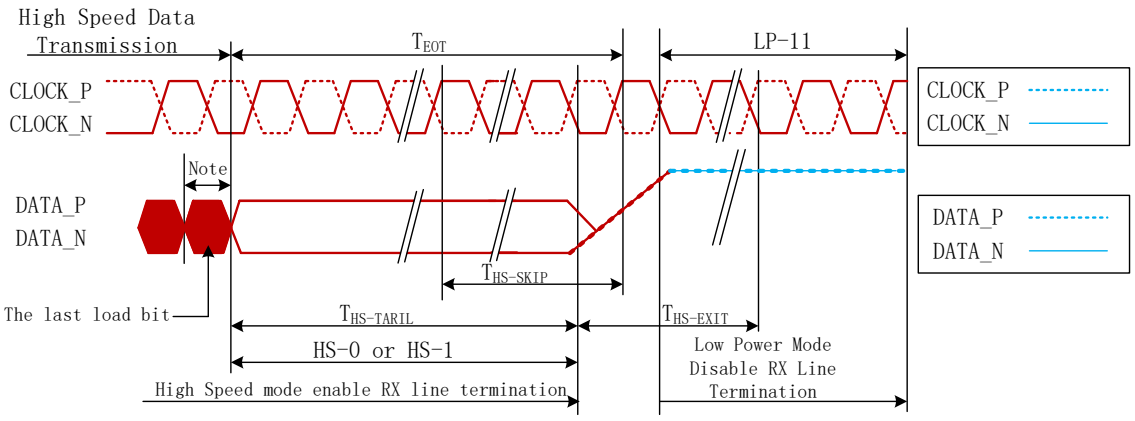
4.6.2.2.2. Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

GC9C01 is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DK_P/N are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes DSI-DATA_P/N are in LP-11 mode.

Data lanes DSI-DATA_P/N of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

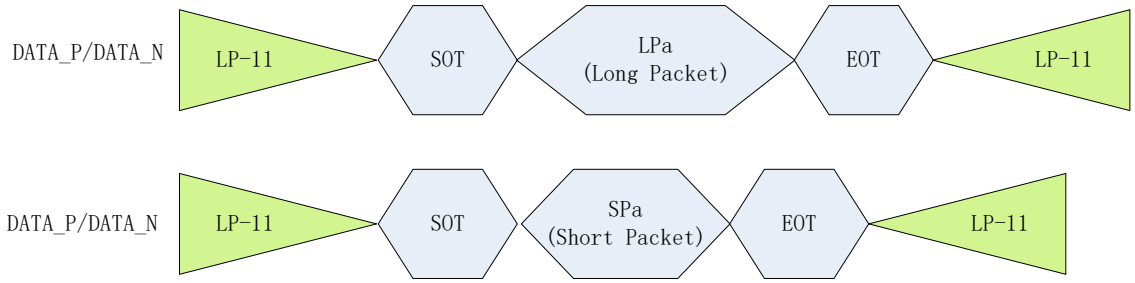
This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below



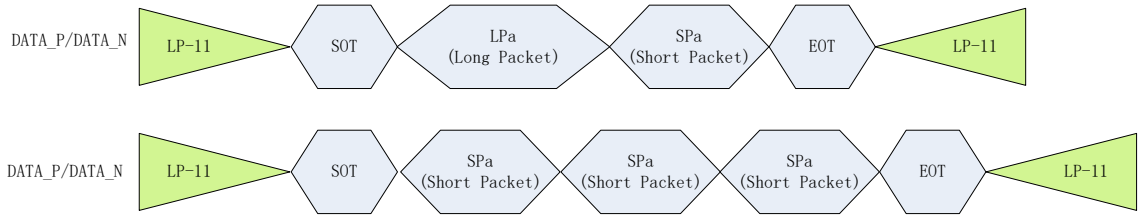
Note: 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.6.2.2.3.Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “4.3.3.1 Short Packet (SPa) and Long Packet (LPa) Structures“.
The single packet in High-Speed Data Transmission is illustrated for reference purposes below:



The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:



Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

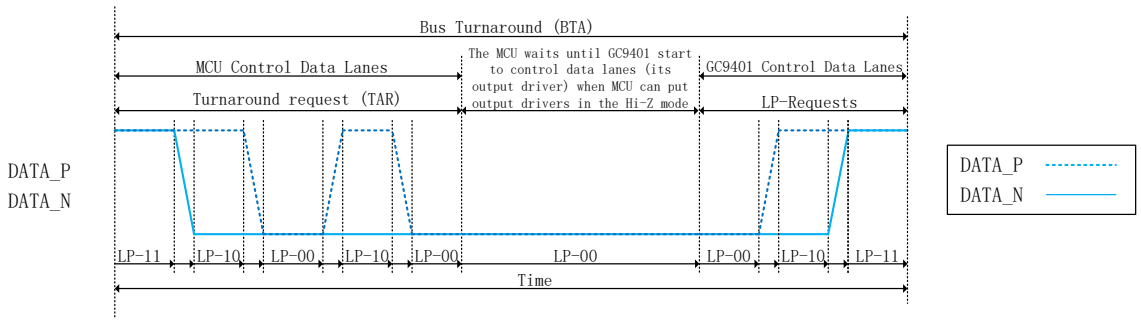
4.6.2.3.Bus Turnaround (BTA)

The MCU or GC9C01, which is controlling DSI-DATA_P/N Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or GC9C01. The MCU and GC9C01 are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to GC9C01, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00=>LP-10=>LP-00
- The MCU waits until GC9C01 is starting to control DSI-DATA_P/N data lanes and the MCU stops to control DSI-DATA_P/N data lanes (= High-Z)

- GC9C01 changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to GC9C01) is illustrated below:



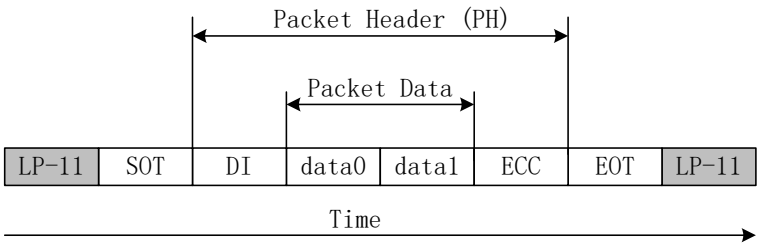
4.5.3. Packet Level Communication

4.5.3.1. Short Packet and Long Packet Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.
The lengths of the packets are：

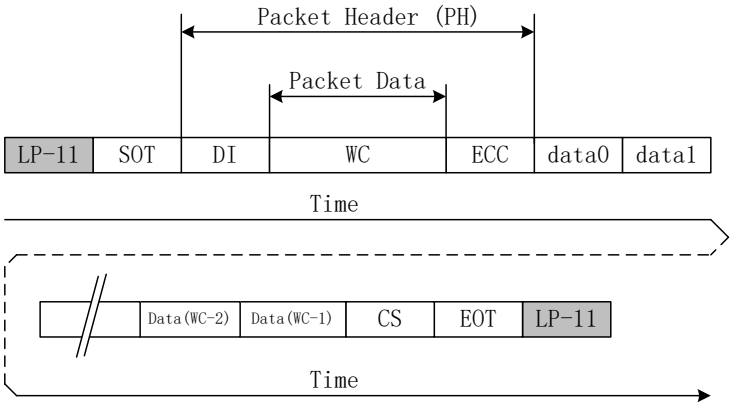
- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH). The Short Packet structure is illustrated as below:



LP-11: low power -Stop State
SOT: Start of Transmisstion
DI: 8-bit data Identification
Data0/data1: 8-bit packet data
ECC: 8-bit Error cerrection code
EOT: End of Transmisstion

The Long Packet structure is illustrated as below:



LP-11: low power -Stop State
SOT: Start of Transmisstion
DI: 8-bit data Identification
WC: 16-bit word count(0-65535)
ECC: 8-bit Error cerrection code
Data0/…/Data(WC-1): 8-bit packet data
CS: 16-bit, the Check Sum = Packet Footer(PF)
EOT: End of Transmisstion

The other possibility is that there is not needed SOT, EOT and LP-11 between packets if packets have sent in multiple packet format e.g.

- LP-11 =>SOT =>SPa =>LPa =>SPa =>SPa =>EOT =>LP-11
- LP-11 =>SOT =>SPa =>SPa =>SPa =>EOT =>LP-11
- LP-11 =>SOT =>LPa =>LPa =>LPa =>EOT =>LP-11

4.5.3.1.1.Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.
This same order is illustrated for reference purposes below.

DI (Data Idetification)								WC - LSB (Word Count - LSB)								WC - MSB (Word Count - MSB)								ECC (Error Correction Code)							
8'h29h								8'h01h								8'h00h								8'h06h							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

4.5.3.1.2. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.
This same order is illustrated for reference purposes below.

WC - LSB (Word Count - LSB)								WC - MSB (Word Count - MSB)							
8'h01h								8'h00h							
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB

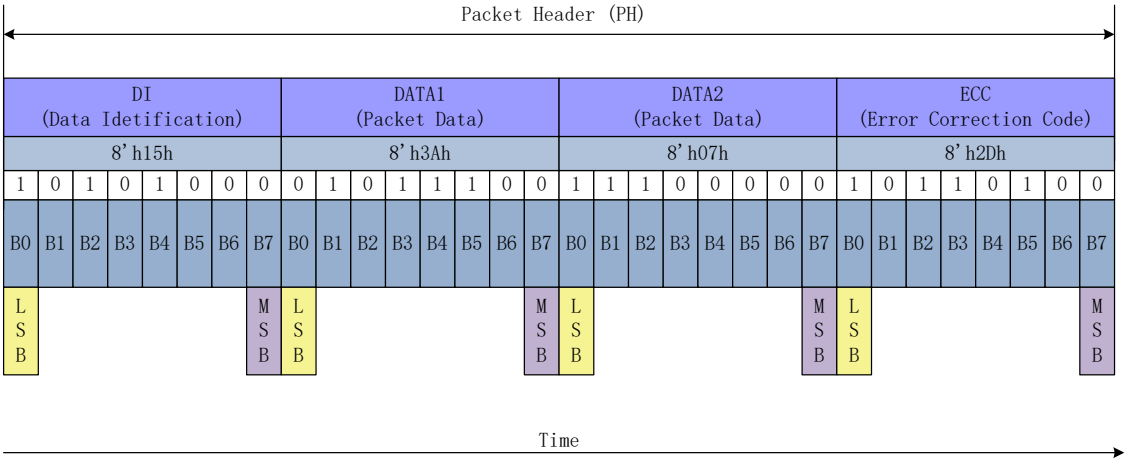
Time

4.5.3.1.3. Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1_{st} byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2_{nd} and 3_{rd} bytes: Packet Data (PD), Data 0 and 1
- 4_{th} byte: Error Correction Code (ECC)

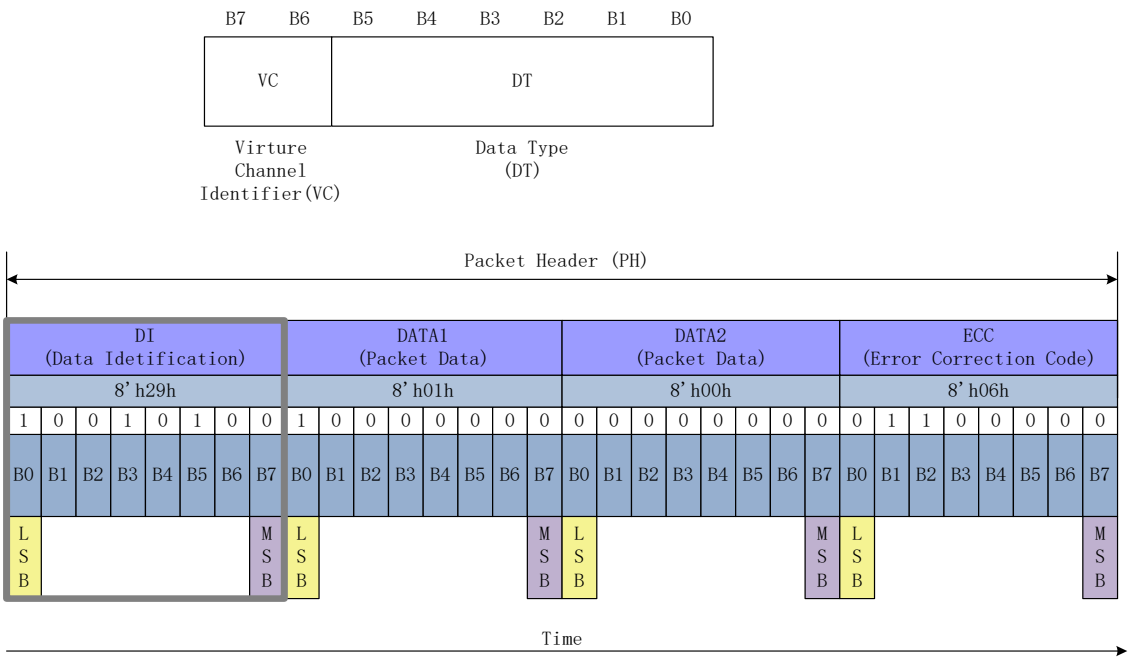


4.5.3.1.3.1. Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

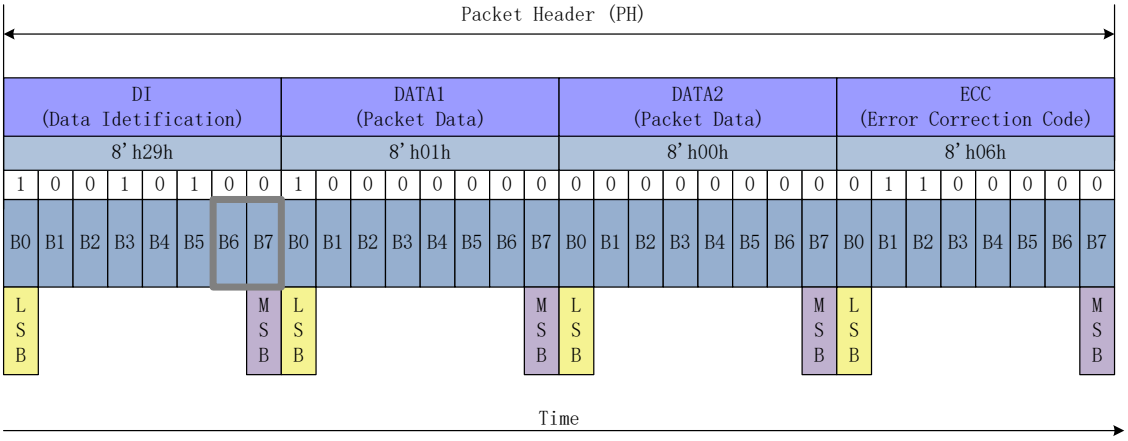
The Data Identification (DI) structure is illustrated on a diagram below.



4.5.3.1.3.1.1. Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Note that packets sent in a single transmission each have their own Virtual Channel assignment and can be directed to different peripherals.

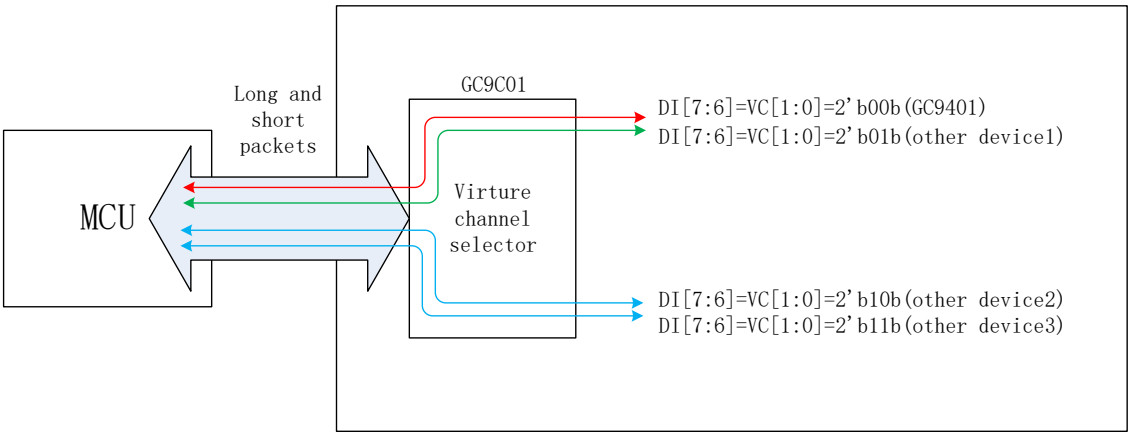
Virtual Channel (VC) is a part of Data Identification (DI [7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.



Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



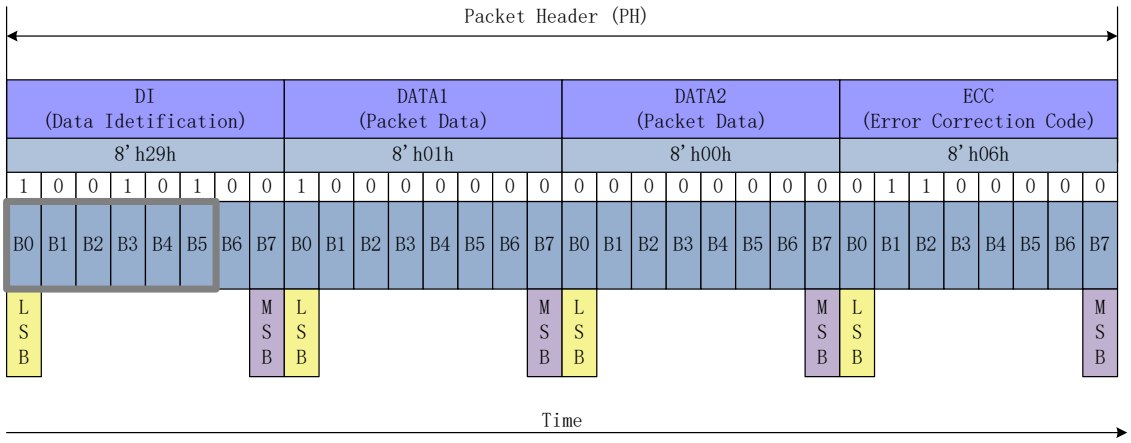
Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00b) when the MCU is sending "End of Transmission Packet" to the display module.

4.5.3.1.3.1.2. Data Type (DT)

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count Field for Long Packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start/end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet.

When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

Data Type (DT) is a part of Data Identification (DI [5…0]) structure and it is used to define a type of the used data on a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.



This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below

From the MCU to GC9C01									
B5	B4	B3	B2	B1	B0	Hex	Description	Short/Long Packet	Abbreviation
0	0	1	0	0	0	08	End of Transmission Packet, Note1	Spa (Short Packet)	EOTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, Note2	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Notes: 1. This can be used when the MCU wants to secure that there is the end of the transmission in High Speed Data Transferring (HSDT) mode.

2. This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.

3. The receiver is ignored other Data Type (DT) if they are not defined on tables.

From the GC9C01 to MCU									
B5	B4	B3	B2	B1	B0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	Spa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long	DCSRR-

								Packet)	L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

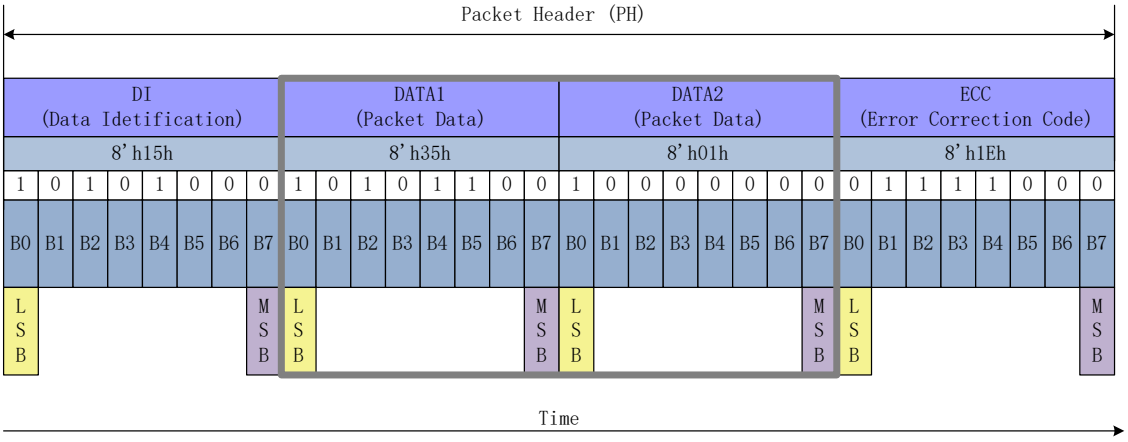
Notes: 1. The receiver is ignored other Data Type (DT) if they are not defined on tables.

4.5.3.1.3.2 Packet Data on the Short Packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send. Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to '0' if the information length is 1 byte.
Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

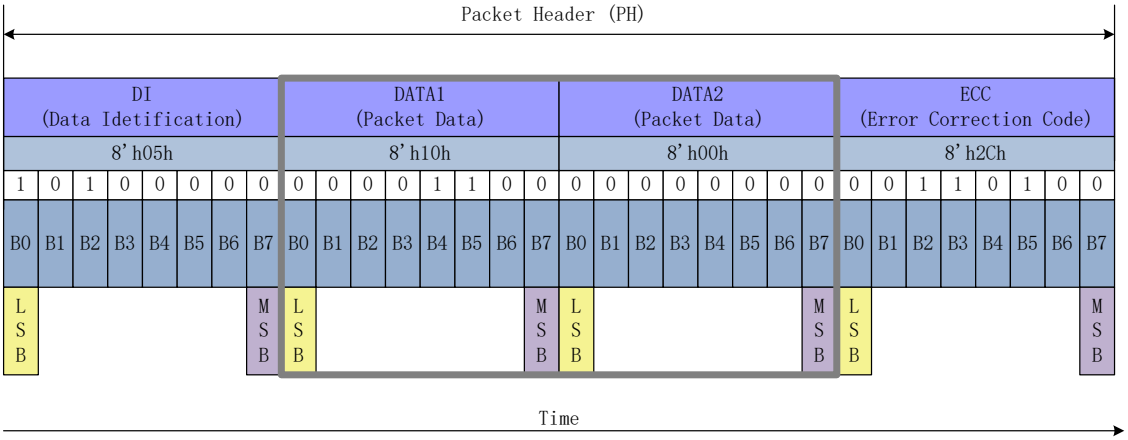
Packet Data (PD) information:

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)



Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)



4.5.3.1.3.3.Word Count on the Long Packet

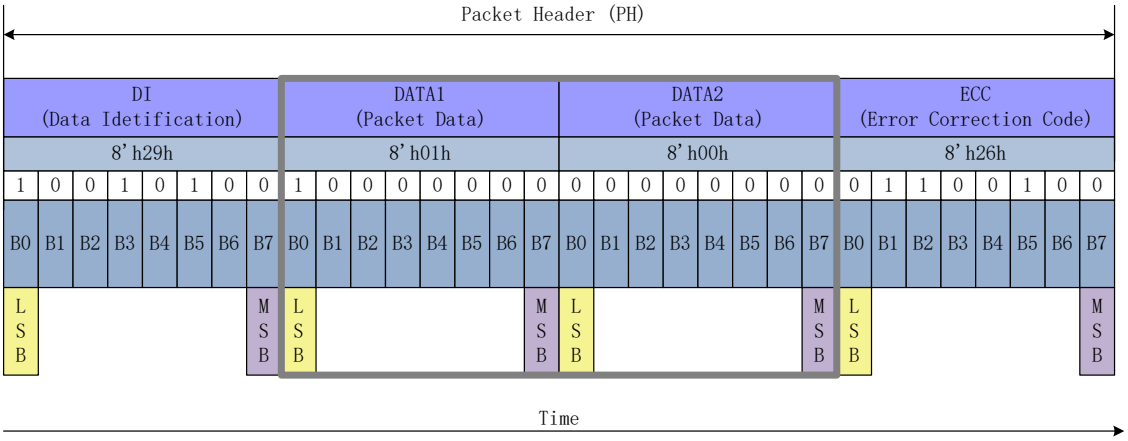
Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

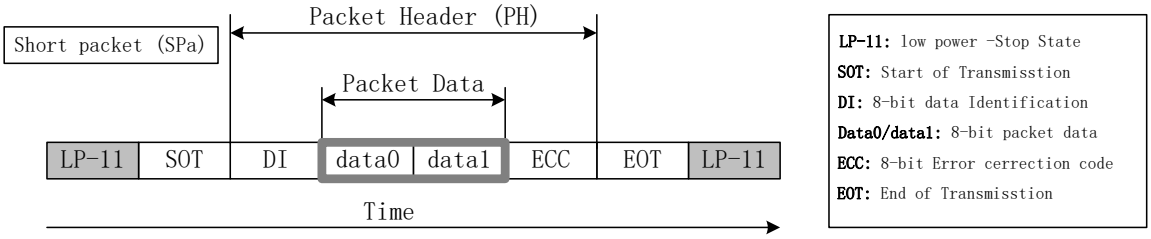
Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) are placed in the Packet Header (PH).

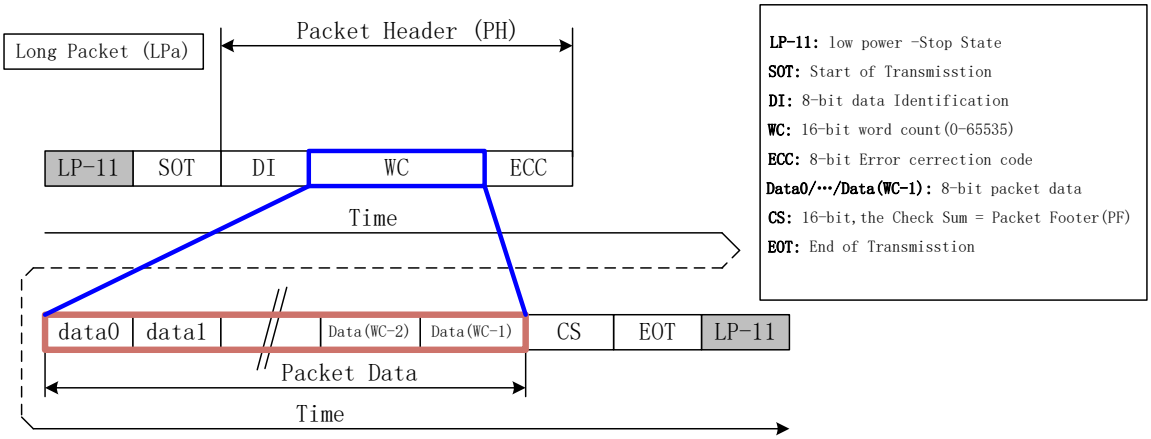
Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.







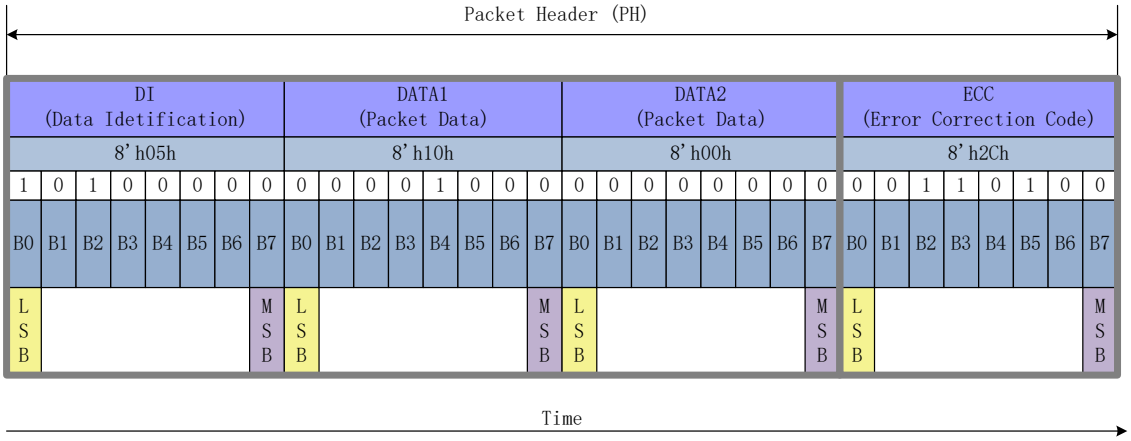
4.5.3.1.3.4. Error Correction Code (ECC)

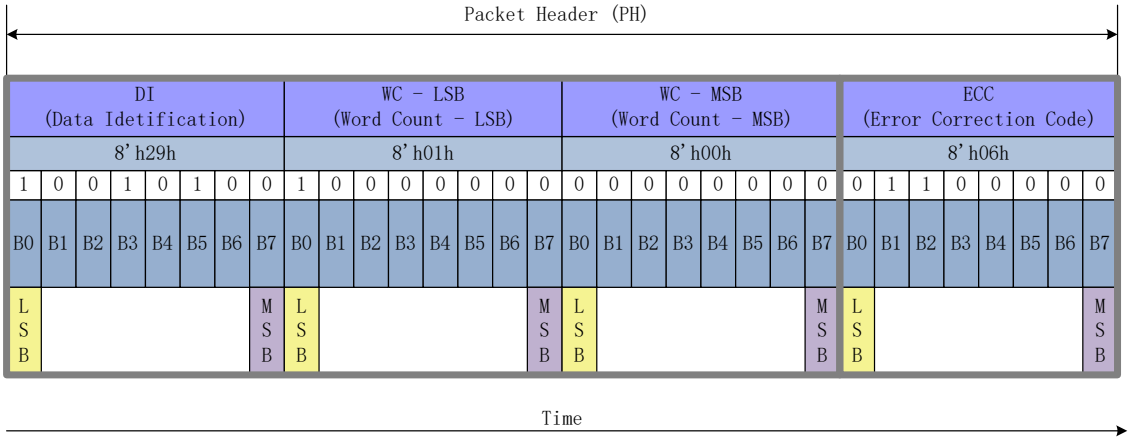
The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte and GC9C01 supports ECC in both forward- and reverse-direction communications.

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D [23…0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D [23…0])

D [23…0] is illustrated for reference purposes below.





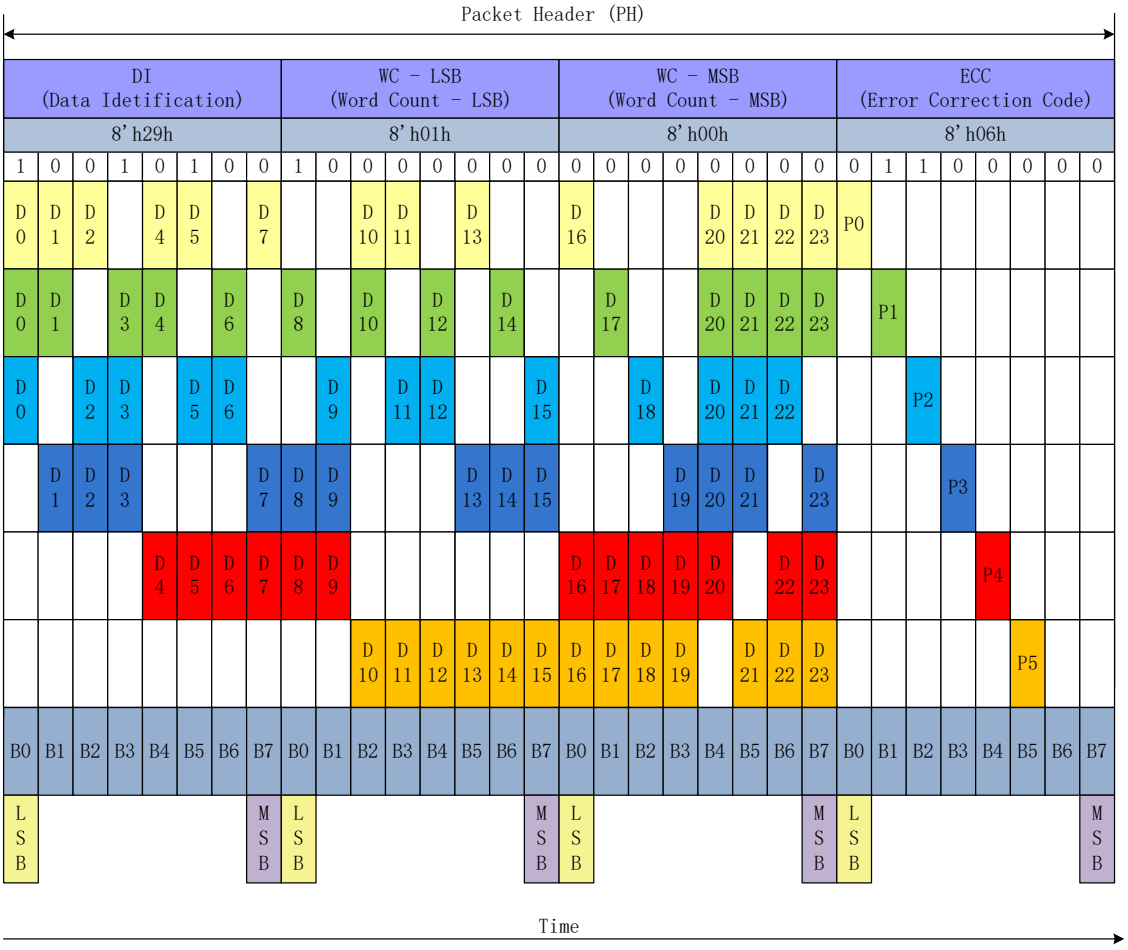
Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

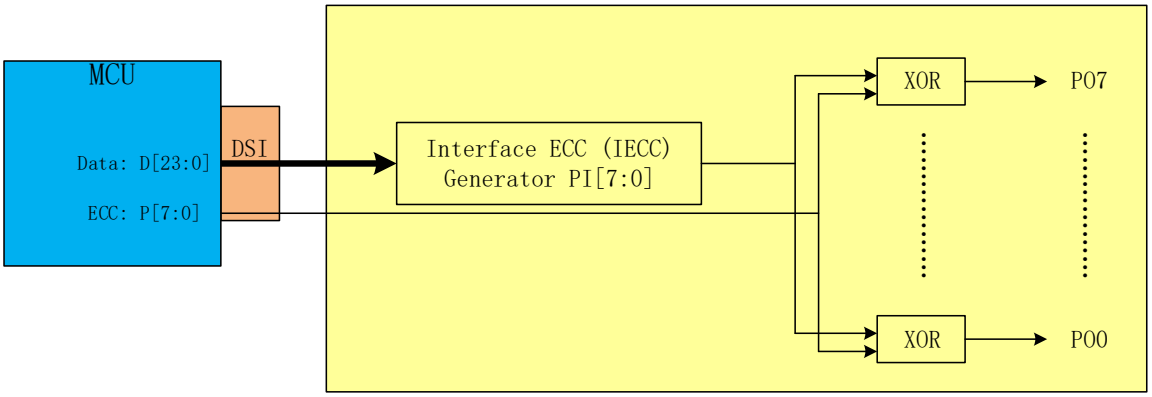
- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to ‘0’ because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, there is only needed 6 bits (P [5…0]) for Error Correction Code (ECC).



The transmitter (The MCU or GC9C01) is sending data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (GC9C01 or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is GC9C01, is illustrated for reference purposes below.



The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	0	0	0	0	0	0	03h
(ECC) ⊕ (IECC) → PO[7:0]	0	0	0	0	0	0	0	0	=00h → No Error
	LSB							MSB	

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	1	1	0	0	0	0	0Fh
(ECC) ⊕ (IECC) → PO[7:0]	0	0	1	1	0	0	0	0	=0Ch → Error
	LSB							MSB	

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah

D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

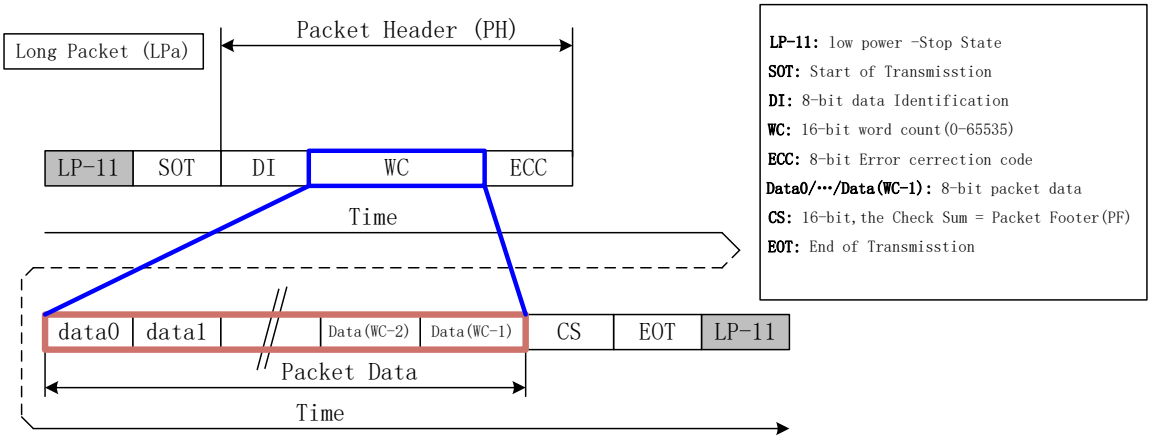
One error is detected if the value of the PO [7…0] is on the above table : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO [7…0] is not on the above table: One Bit Error Value of the Error Correction Code (ECC) e.g. PO [7…0] = 0Ch.

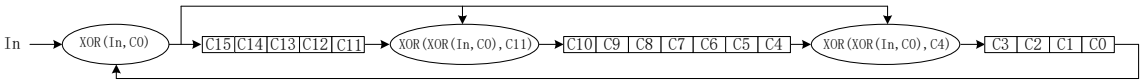
4.5.3.1.4 Packet Data on the Long Packet

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is illustrated as below:

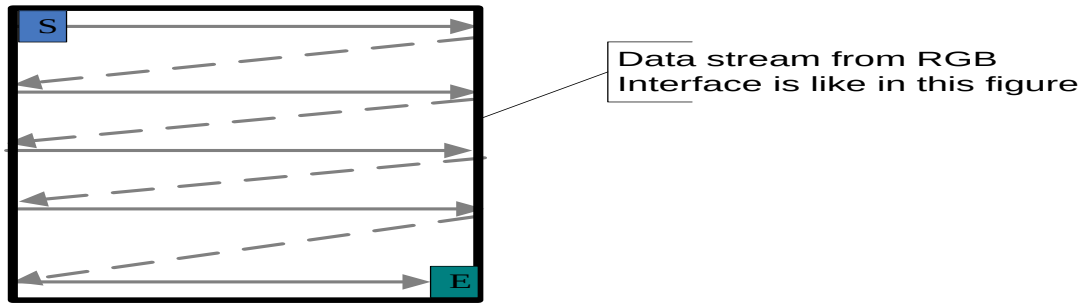


4.5.3.1.5. Packet Footer on the Long Packet

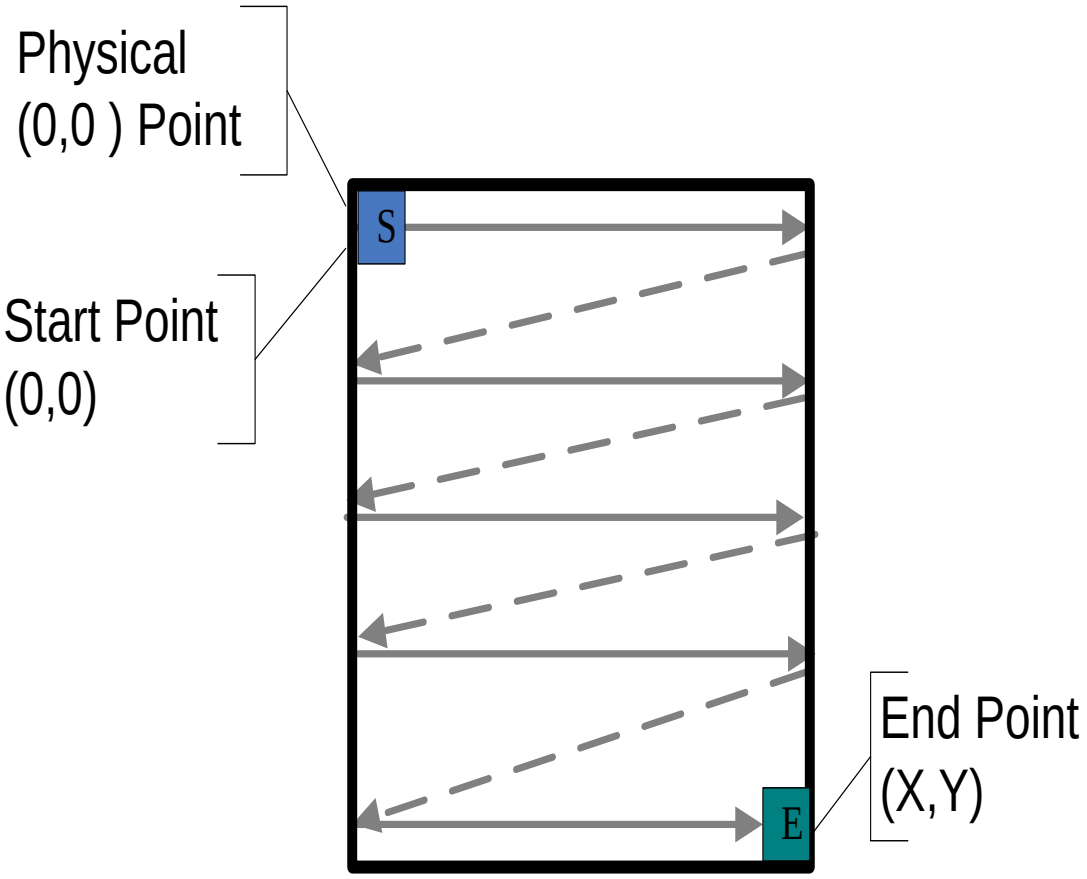
Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X_{16}+X_{12}+X_5+X_0$ as it is illustrated below.



The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.
The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).
An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



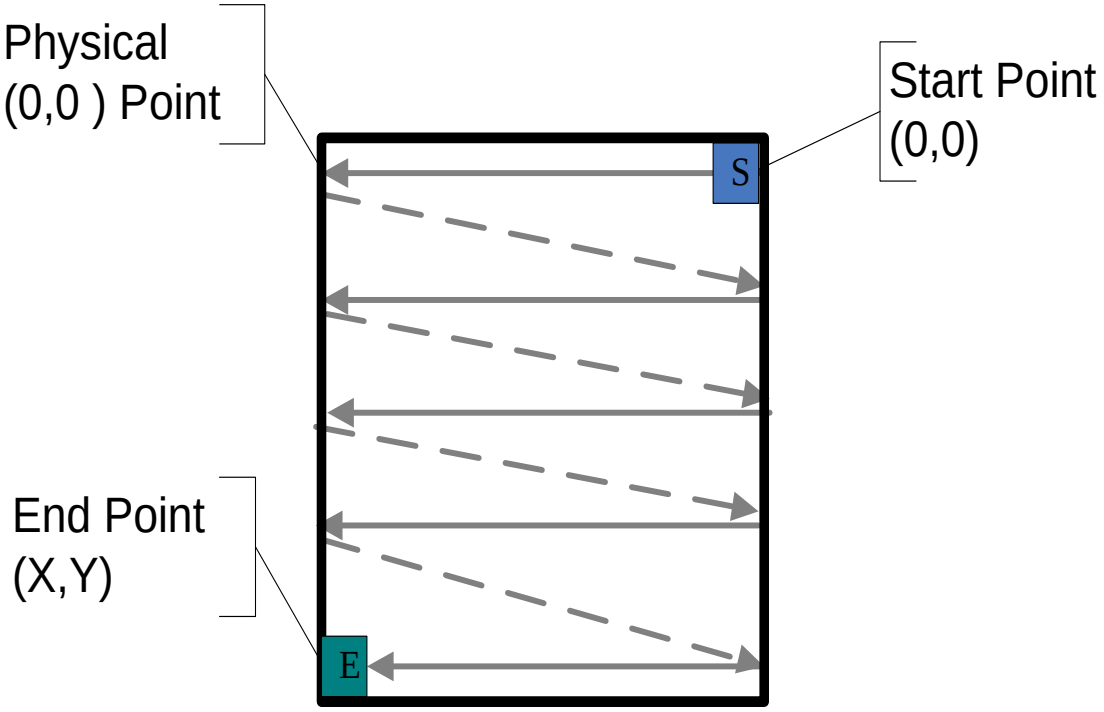
The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.
The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) is equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

4.6. Packet Transmissions

4.6.1. Packet form the MCU to GC9C01

4.6.1.1. Display Command Set (DCS)

Display Command Set (DCS), which is defined on next chapter, is used from the MCU to GC9C01. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated as below.


Physical
(0,0) Point
Start Point
(0,0)
S
End Point
(X,Y)
E

4.6.1.2. Display Command Set Write, no Parameter (DCSWN-S)

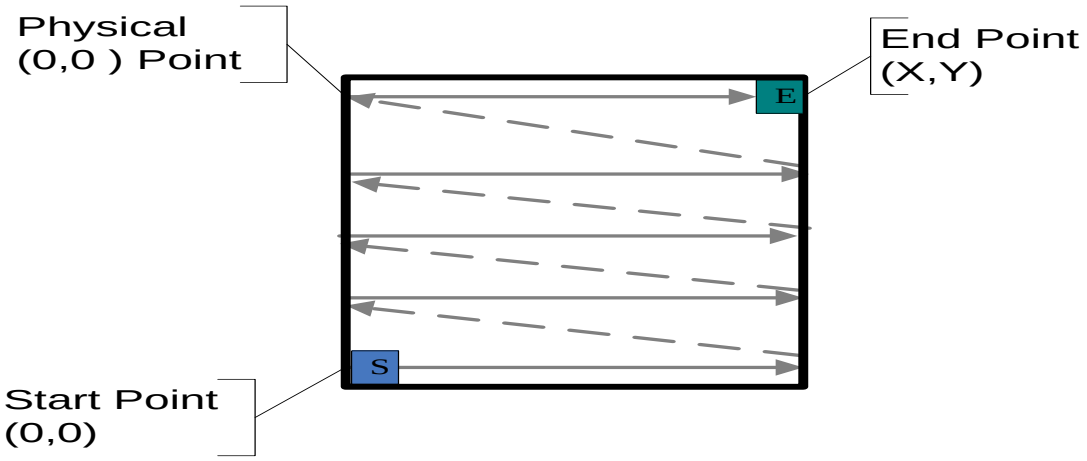
"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to GC9C01. These commands are defined on a table below.

Command
NOP (00h)
Software Reset (01h)
Sleep IN (10h)
Sleep Out (11h)
Partial Mode ON (12h)
Normal Display Mode ON (13h)
Display OFF (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode OFF (38h)
Idle Mode ON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0101b
- Packet Data (PD)
  - Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



4.6.1.3.Display Command Set Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to GC9C01. These commands are defined on a table below.

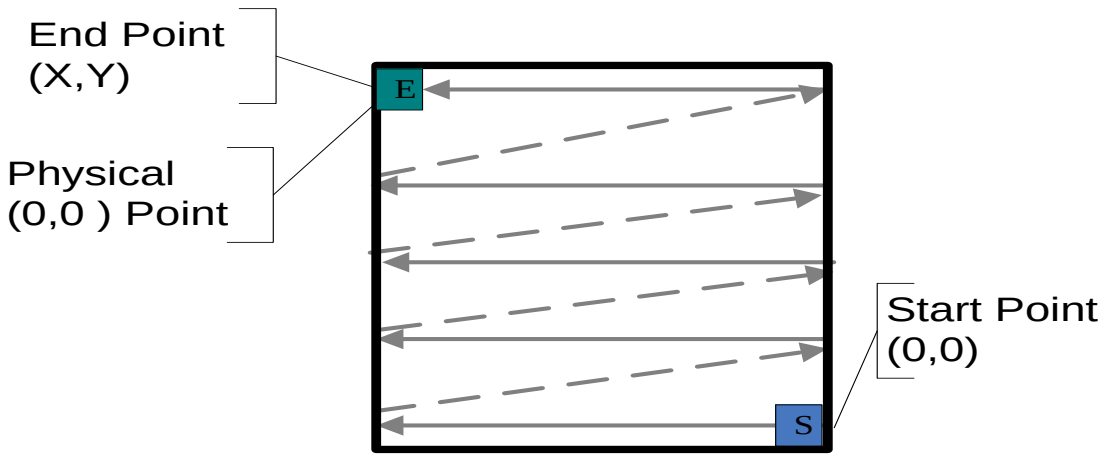
Command
Memory Write (2Ch), Note
Tearing Effect Line ON (35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Partial Mode ON (12h)
Memory Write Continue (3Ch), Note
Write Display Brightness (51h)
Write CTRL Display (53h)
Tearing Effect Line OFF (34h)
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

Note: One Subpixel has been written

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0101b
- Packet Data (PD)
  - Data 0: "Interface Pixel Format (3Ah)", Display Command Set (DCS)
  - Data 1: 55hex, Parameter of the DCS.
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



4.6.1.4.Display Command Set Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to GC9C01. Command (No Parameters) and Write (1 or more parameters) are defined on a table below.

Command
NOP (00h), Note 1
Software Reset (01h), Note 1
Sleep IN (10h) , Note 1
Sleep Out (11h) , Note 1
Partial Mode ON (12h) , Note 1
Normal Display Mode ON (13h) , Note 1
Display OFF (28h) , Note 1
Display ON (29h) , Note 1
Column Address Set (2Ah)
Page Address Set (2Bh)
Memory Write (2Ch), Note 2
Partial Area (30h)
Tearing Effect Line OFF (34h), Note 1
Tearing Effect Line ON (35h), Note 2
Memory Access Control (36h), Note 2
Idle Mode OFF (38h) , Note 1
Idle Mode ON (39h) , Note 1
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note 2
Write Display Brightness (51h), Note 2
Write CTRL Display (53h) , Note 2
Write Content Adaptive Brightness control (55h) , Note 2
Write CABC Minimum Brightness (5Eh)

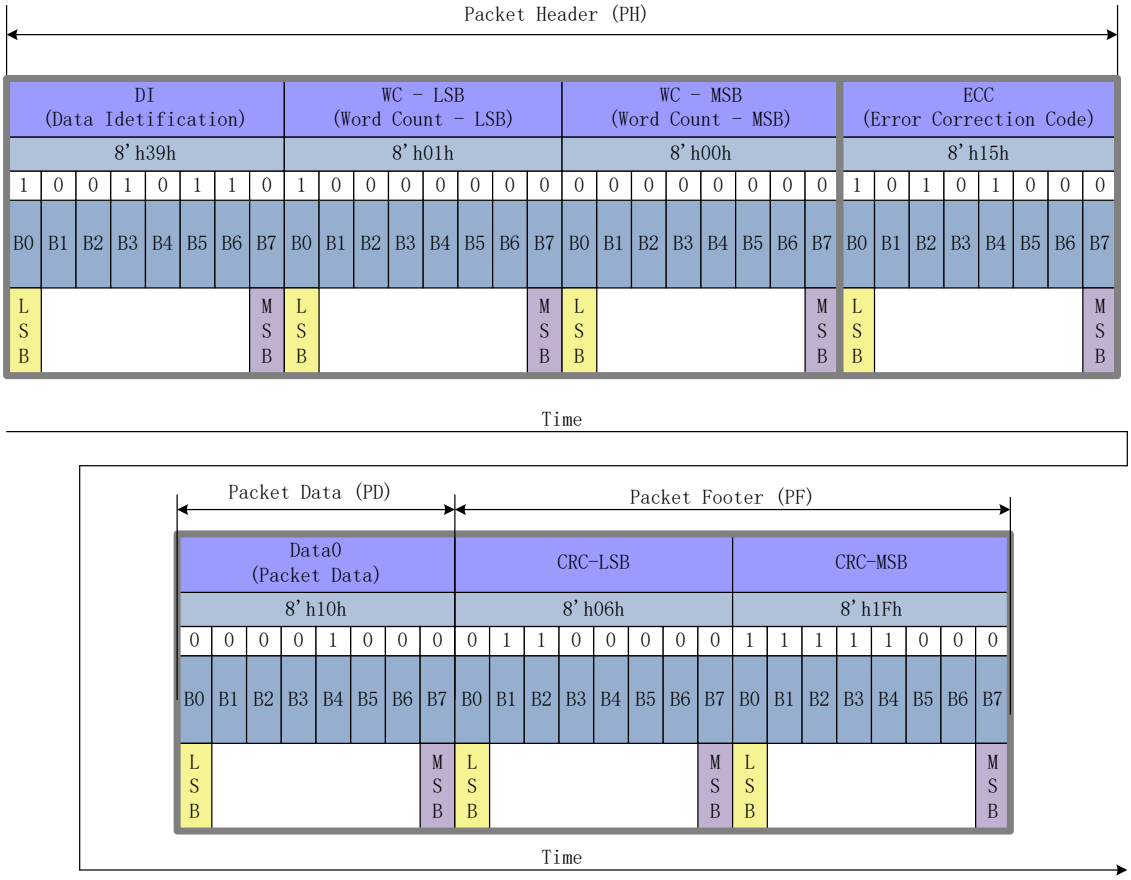
Notes: (1) Also Short Packet (SPa) can be used; See chapter "4.3.3.2.1.2 Display Command Set (DCS) Write, No Parameter"

(2) Also Short Packet (SPa) can be used; See chapter "4.3.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter"

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

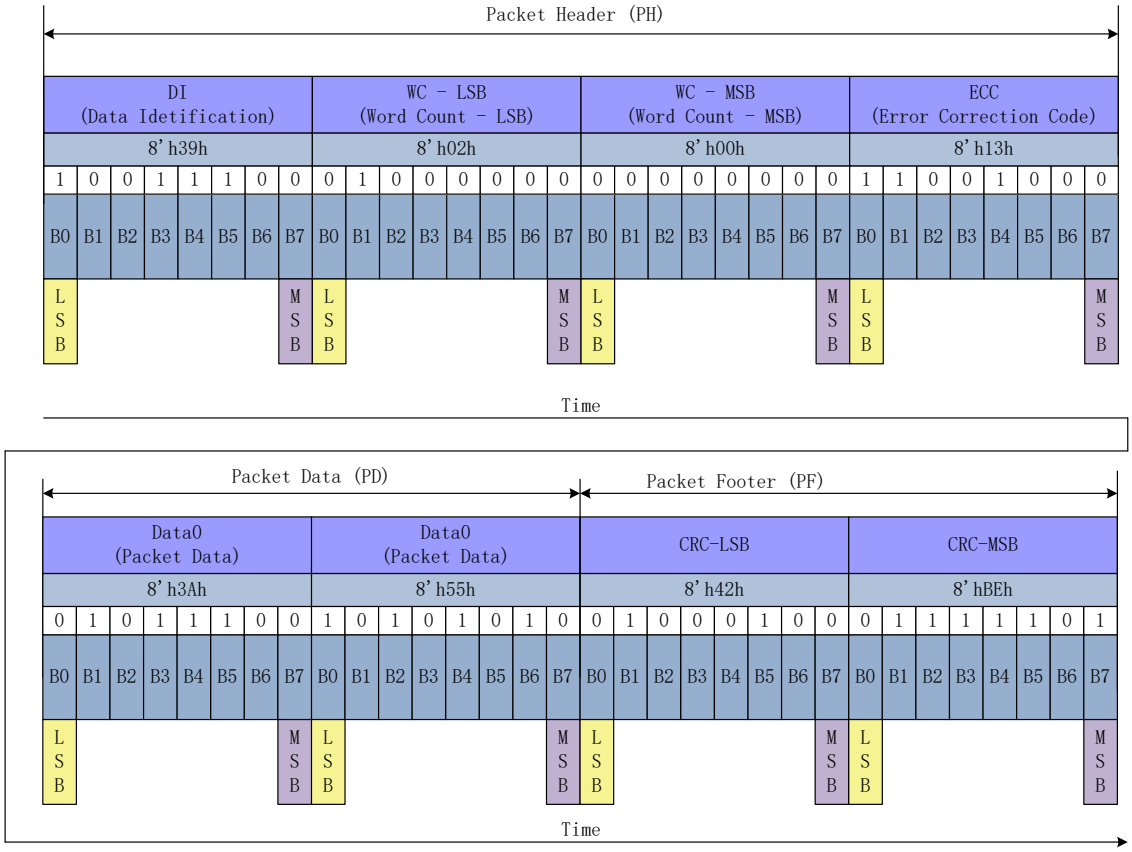
This is defined on the Long Packet (LPa) as follows.



Long Packet (LPa), when a command (1 Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Interface Pixel Format (3Ah)”, Display Command Set (DCS)
  - Data 1: 55hex, Parameter of the DCS
- Packet Footer (PF)

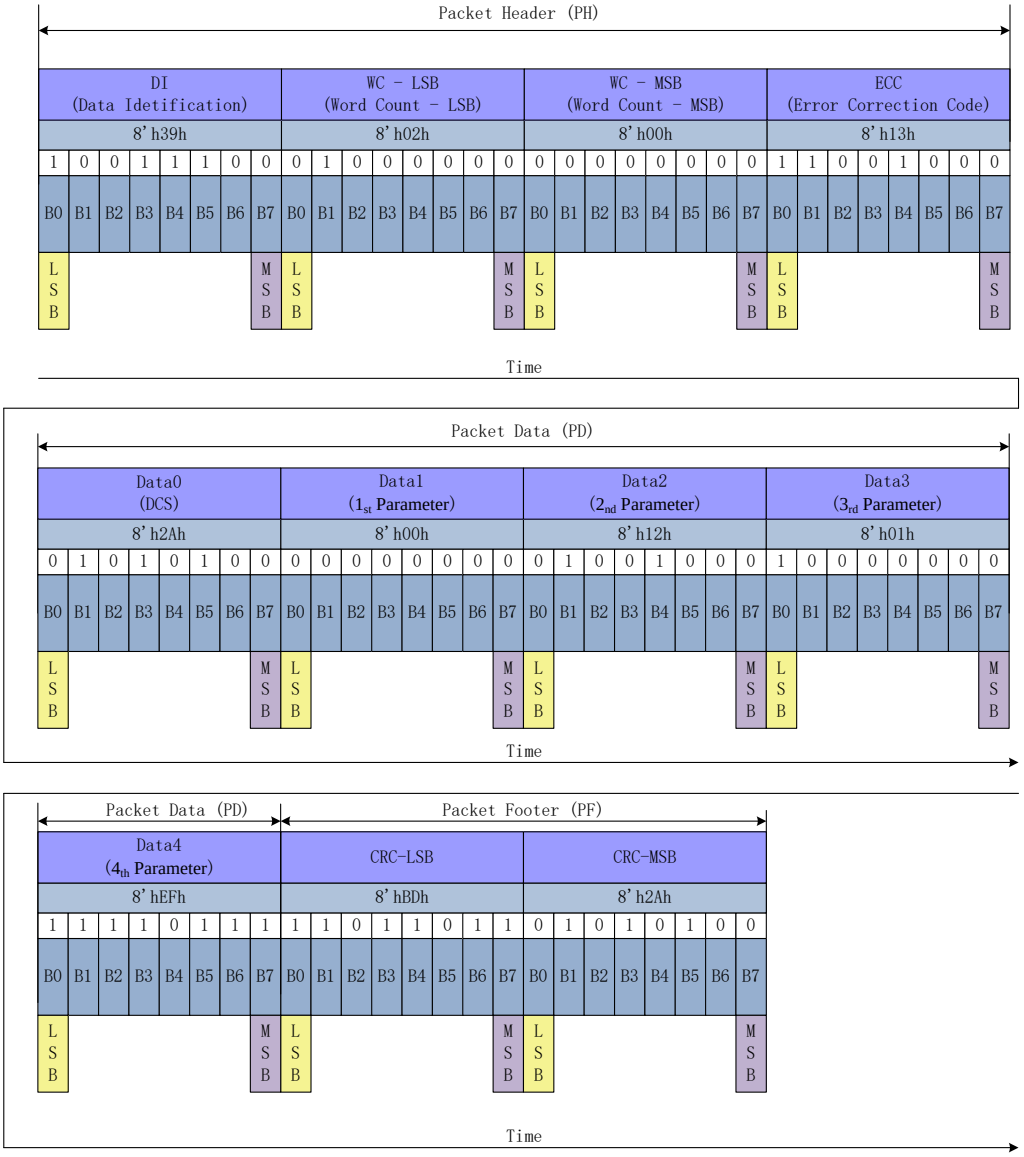
This is defined on the Long Packet (LPa) as follows.



Long Packet (LPa), when a command (4 Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Column Address Set (2Ah)”, Display Command Set (DCS)
  - Data 1: 00hex, 1_{st} Parameter of the DCS, Start Column SC [15…8]
  - Data 2: 12hex, 2_{nd} Parameter of the DCS, Start Column SC [7…0]
  - Data 3: 01hex, 3_{rd} Parameter of the DCS, End Column SC [15…8]
  - Data 4: 01hex, 4_{th} Parameter of the DCS, End Column SC [7…0]
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.


Packet Header (PH)
DI (Data Idetification)
WC - LSB (Word Count - LSB)
WC - MSB (Word Count - MSB)
ECC (Error Correction Code)
8'h39h
8'h02h
8'h00h
8'h13h
1 0 0 1 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 1 0 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Data0 (DCS)
Data1 (1st Parameter)
Data2 (2nd Parameter)
Data3 (3rd Parameter)
8'h2Ah
8'h00h
8'h12h
8'h01h
0 1 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 0 0 0 0 0 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Packet Footer (PF)
Data4 (4th Parameter)
CRC-LSB
CRC-MSB
8'hEFh
8'hBDh
8'h2Ah
1 1 1 1 0 1 1 1 1 1 0 1 1 0 1 1 0 1 0 1 0 1 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB
Time

4.6.1.5. Display Command Set Read, No Parameter (DCSRN-S)

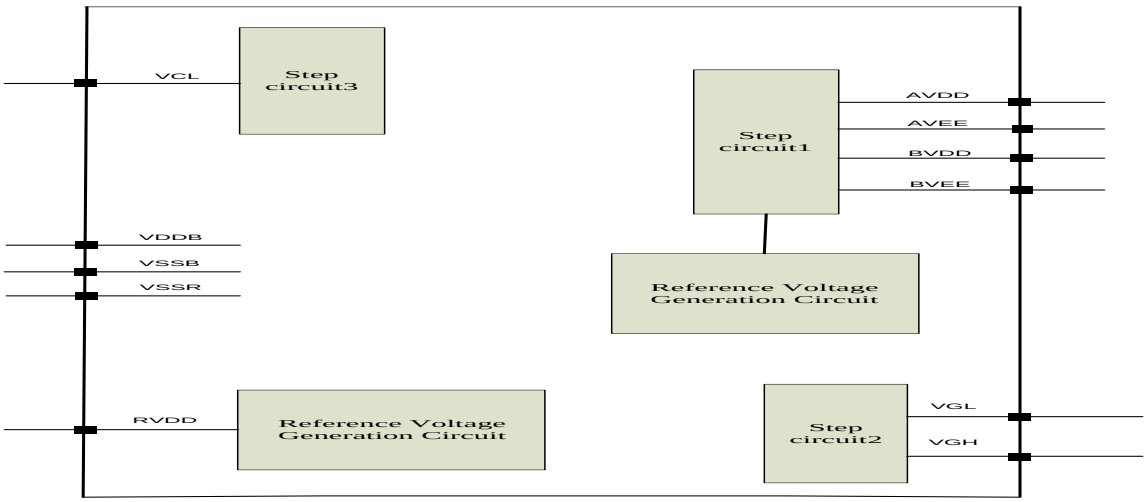
Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to GC9C01. These commands are defined on a table below. The 1st parameter (Dummy Data) is not returned as it is done in MCU parallel interface. The first returned parameter is the 2nd parameter in DSI case.

Command
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh
Memory Read (2Eh)
Memory Read Continue (3Eh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh

The MCU has to define to GC9C01, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to GC9C01. This same sequence is illustrated for reference purposes below.

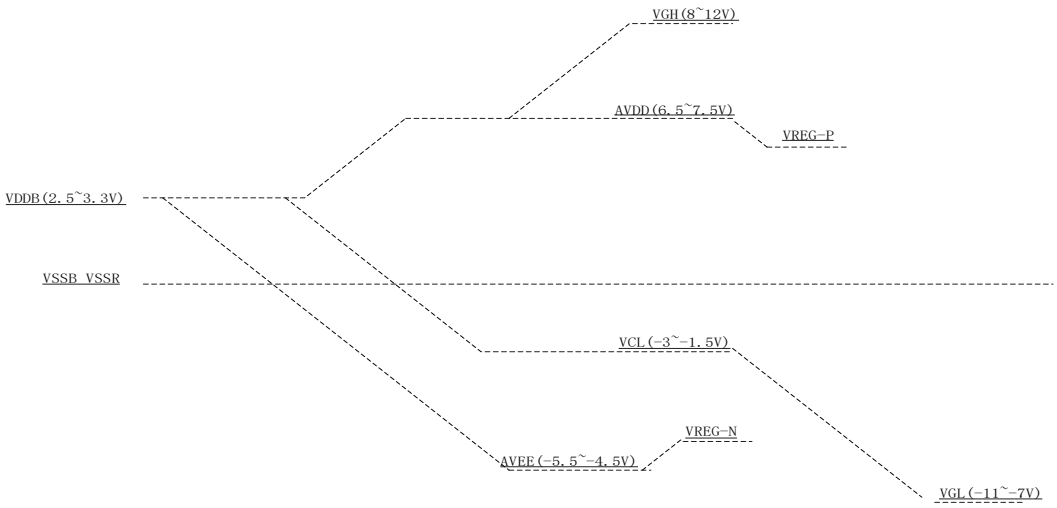
Step 1:

- The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to GC9C01 when it wants to return one byte from GC9C01
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - Data 0: 01hex
  - Data 1: 00hex
- Error Correction Code (ECC)



Step 2:

- The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to GC9C01
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0110b
- Packet Data (PD)
  - Data 0:“Read ID1 (DAh)”, Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)



Step 3: GC9C01 can send 2 different informations to the MCU after Bus Turnaround (BTA)

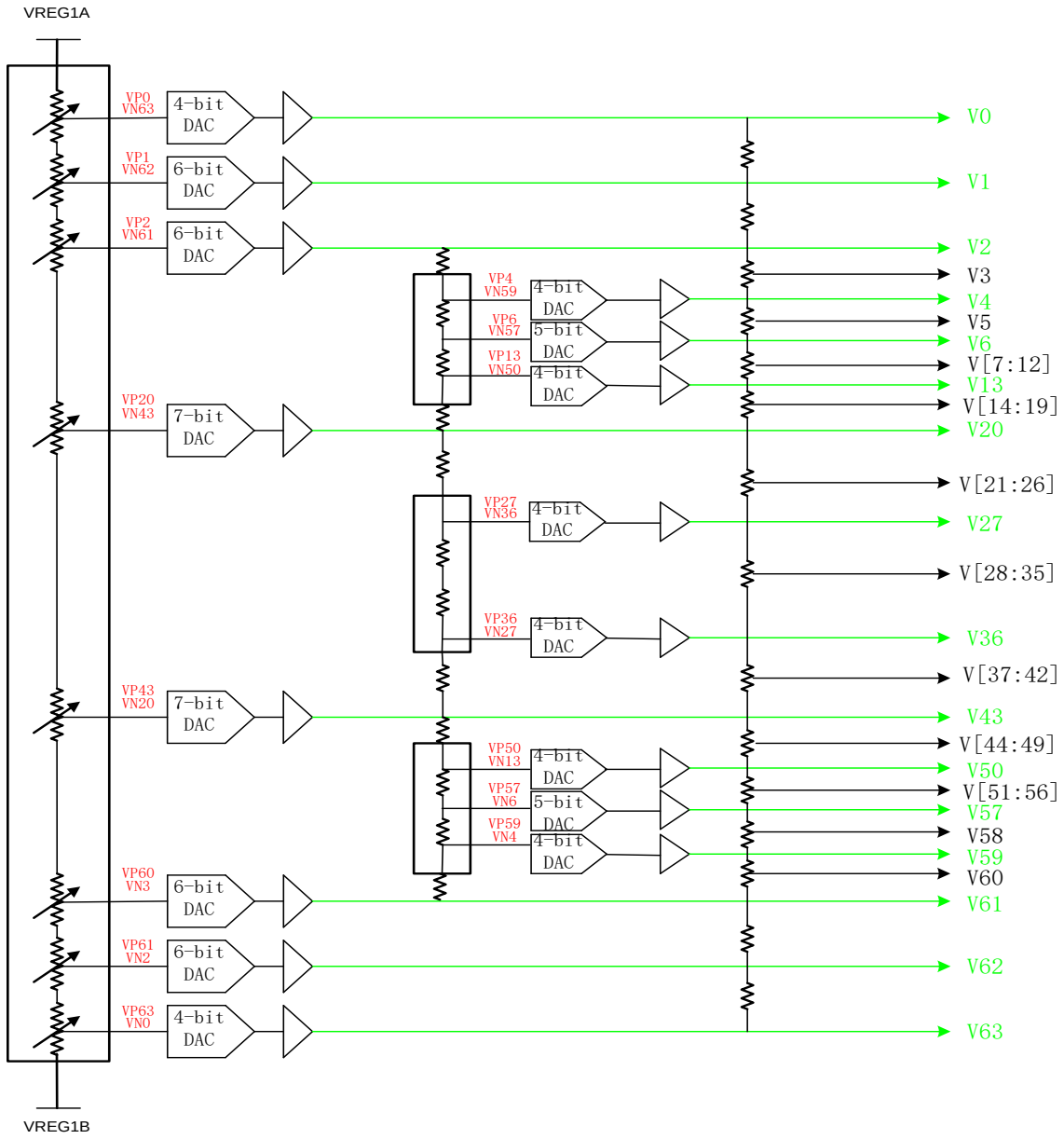
- An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command.
- Information of the received command. Short Packet (SPa) or Long Packet (LPa)

4.6.1.6. Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 00 1001b), from the MCU to GC9C01. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. GC9C01 is ignored Packet Data (PD) what the MCU is sending.
Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex (Random data)
  - Data 1: 23hex (Random data)
  - Data 2: 12hex (Random data)
  - Data 3: A2hex (Random data)
  - Data 4: E2hex (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.


VREG1A
VP0
VN63
4-bit
DAC
VP1
VN62
6-bit
DAC
VP2
VN61
6-bit
DAC
VP4
VN59
4-bit
DAC
VP6
VN57
5-bit
DAC
VP13
VN50
4-bit
DAC
VP20
VN43
7-bit
DAC
VP27
VN36
4-bit
DAC
VP36
VN27
4-bit
DAC
VP43
VN20
7-bit
DAC
VP50
VN13
4-bit
DAC
VP57
VN6
5-bit
DAC
VP59
VN4
4-bit
DAC
VP60
VN3
6-bit
DAC
VP61
VN2
6-bit
DAC
VP63
VN0
4-bit
DAC
V0
V1
V2
V3
V4
V5
V6
V[7:12]
V13
V[14:19]
V20
V[21:26]
V27
V[28:35]
V36
V[37:42]
V43
V[44:49]
V50
V[51:56]
V57
V58
V59
V60
V61
V62
V63
VREG1B

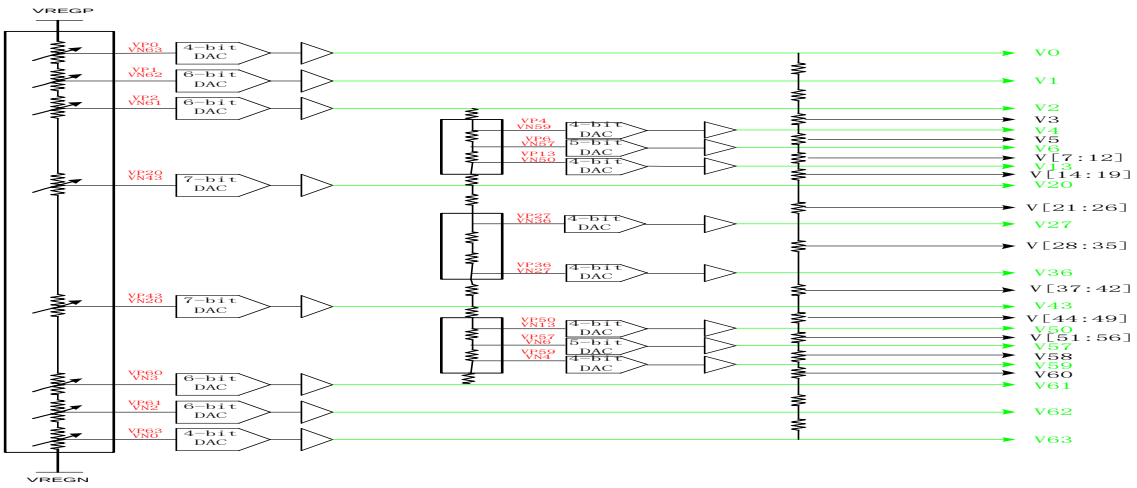
4.6.1.7. End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MCU to GC9C01. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before“End of Transmission” (EoT), which is an interface level functionality.
“End of Transmission Packet” (EoTP) should also be supported in the Low Power Data Transmission (LPDT) mode on GC9C01e even if this functionality has not been designed for this purposes.
The MCU can decide if it wants to use these “End of Transmission Packet” (EoTP) or not but GC9C01 has to be supporting both modes: With or Without “End of Transmission Packet” (EoTP).

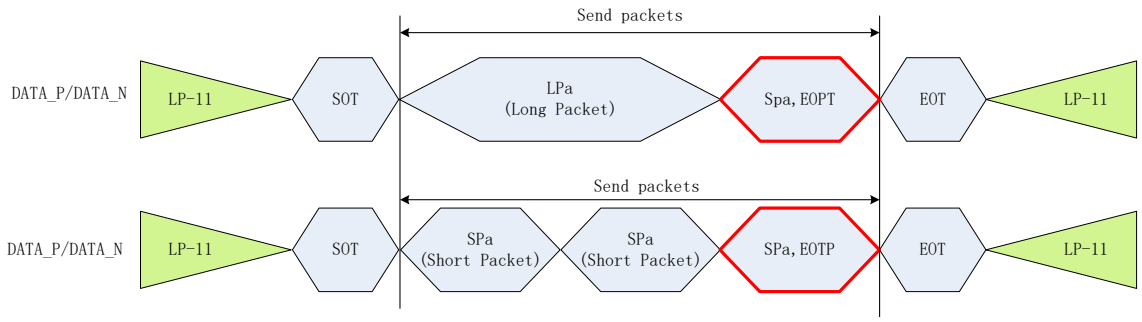
Short Packet (SPa) is using a fixed format as follows

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - Data 0: 0Fhex
  - Data 1: 0Fhex
- Error Correction Code (ECC)
  - ECC: 01hex

This is defined on the Short Packet (SPa) as follows.



Some use cases of the “End of Transmission Packet” (EoTP) are illustrated only for reference purposes below.



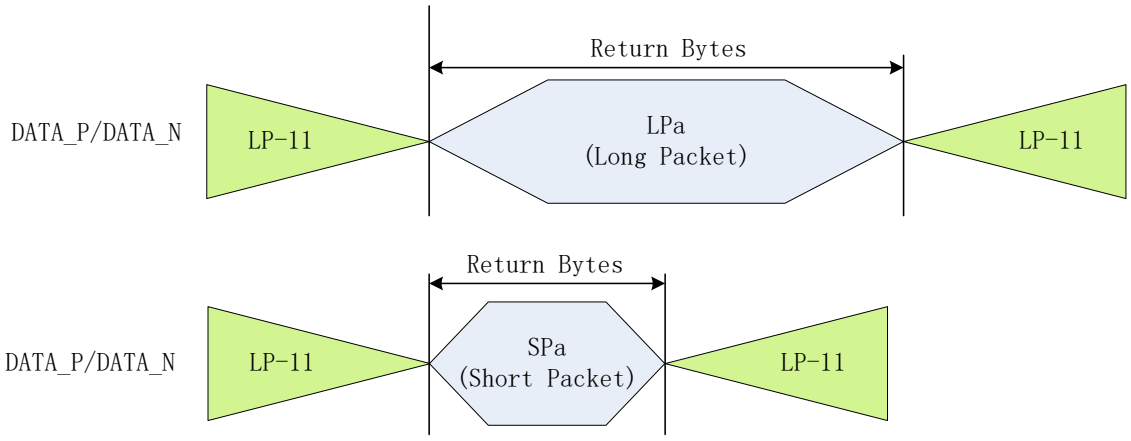
4.6.2.Packet from GC9C01 to MCU

4.6.2.1.Used Packet Types

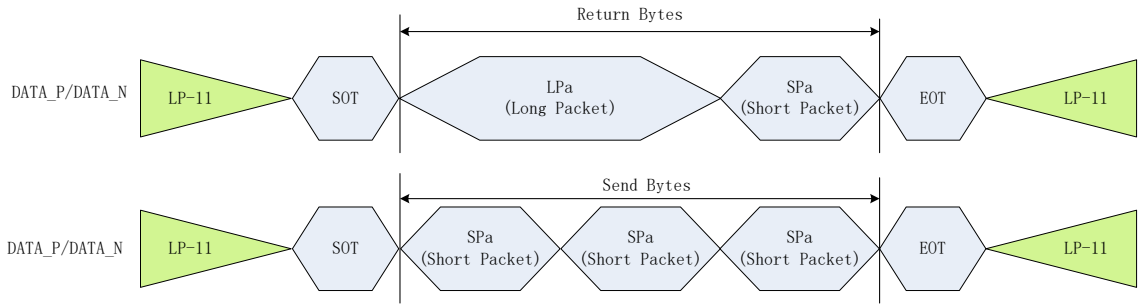
GC9C01 is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from GC9C01. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report (AwER). The used packet type is defined on Data Type (DT).

It is not possible that GC9C01 is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.

The return bytes on a single packet are illustrated for reference purposes below.



The return bytes on several packets are illustrated for reference purposes below.



4.6.2.2.Acknowledge with Error Report

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from GC9C01 to the MCU.
The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

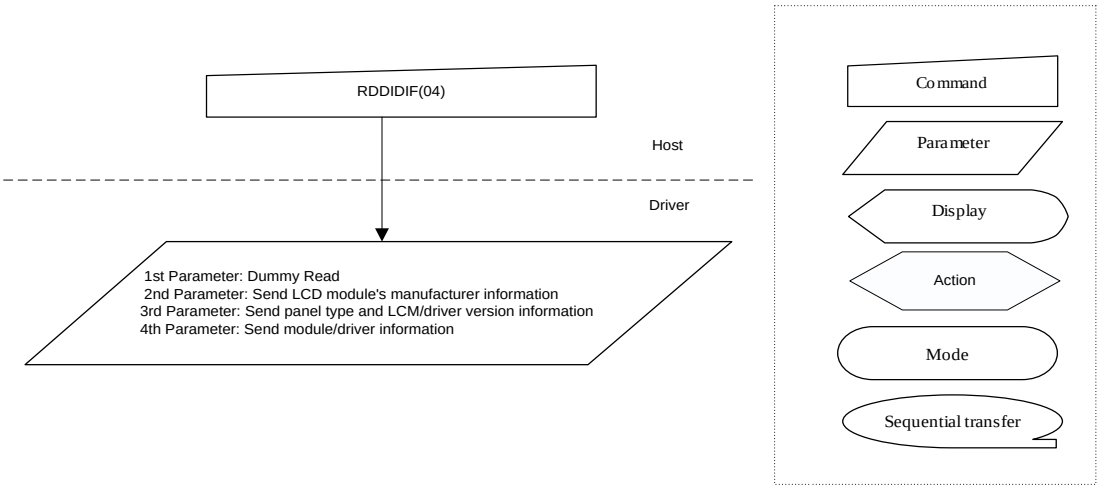
Bit	The Description of Acknowledge Error Report (AwER)	
	Short Packet	Long Packet
0	SoT Error	SoT Error
1	SoT Sync Error	SoT Sync Error
2	EoT Sync Error	EoT Sync Error
3	Escape Mode Entry Command Error	Escape Mode Entry Command Error
4	Low-Power Transmit Error	Low-Power Transmit Error
5	Any Protocol Timer-Out	Any Protocol Timer-Out
6	False Control Error	False Control Error
7	Contention is Detected on the Display Module	Contention is Detected on the Display Module
8	ECC Error, Single-Bit (Detected and Corrected)	ECC Error, Single-Bit (Detected and Corrected)
9	ECC Error, Multi-Bit (Detected, Not Corrected)	ECC Error, Multi-Bit (Detected, Not Corrected)
10	Reserved, Set to '0' internally	Checksum Error
11	DSI Data Type (DT), Not Recognized	DSI Data Type (DT), Not Recognized
12	DSI Virtual Channel (VC) ID Invalid	DSI Virtual Channel (VC) ID Invalid
13	DSI Protocol Violation	DSI Protocol Violation
14	Reserved, Set to '0' internally	Reserved, Set to '0' internally
15	Reserved, Set to '0' internally	Reserved, Set to '0' internally

These errors are included from all packages what has been received from the MCU to GC9C01, before Bus Turnaround (BTA). GC9C01 ignores the received packet which includes error or errors.

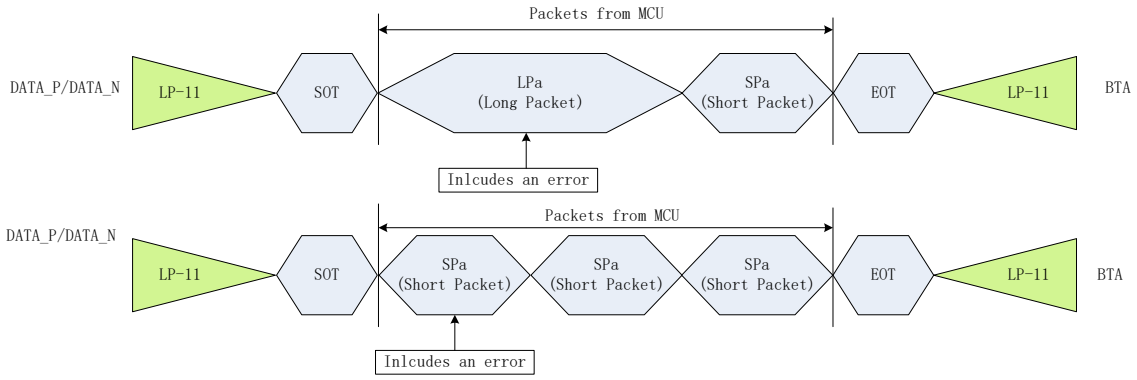
Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



It is possible that GC9C01 has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

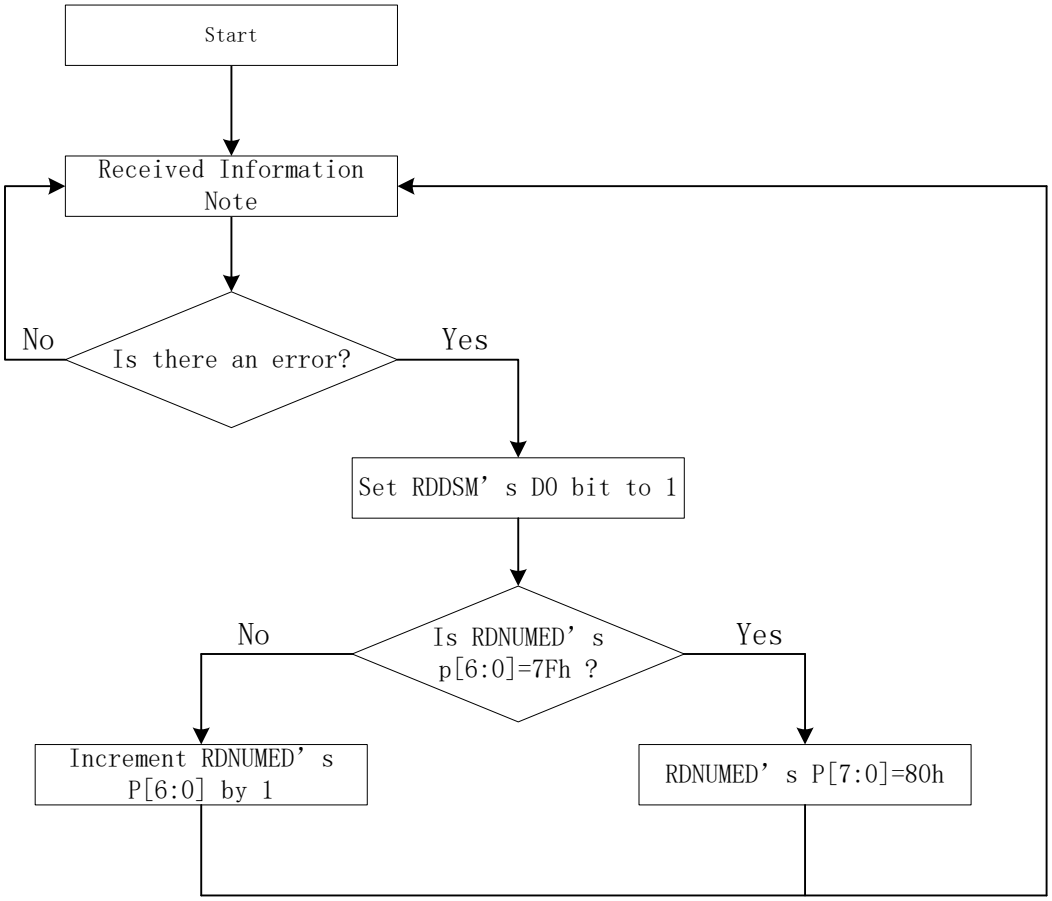


Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The numbers of the packets, which are including an error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from GC9C01.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Note: This information can Interface or Packet Level Communication but it is always from the MCU to GC9C01 in this case.

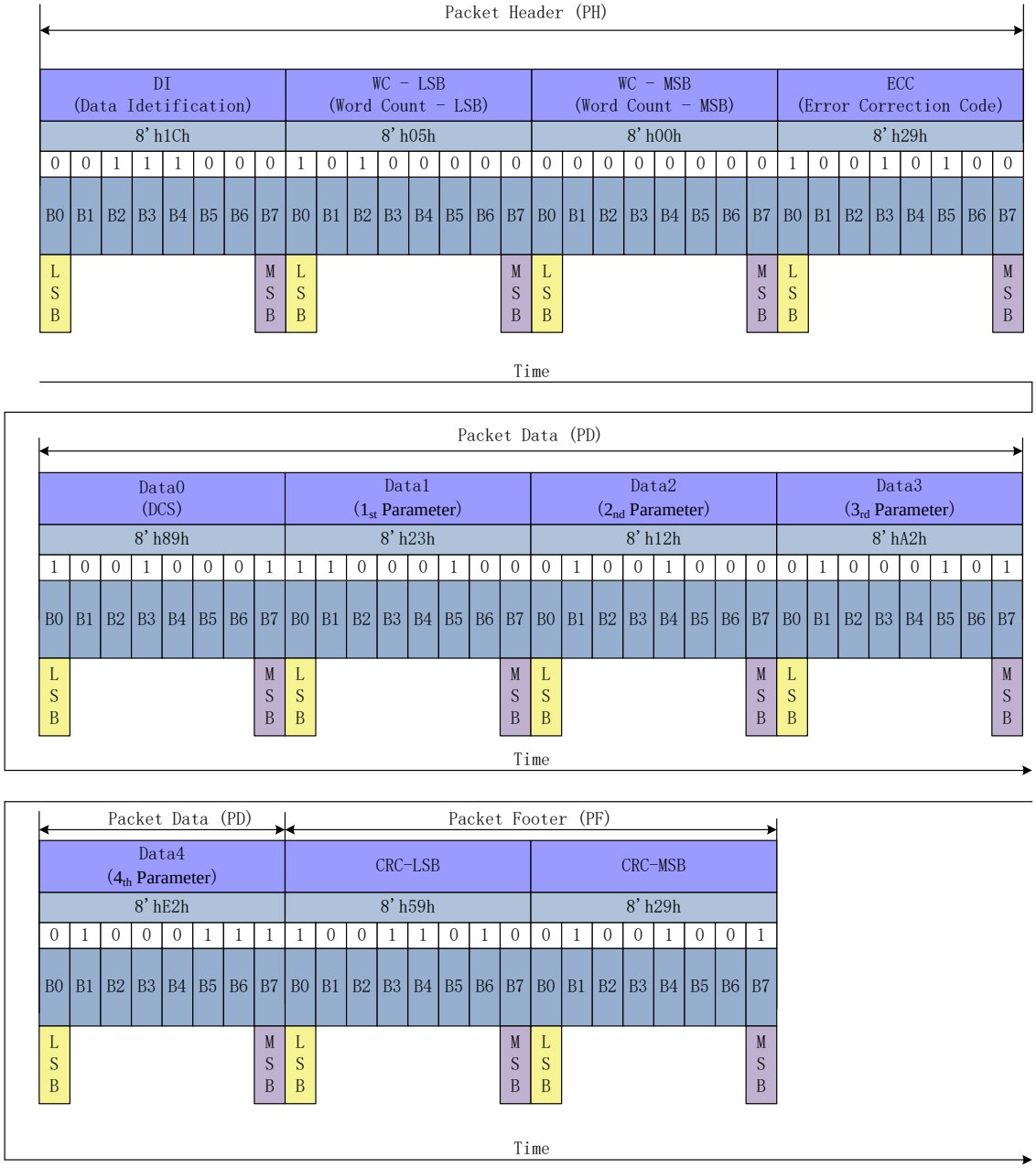
4.6.2.3.DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from GC9C01 to the MCU.
“DCS Read Long Response” (DCSRR-L) is used when GC9C01 wants to response a DCS Read command, which the MCU has sent to GC9C01.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex
  - Data 1: 23hex
  - Data 2: 12hex
  - Data 3: A2hex
  - Data 4: E2hex
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.


Packet Header (PH)
DI (Data Idetification)
WC - LSB (Word Count - LSB)
WC - MSB (Word Count - MSB)
ECC (Error Correction Code)
8'h1Ch
8'h05h
8'h00h
8'h29h
0 0 1 1 1 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Data0 (DCS)
Data1 (1st Parameter)
Data2 (2nd Parameter)
Data3 (3rd Parameter)
8'h89h
8'h23h
8'h12h
8'hA2h
1 0 0 1 0 0 0 1 1 1 0 0 0 1 0 0 0 1 0 0 1 0 0 0 0 1 0 0 0 1 0 1
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Packet Footer (PF)
Data4 (4th Parameter)
CRC-LSB
CRC-MSB
8'hE2h
8'h59h
8'h29h
0 1 0 0 0 1 1 1 1 0 0 1 1 0 1 0 0 1 0 0 1 0 0 1
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB
Time

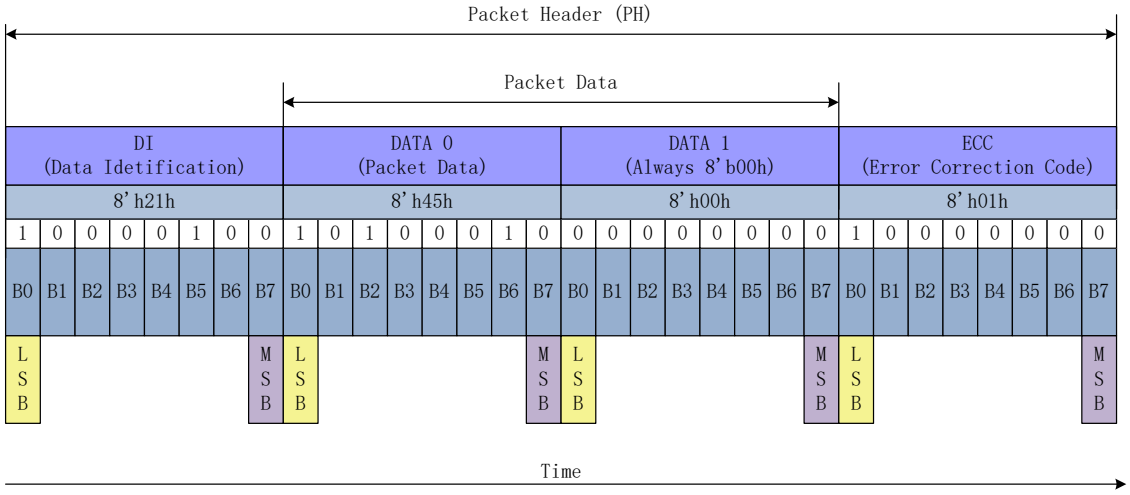
4.6.2.4.DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from GC9C01 to the MCU.
“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is used when GC9C01 wants to response a DCS Read command, which the MCU has sent to GC9C01.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 00hex (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows



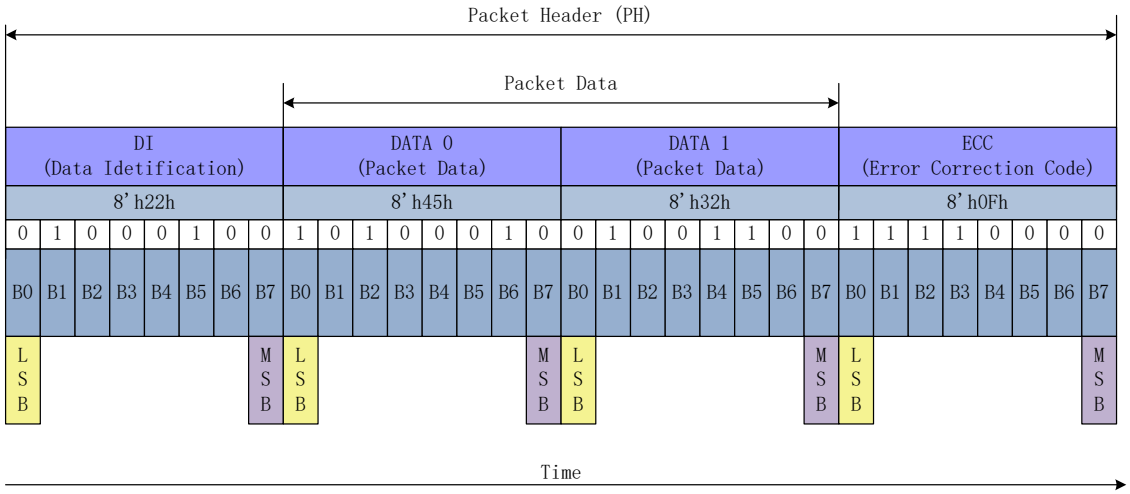
4.6.2.5. DCS Read Short Response, 2 Bytes Returned

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from GC9C01 to the MCU.
"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when GC9C01 wants to response a DCS Read command, which the MCU has sent to GC9C01.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 32hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



4.6.3. Communication Sequences

The communication sequences can be done on interface or packet levels between the MCU and GC9C01. This communication sequence description is for DSI data lanes (DSI-D0+/-) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.
Functions of the interface level communication are described on the following table.

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State

	LPDT	Low power data transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	TEE	Tearing Effect Event
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described on the following table.

Interface	Mode Abbreviation	Packet Size	Interface Action Description
MCU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
GC9C01	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

4.6.3.1.DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter“4.3.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, 1 Parameter Sequence – Example 2				
line	MCU	Information	GC9C01	Comment

	Packet Sender	Interface Mode Control	Direction	Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, 1 Parameter Sequence – Example 3						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	
5	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9C01
6	-	-	←	LP-11	-	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	-	-	←	ACK		No Error
9	-	-	←	LP-11	-	
10	-	BTA	←→	BTA	-	Interface Control Change from the GC9C01 to MCU
11	-	LP-11	→	-	-	End
12						
13	-	-	←	LPDT	AwER	Error Report
14	-	-	←	LP-11	-	
15	-	BTA	←→	BTA	-	
16	-	LP-11	→	-	-	End

4.6.3.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined on chapter"4.3.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, 0 Parameter Sequence – Example 1				
line	MCU	Information	GC9C01	Comment

	Packet Sender	Interface Mode Control	Direction	Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, 0 Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, 0 Parameter Sequence – Example 3						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	
5	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9C01
6	-	-	←	LP-11	-	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	-	-	←	ACK		No Error
9	-	-	←	LP-11	-	
10	-	BTA	←→	BTA	-	Interface Control Change from the GC9C01 to MCU
11	-	LP-11	→	-	-	End
12						
13	-	-	←	LPDT	AwER	Error Report
14	-	-	←	LP-11	-	
15	-	BTA	←→	BTA	-	
16	-	LP-11	→	-	-	End

4.6.3.3. DCS Write, Long Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined on chapter "4.3.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)" and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-l	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, Long Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-L	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, Long Parameter Sequence – Example 3						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-L	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	
5	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9C01
6	-	-	←	LP-11	-	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	-	-	←	ACK		No Error

9	-	-	←	LP-11	-	
10	-	BTA	←→	BTA	-	Interface Control Change from the GC9C01 to MCU
11	-	LP-11	→	-	-	End
12						
13	-	-	←	LPDT	AwER	Error Report
14	-	-	←	LP-11	-	
15	-	BTA	←→	BTA	-	
16	-	LP-11	→	-	-	End

DCS Write, Long Parameter Sequence – Example 4						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-L	HSDT	→	-	-	Memory Write (2Ch)
3	DCSW1-L	HSDT	→	-	-	Memory Write Continue (3Ch)
4	DCSW1-L	HSDT	→	-	-	Memory Write Continue (3Ch)
5	DCSW1-S	HSDT	→			Memory Write Continue (3Ch) with 1 Parameter
6	EoTP	HSDT	→			End of Transmission Packet
7	-	LP-11	→			End

Note: This is an example where is wanted to send image data in 4 packets.

4.6.3.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined on chapter "4.3.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	SMRPS-S	HSDT	→	-	-	Defined how many data byte is wanted to read : 1 byte
3	DCSW-L	HSDT	→	-	-	Wanted to get a response ID1 (DAh)

4	EoTP	HSDT	→	-	-	End of Transmission Packet
5	-	LP-11	→	-	-	
6	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9C01
7	-	-	←	LP-11	-	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is corrected by ECC →Go to Line 19
8						
9	-	-	←	ACK		Responsed 1 byte return
10	-	-	←	LP-11	-	
11	-	BTA	←→	BTA	-	Interface Control Change from the GC9C01 to MCU
12	-	LP-11	→	-	-	End
13						
14	-	-	←	LPDT	AwER	Error Report
15	-	-	←	LP-11	-	
16	-	BTA	←→	BTA	-	
17	-	LP-11	→	-	-	End
18						
19			←	LPDT	DCSRR1-S	Responsed 1 byte return
20			←	LPDT	AwER	Error Report (Error is Corrected by ECC)
21			←	LP-11	-	
22		BTA	←→	BTA	-	Interface Control Change from the GC9C01 to MCU
23		LP-11	→	-	-	End

DCS Read, No Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	SMRPS-S	HSDT	→	-	-	Defined how many data byte is wanted to read : 1 byte
3	DCSW-L	HSDT	→	-	-	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	-	-	End of Transmission Packet
5	-	LP-11	→	-	-	
6	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9C01
7	-	-	←	LP-11	-	If No Error → Go to Line 9

						If Error Occurs → Go to Line 14 If Error is corrected by ECC →Go to Line 19
8						
9	-	-	←	ACK		Responsed 200 byte return
10	-	-	←	LP-11	-	
11	-	BTA	←→	BTA	-	Interface Control Change from the GC9C01 to MCU
12	-	LP-11	→	-	-	End
13						
14	-	-	←	LPDT	AwER	Error Report
15	-	-	←	LP-11	-	
16	-	BTA	←→	BTA	-	
17	-	LP-11	→	-	-	End
18						
19			←	LPDT	DCSRR1-S	Responsed 200 byte return
20			←	LPDT	AwER	Error Report (Error is Corrected by ECC)
21			←	LP-11	-	
22		BTA	←→	BTA	-	Interface Control Change from the GC9C01 to MCU
23		LP-11	→	-	-	End

4.6.3.5.Null Packet, No Data Sequence

A Long Packet (LPa) of "Null Packet, No Data (NP-L)" is defined on chapter "4.3.3.2.1.6 Null Packet, No Data (NP-L)" and an example sequence, how this packet is used, is described on the following table.

Null Packet, No Data Sequence – Example						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	NP-L	HSDT	→	-	-	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

4.6.3.6. End of Transmission Packet

A Short Packet (SPa) of "End of Transmission Packet (EoTP)" is defined on chapter "4.3.3.2.1.7 End of Transmission Packet (EoTP)" and an example sequence, how this packet is used, is described on the following table.

End of Transmission Packet – Example						
line	MCU		Information Direction	GC9C01		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	NP-L	HSDT	→	-	-	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

5. Function Description

5.1. Display data GRAM mapping

The display data RAM stores display dots and consists of 360x360x18 bits. There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

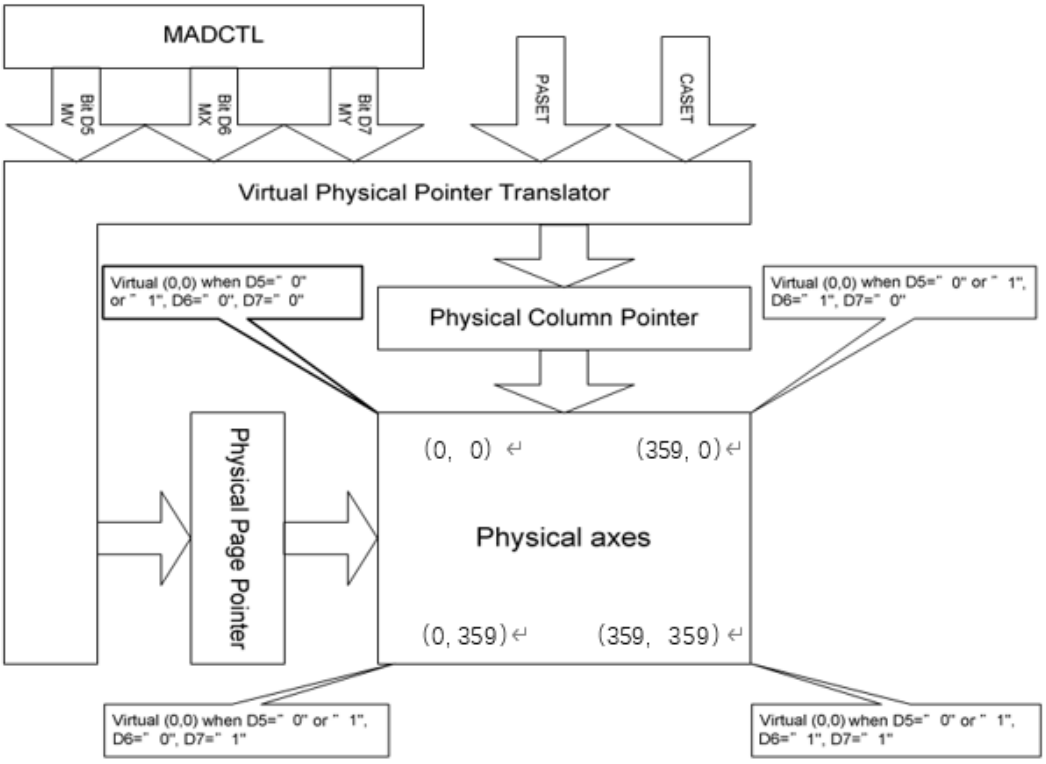
GRAM address for display panel position as shown in the following table

Table31.

(00,00)h	(00,01)h	…… …	(00, 165)h	(00, 166)h	(00,167)h
(01,00)h	(01,01)h	…… …	(01, 165)h	(01, 166)h	(01, 167)h
(02,00)h	(02,01)h	…… …	(02, 165)h	(02, 166)h	(02, 167)h
(03,00)h	(03,01)h	…… …	(03, 165)h	(03, 166)h	(03, 167)h
. . .	. . .	. . .	. . .	. . .	. . .
(165,00)h	(165,01)h	…… …	(165, 165)h	(165, 166)h	(165, 167)h
(166,00)h	(166,01)h	…… …	(166, 165)h	(165, 166)h	(166, 167)h
(167,00)h	(167,01)h	…… …	(167, 165)h	(165, 166)h	(167, 167)h

5.2. MCU to memory write/read direction

The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits D5, D6, and D7 as described below.

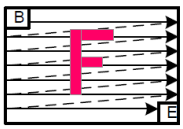
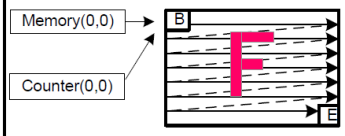
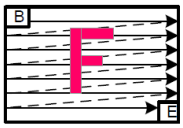
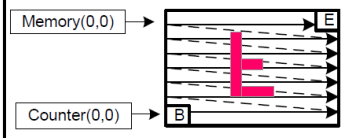
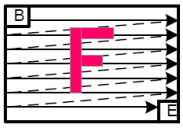
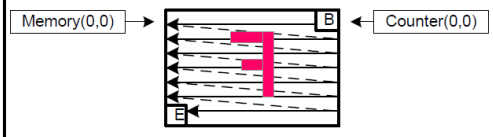
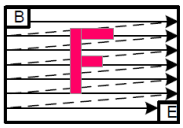
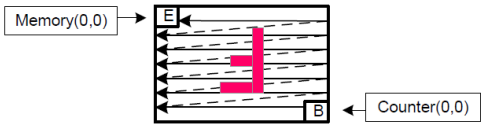
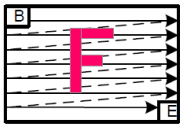
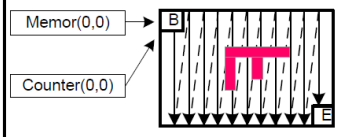
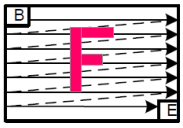
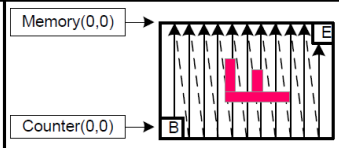
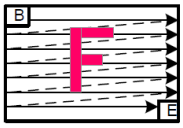
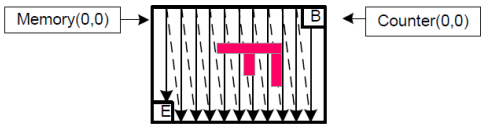
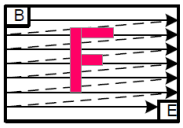
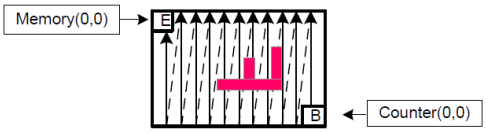


D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (359-Physical Page Pointer)
0	1	0	Direct to (359-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (359-Physical Column Pointer)	Direct to (359-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (359-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (359-Physical Column Pointer)
1	1	1	Direct to (359-Physical Page Pointer)	Direct to (359-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MCU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

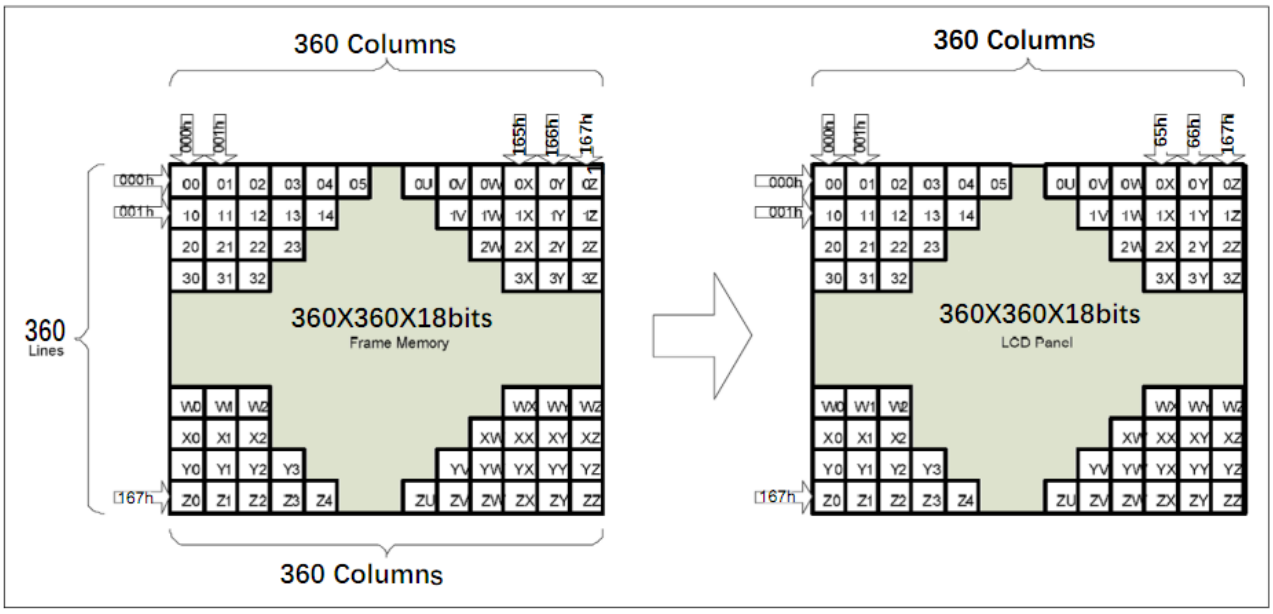
5.3. GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** , the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement.

The following Tables show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

GRAM X address and display panel position:

GC9C01 supports three kinds of display mode: one is Normal Display Mode, the other is Partial Display Mode, and Scrolling Display Mode.

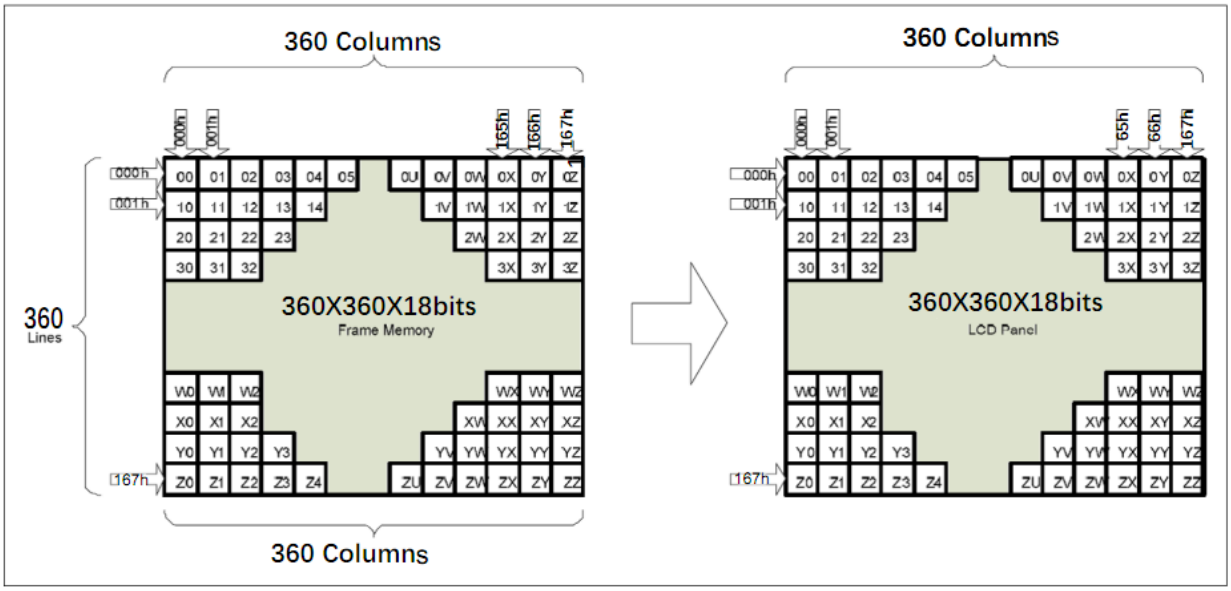


5.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 0167h and page pointer is 0000h to 0167h is displayed.

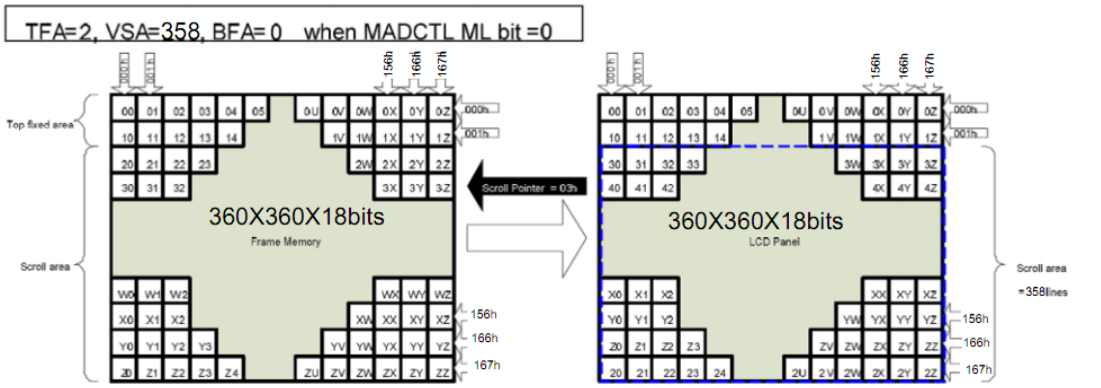
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)

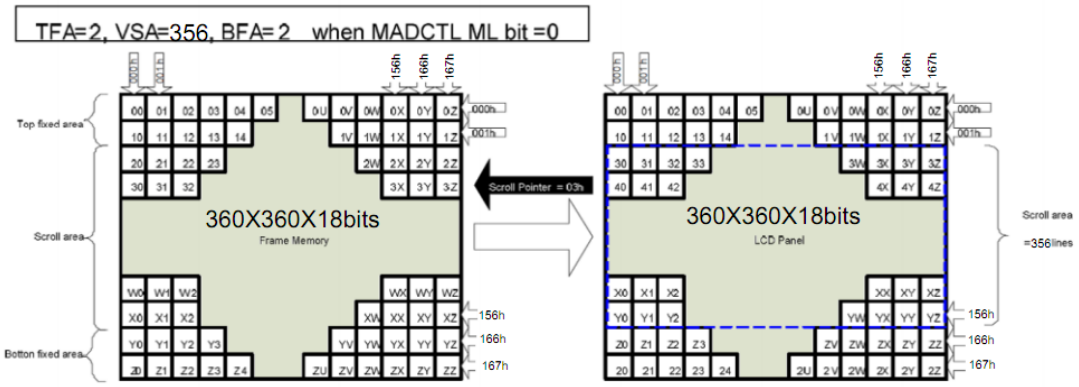
Figure66.

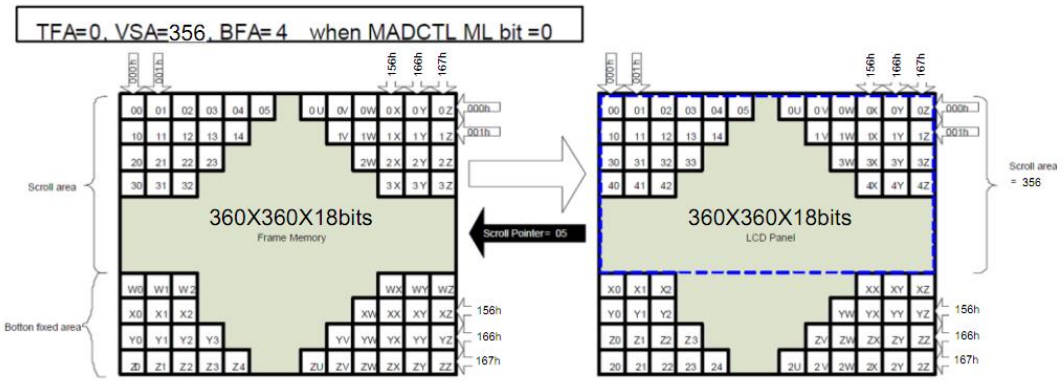


5.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).







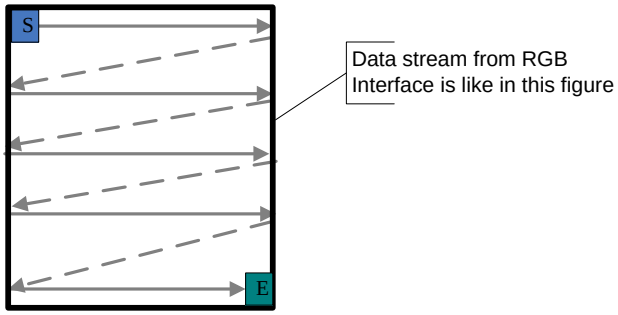
Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠360, Scrolling Mode is undefined.

5.3.3. Updating order on display active area in RGB interface mode

There is defined different kind of updating orders for display in RGB interface mode (**RCM [1:0]** =’1x’).

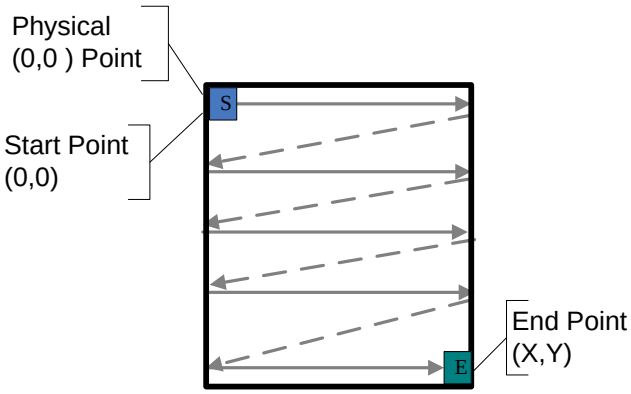
These updating are controlled by **MY** and **MX** bits. Data streaming direction from the host to the display is described in the following figure.

Figure74.



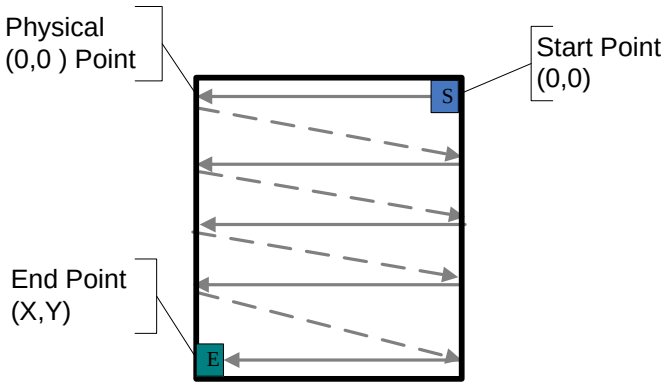
Updating order when MY = ‘0’ and MX = ‘0’

Figure75.



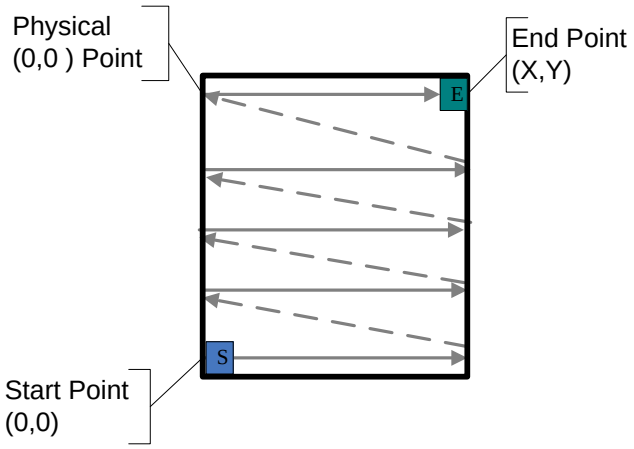
Updating order when MY = ‘0’ and MX = ‘1’

Figure76.



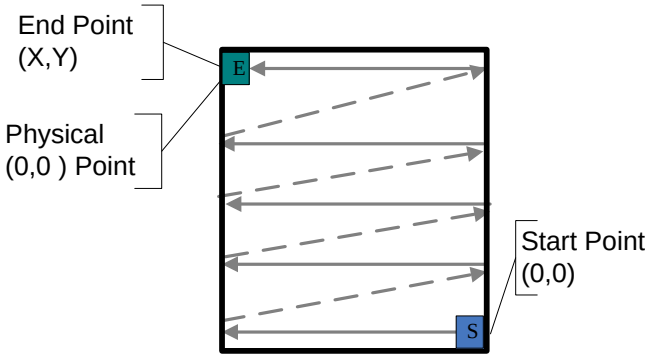
Updating order when MY = ‘1’ and MX = ‘0’

Figure77.



Updating order when MY = '1' and MX = '1'

Figure78.



Rules for updating order on display active area in RGB interface display mode:

Table37.

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to 0 "Start Column"	Return to "Start Page"

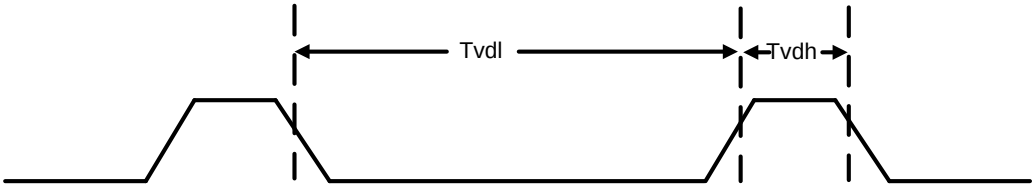
Note: Pixel order is RGB on the display.

5.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

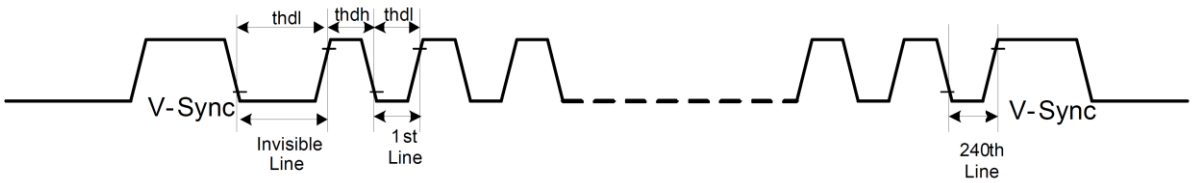
5.4.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:
Figure79.



tVdh= The LCD display is not updated from the Frame Memory
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 360 H-sync pulses per field.
Figure80.

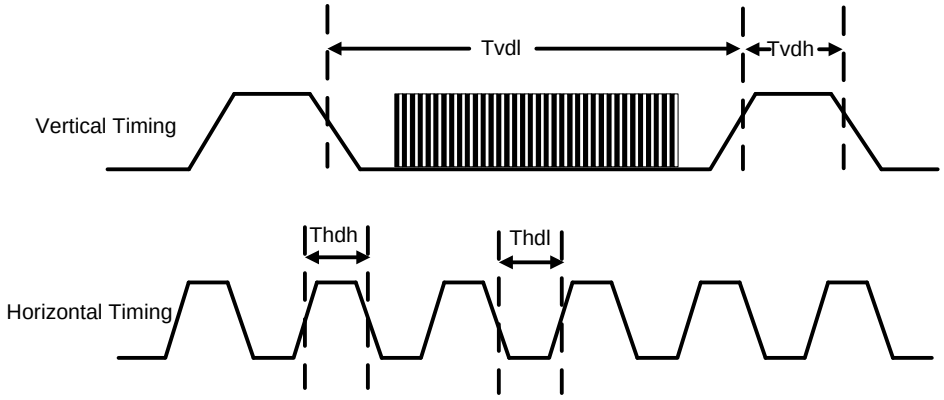


thdh= The LCD display is not updated from the Frame Memory
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

5.4.2. Tearing effect line timing

The Tearing Effect signal is described below.

Figure81.



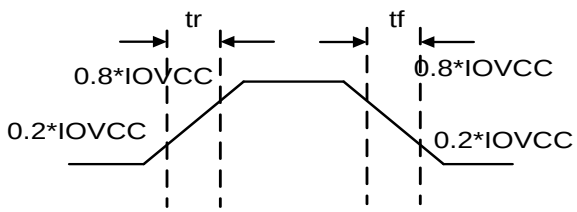
Idle Mode Off (Frame Rate = 20~65 Hz)

Table38.

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 20~65 Hz) ,The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Figure82.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5. Source driver

The GC9C01 contains a 540 channels of source driver (S1~S540) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 540 channels and generates corresponding
gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.6. Gate driver

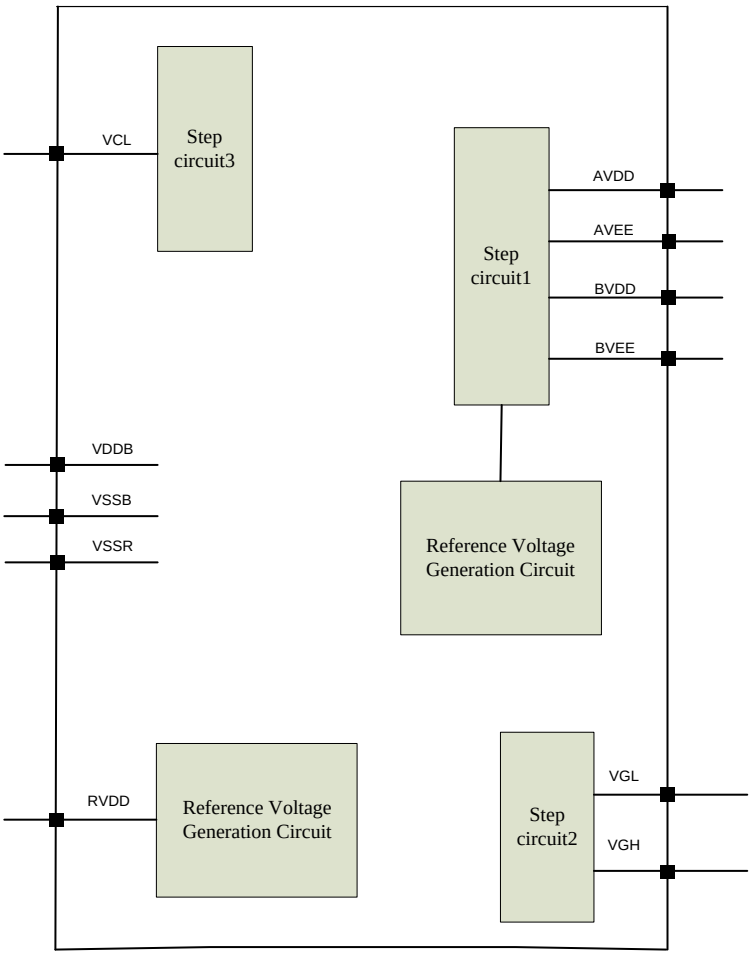
The GC9C01 contains a 32 gate channels of gate driver (G1~G32) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.7. LCD power generation circuit

5.7.1. Power supply circuit

The power circuit of GC9C01 is used to generate supply voltages for LCD panel driving.

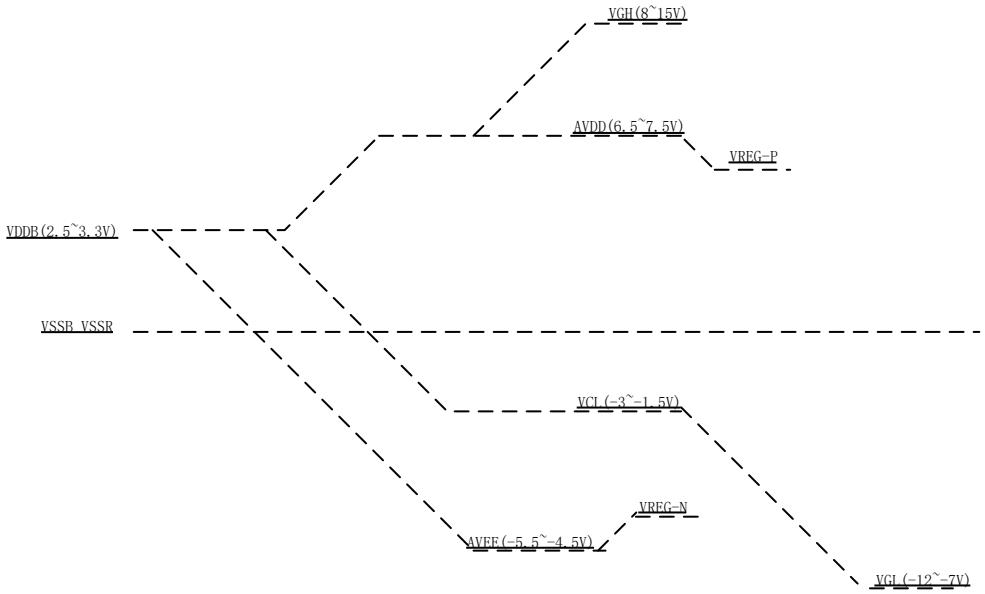
Figure83.



5.7.2. LCD power generation scheme

The boost voltage generated is shown as below.

Figure84.



LCD power generation scheme

5.8. Gamma Correction

GC9C01 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9C01 available with liquid crystal panels of various characteristics.

Figure85.

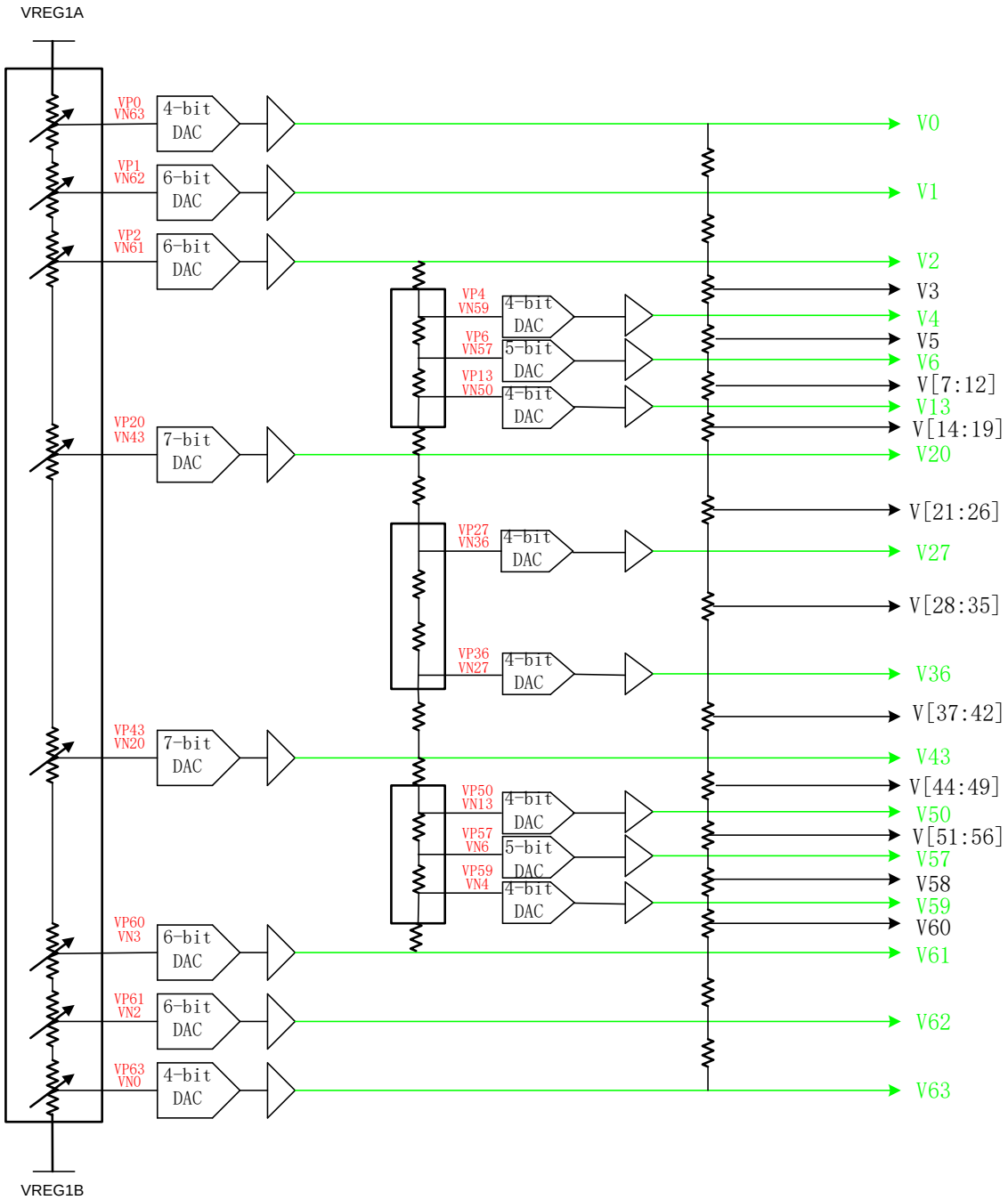
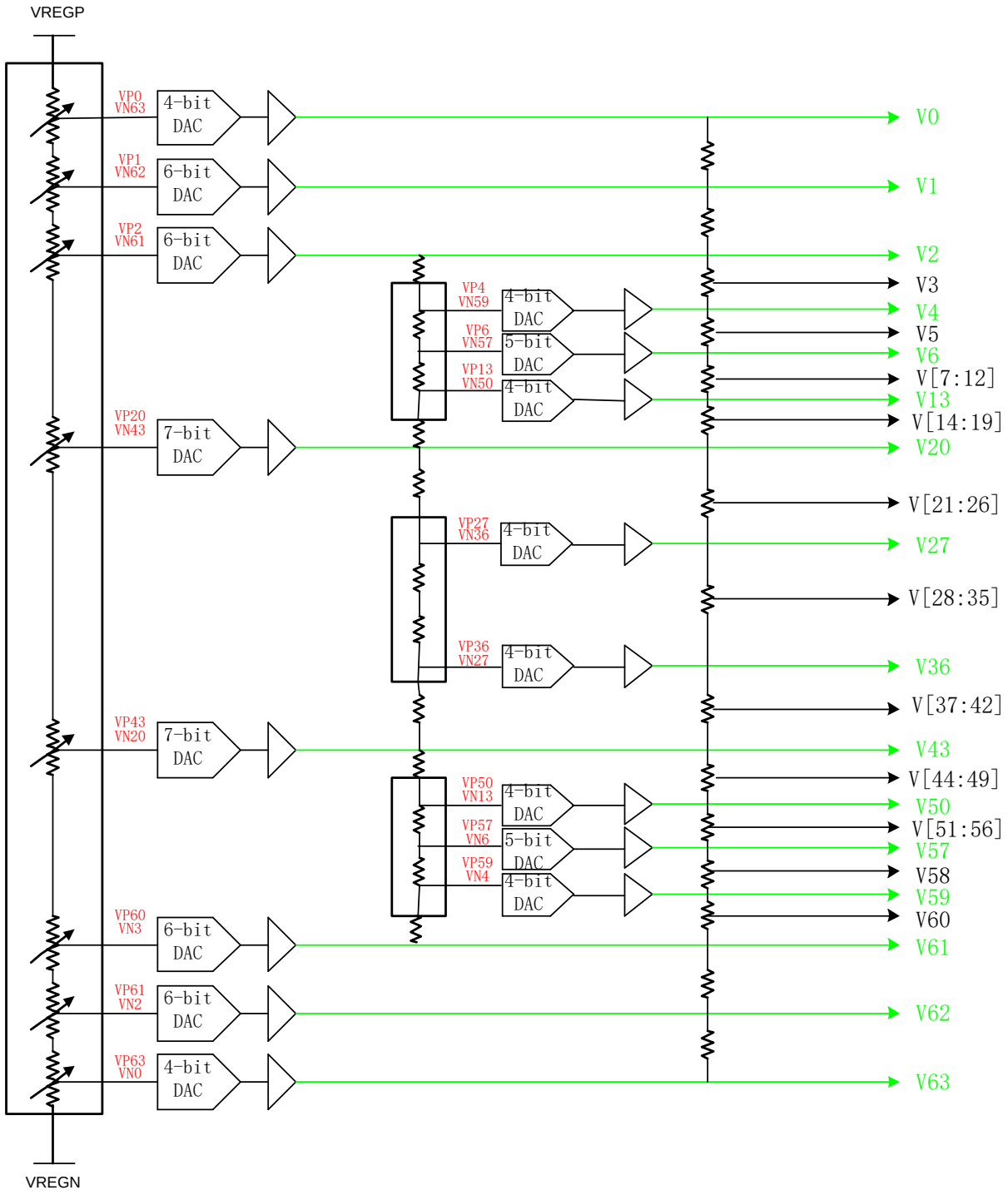
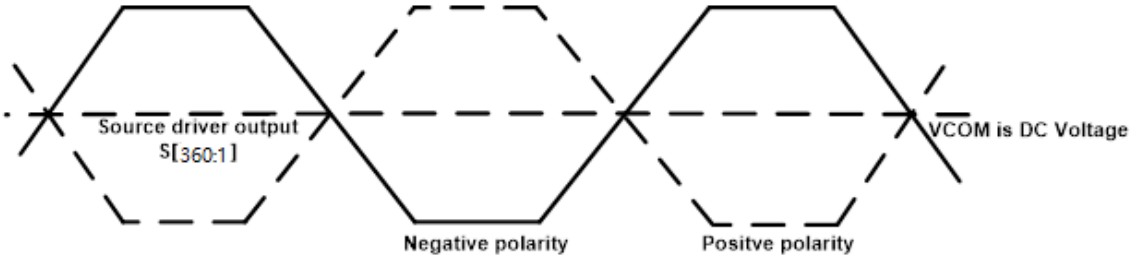


Figure86.



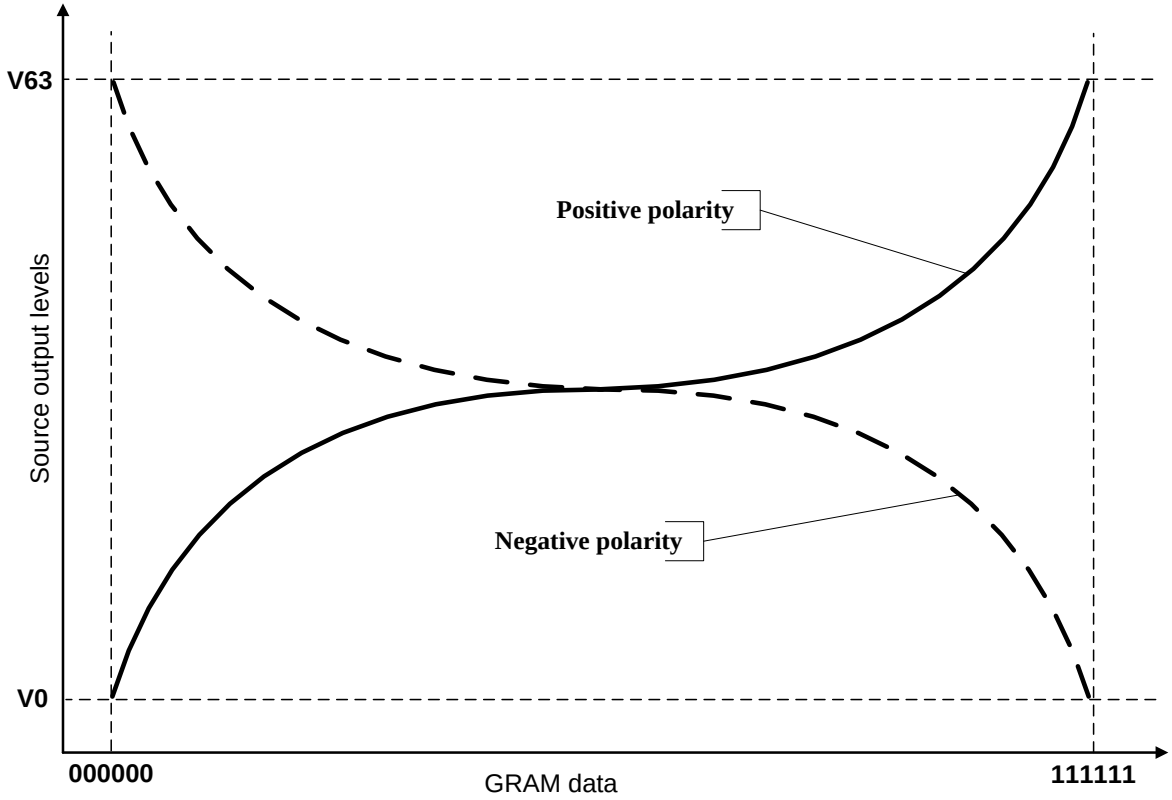
Grayscale Voltage Generation

Figure87.Dot inversion



Relationship between Source Output and VCOM

Figure88.



5.9. Power Level Definition

5.9.1. Power Levels

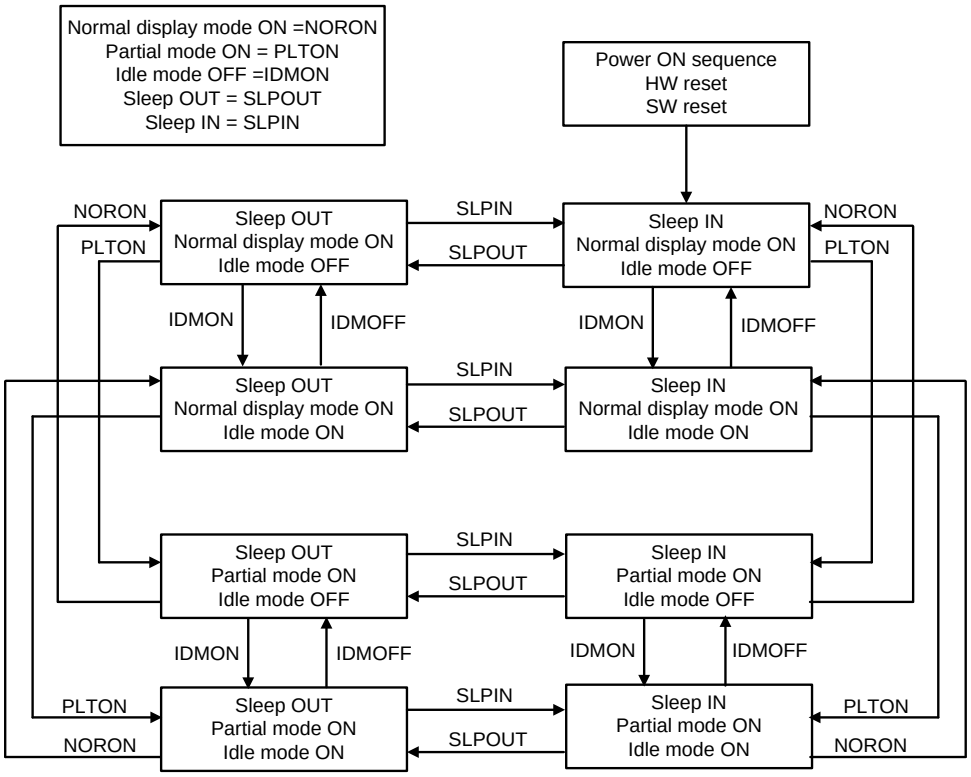
6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VDDB and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

5.9.2. Power Flow Chart

Figure89.



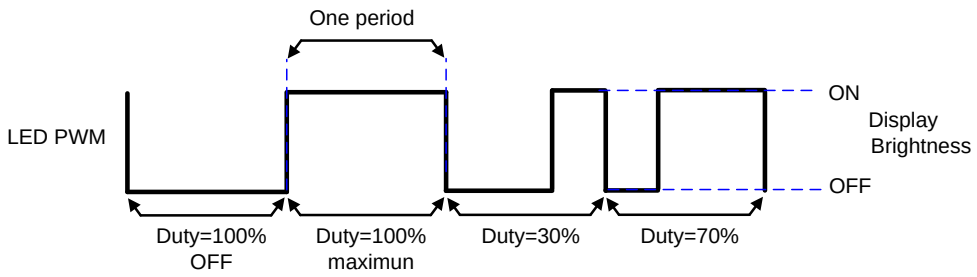
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

5.10.3.Brightness control block

There is an external output signal from brightness block, LEDPWM to control the LED driver IC in order to control display brightness.
There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The LEDPWM duty is calculated as DBV[7:0]/255 x period (affected by OSC frequency).
For example: LEDPWM period = 3ms, and DBV[7:0] = '200DEC'. Then LEDPWM duty = 200 / 255=78.1%.
Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM (high effective) = 2.344ms, and the low-level of LEDPWM = 0.656ms.

Figure90.



LEDPWM output duty

5.10. Input/output pin state

5.10.1. Output pins

Table40.

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDA	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
LEDPWM	Low	Low

Characteristics of output pins

5.10.2. Input pins

Table41.

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
D[17:0]	Input invalid	Input valid	Input valid	Input invalid
IM[4:0]	Input invalid	Input valid	Input valid	Input invalid

Characteristics of input pins

6. Command

6.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Identification Information 2	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID_1[7:0]								00
	1	↑	1	XX	ID_2[7:0]								9C
	1	↑	1	XX	ID_3[7:0]								01
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[31:25]							X	00
	1	↑	1	XX	X	D[22:20]			D[19:16]				61
	1	↑	1	XX	X	X	X	X	X	D[10:8]			00
	1	↑	1	XX	D[7:5]			X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC[15:8]								00
	1	1	↑	XX	SC[7:0]								00
	1	1	↑	XX	EC[15:8]								01
	1	1	↑	XX	EC[7:0]								67h
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP[15:8]								00
	1	1	↑	XX	SP[7:0]								00
	1	1	↑	XX	EP[15:8]								01h

	1	1	↑	XX	EP[7:0]								67h
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D[17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								01
	1	1	↑	XX	ER[7:0]								67
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	VSA[15:8]								01
	1	1	↑	XX	VSA[7:0]								67
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI[2:0]			X	DBI[2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D[17:0]									XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS[8]	00
	1	1	↑	XX	STS[7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	X	GTS [8]	00
	1	↑	1	XX	GTS[7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	↑	1	XX	DBV[7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh

	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								00
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								9C
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								01

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	0	RCM[1:0]		X	VSPL	HSPL	DPL	EPL	01
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	0	0	0	VFP[3:0]				08
	1	1	↑	XX	0	VBP[6:0]							02
	1	1	↑	XX	0	0	0	HBP[4:0]					14
Display Function Control	0	1	1	XX	1	0	1	1	0	1	1	0	B6
	1	1	1	XX	X	X	X	X	X	X	X	X	00
	1	1	1	XX	X	GS	SS	X	X	X	X	Win-con	00
TE Control	0	1	↑	XX	1	0	1	1	1	0	1	0	B4h
	1	1	↑	XX	te_width[7:0]								00
	1	1	↑	XX	X	X	X	X	X	X	X	te_pol	00
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
	1	1	↑	XX	epf[1:0]		Mdt[1:0]		DM[1:0]		RM	RIM	C0

Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Power Criterion Control	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	0	0	0	0	0	0	vcire	0	00
Vreg1a voltage Control	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XX	0	vreg1_vbp_d[6:0]							3C
Vreg1b voltage Control	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XX	0	vreg1_vbn_d[6:0]							3C
Vreg2a voltage Control	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h
	1	1	↑	XX	0	0	vrh[5:0]						28
Inversion	0	1	↑	XX	1	1	1	0	1	1	0	0	ECh
	1	1	↑	XX	0	DINV[2:0]			0	0	0	0	77
	1	1	↑	XX	RTN2[7:0]								40
SPI 2data	0	1	↑	XX	1	1	1	0	1	0	0	1	B1h

control	1	1	↑	XX				DTR _EN	2data_ en	2data_mdt			00
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
SET_GAMMA1	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
	1	1	↑	XX	dig2gam_ dig2j0_n[1:0]	dig2gam_vr1_n[5:0]							80
	1	1	↑	XX	dig2gam_ dig2j1_n[1:0]	dig2gam_vr2_n[5:0]							03
	1	1	↑	XX	0	0	0	dig2gam_vr4_n[4:0]					08
	1	1	↑	XX	0	0	0	dig2gam_vr6_n[4:0]					06
	1	1	↑	XX	dig2gam_vr0_n[3:0]				dig2gam_vr13_n[3:0]				05
	1	1	↑	XX	0	dig2gam_vr20_n[6:0]							2B
SET_GAMMA2	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
	1	1	↑	XX	0	dig2gam_vr43_n[6:0]							41
	1	1	↑	XX	dig2gam_vr27_ n[2:0]	dig2gam_vr57_n[4:0]							97
	1	1	↑	XX	dig2gam_vr36_ n[2:0]	dig2gam_vr59_n[4:0]							98
	1	1	↑	XX	0	0	dig2gam_vr61_n[5:0]						13
	1	1	↑	XX	0	0	dig2gam_vr62_n[5:0]						17
	1	1	↑	XX	dig2gam_vr50_n[3:0]				dig2gam_vr63_n[3:0]				CD
SET_GAMMA3	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
	1	1	↑	XX	dig2gam_ dig2j0_p[1:0]	dig2gam_vr1_p[5:0]							40
	1	1	↑	XX	dig2gam_ dig2j1_p[1:0]	dig2gam_vr2_p[5:0]							03
	1	1	↑	XX	0	0	0	dig2gam_vr4_p[4:0]					08
	1	1	↑	XX	0	0	0	dig2gam_vr6_p[4:0]					0B
	1	1	↑	XX	dig2gam_vr0_p[3:0]				dig2gam_vr13_p[3:0]				08
	1	1	↑	XX	0	dig2gam_vr20_p[6:0]							2E
SET_GAMMA4	0	1	↑	XX	1	1	1	1	0	0	1	1	F3h
	1	1	↑	XX	0	dig2gam_vr43_p[6:0]							3F
	1	1	↑	XX	dig2gam_vr27_ p[2:0]	dig2gam_vr57_p[4:0]							98

	1	1	↑	XX	dig2gam_vr36_p[2:0]		dig2gam_vr59_p[4:0]		B4
	1	1	↑	XX	0	0	dig2gam_vr61_p[5:0]		14
	1	1	↑	XX	0	0	dig2gam_vr62_p[5:0]		18
	1	1	↑	XX	dig2gam_vr50_p[3:0]			dig2gam_vr63_p[3:0]	CD

6.2. Description of Level 1 Command

6.2.1. Read display identification information (04h)

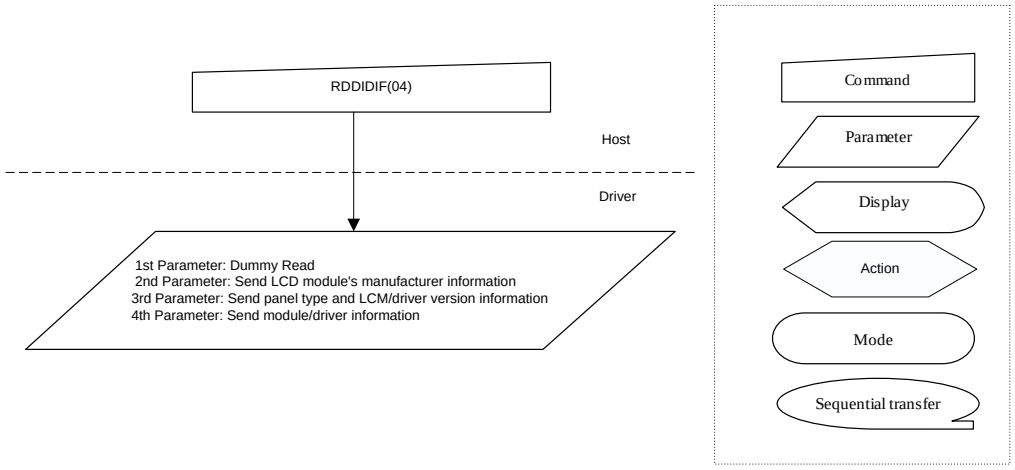
04h	Read display identification information 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID_1[7:0]								00
3rd Parameter	1	↑	1	XX	ID_2[7:0]								9C
4th Parameter	1	↑	1	XX	ID_3[7:0]								01
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID2_1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID2_2 [7:0]): LCD module/driver version ID. The 4th parameter (ID2_3 [7:0]): LCD module/driver ID.												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h009C01
SW Reset	24'h009C01
HW Reset	24'h009C01

Flow Chart


RDDIDIF(04)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send LCD module's manufacturer information
3rd Parameter: Send panel type and LCM/driver version information
4th Parameter: Send module/driver information
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.2. Read Display Status (09h)

09h	Read Display Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D[31:25]							X	00
3rd Parameter	1	↑	1	XX	0	D[22:20]			D[19:16]				61
4th Parameter	1	↑	1	XX	0	0	0	0	0	D[10:8]			00
5th Parameter	1	↑	1	XX	D[7:5]			0	0	0	0	0	00

Description

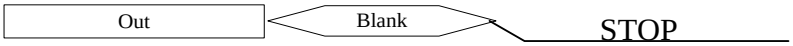
This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	O	Booster OFF
		1	Booster ON
D30	Row address order	O	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	O	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	O	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	O	LCD Refresh Top to BoUom (When MADCTL B4='0')
		1	LCD Refresh BoUom to Top (When MADCTL B4='1').
D26	RGB/BGR order	O	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	O	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	O	-
D23	Not used	O	-
D22	Interface color pixel format definition	101	16-bit/pixel
D21			
D20		110	18-bit/pixel

		D19	Idle mode ON/OFF	O	Idle Mode OFF
				1	Idle Mode ON
		D18	Partial mode ON/OFF	O	Partial Mode OFF
				1	Partial Mode ON
		D17	Sleep IN/OUT	O	Sleep IN Mode
				1	Sleep OUT Mode
		D16	Display normal mode ON/OFF	O	Display Normal Mode OFF.
				1	Display Normal Mode ON.
		D15	Vertical scrolling status	O	Scroll OFF
		D14	Not used	O	-
		D13	Inversion status	O	Not defined
		D12	All pixel ON	O	Not defined
		D11	All pixel OFF	O	Not defined
		D10	Display ON/OFF	O	
				1	Display is ON
		D9	Tearing effect line ON/OFF	O	Tearing Effect Line OFF
				1	Tearing Effect ON
		D5	Tearing effect line mode	0	Mode 1, V-Blanking only
				1	Mode 2, both H-Blanking and V-Blanking
		D4	Not used	O	-
		D3	Not used	O	-
		D2	Not used	O	-
		D1	Not used	O	-
		D0	Not used	O	-
Restriction					
Register Availability					

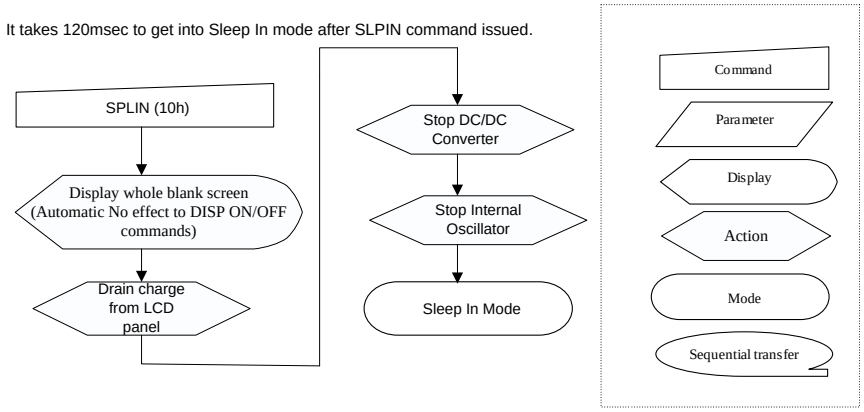
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

6.2.3. Enter Sleep Mode (10h)

10h	Enter Sleep Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped  MCU interface and memory are still working and the memory keeps its contents. X = Don't care												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart	

It takes 120msec to get into Sleep In mode after SLPIN command issued.
SPLIN (10h)
Display whole blank screen (Automatic No effect to DISP ON/OFF commands)
Drain charge from LCD panel
Stop DC/DC Converter
Stop Internal Oscillator
Sleep In Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

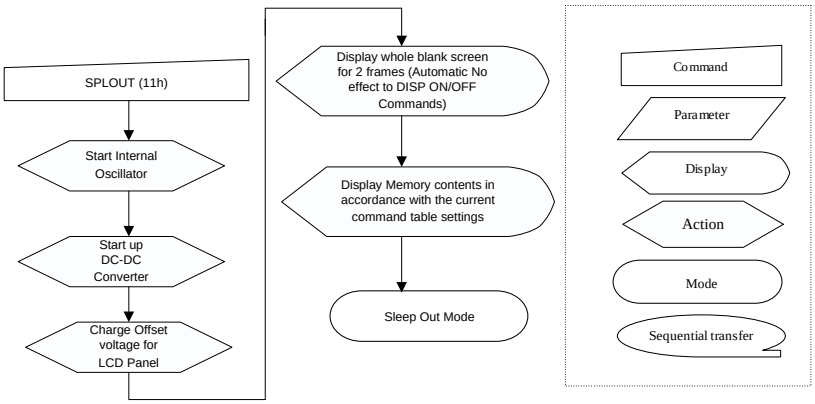
6.2.4. Sleep Out Mode (11h)

11h	Sleep Out Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Parameter	No Parameter												
Description	This command turns off sleep mode. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started. X = Don't care												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart	

SPLOUT (11h)
Start Internal Oscillator
Start up DC-DC Converter
Charge Offset voltage for LCD Panel
Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)
Display Memory contents in accordance with the current command table settings
Sleep Out Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.5. Partial Mode ON (12h)

12h	Partial Mode ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Parameter	No Parameter												
Description	This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written. X = Don't care												
Restriction	This command has no effect when Partial mode is active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode ON
SW Reset	Normal Display Mode
HW Reset	Normal Display Mode ON

Flow Chart	See Partial Area (30h)

6.2.6. Normal Display Mode ON (13h)

13h	Normal Display Mode ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Parameter	No Parameter												
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) X = Don't care												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	
Status	Default Value
Power On Sequence	Normal Display Mode ON
SW Reset	Normal Display Mode
HW Reset	Normal Display Mode ON

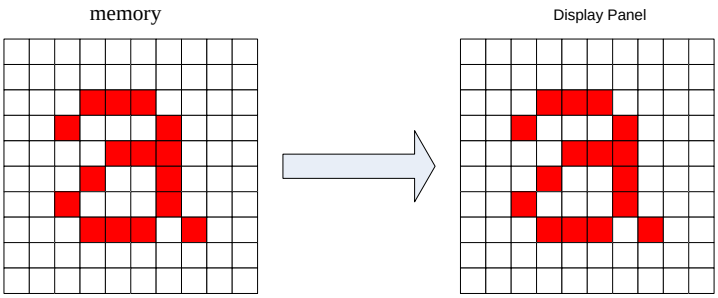
Flow Chart	See Partial Area (30h)

6.2.7. Display Inversion OFF (20h)

20h	Display Inversion OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												

Description

This command is used to recover from display inversion mode.
This command makes no change of the content of frame memory.
This command doesn't change any other status.



X = Don't care

Restriction

This command has no effect when module already is inversion OFF mode.

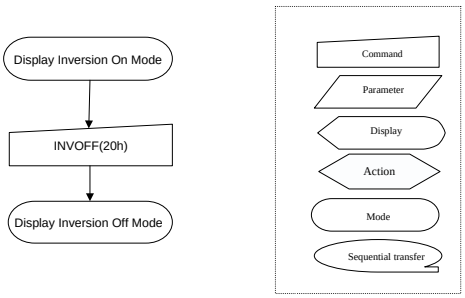
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart

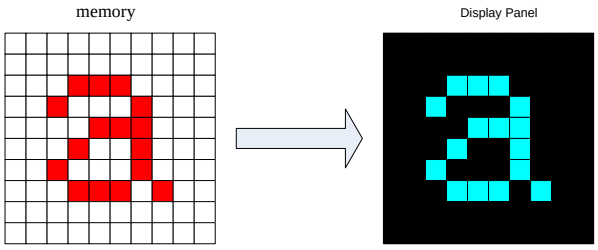


6.2.8. Display Inversion ON (21h)

21h	Display Inversion ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter												

Description

This command is used to enter into display inversion mode.
This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.
This command doesn't change any other status.
To exit Display inversion mode, the Display inversion OFF command (20h) should be written..



X = Don't care

Restriction

This command has no effect when module already is inversion ON mode.

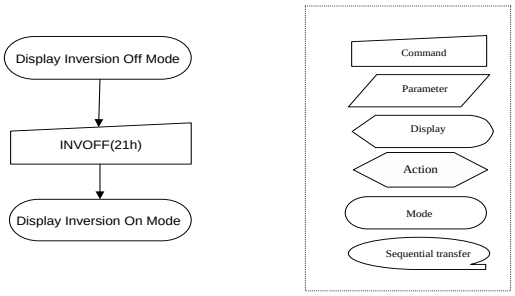
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

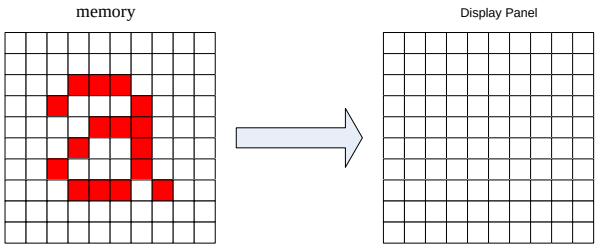
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



6.2.9. Display OFF (28h)

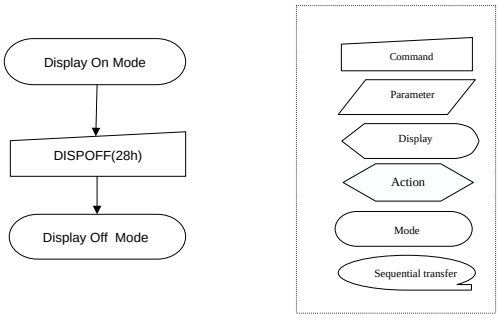
28h	Display OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.  X = Don't care												
Restriction	This command has no effect when module is already in display off mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

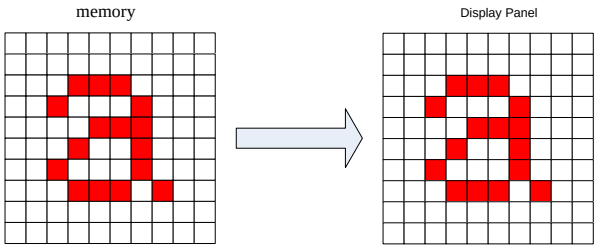
Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



6.2.10. Display ON (29h)

29h	Display ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status.  X = Don't care												
Restriction	This command has no effect when module is already in display on mode.												

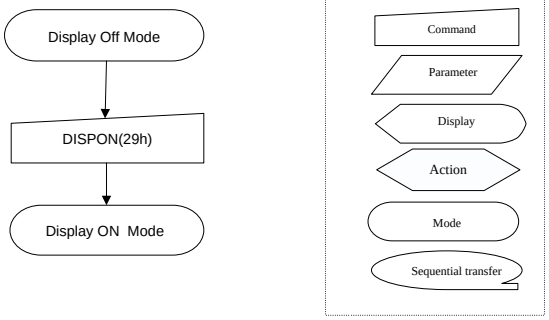
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

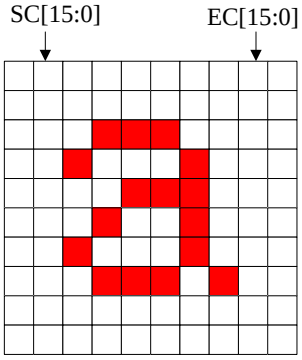


6.2.11. Column Address Set (2Ah)

2Ah	Column Address Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2nd Parameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1
4th Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value
represents one column line in the Frame Memory..



X = Don't care

Restriction

SC [15:0] always must be equal to or less than EC [15:0].
Note 1: When SC [15:0] or EC [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 0167h (When MADCTL's B5 = 1), data of out of range will be ignored

Register Availability

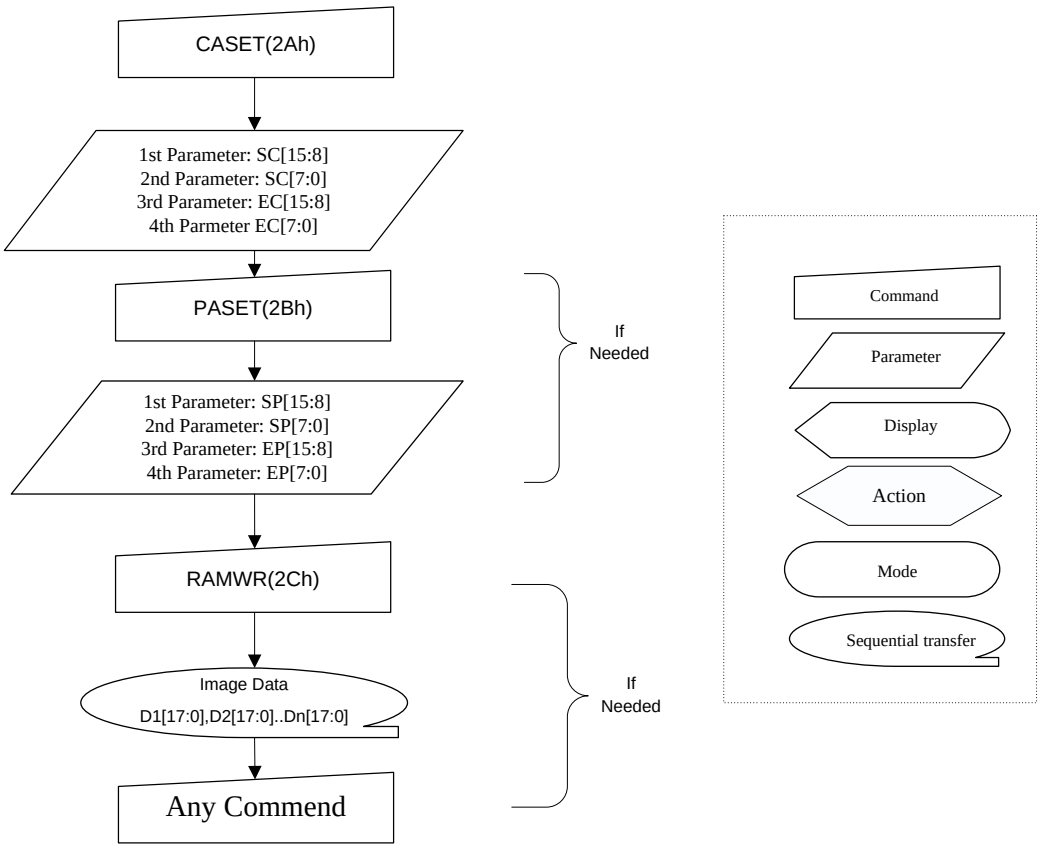
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC [15:0]=0000h	EC [15:0]=0167h

	SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=0167h
			If MADCTL's B5 = 1: EC [15:0]=0167h
	HW Reset	SC [15:0]=0000h	EC [15:0]=0167h

Flow Chart

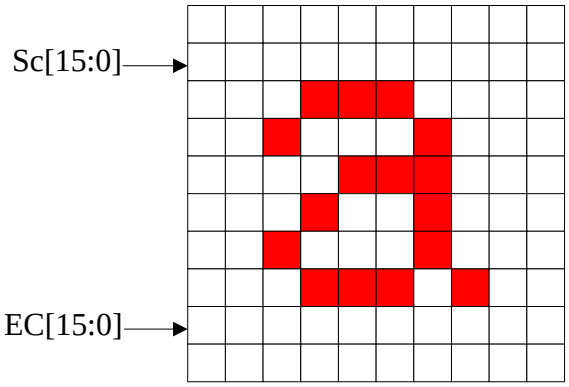


6.2.12. Row Address Set (2Bh)

2Bh	Row Address Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1
2nd Parameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd Parameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1
4th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the
other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value
represents one Page line in the Frame Memory.



X = Don't care

Restriction

SP [15:0] always must be equal to or less than EP [15:0]
Note 1: When SP [15:0] or EP [15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored.

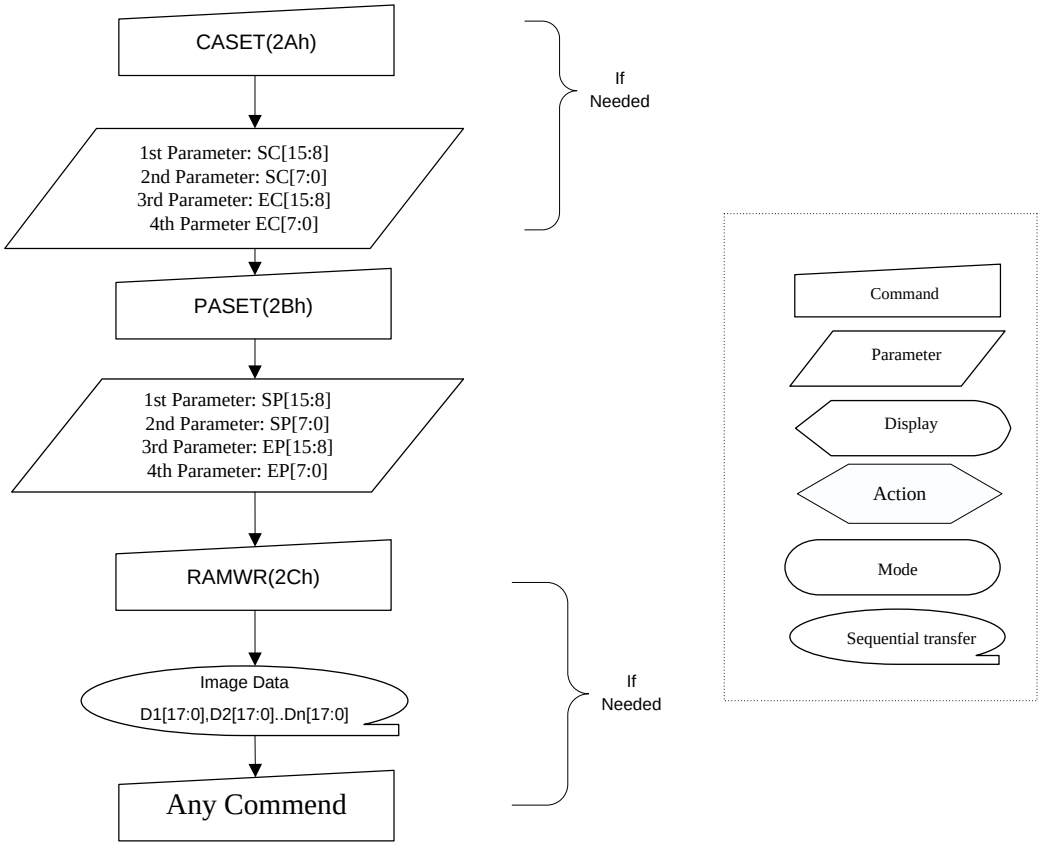
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP [15:0]=0000h	EP [15:0]=00EFh
SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=0167h
		If MADCTL's B5 = 1: EP [15:0]=0167h
HW Reset	SP [15:0]=0000h	EP [15:0]=0167h

Flow Chart



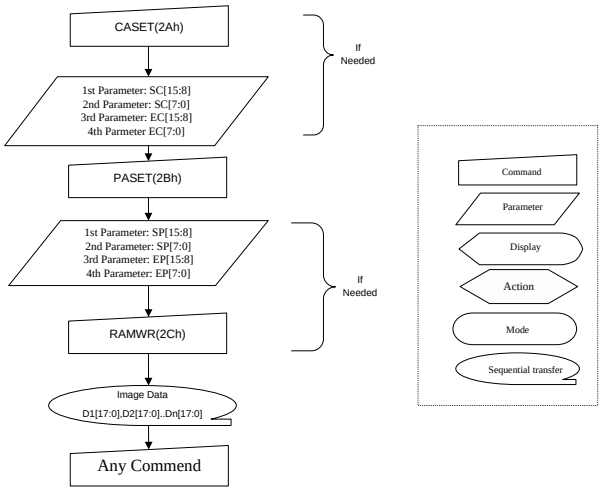
6.2.13. Memory Write (2Ch)

2Ch	Memory Write												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
Nth Parameter	1	1	↑	Dn [17:0]									XX
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.												
Restriction	In all color modes, there is no restriction on length of parameters.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	 CASET(2Ah) 1st Parameter: SC[15:8] 2nd Parameter: SC[7:0] 3rd Parameter: EC[15:8] 4th Parmeter EC[7:0] If Needed PASET(2Bh) 1st Parameter: SP[15:8] 2nd Parameter: SP[7:0] 3rd Parameter: EP[15:8] 4th Parameter: EP[7:0] If Needed RAMWR(2Ch) Image Data D1[17:0],D2[17:0]..Dn[17:0] Any Commend Command Parameter Display Action Mode Sequential transfer

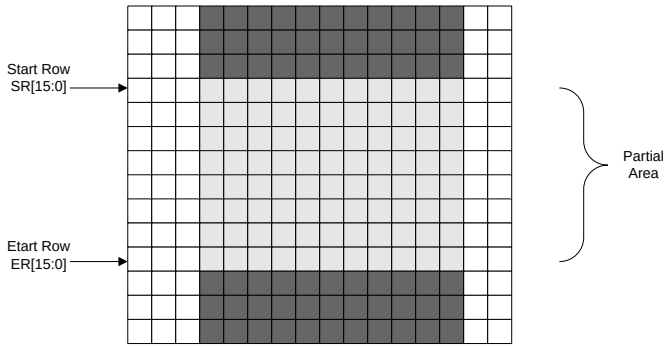
6.2.14. Partial Area (30h)

30h	Partial Area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	67

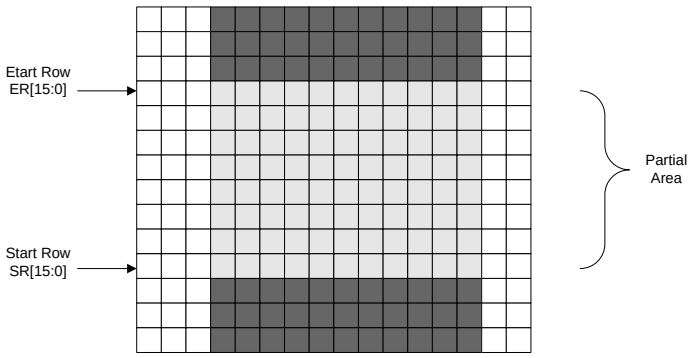
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

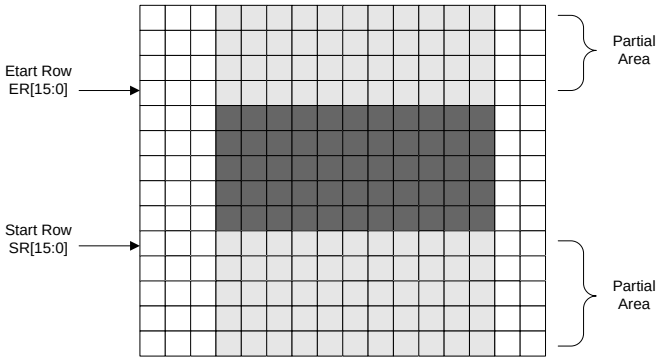
If End Row>Start Row when MADCTL B4=0:-



If End Row>Start Row when MADCTL B4=1:-



If End Row<Start Row when MADCTL B4=0:-



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 0167h.

Register Availability

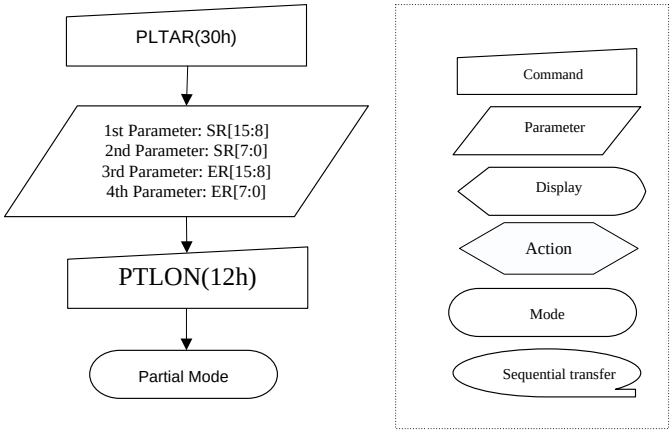
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

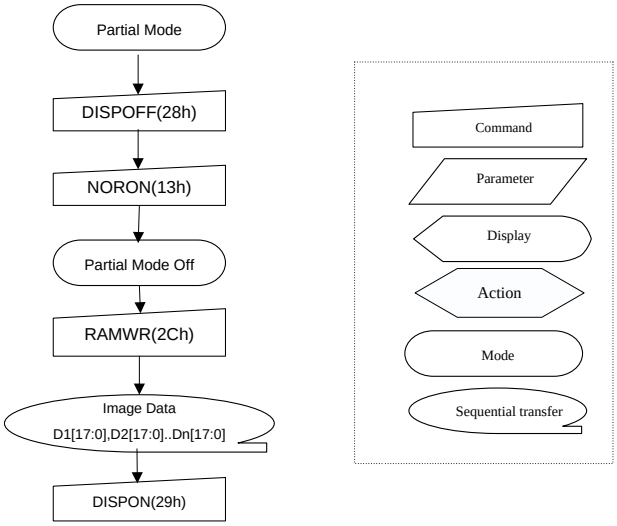
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h0167h
SW Reset	16'h0000h	16'h0167 h
HW Reset	16'h0000h	16'h0167 h

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



6.2.15. Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition												
	D/C X	RDX	WR X	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								01
4th Parameter	1	1	↑	XX	VSA [7:0]								67

Description

This command defines the Vertical Scrolling Area of the display.

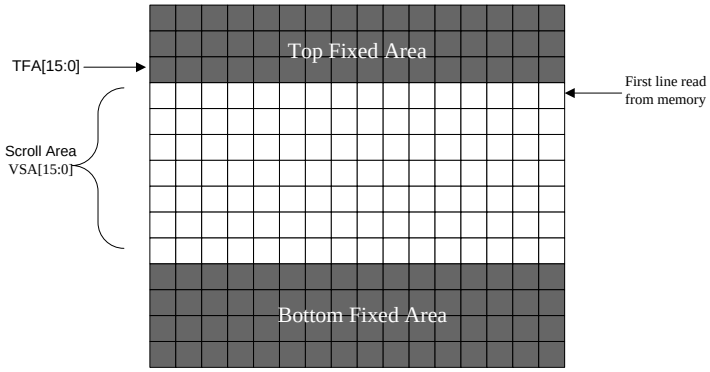
When MADCTL B4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame

Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears

immediately after the bottom most line of the Top Fixed Area.



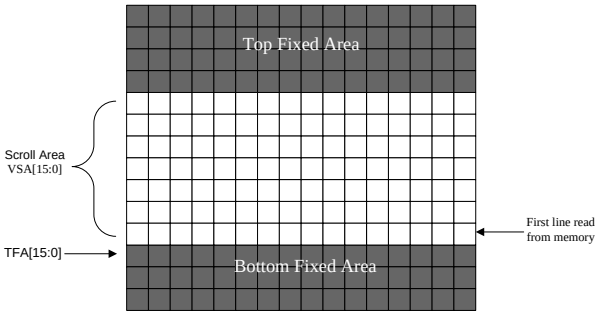
When MADCTL B4=1

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame

Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears

immediately after the top most line of the Top Fixed Area.



X = Don’t care.

Restriction

Register Availability

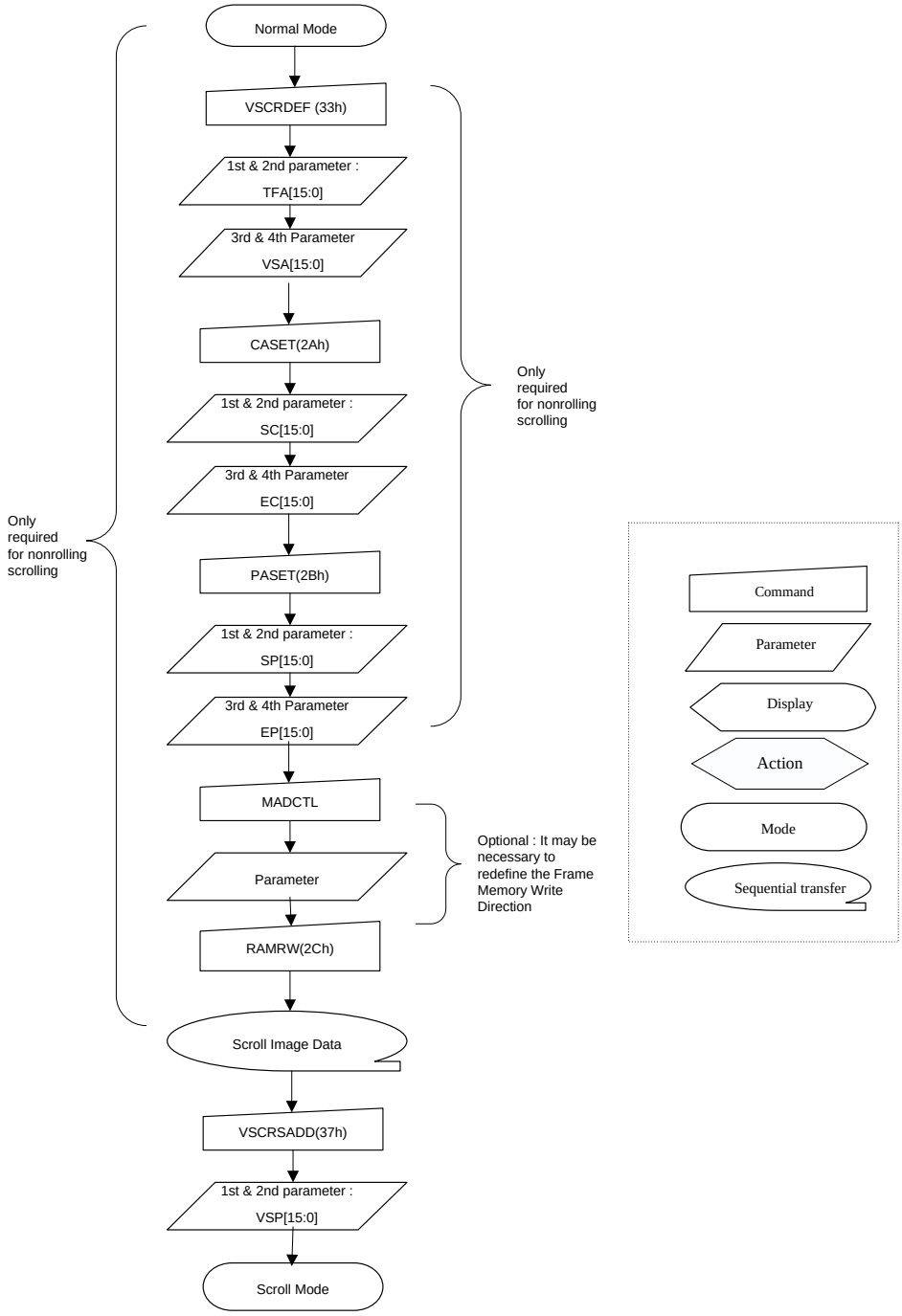
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	16’h0000h	16’h0167h
SW Reset	16’h0000h	16’h0167h
HW Reset	16’h0000h	16’h0167h

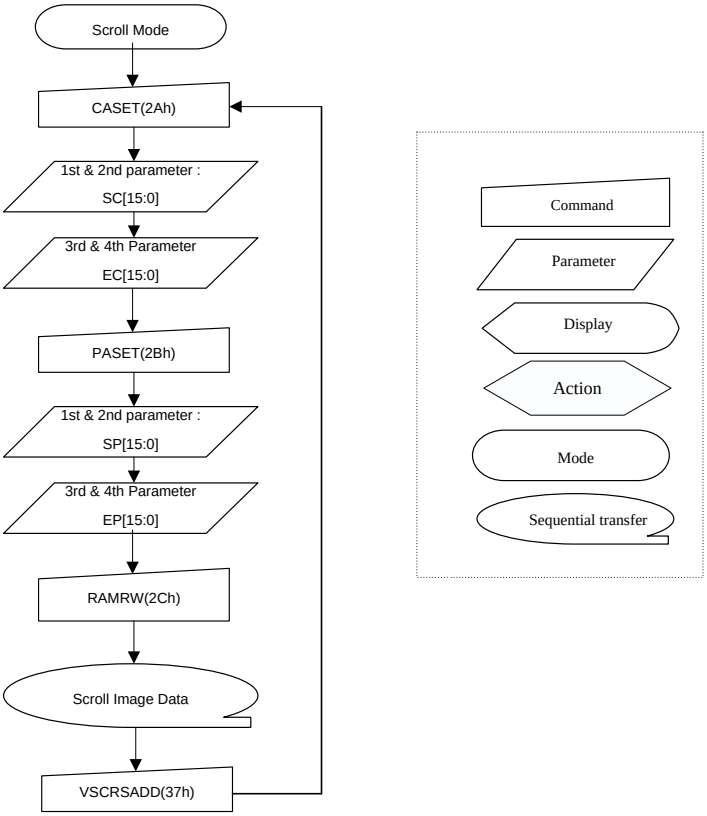
Flow Chart

1. To enter Vertical Scroll Mode :

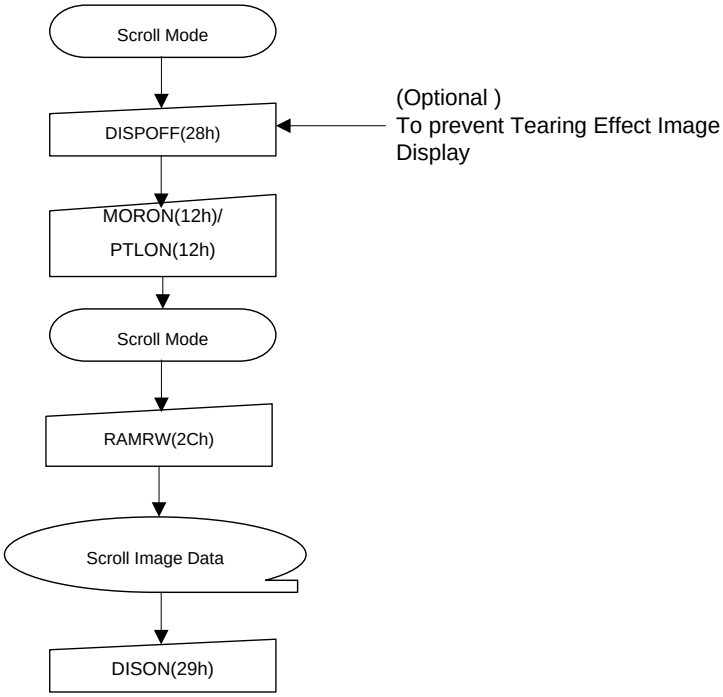


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :



3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

6.2.16. Tearing Effect Line OFF (34h)

34h	Tearing Effect Line OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Parameter	No Parameter												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. X = Don't care.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												

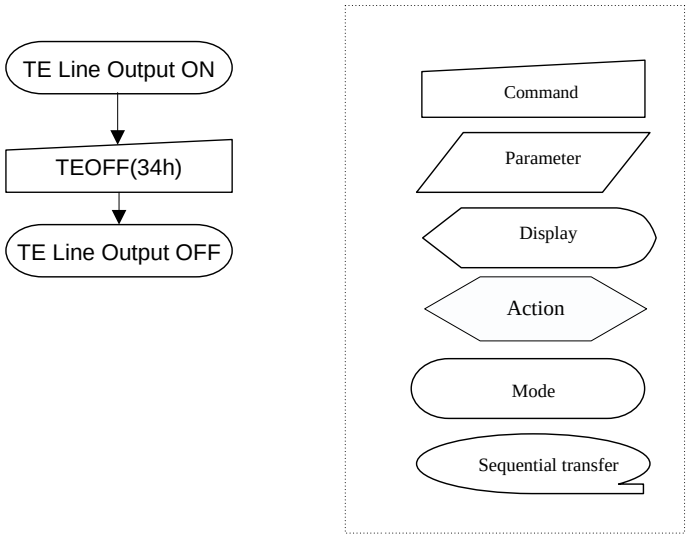
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



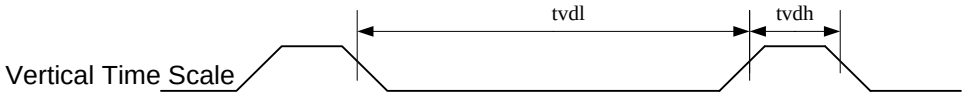
6.2.17. Tearing Effect Line ON (35h)

35h	Tearing Effect Line ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	M	00

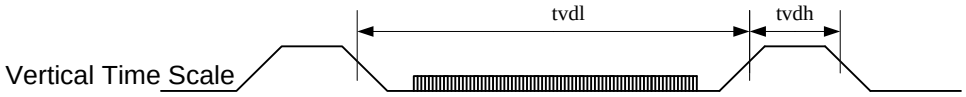
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by
changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**:
The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don't care.

Restriction

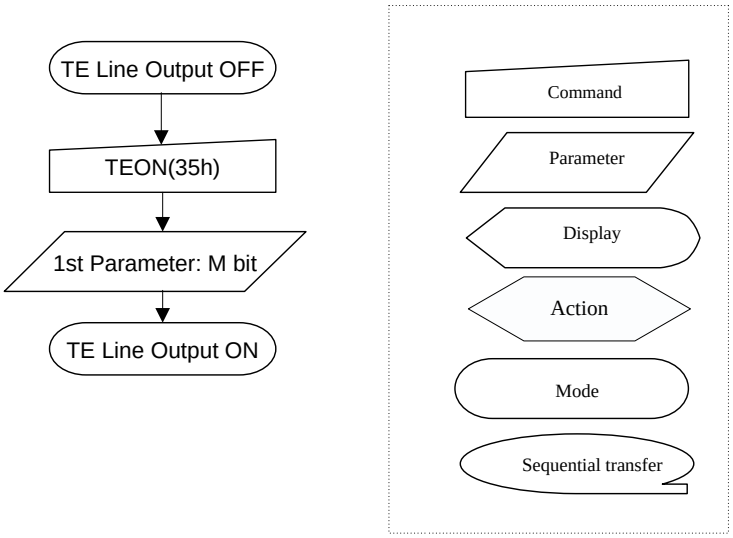
This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart	

TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.18. Memory Access Control(36h)

36h	Tearing Effect Line ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00

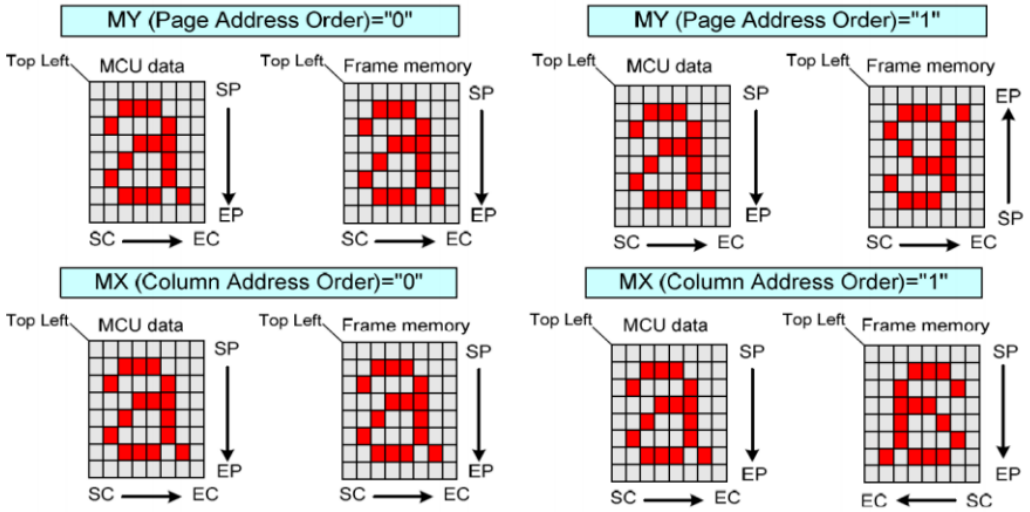
Description

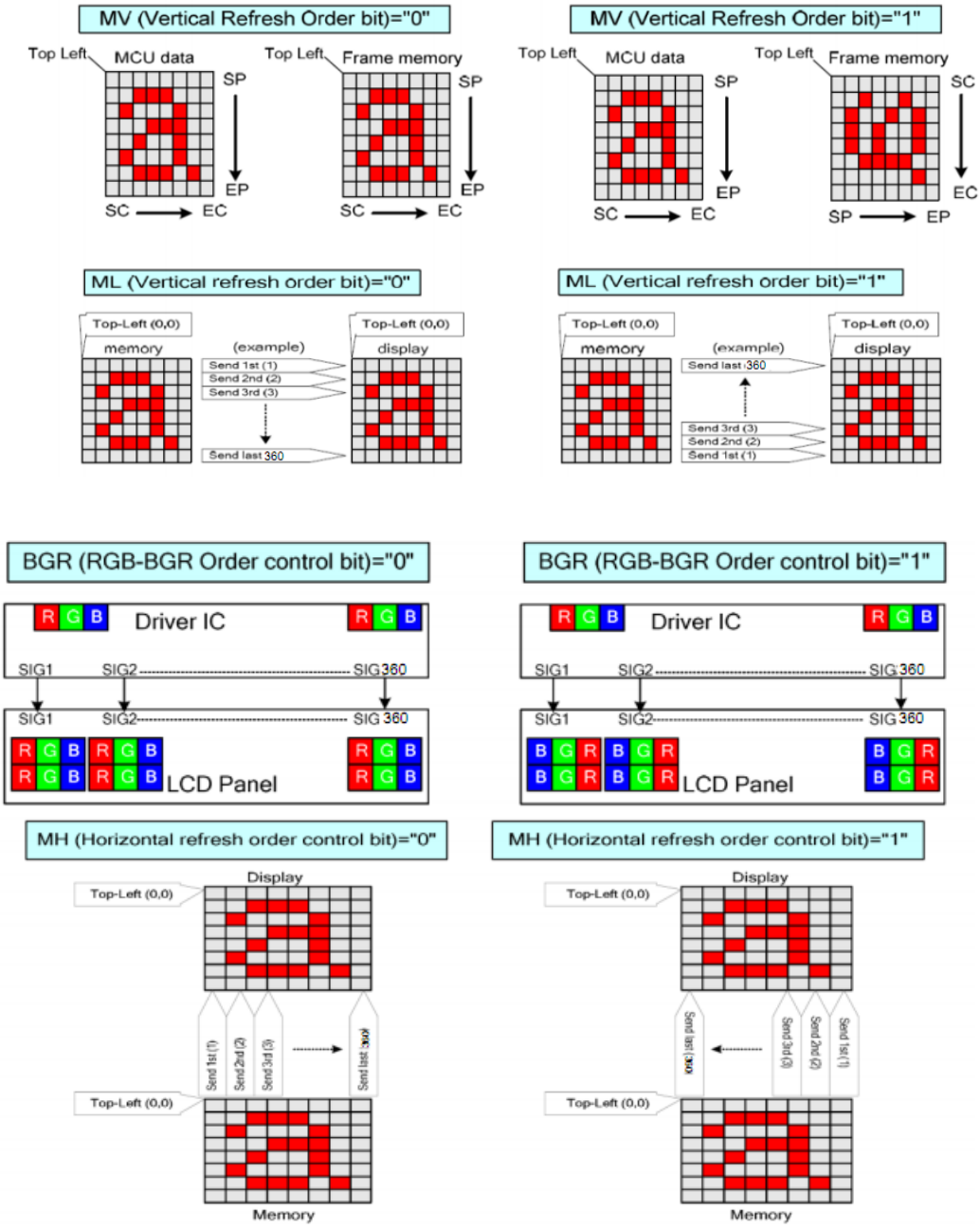
This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

Bit	Name	Description
MY	Row Address Order	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.





Note: Top-Left (0,0) means a physical memory location.

Restriction

This command has no effect when Tearing Effect output is already ON

Register Availability

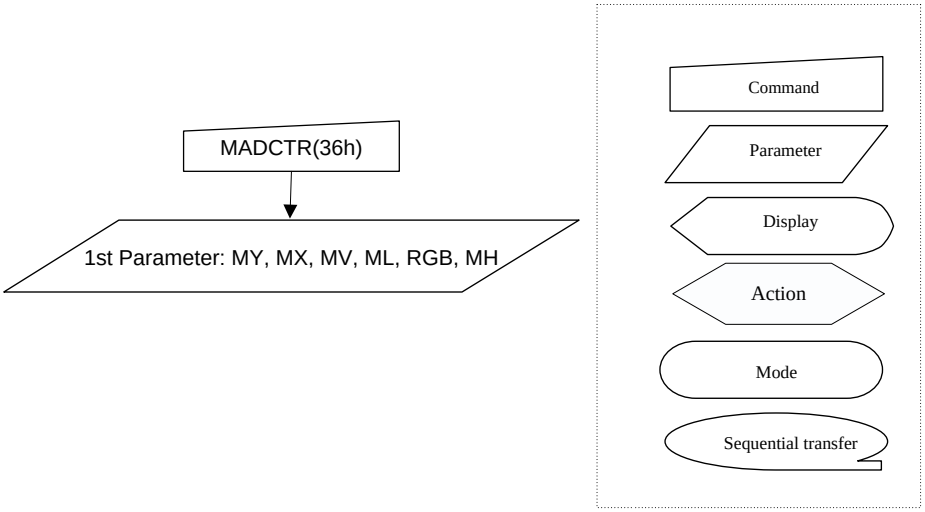
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value

Power On Sequence	8’h00h
SW Reset	No change
HW Reset	8’h00h

Flow Chart



6.2.19. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	1	↑	XX	VSP [15:8]								00
2nd Parameter	1	1	↑	XX	VSP [7:0]								00

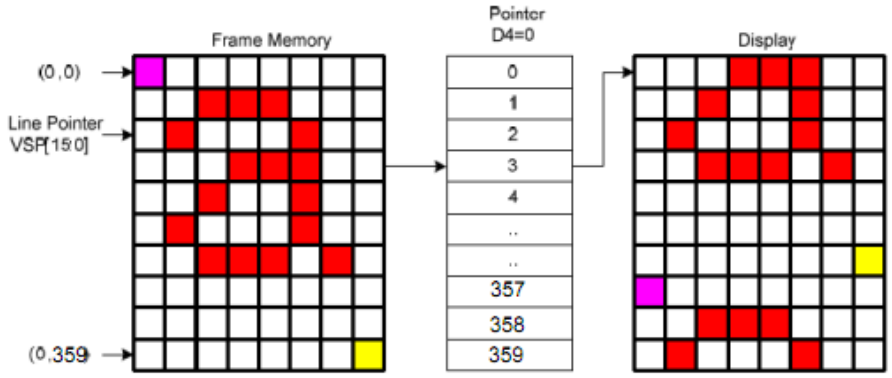
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area
and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

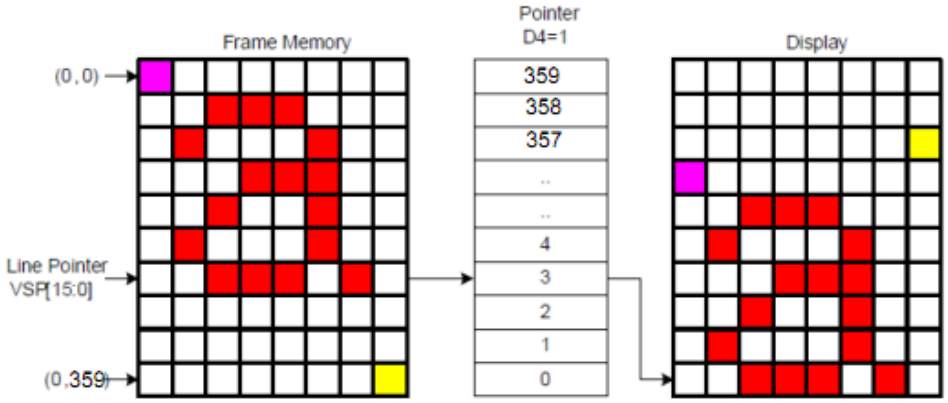
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 360 and VSP=’3’.



When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 360 and VSP=’3’.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line

	Pointer. *(2) This command is ignored when the GC9C01 enters Partial mode.* X = Don’t care
Restriction	This command has no effect when Tearing Effect output is already ON

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.2.20. Idle Mode OFF (38h)

38h	Idle Mode OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Parameter	No Parameter												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors. X = Don't care.												
Restriction	This command has no effect when module is already in idle off mode.												

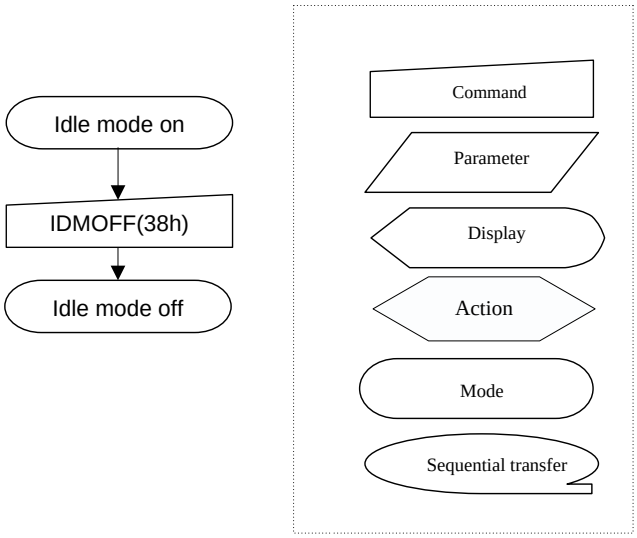
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart



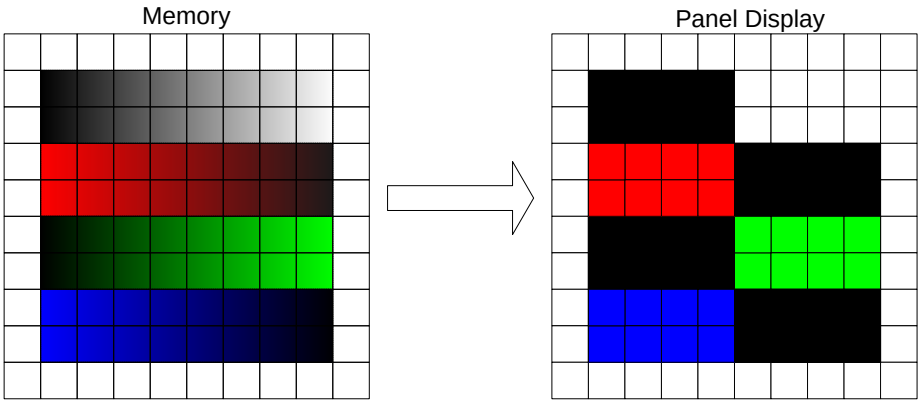
6.2.21. Idle Mode ON (39h)

39h	Idle Mode ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter												

Description

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



	Memory Contents vs. Display Color		
	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X = Don’t care.

Restriction

This command has no effect when module is already in idle off mode.

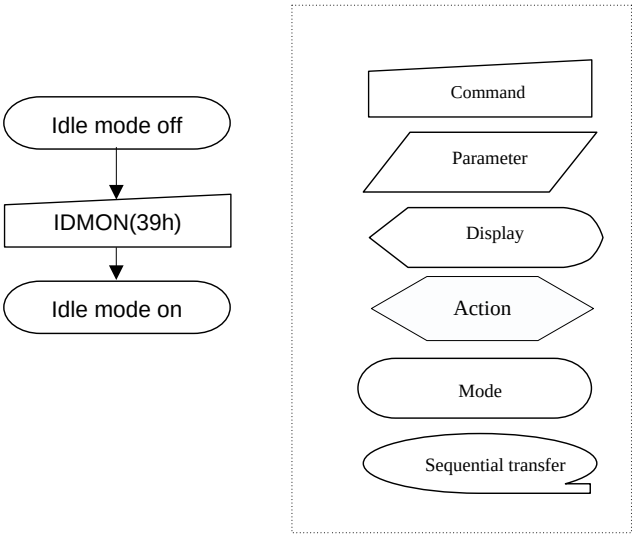
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart



6.2.22. COLMOD: Pixel Format Set (3Ah)

3Ah	Pixel Format Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
Parameter	1	1	↑	XX	0	DPI [2:0]			0	DBI [2:0]			66

Description

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

DBI [2:0]			MCU Interface Format
0	0	0	Gray256（QSPI only）
0	0	1	3bits/ pixel（QSPI only）
0	1	0	8bits/ pixel（QSPI only）
0	1	1	12 bits / pixel
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	24bits/pixel（QSPI &dither on）

If using RGB Interface must selection serial interface.

X = Don’t care.

Restriction

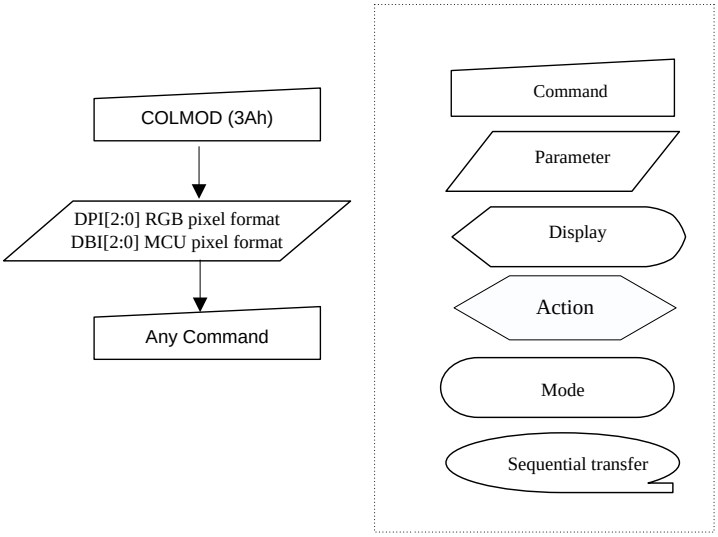
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3’b110	3’b110
SW Reset	No Change	No Change
HW Reset	3’b110	3’b110

Flow Chart	 COLMOD (3Ah) DPI[2:0] RGB pixel format DBI[2:0] MCU pixel format Any Command Command Parameter Display Action Mode Sequential transfer

6.2.23. Write Memory Contiue (3Ch)

3Ch	write_memory_continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	D1[17..8]	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	Dx[17..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	0003FF
Xth Parameter	1	1	↑	D1[17..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	0003FF
Nth Parameter	1	1	↑	Dn[17..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	0003FF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. **If set_address_mode B5 = 0:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC –SC + 1) * (EP – SP + 1) the extra pixels are ignored. **If set_address_mode B5 = 1:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP –SP + 1) the extra pixels are ignored. Sending any other command can stop frame Write. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number												

	will be reset, and the exceeding data will be written into the following column and page.
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

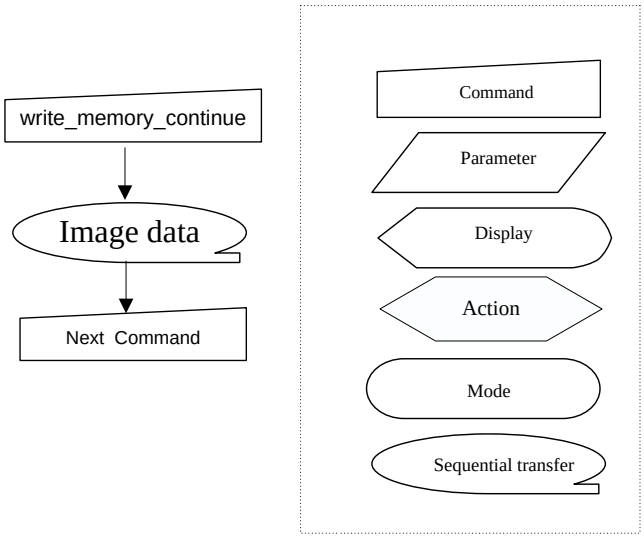
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random value
SW Reset	No change
HW Reset	No change

Flow Chart

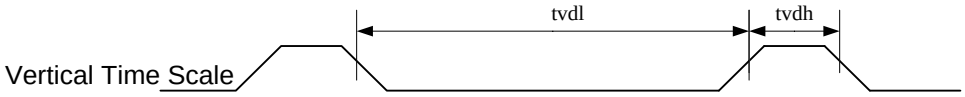


6.2.24. Set_Tear_Scanline (44h)

44h	Set_Tear_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	STS [8]	00
2nd Parameter	1	1	↑	XX	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	00

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of STS[8:0]



Note:that set_tear_scanline with STS is equivalent to set_tear_on with 8+GateN(N=1、2、3...260)

eg:when the STS[8:0]=8,the TE will output at the position of Gate1.

when the STS[8:0]=9,the TE will output at the position of Gate2.

when the STS[8:0]=10,the TE will output at the position of Gate3.

…….

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

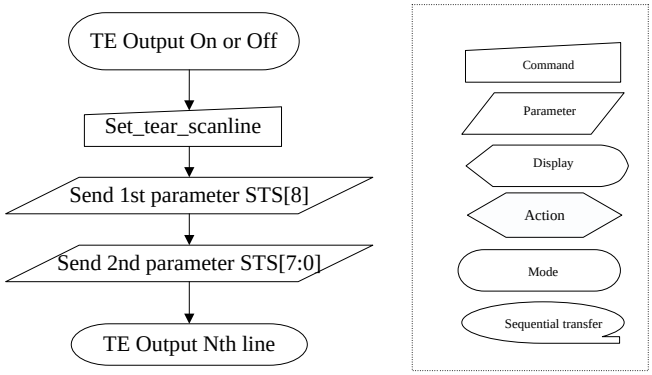
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS [8:0]=0000h
SW Reset	STS [8:0]=0000h
HW Reset	STS [8:0]=0000h

Flow Chart	 TE Output On or Off Set_tear_scanline Send 1st parameter STS[8] Send 2nd parameter STS[7:0] TE Output Nth line Command Parameter Display Action Mode Sequential transfer

6.2.25. Get_Scanline (45h)

45h	Get_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XX	0	0	0	0	0	0	0	GTS [8]	00
2nd Parameter	1	↑	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00
Description	This command returns the setting value of STS[8:0] . When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	None												

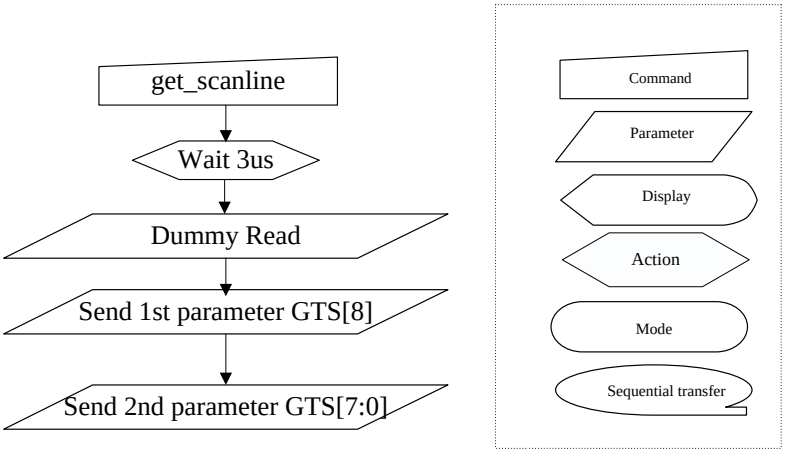
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	GTS [9:0]=0000h
SW Reset	GTS [9:0]=0000h
HW Reset	GTS [9:0]=0000h

Flow Chart

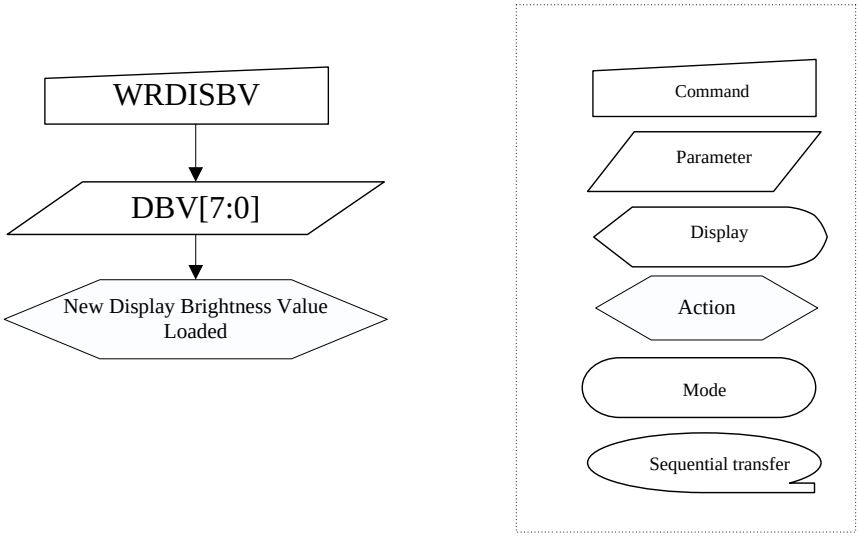


6.2.26. Write Display Brightness (51h)

51h	Write Display Brightness												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
1st Parameter	1	1	↑	XX	DBV [7]	DBV [6]	DBV [5]	DBV [4]	DBV [3]	DBV [6]	DBV [5]	DBV [4]	00
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	None												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	DBV [7:0]= 8’h00
SW Reset	DBV [7:0]= 8’h00
HW Reset	DBV [7:0]= 8’h00

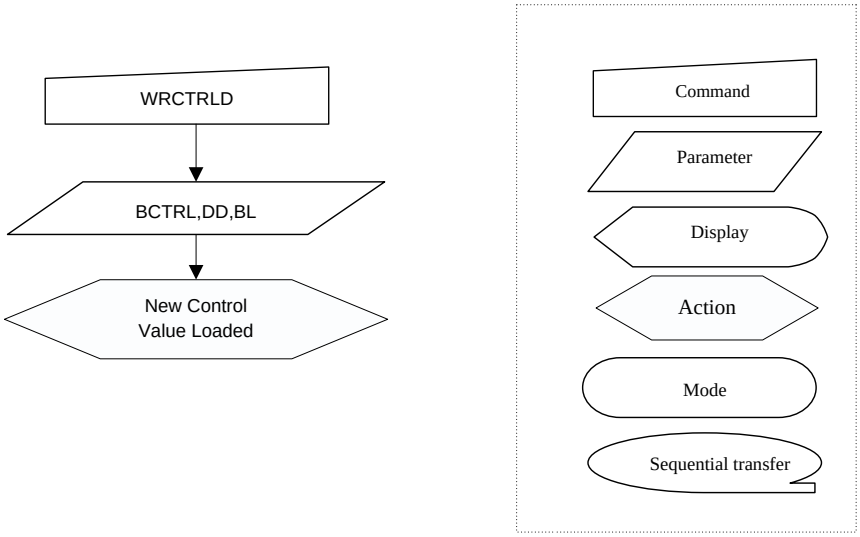
Flow Chart	 WRDISBV DBV[7:0] New Display Brightness Value Loaded Command Parameter Display Action Mode Sequential transfer

6.2.27. Write CTRL Display (53h)

53h	Write CTRL Display												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
1st Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00
Description	This command is used to return brightness setting. **BCTRL**: Brightness Control Block On/Off, '0' = Off (Brightness registers are 00h) '1' = On (Brightness registers are active, according to the DBV[7..0] parameters.) **DD**: Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on **BL**: Backlight On/Off '0' = Off (Completely turn off backlight circuit. Control lines must be low.) '1' = On												
Restriction	The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

Flow Chart	

WRCTRLD
BCTRL,DD,BL
New Control
Value Loaded
Command
Parameter
Display
Action
Mode
Sequential transfer

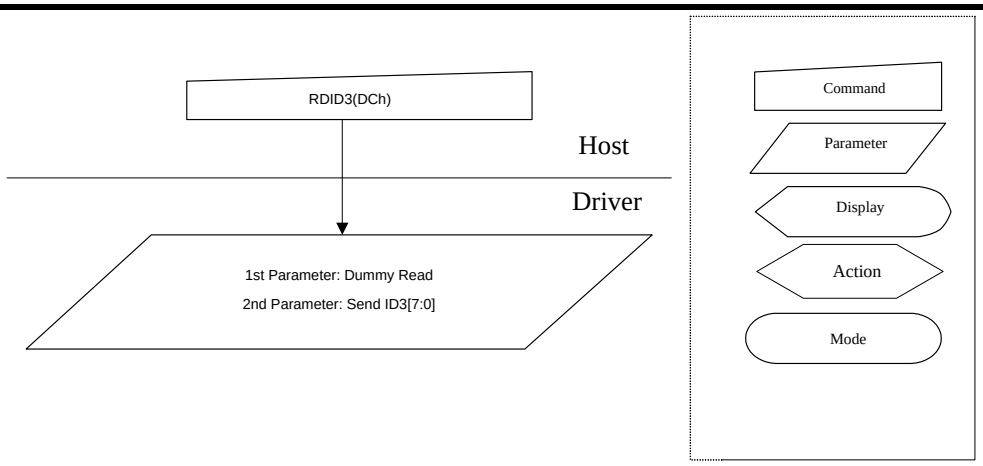
6.2.28. Read ID1 (DAh)

DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								Program value
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (After MTP program)
Power On Sequence	8'h00
SW Reset	8'h00
HW Reset	8'h00

Flow Chart	

RDID3(DCh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send ID3[7:0]
Command
Parameter
Display
Action
Mode

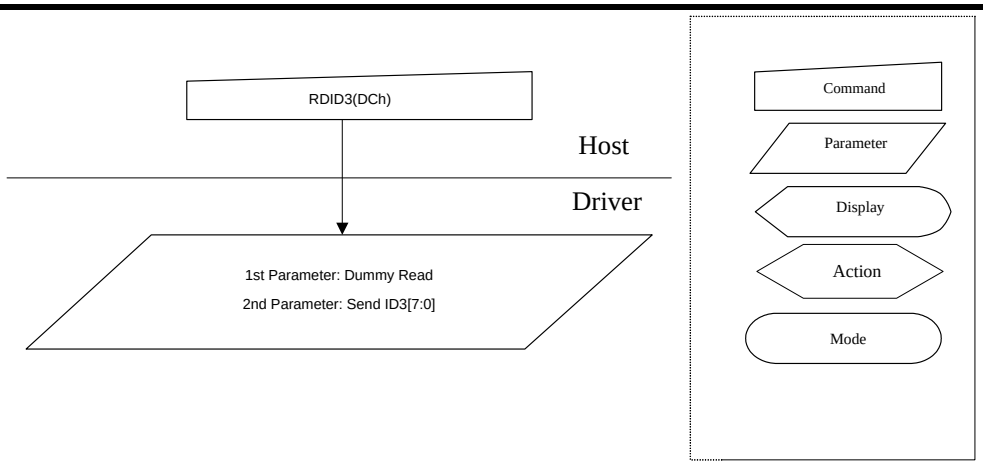
6.2.29. Read ID2 (DBh)

DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								Program value
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (After MTP program)
Power On Sequence	8'h9C
SW Reset	8'h9C
HW Reset	8'h9C

Flow Chart	

RDID3(DCh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send ID3[7:0]
Command
Parameter
Display
Action
Mode

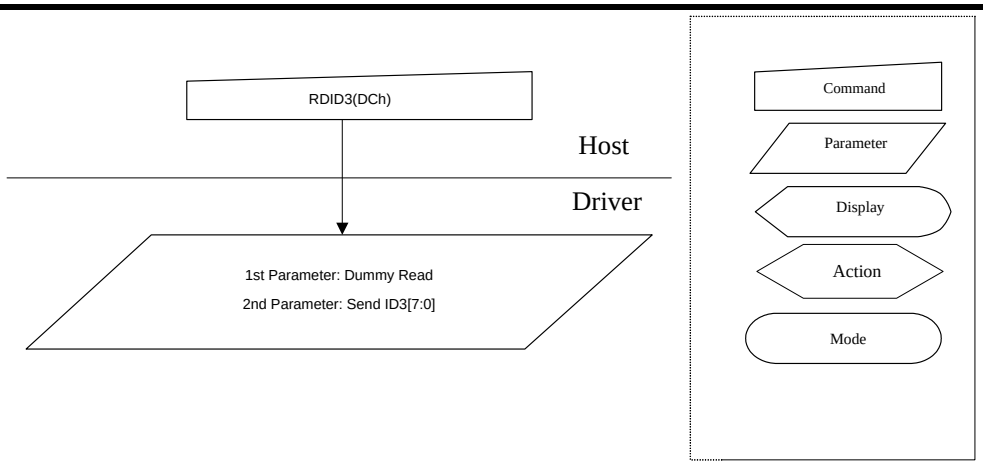
6.2.30. Read ID3 (DCh)

DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								Program value
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (After MTP program)
Power On Sequence	8'h01
SW Reset	8'h01
HW Reset	8'h01

Flow Chart	

RDID3(DCh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send ID3[7:0]
Command
Parameter
Display
Action
Mode

6.3. Description of Level 2 Command

6.3.1. RGB Interface Signal Control (B0h)

B0h	RGB Interface Signal Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
1st Parameter	1	1	↑	XX	0	RCM[1：0]		0	VSPL	HSPL	DPL	EPL	01

Description

Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.

EPL: DE polarity (“0”= High enable for RGB interface, “1”= Low enable for RGB interface)

DPL: DOTCLK polarity set (“0”= data fetched at the rising time, “1”= data fetched at the falling time)

HSPL: HSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)

VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)

RCM [1:0]: RGB interface selection (refer to the RGB interface section).

RCM [1:0]		RIM	DPI[1:0]			RGB interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	DE Mode Valid data is determined by the DE signal	VSYNC,HSYNC,DE, DOTCLK,D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DE, DOTCLK,D[17:13] & D[11:1]
1	0	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DE, DOTCLK,D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	SYNC Mode In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command	VSYNC,HSYNC,DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DOTCLK, D[17:13] & D[11:1]
1	1	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DOTCLK, D[5:0]

Restriction

Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	RCM[1:0]	VSPL	HSPL	DPL	EPL
Power On Sequence	2’b00	1’b0	1’b0	1’b0	1’b1
SW Reset	2’b00	1’b0	1’b0	1’b0	1’b1
HW Reset	2’b00	1’b0	1’b0	1’b0	1’b1

HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31

11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32

6.3.2. Blanking Porch Control (B5h)

B5h	Blanking Porch Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	VFP [7:0]								08
2nd Parameter	1	1	↑	XX	0	VBP [6:0]							08
3rd Parameter	1	1	↑	XX	0	0	0	HBP [4:0]					14

Description

Note: The Third parameter must write,but it is not valid.

VFP [6:0] / VBP [6:0]: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	109.5
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HBP [4:0]: HBP [4:0] bits specify the line number of horizontal back porch period respectively.

HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31

	11111 | 32
Restriction	EXTC should be high to enable this command
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	VFP [6:0]	VBP [6:0]	HBP [4:0]
Power On Sequence	7’h08	7’h08	5’h14
SW Reset	7’h08	7’h08	5’h14
HW Reset	7’h08	7’h08	5’h14

6.3.3. Display Function Control (B6h)

B6h	Display Function Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00
2nd Parameter	1	1	↑	XX	0	GS	SS	0	0	0	0	Win-con	00

Description

note:the first parameter must write,but it is not valid.

SS: Select the shift direction of outputs from the source driver.

SS	Source Output Scan Direction
0	S1 → S540
1	S540 → S1

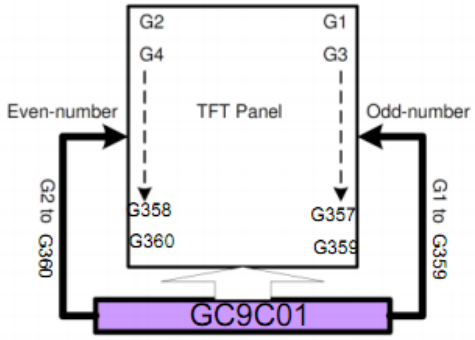
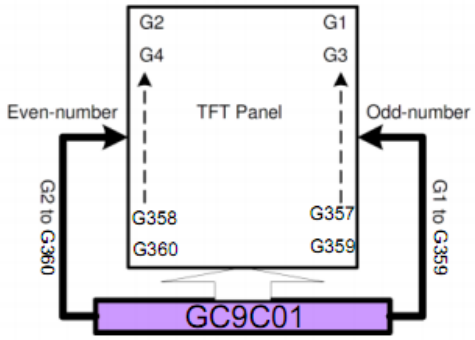
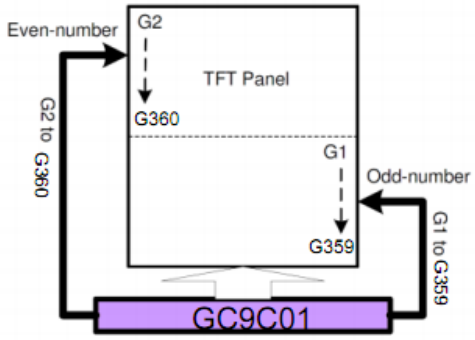
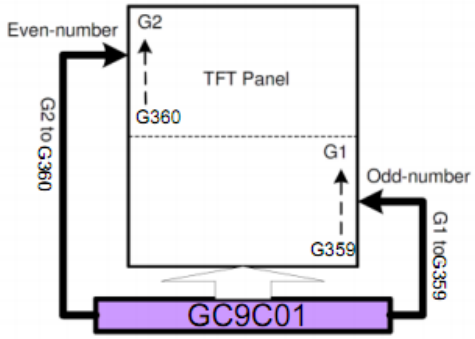
In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S360, set SS = 0.

To assign R, G, B dots to the source driver pins from S360 to S1, set SS = 1.

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1→G360
1	G360→G1

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ ....→G357 → G358→ G359→ G360
0	1		G360 → G359->G358 →G357 →..... .... →G4→G3→G2→G1
1	0		G1→G3→.....→G357 → G359→ G2→G4→.....→G358 → G360
1	1		G360 →G358 →.....→G4→G2→ G359 → G357→.....→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected
by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary
for the size of the liquid crystal panel.

NL [5:0]	LCD Drive Line	NL [5:0]	LCD Drive Line

0	0	0	0	0	0	Setting prohibited	0	1	0	1	0	1	176 lines
0	0	0	0	0	1	16 lines	0	1	0	1	1	0	184 lines
0	0	0	0	1	0	24 lines	0	1	0	1	1	1	192 lines
0	0	0	0	1	1	32 lines	0	1	1	0	0	0	200 lines
0	0	0	1	0	0	40 lines	0	1	1	0	0	1	208 lines
0	0	0	1	0	1	48 lines	……						
0	0	0	1	1	0	56 lines	1	1	0	0	1	1	344 lines
0	0	0	1	1	1	64 lines	1	1	0	1	0	0	352 lines
0	0	1	0	0	0	72 lines	1	1	0	1	0	1	360 lines
0	0	1	0	0	1	80 lines	Others						Setting prohibited
0	0	1	0	1	0	88 lines							
0	0	1	0	1	1	96 lines							
0	0	1	1	0	0	104 lines							
0	0	1	1	0	1	112 lines							
0	0	1	1	1	0	120 lines							
0	0	1	1	1	1	128 lines							
0	1	0	0	0	0	136 lines							
0	1	0	0	0	1	144 lines							
0	1	0	0	1	0	152 lines							
0	1	0	0	1	1	160 lines							

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	-	GS	SS	/
Power On Sequence	-	1’b0	1’b0	/
HW Reset	-	1’b0	1’b0	/

6.3.4. Tearing Effect Control (B4h)

B4h	Tearing Effect Width Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	0	B4h
Parameter1	1	1	↑	XX	te_width[7:0]								00
Parameter2	1	1	↑	XX	X	X	X	X	X	X	X	te_pol	00

Description

te_pol is used to adjust the Tearing Effect output signal pulse polarity.

te_pol	Tearing Effect polarity
0	Positive pulse
1	negative pulse

te_width[6:0] is used to adjust the Tearing Effect output signal pulse width with display lines in unit

te_width[7:0]	Tearing Effect width(display line time)
0	1line time
1	2line time
…	…
N	N+1 line time
…	…
7f	128 line time

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = Don't care.

Restriction

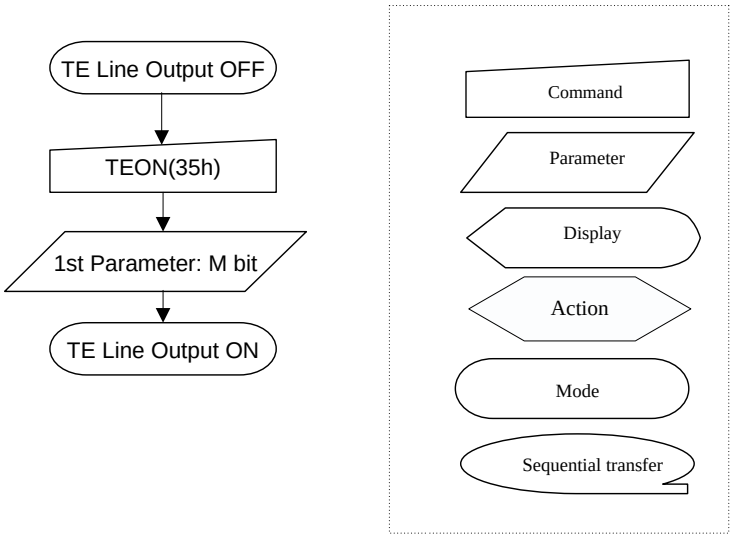
This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0x00
SW Reset	0x00
HW Reset	0x00

Flow Chart	 TE Line Output OFF TEON(35h) 1st Parameter: M bit TE Line Output ON Command Parameter Display Action Mode Sequential transfer

6.3.5. Interface Control (F6h)

F6h	Interface Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
1st Parameter	1	1	1	XX	1	1	0	0	DM [1:0]		RM	RIM	C0

Description

DM [1:0]: Select the display operation mode.

DM[1]	DM[0]	Display Operation Mode
0	0	Internal clock operation
0	1	RGB Interface Mode
1	0	VSYNC interface Mode
1	1	Setting disabled

RM: Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

MDT[1:0] : Method of pixel data transfer. Please refer to section 4.5.6 Data Color Coding

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
1	(262K color)	6- bit RGB interface (3 transfer/pixel)

Restriction

EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	MDT[1:0]	DM [1:0]	RM	RIM
Power On Sequence	2'b00	2'b00	1'b0	1'b0
SW Reset	2'b00	2'b00	1'b0	1'b0
HW Reset	2'b00	2'b00	1'b0	1'b0

6.4. Description of Level 3 Command

6.4.1. Inversion (ECh)

ECh	Iversion												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	0	0	ECh
1st Parameter	1	1	↑	XX	0	dinv[2:0]			0	0	0	0	0x70
Description	**DINV[2:0] :** Set display inversion mode DINV[2:0] — Inversion 0 — 1dot_a inversion 1 — 1dot_b inversion 2 — 1dot_c inversion 3 — 2dot inversion 4 — 4dot inversion 7 — 2 column inversion												
Restriction	Inter_command should be set high to enable this command												
Register Availability	Status — Availability Normal Mode On, Idle Mode Off, Sleep Out — Yes Normal Mode On, Idle Mode On, Sleep Out — Yes Partial Mode On, Idle Mode Off, Sleep Out — Yes Partial Mode On, Idle Mode On, Sleep Out — Yes Sleep In — Yes												

Default		Status	Default Value DINV[2:0]
		Power On Sequence	4’h1
		SW Reset	4’h1
		HW Reset	4’h1

6.4.2. SPI 2DATA control(B1h)

B1h	SPI 2DATA control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XX	X	X	X	DTR_EN	2data_en	2data_mdt[2:0]			00

Description

DTR_EN: Dithering enable.
2DATA_EN: Set 2_data_line mode in 3-wire/4-wire SPI.
2DATA_MDT[2:0] Set pixel data format in 2_data_line mode.

2DATA_MDT[2:0]	Data Format
000	65K color 1pixle/transition
001	262K color 1pixle/transition
010	262K color 2/3pixle/transition

Restriction

Inter command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	2DATA_EN	2DATA_MDT[2:0]
Power On Sequence	1’b0	3’b000
SW Reset	1’b0	3’b000
HW Reset	1’b0	3’b000

6.4.3. Power Control 1 (C1h)

<table>
<tr><th>C1h</th><th colspan="13">Power Control 1</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>vcire</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">vcire: Select the external reference voltage VDDB or internal reference voltage VDDBR.
<table>
<tr><td>vcire =0</td><td>Internal reference voltage 2.5V (default)</td></tr>
<tr><td>vcire =1</td><td>External reference voltage VDDB</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vcire</th></tr>
<tr><td>Power On Sequence</td><td>1’b0</td></tr>
<tr><td>SW Reset</td><td>1’b0</td></tr>
<tr><td>HW Reset</td><td>1’b0</td></tr>
</table></td></tr>
</table>

6.4.4. Power Control 2 (C3h)

C3h	Power Control 2												
	D/C X	RD X	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
1st Parameter	1	1	↑	XX	X	vreg1_vbp_d[6:0]							3C

Description

Set the voltage level value to output the VREG1A and VREG1B OUT level, which is a reference level for the grayscale voltage level.(Table is valid when vrh=0x28)

VREG1A=(vrh+vbp_d)*0.02+4

VREG1B=vbp_d*0.02+0.3

vreg1_vbp_d[6:0]	**VREG1A/V**	**VREG1B/V**
7'h00	4.8	0.3
…	…	…
N	(N+40)*0.02+4	N*0.02+0.3
…	…	…
7’h55	6.5	2.0
7’h56	reserved	reserved
…	…	
7’h7F	reserved	reserved

Restriction

Inter_command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	vreg1_vbp_d[6:0]
Power On Sequence	7h3c
SW Reset	7h3c
HW Reset	7h3c

6.4.5. Power Control 3 (C4h)

C4h	Power Control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
1st Parameter	1	1	↑	XX	X	vreg1_vbn_d[6:0]							3C

Description

Set the voltage level value to output the VREG2A OUT level, which is a reference level for the grayscale voltage level(Table is valid when vrh=0x28)

VREG2A=(vbn_d-vrh)*0.02-3.4

VREG2B=vbn_d*0.02+0.3

vreg1_vbn_d[6:0]	**VREG2A/V**	**VREG2B/V**
7'h00	-4.2	0.3
…	…	…
N	N*0.02-4.2	N*0.02+0.3
…	…	…
7’h55	-2.5	2.0
7’h56	reserved	reserved
…	…	…
7’h7F	reserved	reserved

Restriction

Inter_command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	vreg1_vbn_d[6:0]
Power On Sequence	7’h3C
SW Reset	7’h3C
HW Reset	7’h3C

6.4.6. Power Control 4 (C9h)

C9h	Power Control 4												
	D/C X	RD X	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h
1st Parameter	1	1	↑	XX	X	X	vrh[5:0]						28

Description

Set the voltage level value to output the VREG1A OUT level, which is a reference level for the grayscale voltage level. (Table is valid when vbp_d=0x3C and vbn_d=0x3C)

VREG1A=(vrh+vbp_d)*0.02+4

VREG2A=(vbn_d-vrh)*0.02-3.4

vrh[5:0]	**VREG1A/V**	**VREG2A/V**
6'h00	5.2	-2.2
…	…	…
N	(N+60)*0.02+4	(100-N)*0.02-4.2
…	…	…
6’h28	6	-3
…	…	…
6’h3F	6.46	-3.46

Restriction

Inter_command should be set high to enable this command

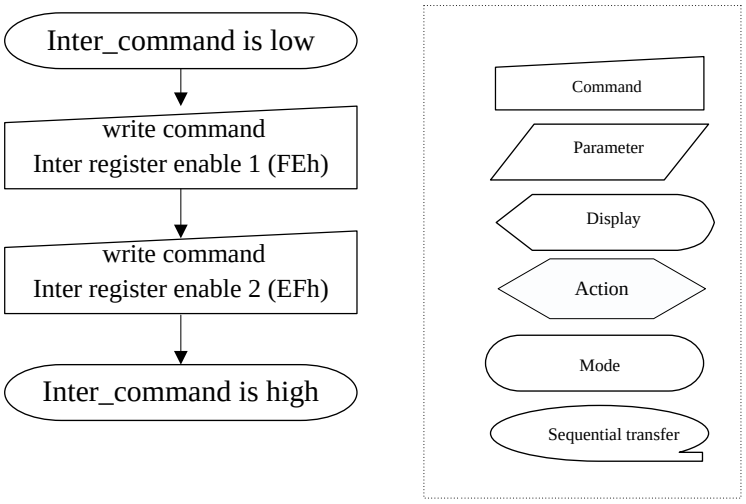
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	vrh[5:0]
Power On Sequence	6’h28
SW Reset	6’h28
HW Reset	6’h28

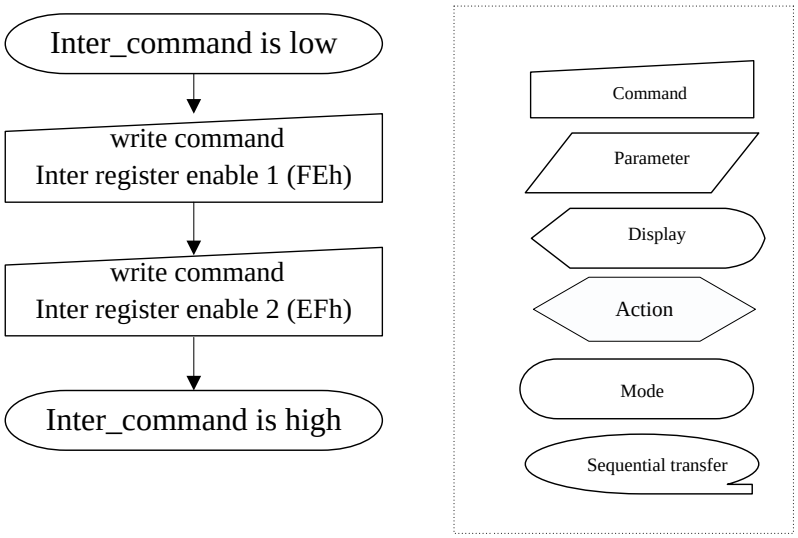
6.4.7. Inter Register Enable1(FEh)

FEh	Inter register enable 1												
	D/C X	RD X	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

6.4.8. Inter Register Enable2(EFh)

EFh	Inter register enable 2												
	D/C X	RD X	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

6.4.9. SET_GAMMA1 (F0h)

F0h	SET_GAMMA1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
1st Parameter	1	1	↑	XX	dig2gam_dig2j0_n[1:0]		dig2gam_vr1_n[5:0]						80
2nd Parameter	1	1	↑	XX	dig2gam_dig2j1_n[1:0]		dig2gam_vr2_n[5:0]						03
3st Parameter	1	1	↑	XX				dig2gam_vr4_n[4:0]					08
4nd Parameter	1	1	↑	XX				dig2gam_vr6_n[4:0]					06
5st Parameter	1	1	↑	XX	dig2gam_vr0_n[3:0]				dig2gam_vr13_n[3:0]				05
6nd Parameter	1	1	↑	XX		dig2gam_vr20_n[6:0]							2B
Description	dig2gam_dig2j0_n[1:0]: γ gradient adjustment register for negative polarity dig2gam_dig2j1_n[1:0]: γ gradient adjustment register for negative polarity dig2gam_vr0_n[3:0]: γ gradient adjustment register for negative polarity dig2gam_vr1_n[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr2_n[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr4_n[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr6_n[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr13_n[3:0]: γ gradient adjustment register for negative polarity dig2gam_vr20_n[6:0]: γ gradient adjustment register for negative polarity												
Restriction	Inter_command should be set high to enable this command												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Id e Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	Status	Default Value					
		dig2gam_dig2j0_n[1:0]	dig2gam_dig2j1_n[1:0]	dig2gam_vr0_n[3:0]	dig2gam_vr1_n[5:0]	dig2gam_vr2_n[5:0]	dig2gam_vr4_n[4:0]
	Power On Sequence	2’h02	2’h00	4’h00	6’h00	6’h03	5’h08
	SW Reset	2’h02	2’h00	4’h00	6’h00	6’h03	5’h08
	HW Reset	2’h02	2’h00	4’h00	6’h00	6’h03	5’h08
Default	Status	Default Value					
		dig2gam_vr6_n[4:0]	dig2gam_vr13_n[3:0]	dig2gam_vr20_n[6:0]			
	Power On Sequence	5’h06	4’h05	7’h2b			
	SW Reset	5’h06	4’h05	7’h2b			
	HW Reset	5’h06	4’h05	7’h2b			

6.4.10. SET_GAMMA2 (F1h)

F1h	SET_GAMMA2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
1st Parameter	1	1	↑	XX		dig2gam_vr43_n[6:0]							41
2nd Parameter	1	1	↑	XX	dig2gam_vr27_n[2:0]			dig2gam_vr57_n[4:0]					97
3st Parameter	1	1	↑	XX	dig2gam_vr36_n[2:0]			dig2gam_vr59_n[4:0]					98
4nd Parameter	1	1	↑	XX			dig2gam_vr61_n[5:0]						13
5st Parameter	1	1	↑	XX			dig2gam_vr62_n[5:0]						17
6nd Parameter	1	1	↑	XX	dig2gam_vr50_n[3:0]				dig2gam_vr63_n[3:0]				CD
Description	dig2gam_vr43_p[6:0]: γ gradient adjustment register for negative polarity dig2gam_vr27_p[2:0]: γ gradient adjustment register for negative polarity dig2gam_vr57_p[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr59_p[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr36_p[2:0]: γ gradient adjustment register for negative polarity dig2gam_vr61_p[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr62_p[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr50_p[3:0]: γ gradient adjustment register for negative polarity dig2gam_vr63_p[3:0]: γ gradient adjustment register for negative polarity												
Restriction	Inter_command should be set high to enable this command												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mo e On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr59_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr61_p[5:0]
Power On Sequence	7’h41	3’h04	5’h17	5’h18	3’h04	6’h13
SW Reset	7’h41	3’h04	5’h17	5’h18	3’h04	6’h13
HW Reset	7’h41	3’h04	5’h17	5’h18	3’h04	6’h13

Default

Status	Default Value					
	dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Power On Sequence	6’h17	4’h0C	4’h0D			
SW Reset	6’h17	4’h0C	4’h0D			
HW Reset	6’h17	4’h0C	4’h0D			

6.4.11. SET_GAMMA3 (F2h)

F2h	SET_GAMMA3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
1st Parameter	1	1	↑	XX	dig2gam_dig2j0_p[1:0]		dig2gam_vr1_p[5:0]						40
2nd Parameter	1	1	↑	XX	dig2gam_dig2j1_p[1:0]		dig2gam_vr2_p[5:0]						03
3st Parameter	1	1	↑	XX				dig2gam_vr4_p[4:0]					08
4nd Parameter	1	1	↑	XX				dig2gam_vr6_p[4:0]					0B
5st Parameter	1	1	↑	XX	dig2gam_vr0_p[3:0]				dig2gam_vr13_p[3:0]				08
6nd Parameter	1	1	↑	XX		dig2gam_vr20_p[6:0]							2E
Description	dig2gam_dig2j0_p[1:0]: γ gradient adjustment register for positive polarity dig2gam_dig2j1_p[1:0]: γ gradient adjustment register for positive polarity dig2gam_vr1_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr2_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr4_p[4:0]: γ gradient adjustment register for positive polarity dig2gam_vr6_p[4:0]: γ gradient adjustment register for positive polarity dig2gam_vr0_p[3:0]: γ gradient adjustment register for positive polarity dig2gam_vr13_p[3:0]: γ gradient adjustment register for positive polarity dig2gam_vr20_p[6:0]: γ gradient adjustment register for positive polarity												
Restriction	Inter_command should be set high to enable this command												
Register Availability													

Status	Availability
Normal Mode On, Idle M de Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	dig2gam_dig2j0_p[1:0]	dig2gam_dig2j1_p[1:0]	dig2gam_vr1_p[5:0]	dig2gam_vr2_p[5:0]	dig2gam_vr4_p[4:0]	dig2gam_vr6_p[4:0]
Power On Sequence	2’h01	2’h00	6’h00	6’h03	5’h08	5’h0B
SW Reset	2’h01	2’h00	6’h00	6’h03	5’h08	5’h0B
HW Reset	2’h01	2’h00	6’h00	6’h03	5’h08	5’h0B

Default

Status	Default Value					
	dig2gam_vr0_p[3:0]	dig2gam_vr13_p[3:0]	dig2gam_vr20_p[6:0]			
Power On Sequence	4’h00	4’h08	7’h2E			
SW Reset	4’h00	4’h08	7’h2E			
HW Reset	4’h00	4’h08	7’h2E			

6.4.12. SET_GAMMA4 (F3h)

F3h	SET_GAMMA4												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	1	1	F3h
1st Parameter	1	1	↑	XX		dig2gam_vr43_p[6:0]							3F
2nd Parameter	1	1	↑	XX	dig2gam_vr27_p[2:0]			dig2gam_vr57_p[4:0]					98
3st Parameter	1	1	↑	XX	dig2gam_vr36_p[2:0]			dig2gam_vr59_p[4:0]					B4
4nd Parameter	1	1	↑	XX			dig2gam_vr61_p[5:0]						14
5st Parameter	1	1	↑	XX			dig2gam_vr62_p[5:0]						18
6nd Parameter	1	1	↑	XX	dig2gam_vr50_p[3:0]				dig2gam_vr63_p[3:0]				CD
Description	dig2gam_vr43_p[6:0]: γ gradient adjustment register for positive polarity dig2gam_vr27_p[2:0]: γ gradient adjustment register for positive polarity dig2gam_vr57_p[4:0]: γ gradient adjustment register for positive polarity dig2gam_vr36_p[2:0]: γ gradient adjustment register for positive polarity dig2gam_vr59_p[4:0]: γ gradient adjustment register for positive polarity dig2gam_vr61_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr62_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr50_p[3:0]: γ gradient adjustment register for positive polarity dig2gam_vr63_p[3:0]: γ gradient adjustment register for positive polarity												
Restriction	Inter_command should be set high to enable this command												
Register Availability													

Status	Avail bility
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr59_p[4:0]	dig2gam_vr61_p[5:0]
Power On Sequence	7’h3F	3’h04	5’h18	3’h05	5’h14	6’h14
SW Reset	7’h3F	3’h04	5’h18	3’h05	5’h14	6’h14
HW Reset	7’h3F	3’h04	5’h18	3’h05	5’h14	6’h14

Default

Status	Default Value					
	dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Power On Sequence	6’h18	4’h0C	4’h0D			
SW Reset	6’h18	4’h0C	4’h0D			
HW Reset	6’h18	4’h0C	4’h0D			

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9C01 is used out of the absolute maximum ratings, GC9C01 may be permanently damaged. To use GC9C01 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9C01 will malfunction and cause poor reliability.

Table43.

Item	Symbol	Unit	Value
Supply voltage	VDDB	V	-0.3~+4.6
Supply voltage(Logic)	VDDI	V	-0.3~+4.6
Supply voltage(Digital)	DVDD	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+27.0
Logic input voltage range	VIN	V	-0.3~VDDI+0.3
Logic output voltage range	VO	V	-0.3~VDDI+0.3
Operation temperature	Topr	℃	-40~+80
Storage temperature	Tstg	℃	-40~+80
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

7.2. DC Characteristics

7.2.1. DC Characteristics for Panel Driving

General DC Characteristics

Table44.

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VDDB	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	DVDD	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	8.0	-	15.0	Note3
Gate Driver Low Voltage	VGL	V	-	-12.0	-	-7.0	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSSB	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSSB	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSSB	-0.1	-	+0.1	Note1,2,3
Source Driver							
Positive Source Output Range	Vsout	V	-	VREG1B	-	VREG1A	
Negative Source Output Range	Vsout	V	-	VREG2A	-	VREG2B	

Note 1: VDDI=1.65 to 3.3V, VDDB=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital VDDI voltage equal or less than analog VDDB voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1,IM0, and Test pins.

7.2.2. DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MCU interface.

parameter	symbol	condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA ;Note 2	0.8IOVCC	-	IOVCC	V
Logic Low level output voltage	V_{OL}	I_{OUT}=-1mA ; Note 2	0.0	-	0.2 IOVCC	V
Logic High level input voltage	V_{IHLPCD}	LP-CD ; Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD ; Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLOCK, DATA) ; Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLOCK, DATA) ; Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLOCK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (DATA), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (DATA), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

Note: (1) Ta=-30℃ to 70℃ (to +85℃ no damage)

(2) PWM_OUT, TE

(3) DSI High Speed mode is off

7.2.3. DC characteristics for DSI HS mode

DC levels of the HS-0 and HS-0 are defined on table below: DC Characteristics for DSI HS mode.

parameter	symbol	condition	Specification			Unit
			Min.	Typ.	Max.	
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLOCK_P/N ; Note 2,3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-DATA_P/N ; Note 2,3	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLOCK_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-DATA_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLOCK_P/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-DATA_P/N	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLOCK_P/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-DATA_P/N	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLOCK_P/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-DATA_P/N	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	80	100	125	Ω
Single-ended Threshold	$V_{TERM-EN}$	DSI-CLOCK_P/N,	-	-	450	mV

Voltage for Termination Enable		DSI-DATA_P/N				
Termination Capacitor	C_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	-	-	14	pF

Note: (1) Ta = -30 to 70 °C (to +85 °C no damage), IOVCC = 1.65 to 1.95V, GND = 0V

(2) Includes 50mV (-50mV to 50mV) ground difference

(3) Without $V_{CMRCLKM450}$/$V_{CMRDATAM450}$

(4) Without 50mV (-50mV to 50mV) ground difference

7.3. AC Characteristics

7.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ)

Figure90.

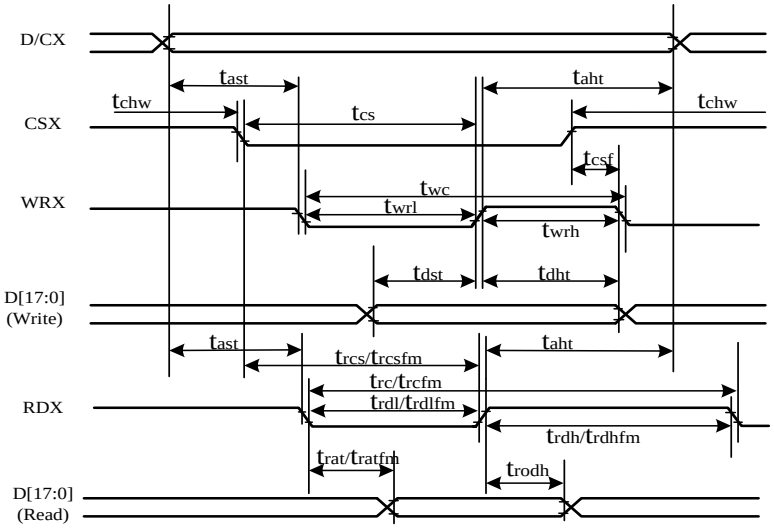


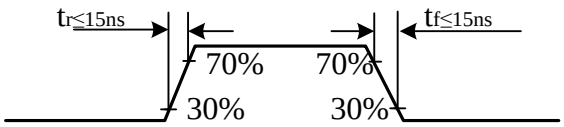
Table45.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	70	-	ns	
D[17:0],D[15:0],D[8:0	tdst	Write data setup time	10	-	ns	For maximum CL=30pF
	tdht	Write data hold time	10	-	ns	

], D[7:0]	trat	Read access time	-	40	ns	For minimum CL=8pF
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

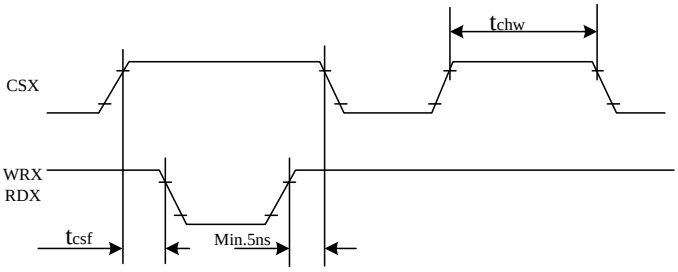
Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSS=0V

Figure91.



CSX timings :

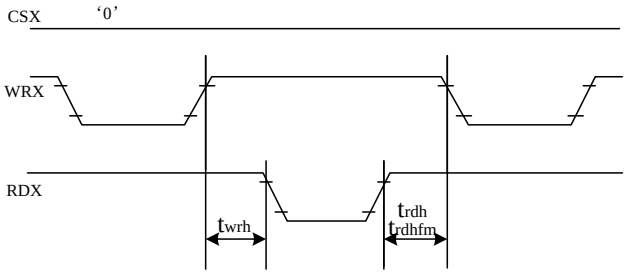
Figure92.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

Figure92.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅱ)

Figure93.

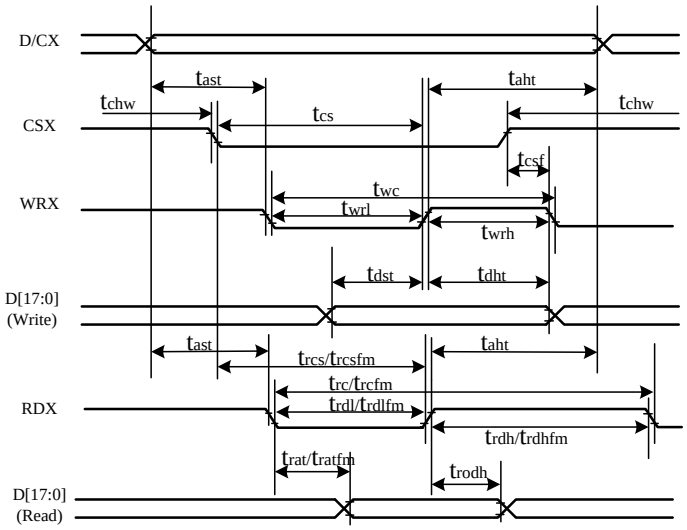
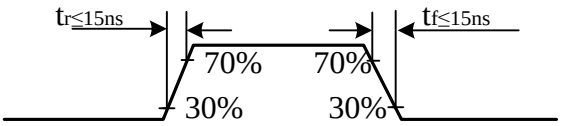


Table46.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	70	-	ns	
D[17:0], D[17:10] &D[8:1], D[17:10] ,D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

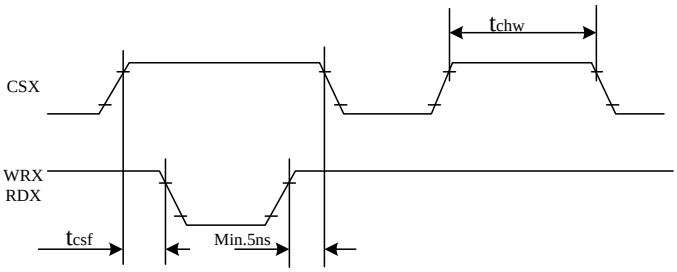
Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSS=0V.

Figure94.



CSX timings :

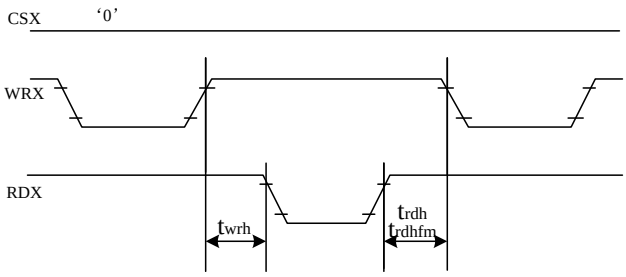
Figure95.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

Figure96.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)

Figure97.

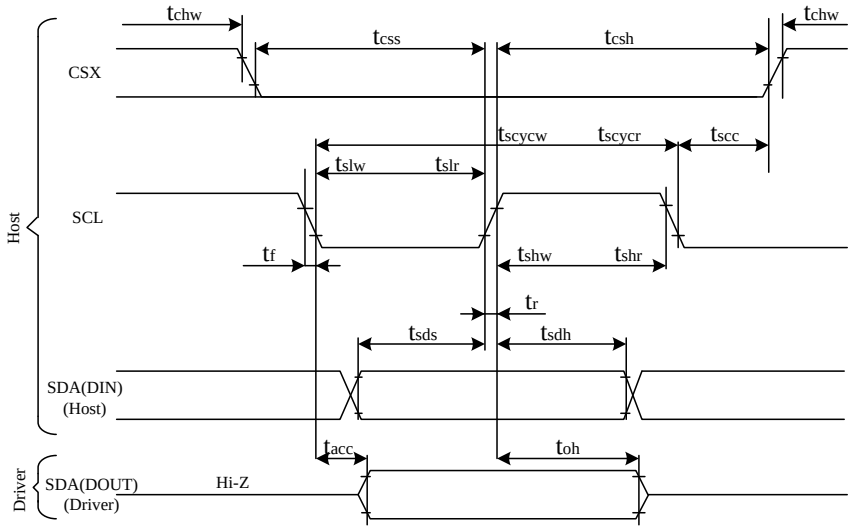
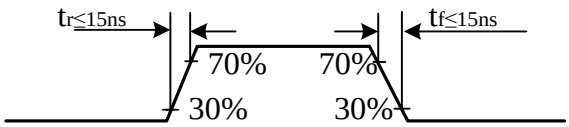


Table47.

Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/SD0(Outp)	tacc	Access time (Read)	10	-	ns	
CSX	tscc	SCL-CSX	10	-	ns	
	tchw	CSX "H" Pulse Width	10	-	ns	
	tcss	CSX-SCL Time	20	-	ns	
	tcsh		40	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSSB=VSSB=0V

Figure98.



7.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)

Figure98.

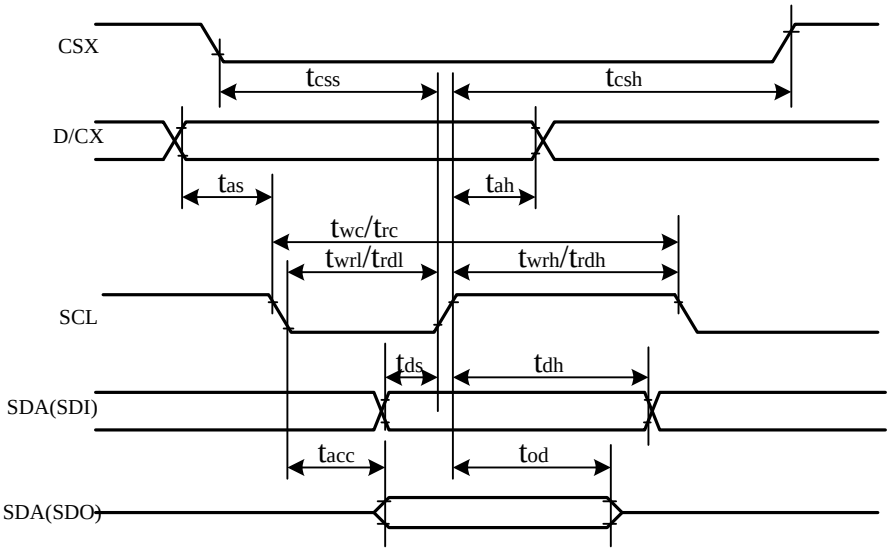
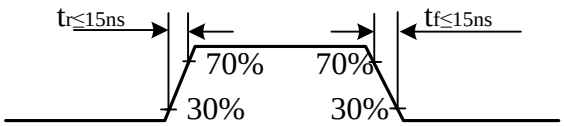


Table48.

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, AGND=VSS=0V

Figure99.



7.3.5. Parallel 18/16/6-bit RGB Interface Timing Characteristics

Figure100.

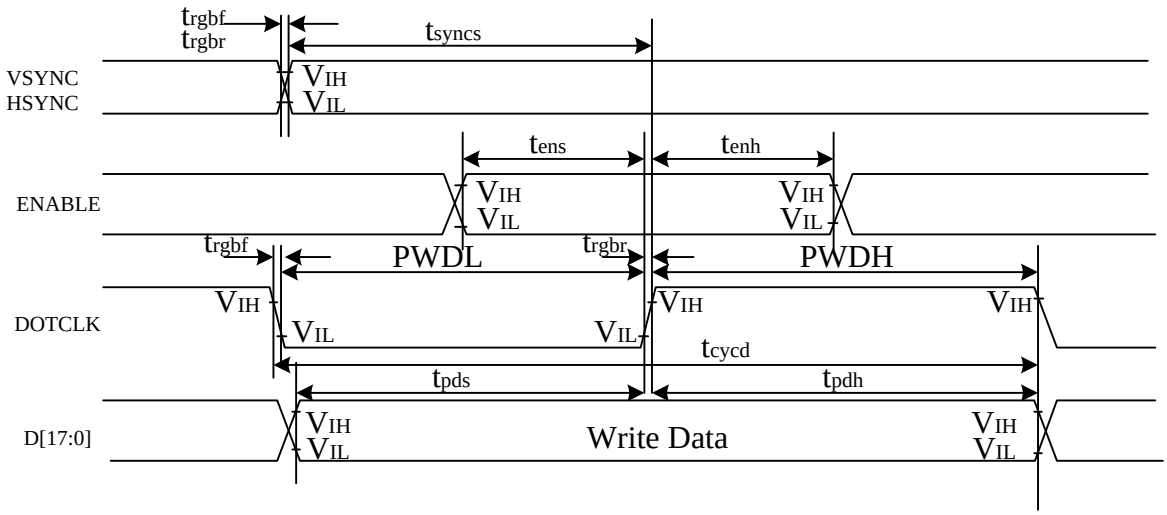
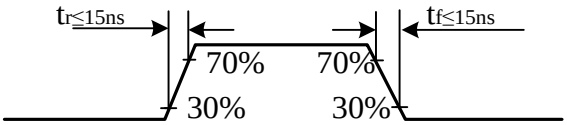


Table49.

Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

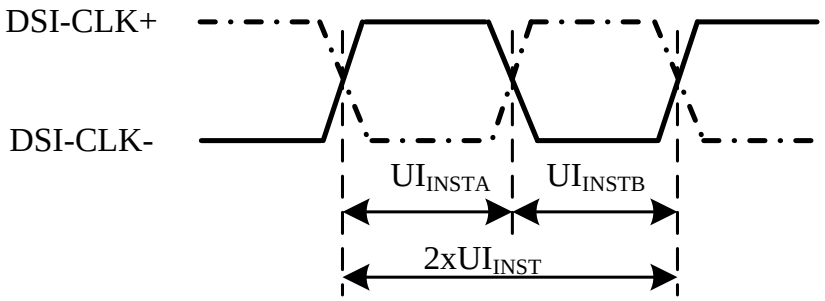
Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, AGND=VSS=0V

Figure101.



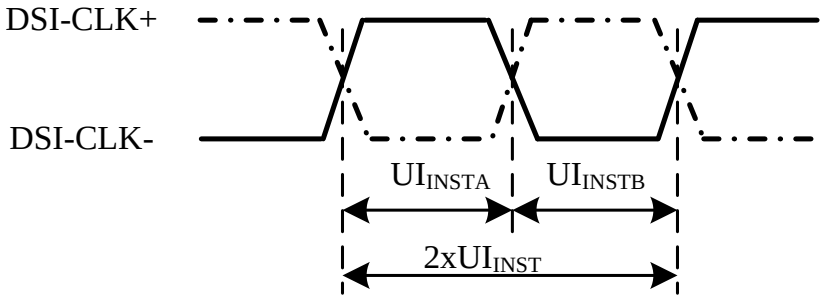
7.3.6. MIPI

7.3.6.1. High Speed Mode – Clock Channel Timing

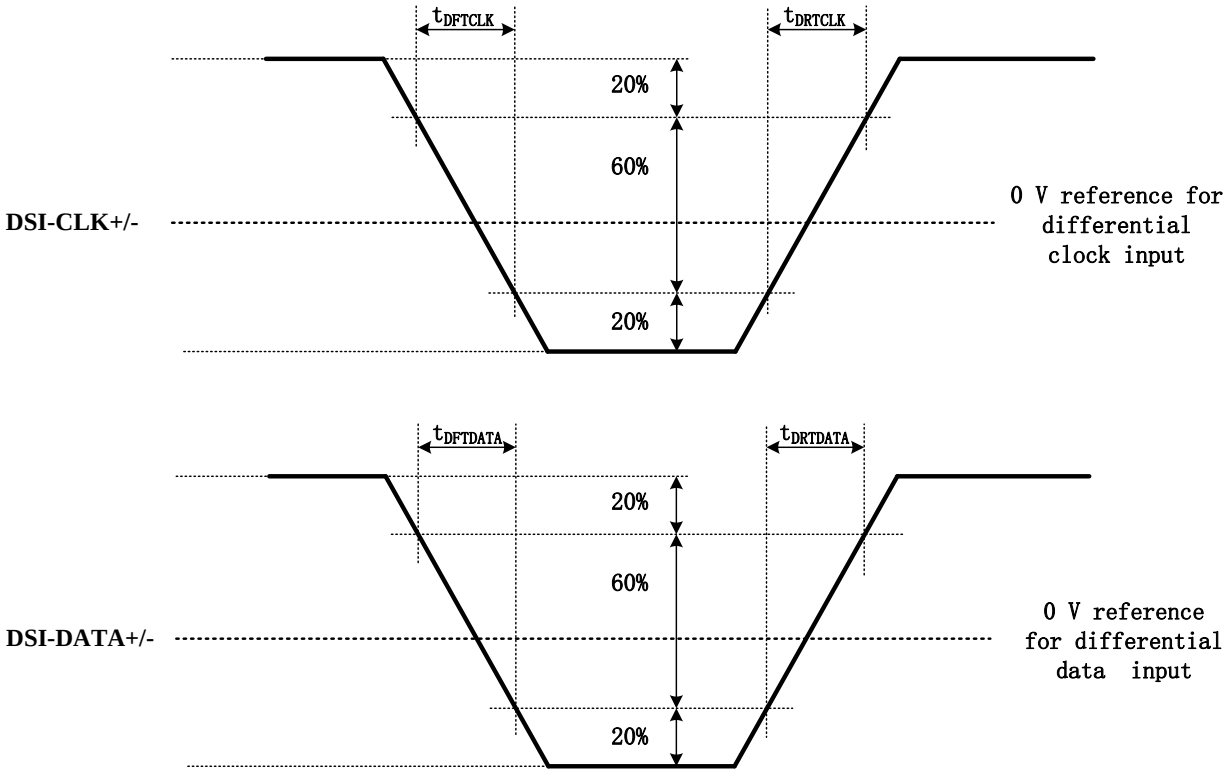


Signal	Symbol	Parameter	Min	Max	Unit
DSI_CLOCK_P/N	$2xUI_{INST}$	Double UI instantaneous	8	25	ns
DSI_CLOCK_P/N	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	4	12.5	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

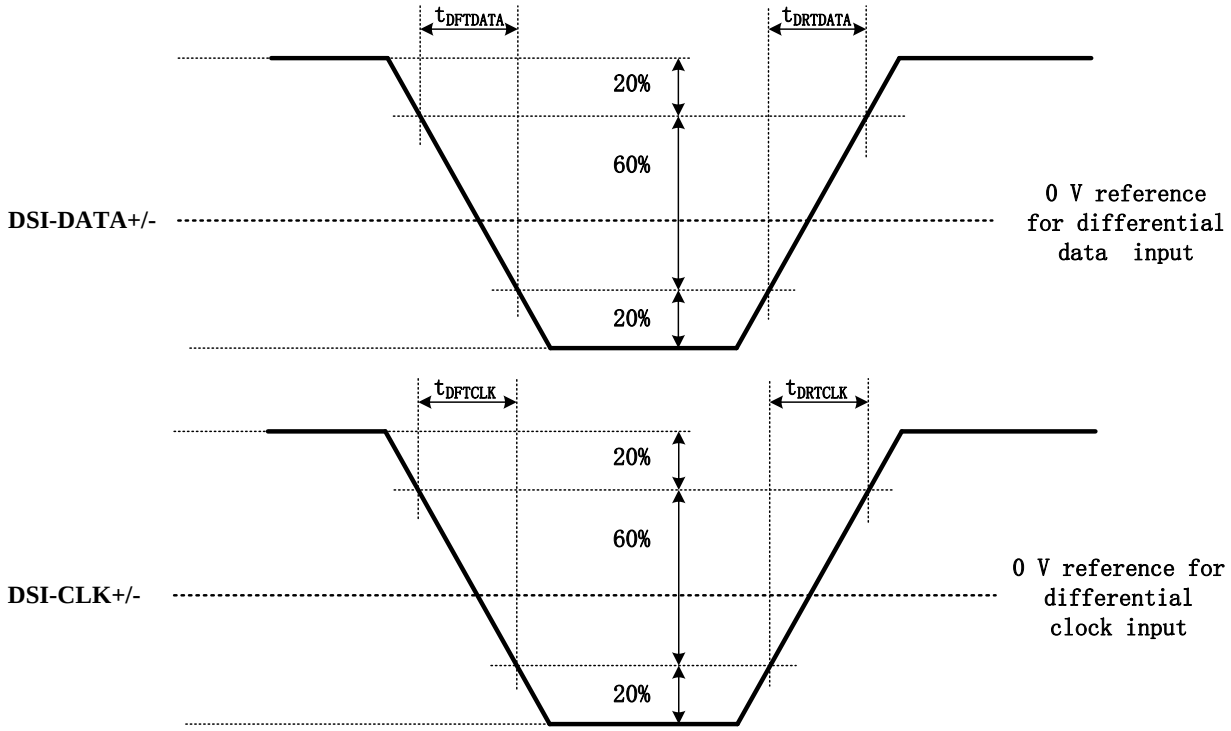


7.3.6.2.High Speed Mode – Rise and Fall Timings



Signal	Symbol	Condition	specification			Unit
			Min	Max	Type	
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLOCK_P/N	-	-	900	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-DATA_P/N	-	-	900	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLOCK_P/N	-	-	900	Ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-DATA_P/N	-	-	900	ps

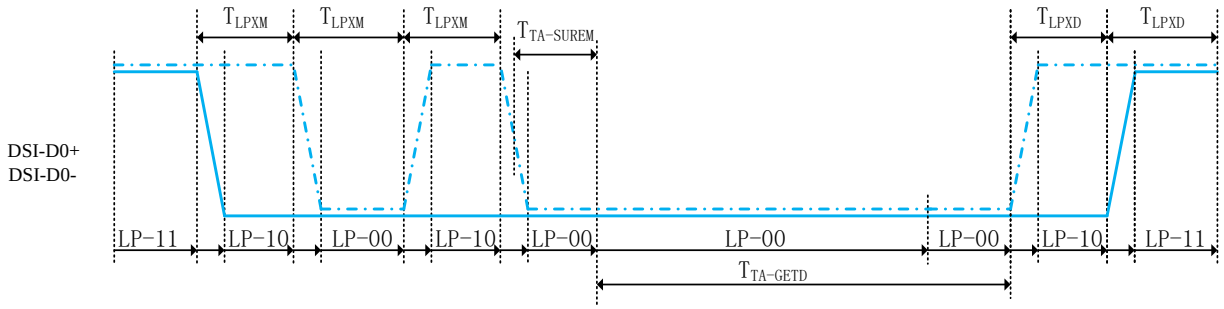
7.3.6.3.High Speed Mode – Rise and Fall Timings



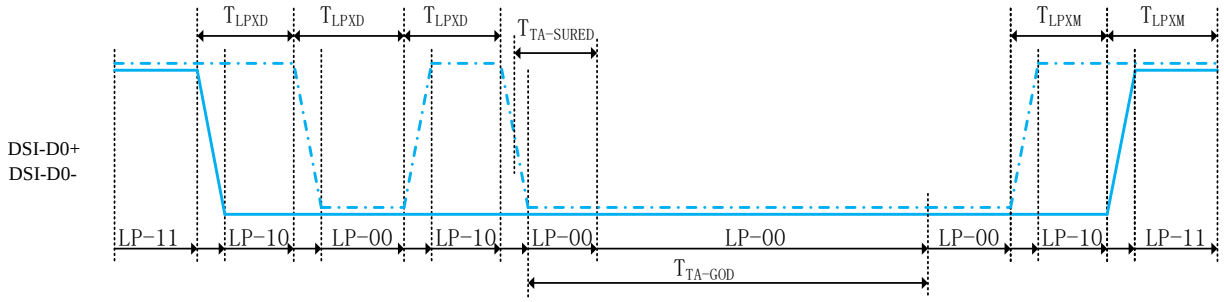
Signal	Symbol	Condition	specification			Unit
			Min	Max	Type	
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLOCK_P/N	-	-	900	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-DATA_P/N	-	-	900	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLOCK_P/N	-	-	900	Ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-DATA_P/N	-	-	900	ps

7.3.6.4.Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MCU to the GC9C01sequence below.



Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from GC9C01to the MCU sequence below.

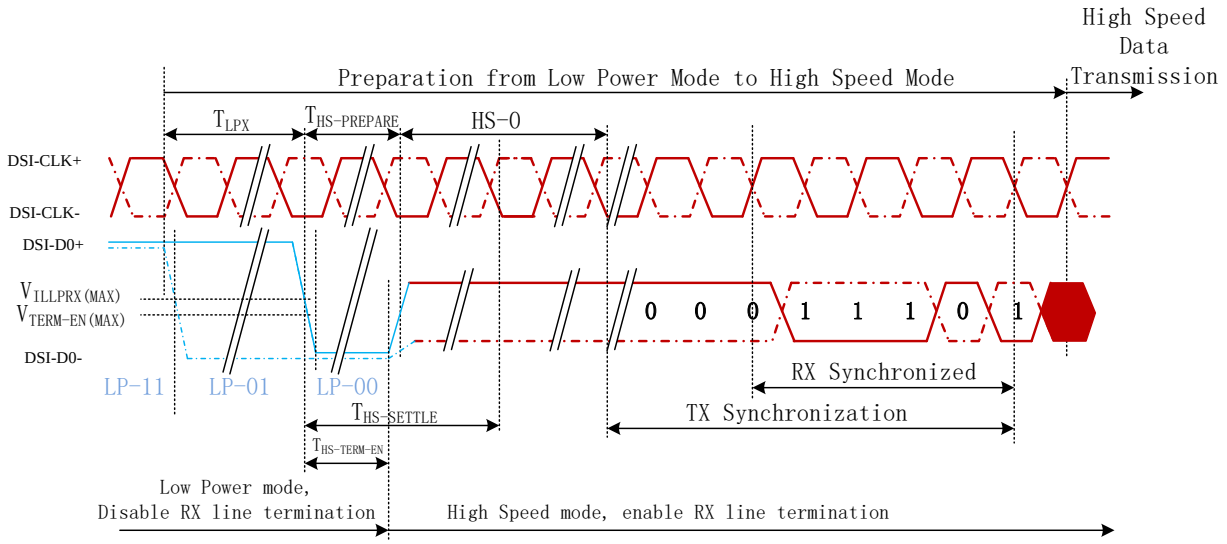


Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → GC9C01	50	-	ns
Input (DSI-DATA_P/N)	$T_{TA-SUREM}$	Time-out before the GC9C01starts driving	T_{LPXM}	$2xT_{LPXM}$	ns
Output (DSI-DATA_P/N)	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods GC9C01→ MCU	50	75	ns
Output (DSI-DATA_P/N)	$T_{TA-SURED}$	Time-out before the MCU starts driving	T_{LPXD}	$2xT_{LPXD}$	

8.

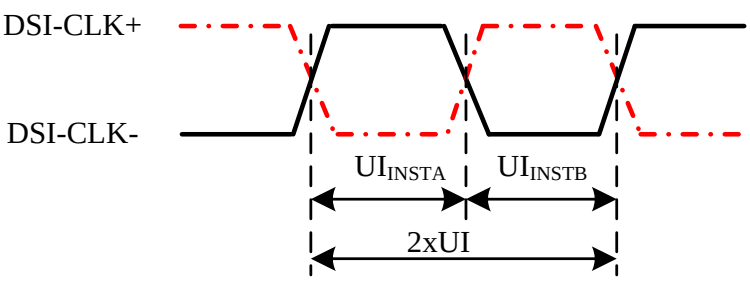
Signal	Symbol	Description	Time	Unit
Input (DSI-DATA_P/N)	$T_{TA-GETD}$	Time to drive LP-00 by GC9C01	$5xT_{LPXD}$	ns
Output (DSI-DATA_P/N)	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

7.2.6.5. Data Lanes from Low Power Mode to High Speed Mode

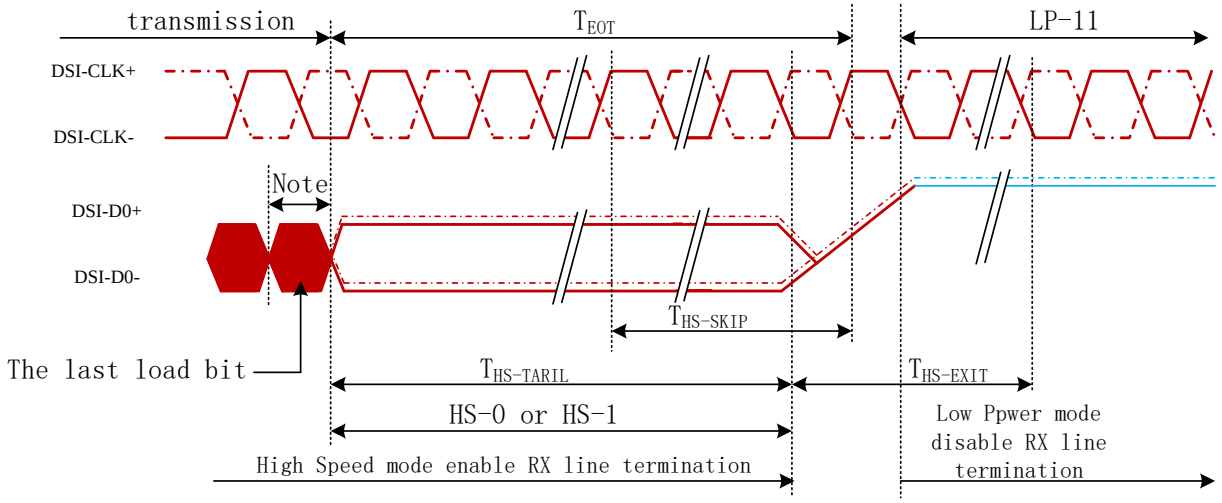


Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	T_{LPX}	Length of any low power state period	50	-	ns
Input (DSI-DATA_P/N)	$T_{HS-PREPARE}$	Time to Drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
Input (DSI-DATA_P/N)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses V_{ILMAX}	-	35+4xUI	ns

Note: UI definition: UI = UI_{INSTA} = UI_{INSTB}



7.2.6.6. Data Lanes from High Speed Mode to Low Power Mode



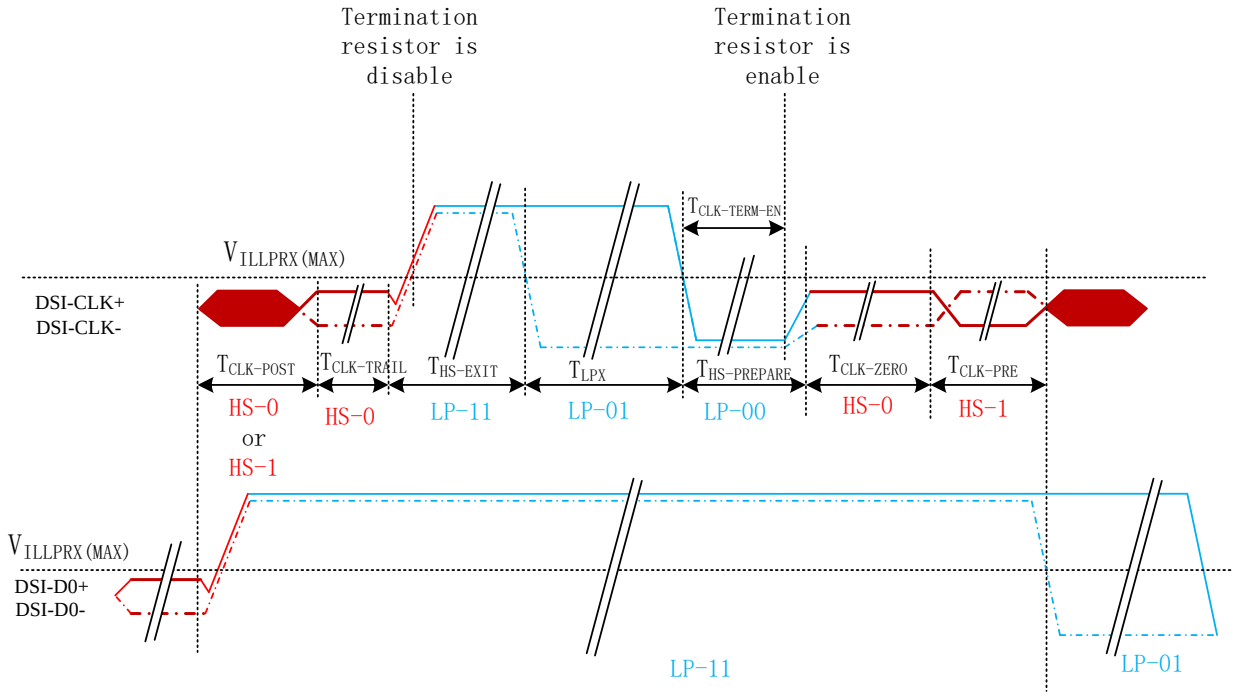
Note:

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

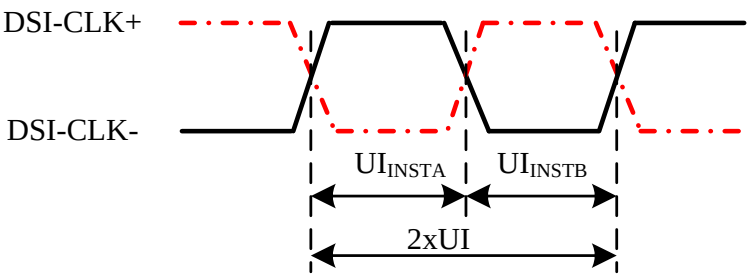
Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	$T_{TA-SKIP}$	Time-out at GC9C01to Ignore Transition Period of EoT	40	4xUI	ns
Output (DSI-DATA_P/N)	$T_{TA-EXIT}$	Time to Driver LP-11 after HS burst	100	-	ns

7.2.6.7.DSI Clock Burst – High Speed Mode to/from Low Power Mode



Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
Input (DSI-DATA_P/N)	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
Input (DSI-DATA_P/N)	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
Input (DSI-DATA_P/N)	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	
Input (DSI-DATA_P/N)	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	38	-	
Input (DSI-DATA_P/N)	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300		
Input (DSI-DATA_P/N)	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI		

Note: UI definition: UI = UI_{INSTA} = UI_{INSTB}


DSI-CLK+
DSI-CLK-
UI_INSTA
UI_INSTB
2xUI