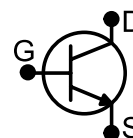
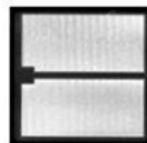


Normally – OFF Silicon Carbide Junction Transistor

V_{DS}	=	1700 V
$R_{DS(ON)}$	=	20 mΩ
$I_D @ 25\text{ }^{\circ}\text{C}$	=	100 A
h_{FE}	=	85

Features

- 210 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode



Die Size = 4.35 mm x 4.35 mm

Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 μs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

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Section I: Absolute Maximum Ratings

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	V_{DS}	$V_{GS} = 0\text{ V}$	1700	V	
Continuous Drain Current	I_D	$T_C = 25\text{ }^{\circ}\text{C}$	100	A	
Continuous Drain Current	I_D	$T_C > 125\text{ }^{\circ}\text{C}$, assumes $R_{\theta JC} < 0.26\text{ }^{\circ}\text{C/W}$	50	A	
Continuous Gate Current	I_G		3.5	A	
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 210\text{ }^{\circ}\text{C}$, Clamped Inductive Load	$I_{D,max} = 50$ @ $V_{DS} \leq V_{DS,max}$	A	Fig. 16
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 210\text{ }^{\circ}\text{C}$, $I_G = 1\text{ A}$, $V_{DS} = 1200\text{ V}$, Non Repetitive	>20	μs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Operating Junction and Storage Temperature	T_j, T_{stg}		-55 to 210	$^{\circ}\text{C}$	
Maximum Processing Temperature	T_{Proc}	10 min. maximum	325	$^{\circ}\text{C}$	

Section II: Static Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
A: On State							
Drain – Source On Resistance	R _{DS(ON)}	I _D = 50 A, T _J = 25 °C		20		mΩ	Fig. 4
		I _D = 50 A, T _J = 150 °C		36			
		I _D = 50 A, T _J = 175 °C		42			
Gate – Source Saturation Voltage	V _{GS,SAT}	I _D = 50 A, I _D /I _G = 40, T _J = 25 °C		3.42		V	Fig. 7
		I _D = 50 A, I _D /I _G = 30, T _J = 175 °C		3.23			
DC Current Gain	h _{FE}	V _{DS} = 8 V, I _D = 50 A, T _J = 25 °C		80		–	Fig. 5
		V _{DS} = 8 V, I _D = 50 A, T _J = 125 °C		60			
		V _{DS} = 8 V, I _D = 50 A, T _J = 175 °C		50			
B: Off State							
Drain Leakage Current	I _{DSS}	V _{DS} = 1700 V, V _{GS} = 0 V, T _J = 25 °C		10		μA	Fig. 8
		V _{DS} = 1700 V, V _{GS} = 0 V, T _J = 150 °C		10			
		V _{DS} = 1700 V, V _{GS} = 0 V, T _J = 175 °C		20			
Gate Leakage Current	I _{SG}	V _{SG} = 20 V, T _J = 25 °C		20		nA	

Section III: Dynamic Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
A: Capacitance and Gate Charge							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 1200 V, f = 1 MHz		7205		pF	Fig. 9
Reverse Transfer/Output Capacitance	C _{rss} /C _{oss}	V _{DS} = 1200 V, f = 1 MHz		120		pF	Fig. 9
Output Capacitance Stored Energy	E _{OSS}	V _{GS} = 0 V, V _{DS} = 1200 V, f = 1 MHz		100		μJ	Fig. 10
Effective Output Capacitance, time related	C _{oss,tr}	I _D = constant, V _{GS} = 0 V, V _{DS} = 0...1200 V		194		pF	
Effective Output Capacitance, energy related	C _{oss,er}	V _{GS} = 0 V, V _{DS} = 0...1200 V		139		pF	
Gate-Source Charge	Q _{GS}	V _{GS} = -5...3 V		55		nC	
Gate-Drain Charge	Q _{GD}	V _{GS} = 0 V, V _{DS} = 0...1200 V		233		nC	
Gate Charge - Total	Q _G			288		nC	
B: Switching ¹							
Internal Gate Resistance – zero bias	R _{G(INT-ZERO)}	f = 1 MHz, V _{AC} = 50 mV, V _{DS} = 0 V, V _{GS} = 0 V, T _J = 175 °C		0.59		Ω	
Internal Gate Resistance – ON	R _{G(INT-ON)}	V _{GS} > 2.5 V, V _{DS} = 0 V, T _J = 175 °C		0.09		Ω	
Turn On Delay Time	t _{d(on)}	T _J = 25 °C, V _{DS} = 1200 V, I _D = 50 A, Inductive Load		17		ns	
Fall Time, V _{DS}	t _f	Refer to Section V for additional driving information.		47		ns	Fig. 11, 13
Turn Off Delay Time	t _{d(off)}			39		ns	
Rise Time, V _{DS}	t _r			25		ns	Fig. 12, 14
Turn On Delay Time	t _{d(on)}			17		ns	
Fall Time, V _{DS}	t _f	T _J = 175 °C, V _{DS} = 1200 V, I _D = 50 A, Inductive Load		47		ns	Fig. 11
Turn Off Delay Time	t _{d(off)}			44		ns	
Rise Time, V _{DS}	t _r			23		ns	Fig. 12
Turn-On Energy Per Pulse	E _{on}	T _J = 25 °C, V _{DS} = 1200 V, I _D = 50 A, Inductive Load		1830		μJ	Fig. 11, 13
Turn-Off Energy Per Pulse	E _{off}	Refer to Section V.		628		μJ	Fig. 12, 14
Total Switching Energy	E _{tot}			2458		μJ	
Turn-On Energy Per Pulse	E _{on}	T _J = 175 °C, V _{DS} = 1200 V, I _D = 50 A, Inductive Load		1800		μJ	Fig. 11
Turn-Off Energy Per Pulse	E _{off}			577		μJ	Fig. 12
Total Switching Energy	E _{tot}			2377		μJ	

¹ – All times are relative to the Drain-Source Voltage V_{DS}

Section IV: Figures

A: Static Characteristics

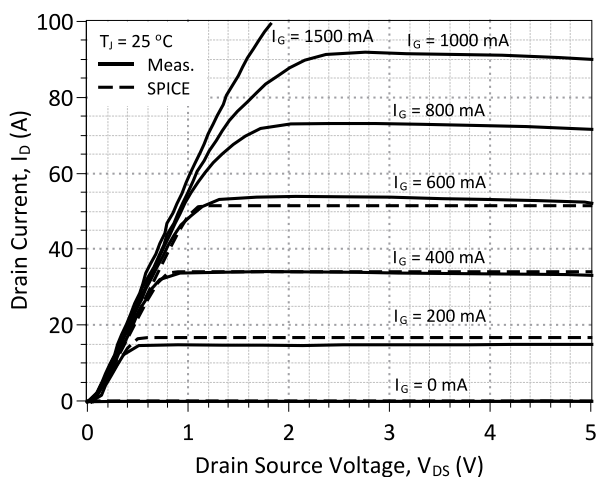


Figure 1: Typical Output Characteristics at 25 °C

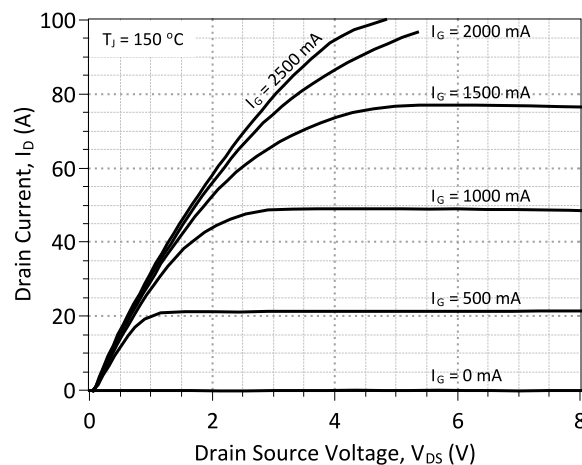


Figure 2: Typical Output Characteristics at 150 °C

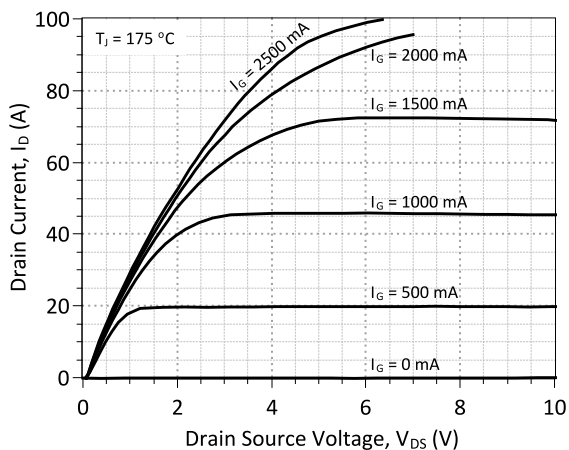


Figure 3: Typical Output Characteristics at 175 °C

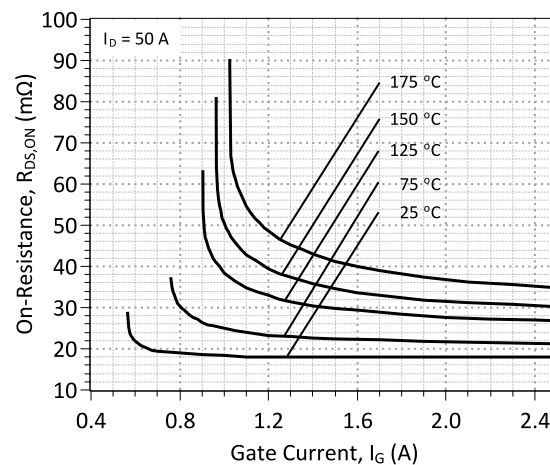


Figure 4: On-Resistance vs. Gate Current

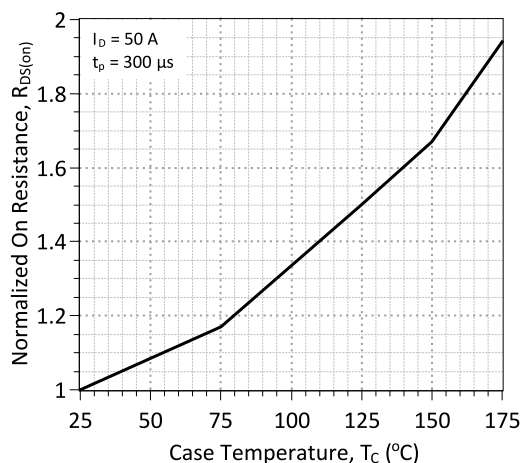


Figure 5: Normalized On-Resistance vs. Temperature

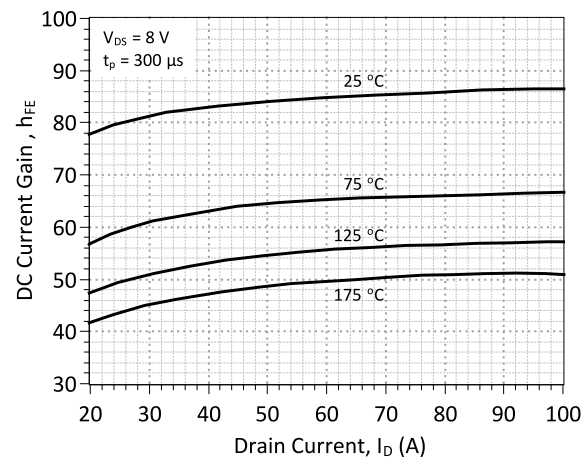


Figure 6: DC Current Gain vs. Drain Current

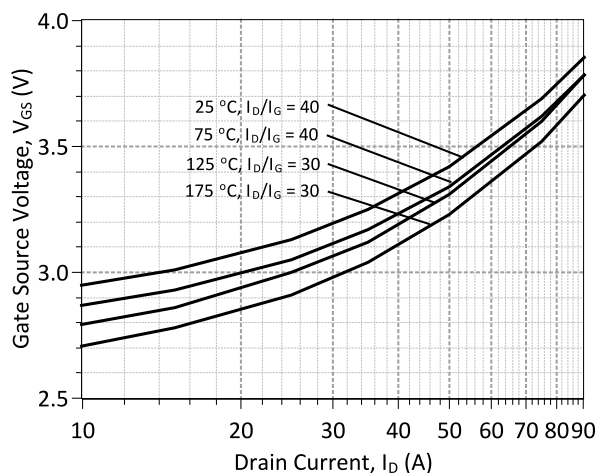


Figure 7: Typical Gate – Source Saturation Voltage

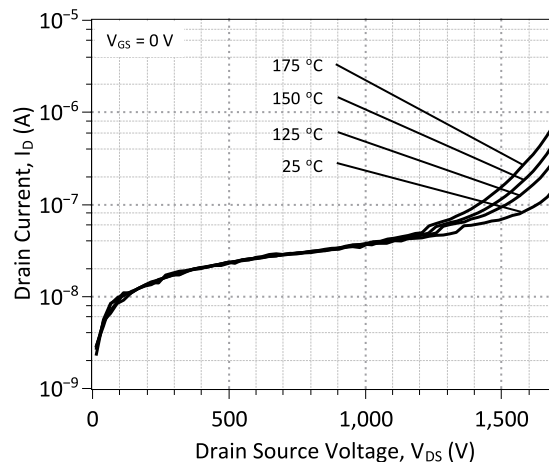


Figure 8: Typical Blocking Characteristics

B: Dynamic Characteristics

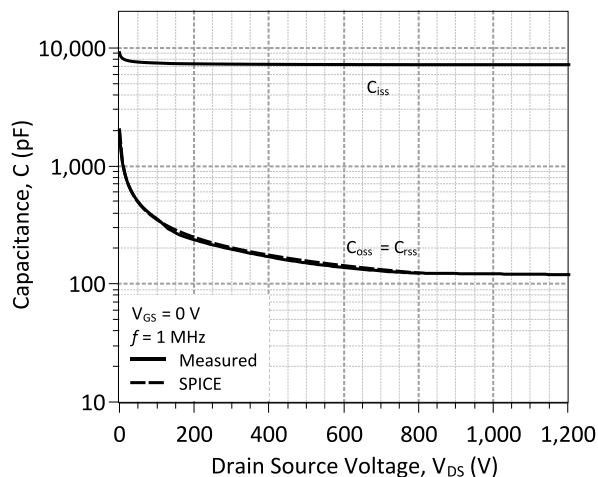


Figure 9: Input, Output, and Reverse Transfer Capacitance

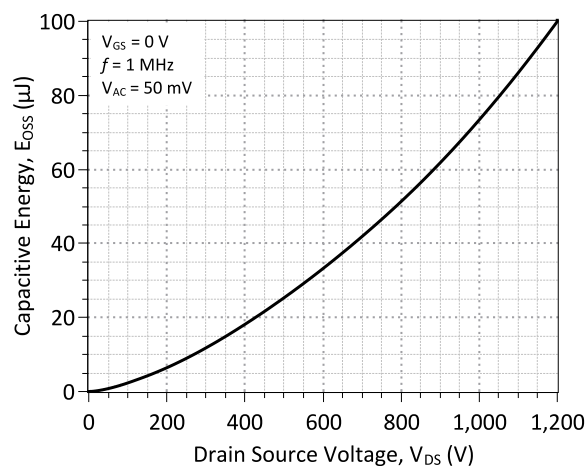


Figure 10: Energy Stored in Output Capacitance

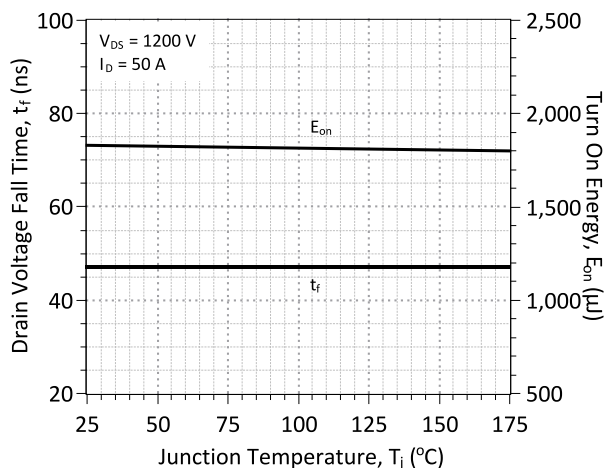


Figure 11: Typical Switching Times and Turn On Energy Losses vs. Temperature

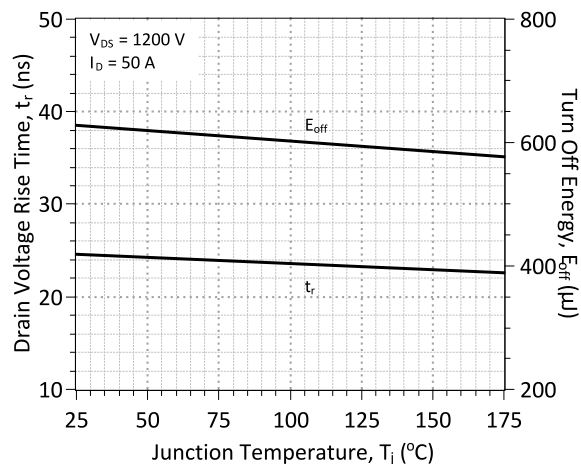


Figure 12: Typical Switching Times and Turn Off Energy Losses vs. Temperature

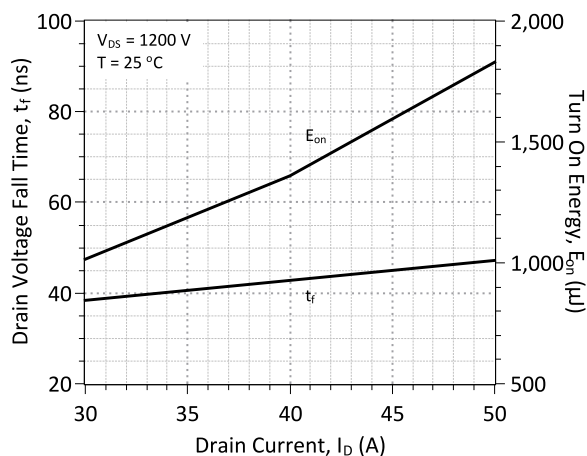


Figure 13: Typical Switching Times and Turn On Energy Losses vs. Drain Current

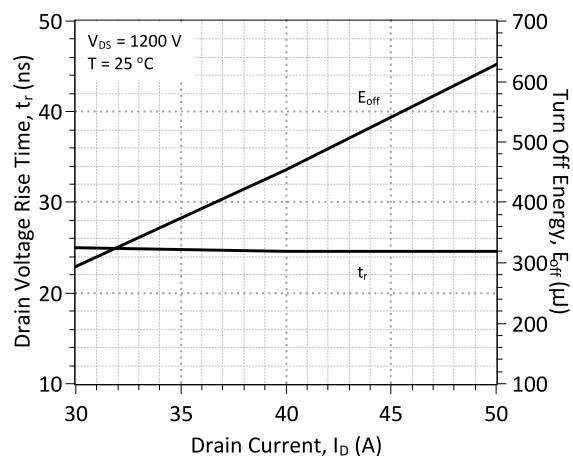


Figure 14: Typical Switching Times and Turn Off Energy Losses vs. Drain Current

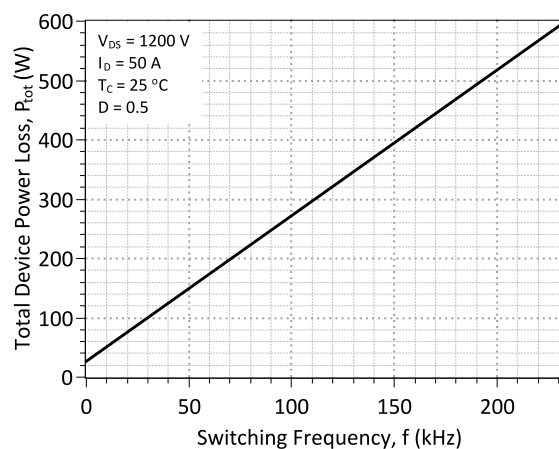


Figure 15: Typical Hard Switched Device Power Loss vs. Switching Frequency²

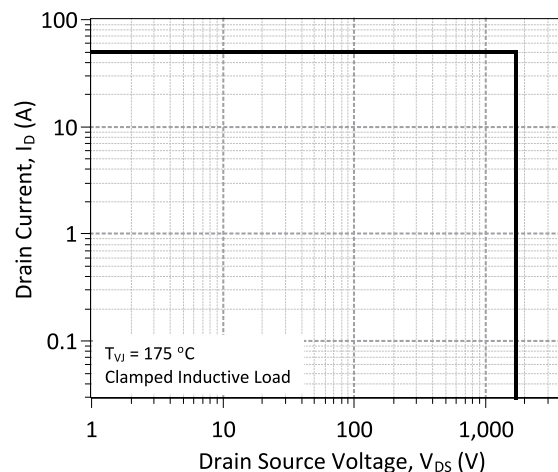


Figure 16: Turn-Off Safe Operating Area

² – Representative values based on device conduction and switching loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

Section V: Driving the GA50JT17-CAL

Drive Topology	Gate Drive Power Consumption	Switching Frequency	Application Emphasis	Availability
TTL Logic	High	Low	Wide Temperature Range	Coming Soon
Constant Current	Medium	Medium	Wide Temperature Range	Coming Soon
High Speed – Boost Capacitor	Medium	High	Fast Switching	Production
High Speed – Boost Inductor	Low	High	Ultra Fast Switching	Coming Soon
Proportional	Lowest	High	Wide Drain Current Range	Coming Soon
Pulsed Power	Medium	N/A	Pulse Power	Coming Soon

A: Static TTL Logic Driving

The GA50JT17-CAL may be driven using direct (5 V) TTL logic after current amplification. The (amplified) current level of the supply must meet or exceed the steady state gate current ($I_{G,steady}$) required to operate the GA50JT17-CAL. The power level of the supply can be estimated from the target duty cycle of the particular application. $I_{G,steady}$ is dependent on the anticipated drain current I_D through the SJT and the DC current gain h_{FE} , it may be calculated from the following equation. An accurate value of the h_{FE} may be read from Figure 6.

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

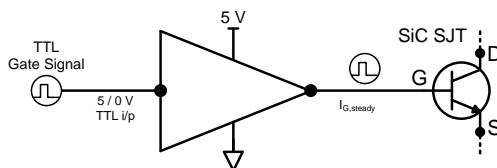


Figure 17: TTL Gate Drive Schematic

B: High Speed Driving

The SJT is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 18 which features a positive current peak during turn-on, a negative current peak during turn-off, and continuous gate current to remain on.

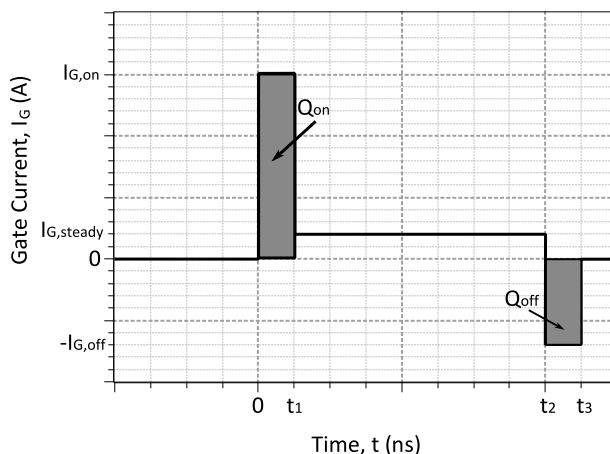


Figure 18: An idealized gate current waveform for fast switching of an SJT.

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G , for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS} , and gate-drain capacitance, C_{GD} , are fully charged.

$$Q_{on} = I_{G,on} * t_1$$

$$Q_{on} \geq Q_{gs} + Q_{gd}$$

Ideally, $I_{G,pon}$ should terminate when the drain voltage falls to its on-state value in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the device package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The voltage applied to the gate pin should be maintained high enough, above the $V_{GS,sat}$ (see Figure 7) level to counter these effects.

A high negative peak current, $-I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with $V_{GS} = 0$ V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

Two high-speed drive topologies for the SiC SGTs are presented below.

B:1: High Speed, Low Loss Drive with Boost Capacitor, GA15IDDJT22-FR4

The GA50JT17-CAL may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide fast switching current peaks at turn-on and turn-off and a continuous gate current while in on-state. An evaluation gate drive board (GA15IDDJT22-FR4) utilizing this topology is commercially available for low-side driving, its datasheet provides additional details.

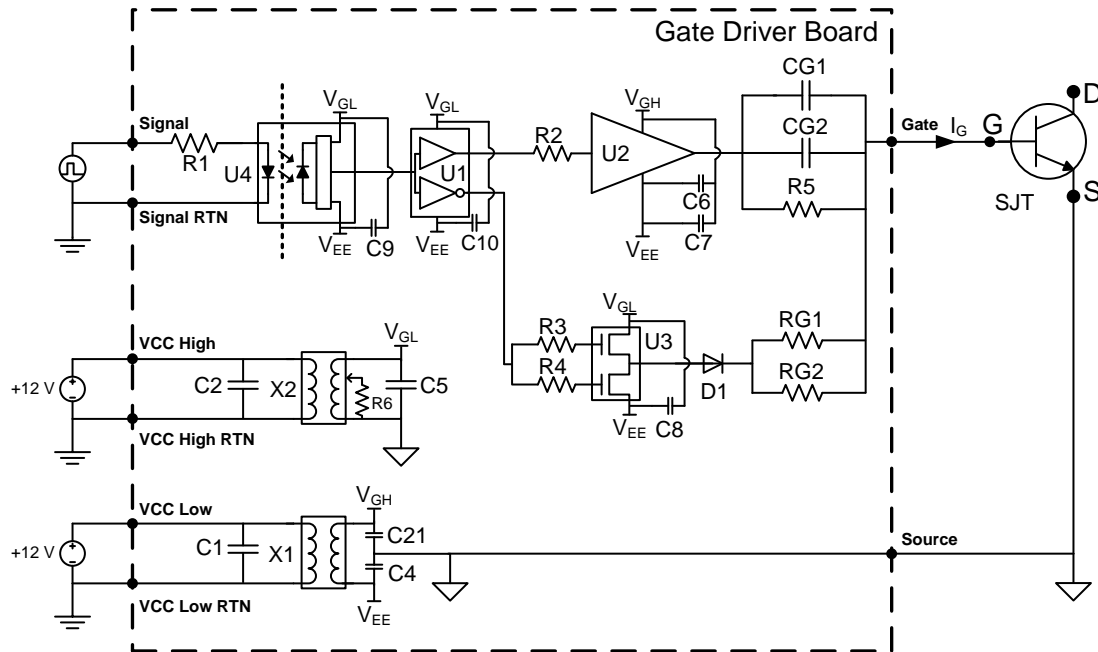


Figure 19: Topology of the GA03IDDJT30-FR4 Two Voltage Source gate driver.

The GA15IDDJT22-FR4 evaluation board comes equipped with two on board gate drive resistors (RG1, RG2) pre-installed for an effective gate resistance³ of $R_G = 0.7 \Omega$. It may be necessary for the user to reduce RG1 and RG2 under high drain current conditions for safe operation of the GA50JT17-CAL. The steady state current supplied to the gate pin of the GA50JT17-CAL with on-board $R_G = 0.7 \Omega$, is shown in **Error! Reference source not found..** The maximum allowable safe value of R_G for the user's required drain current can be read from **Error! Reference source not found..**

For the GA50JT17-CAL, R_G must be reduced for $I_D \geq \sim 60$ A for safe operation with the GA15IDDJT22-FR4.

For operation at $I_D \geq \sim 60$ A, R_G may be calculated from the following equation, which contains the DC current gain h_{FE} (Figure 6) and the gate-source saturation voltage $V_{GS,sat}$ (**Error! Reference source not found.**).

$$R_{G,max} = \frac{(4.7V - V_{GS,sat}) * h_{FE}(T, I_D)}{I_D * 1.5} - 0.1\Omega$$

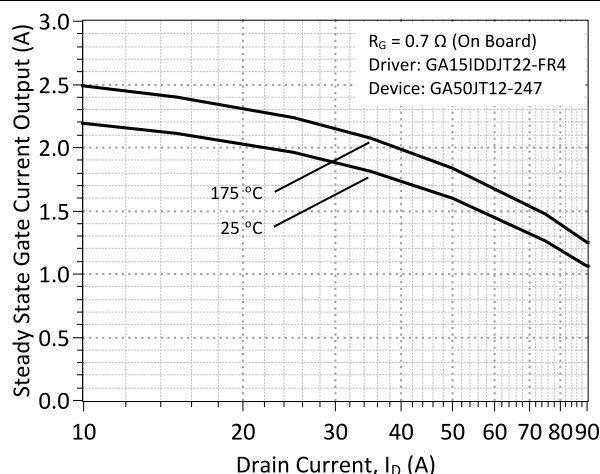


Figure 20: Typical steady state gate current supplied by the GA15IDDJT22-FR4 board for the GA50JT17-CAL with the on board resistance of 0.7 Ω

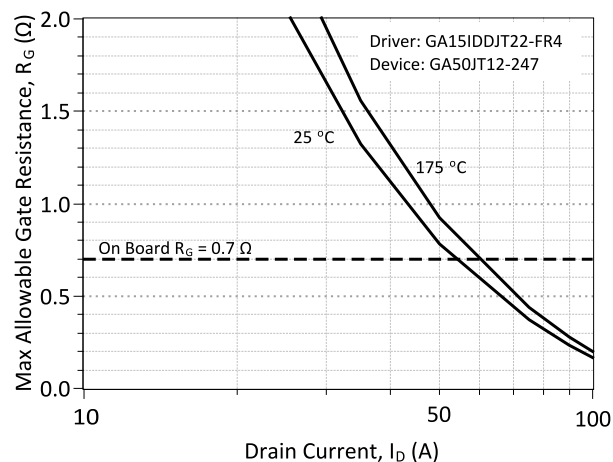


Figure 21: Maximum gate resistance for safe operation of the GA50JT17-CAL at different drain currents using the GA15IDDJT22-FR4 board.

B:2: High Speed, Low Loss Drive with Boost Inductor

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the GA50JT17-CAL at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses $I_{G,on}$ and $I_{G,off}$. During operation, inductor L is charged to a specified $I_{G,on}$ current value then made to discharge I_L into the SiC gate pin using logic control of S_1 , S_2 , S_3 , and S_4 , as shown in Figure 22. After turn on, while the device remains on the necessary steady state gate current $I_{G,steady}$ is supplied from source V_{CC} through R_G . Please refer to the article "A current-source concept for fast and efficient driving of silicon carbide transistors" by Dr. Jacek Rąbkowski for additional information on this driving topology.⁴

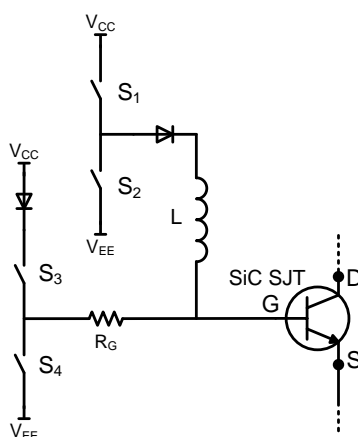


Figure 22: Simplified Inductive Pulsed Drive Topology

³ – $R_G = (1/R_{G1} + 1/R_{G2})^{-1}$. Driver is pre-installed with $R_{G1} = R_{G2} = 7.5 \Omega$

⁴ – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/ae-2013-0026, June 2013

C: Proportional Gate Current Driving

For applications in which the GA50JT17-CAL will operate over a wide range of drain current conditions, it may be beneficial to drive the device using a proportional gate drive topology to optimize gate drive power consumption. A proportional gate driver relies on instantaneous drain current I_D feedback to vary the steady state gate current $I_{G,steady}$ supplied to the GA50JT17-CAL.

C:1: Voltage Controlled Proportional Driver

The voltage controlled proportional driver relies on a gate drive IC to detect the GA50JT17-CAL drain-source voltage V_{DS} during on-state to sense I_D . The gate drive IC will then increase or decrease $I_{G,steady}$ in response to I_D . This allows $I_{G,steady}$, and thus the gate drive power consumption, to be reduced while I_D is relatively low or for $I_{G,steady}$ to increase when I_D is higher. A high voltage diode connected between the drain and sense protects the IC from high-voltage when the driver and GA50JT17-CAL are in off-state. A simplified version of this topology is shown in Figure 23, additional information will be available in the future at <http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/>

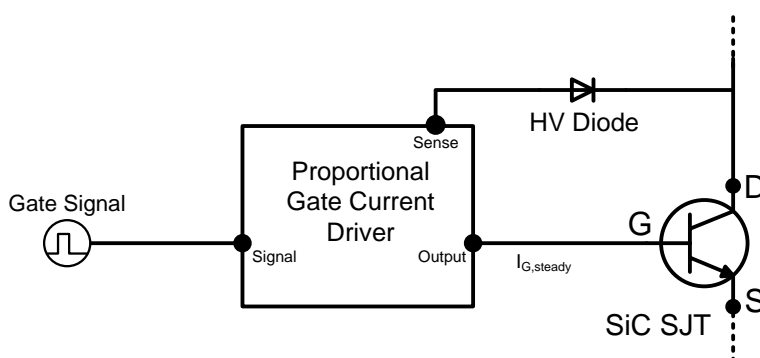


Figure 23: Simplified Voltage Controlled Proportional Driver

C:2: Current Controlled Proportional Driver

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback I_D of the GA50JT17-CAL during on-state to supply $I_{G,steady}$ into the device gate. $I_{G,steady}$ will then increase or decrease in response to I_D at a fixed forced current gain which is set by the turns ratio of the transformer, $h_{force} = I_D / I_G = N_2 / N_1$. GA50JT17-CAL is initially tuned-on using a gate current pulse supplied into an RC drive circuit to allow I_D current to begin flowing. This topology allows $I_{G,steady}$, and thus the gate drive power consumption, to be reduced while I_D is relatively low or for $I_{G,steady}$ to increase when I_D is higher. A simplified version of this topology is shown in Figure 24, additional information will be available in the future at <http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/>.

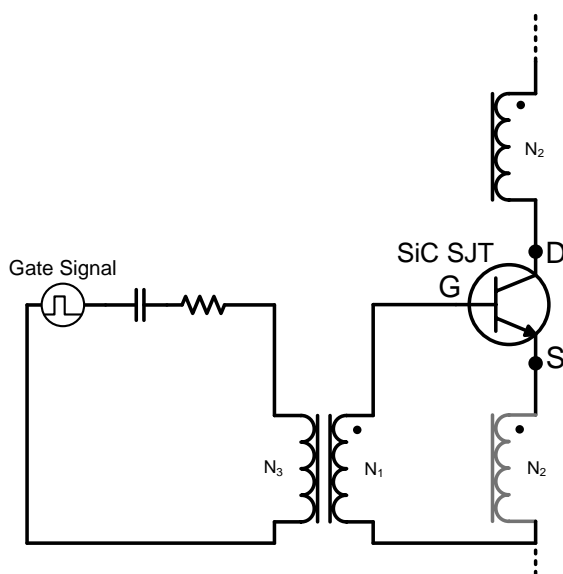
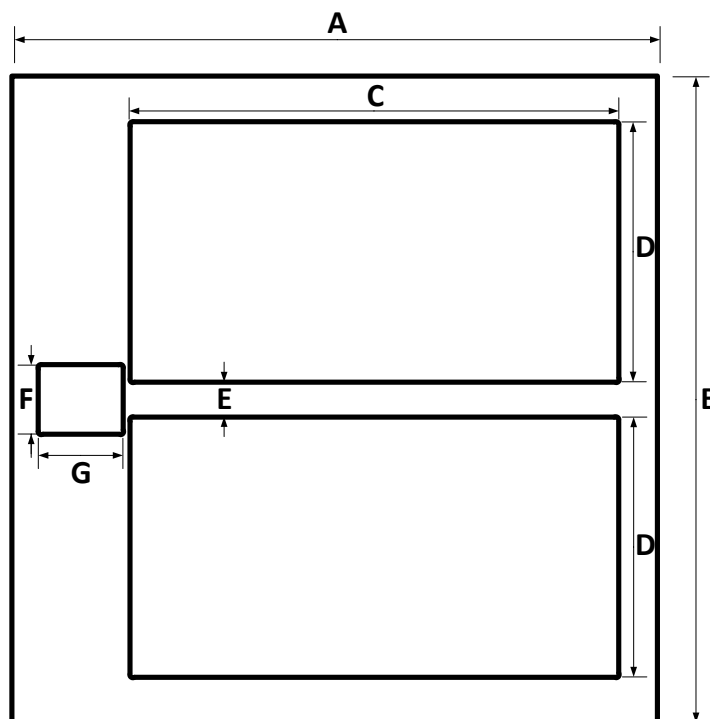


Figure 24: Simplified Current Controlled Proportional Driver

Section VI: Mechanical Parameters

Die Dimensions	4.35 x 4.35	mm ²	171 x 171	mil ²
Die Area total / active	18.92/16.56	mm ²	29330/25677	mil ²
Die Thickness	360	μm	14	mil
Wafer Size	100	mm	3937	mil
Flat Position	0	deg	0	deg
Die Frontside Passivation	Polyimide			
Gate/Source Pad Metallization	4000 nm Al			
Bottom Drain Pad Metallization	400 nm Ni + 200 nm Au			
Die Attach	Electrically conductive glue or solder			
Wire Bond	Al ≤ 12 mil (Source) Al ≤ 5 mil (Gate)			
Reject ink dot size	Φ ≥ 0.3 mm			
Recommended storage environment	Store in original container, in dry nitrogen, < 6 months at an ambient temperature of 23 °C			

Section VII: Chip Dimensions


		mm	mil
DIE	A	4.35	171
	B	4.35	171
SOURCE WIREBONDABLE	C	3.30	130
	D	1.75	69
	E	0.24	9
GATE WIREBONDABLE	F	0.46	18
	G	0.57	22

Revision History

Date	Revision	Comments	Supersedes
2016/02/26	2	Updated Electrical Characteristics	
2015/02/06	1	Updated Electrical Characteristics	
2014/07/14	0	Initial release	

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Section VIII: SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/hit_sic/baredie/sjt/GA50JT17-CAL_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA50JT17-CAL.

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*
*      $Revision:   2.2                $
*      $Date:      29-JAN-2015        $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*
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*      TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
.model GA50JT17 NPN
+ IS      9.833E-48
+ ISE     1.073E-26
+ EG      3.23
+ BF      89
+ BR      0.55
+ IKF     9000
+ NF      1
+ NE      2
+ RB      0.95
+ IRB     0.005
+ RBM     0.073
+ RE      0.004
+ RC      0.0125
+ CJC     2.124E-9
+ VJC     3.788
+ MJC     0.537
+ CJE     6.026E-09
+ VJE     3.1791
+ MJE     0.5295
+ XTI     3
+ XTB     -1.5
+ TRC1    9.00E-3
+ VCEO    1700
+ ICRATING 50
+ MFG     GeneSiC_Semiconductor
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*      End of GA50JT17 SPICE Model
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