NGTG50N60FWG

IGBT

This Insulated Gate Bipolar Transistor (IGBT) features a robust and cost effective Trench construction, and provides superior performance in demanding switching applications, offering both low on state voltage and minimal switching loss.

Features
- Optimized for Very Low V_{CEsat}
- Low Switching Loss Reduces System Power Dissipation
- 5 μs Short−Circuit Capability
- These are Pb−Free Devices

Typical Applications
- Solar Inverters
- Uninterruptible Power Supples (UPS)
- Motor Drives

ABSOLUTE MAXIMUM RATINGS

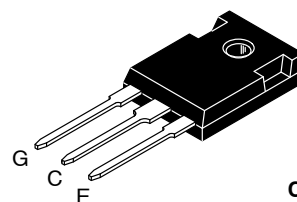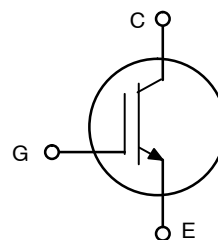| Rating	Symbol	Value	Unit
Collector−emitter voltage	V_{CES}	600	V
Collector current @ T_C = 25°C @ T_C = 100°C	I_C	 100 50	A
Pulsed collector current, T_{pulse} limited by T_{Jmax}	I_{CM}	200	A
Short−circuit withstand time V_{GE} = 15 V, V_{CE} = 300 V, $T_J \leq$ +150°C	t_{SC}	5	μs
Gate−emitter voltage Transient Gate−Emitter Voltage	V_{GE}	±20 ±30	V
Power Dissipation @ T_C = 25°C @ T_C = 100°C	P_D	 223 89	W
Operating junction temperature range	T_J	−55 to +150	°C
Storage temperature range	T_{stg}	−55 to +150	°C
Lead temperature for soldering, 1/8" from case for 5 seconds	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

50 A, 600 V
V_{CEsat} = 1.50 V

TO−247
CASE 340L
STYLE 4

MARKING DIAGRAM

G50N60F
AYWWG

A   = Assembly Location
Y   = Year
WW = Work Week
G   = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
NGTG50N60FWG	TO−247 (Pb−Free)	30 Units / Rail

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal resistance junction–to–case, for IGBT	$R_{\theta JC}$	0.56	°C/W
Thermal resistance junction–to–ambient	$R_{\theta JA}$	40	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTIC						
Collector–emitter breakdown voltage, gate–emitter short–circuited	V_{GE} = 0 V, I_C = 500 μA	$V_{(BR)CES}$	600	–	–	V
Collector–emitter saturation voltage	V_{GE} = 15 V, I_C = 50 A V_{GE} = 15 V, I_C = 50 A, T_J = 150°C	V_{CEsat}	1.25 –	1.45 1.7	1.7 –	V
Gate–emitter threshold voltage	V_{GE} = V_{CE}, I_C = 350 μA	$V_{GE(th)}$	4.5	5.5	6.5	V
Collector–emitter cut–off current, gate–emitter short–circuited	V_{GE} = 0 V, V_{CE} = 600 V V_{GE} = 0 V, V_{CE} = 600 V, T_J = 150°C	I_{CES}	– –	– –	0.5 2	mA
Gate leakage current, collector–emitter short–circuited	V_{GE} = 20 V , V_{CE} = 0 V	I_{GES}	–	–	200	nA
DYNAMIC CHARACTERISTIC						
Input capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 1 MHz	C_{ies}	–	7300	–	pF
Output capacitance		C_{oes}	–	195	–	
Reverse transfer capacitance		C_{res}	–	170	–	
Gate charge total	V_{CE} = 480 V, I_C = 50 A, V_{GE} = 15 V	Q_g	–	310	–	nC
Gate to emitter charge		Q_{ge}	–	60	–	
Gate to collector charge		Q_{gc}	–	150	–	
SWITCHING CHARACTERISTIC, INDUCTIVE LOAD						
Turn–on delay time	T_J = 25°C V_{CC} = 400 V, I_C = 50 A R_g = 10 Ω V_{GE} = 0 V/ 15 V*	$t_{d(on)}$	–	117	–	ns
Rise time		t_r	–	43	–	
Turn–off delay time		$t_{d(off)}$	–	285	–	
Fall time		t_f	–	105	–	
Turn–on switching loss		E_{on}	–	1.1	–	mJ
Turn–off switching loss		E_{off}	–	1.2	–	
Total switching loss		E_{ts}	–	2.3	–	
Turn–on delay time	T_J = 150°C V_{CC} = 400 V, I_C = 50 A R_g = 10 Ω V_{GE} = 0 V/ 15 V*	$t_{d(on)}$	–	112	–	ns
Rise time		t_r	–	45	–	
Turn–off delay time		$t_{d(off)}$	–	300	–	
Fall time		t_f	–	214	–	
Turn–on switching loss		E_{on}	–	1.4	–	mJ
Turn–off switching loss		E_{off}	–	2.0	–	
Total switching loss		E_{ts}	–	3.4	–	

*Includes diode reverse recovery loss using NGTB50N60FWG.
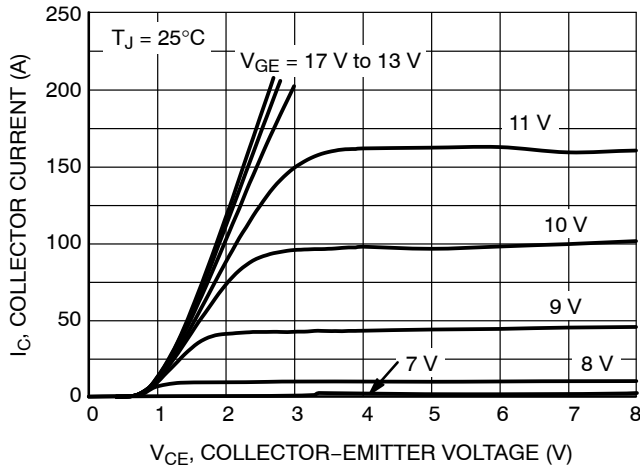
NGTG50N60FWG

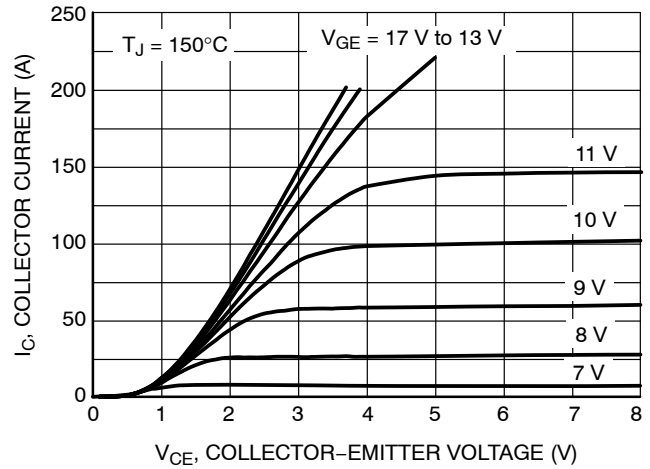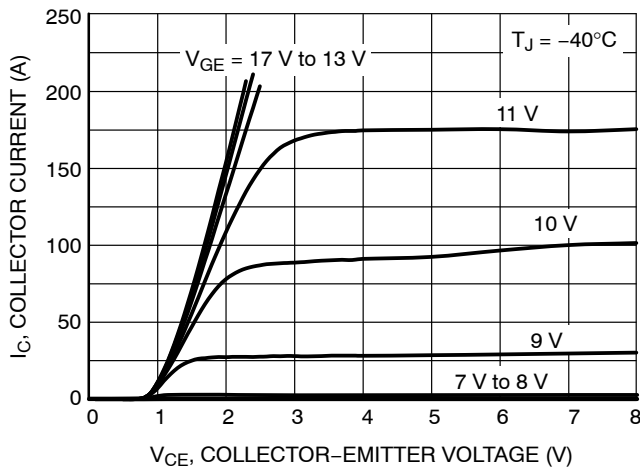## TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

$T_J = 25°C$, V_{GE} = 17 V to 13 V, 11 V, 10 V, 9 V, 8 V, 7 V

I_C, COLLECTOR CURRENT (A) vs V_{CE}, COLLECTOR–EMITTER VOLTAGE (V)

Figure 2. Output Characteristics

$T_J = 150°C$, V_{GE} = 17 V to 13 V, 11 V, 10 V, 9 V, 8 V, 7 V

I_C, COLLECTOR CURRENT (A) vs V_{CE}, COLLECTOR–EMITTER VOLTAGE (V)

Figure 3. Output Characteristics

V_{GE} = 17 V to 13 V, $T_J = -40°C$, 11 V, 10 V, 9 V, 7 V to 8 V

I_C, COLLECTOR CURRENT (A) vs V_{CE}, COLLECTOR–EMITTER VOLTAGE (V)
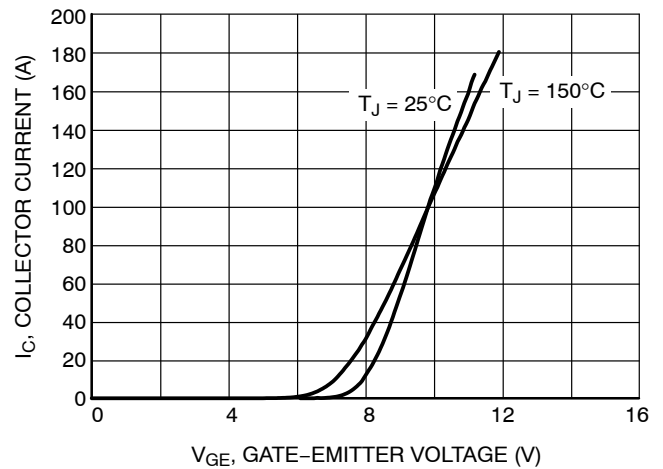
Figure 4. Typical Transfer Characteristics

$T_J = 25°C$, $T_J = 150°C$

I_C, COLLECTOR CURRENT (A) vs V_{GE}, GATE–EMITTER VOLTAGE (V)

Figure 5. $V_{CE(sat)}$ vs. T_J

I_C = 100 A, I_C = 50 A, I_C = 10 A, I_C = 5 A

V_{CE}, COLLECTOR–EMITTER VOLTAGE (V) vs T_J, JUNCTION TEMPERATURE (°C)
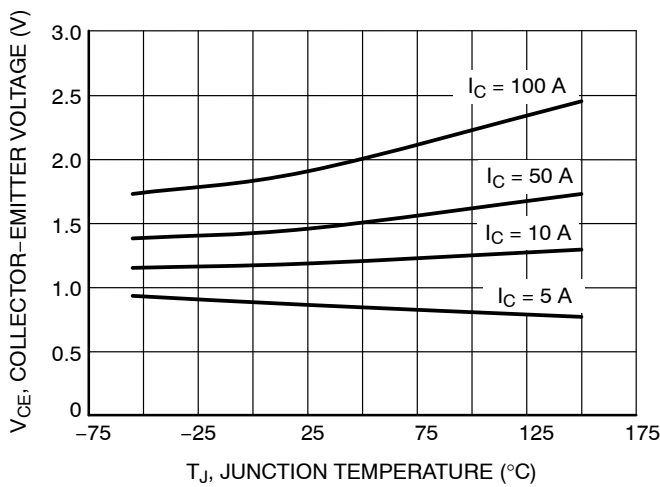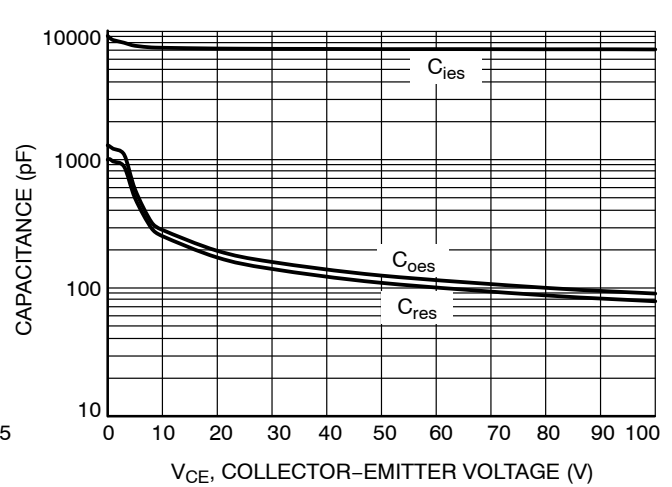
Figure 6. Typical Capacitance

C_{ies}, C_{oes}, C_{res}

CAPACITANCE (pF) vs V_{CE}, COLLECTOR–EMITTER VOLTAGE (V)

NGTG50N60FWG

TYPICAL CHARACTERISTICS
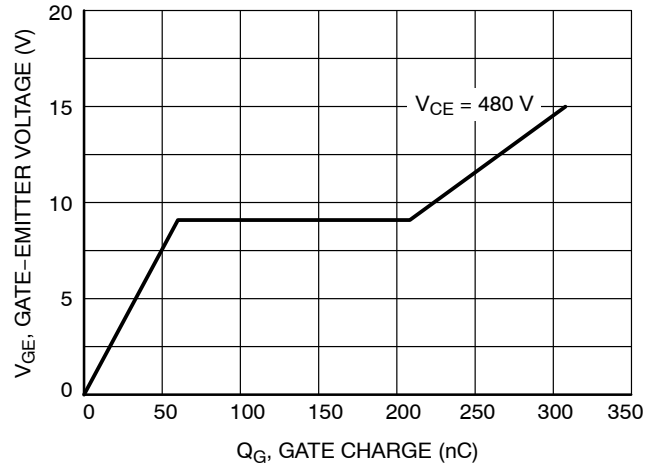
Figure 7. Typical Gate Charge
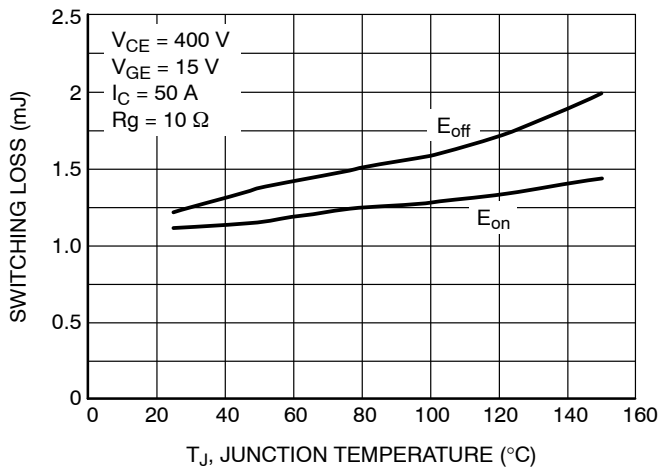
Figure 8. Switching Loss vs. Temperature
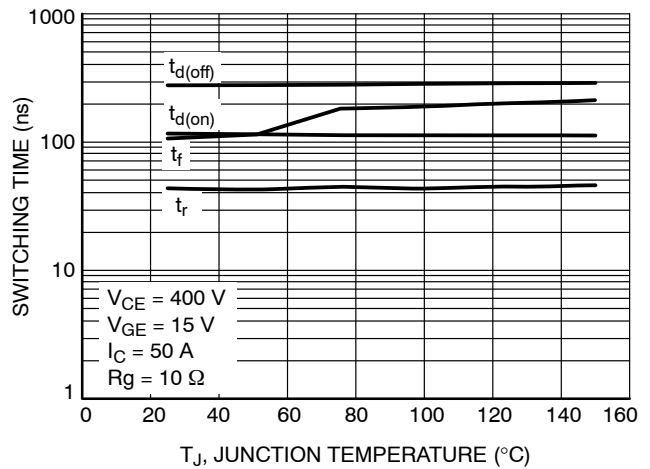
Figure 9. Switching Time vs. Temperature
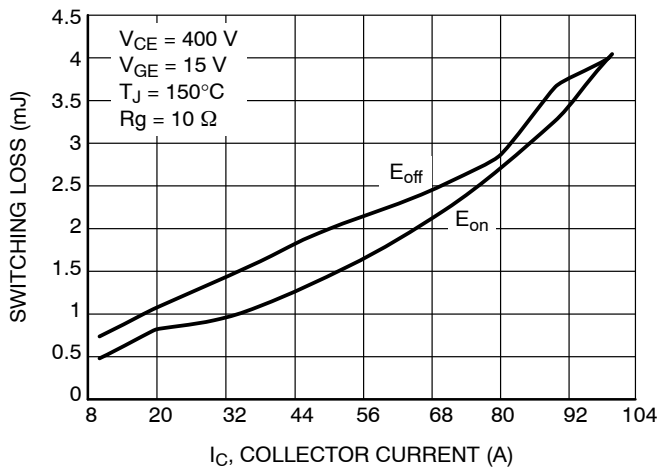
Figure 10. Switching Loss vs. I_C
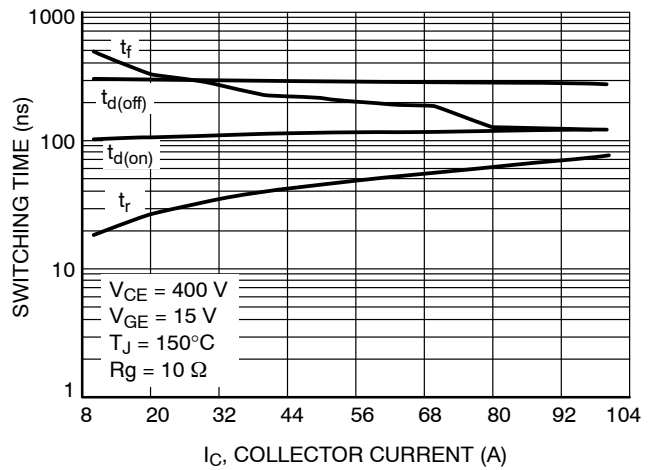
Figure 11. Switching Time vs. I_C

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TYPICAL CHARACTERISTICS
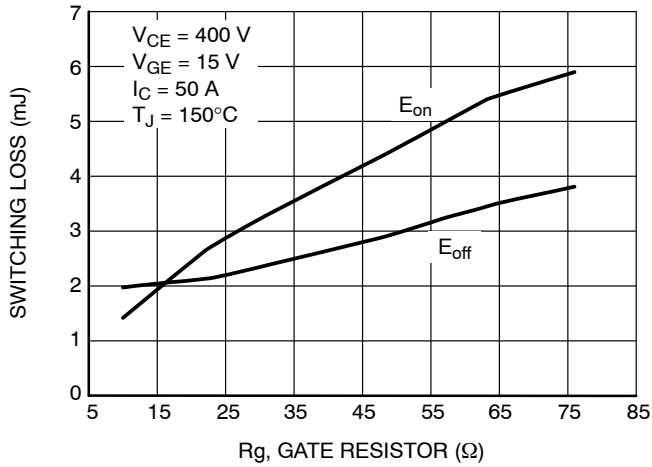
Figure 12. Switching Loss vs. Rg
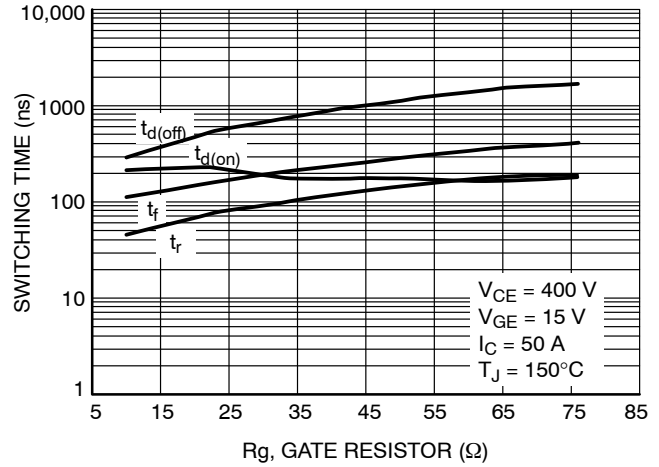
Figure 13. Switching Time vs. Rg
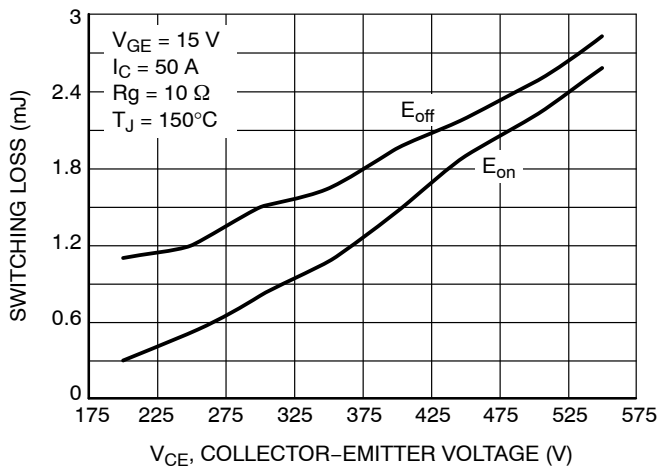
Figure 14. Switching Loss vs. V_{CE}
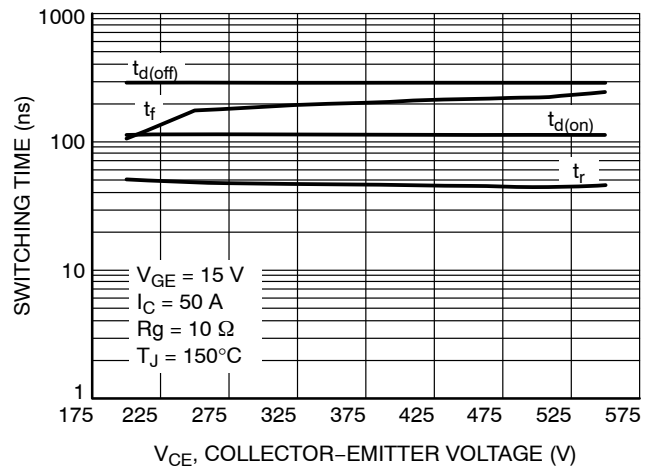
Figure 15. Switching Time vs. V_{CE}
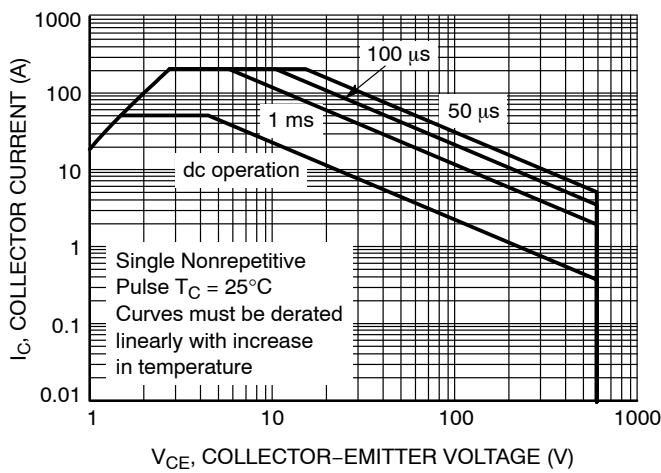
Figure 16. Safe Operating Area
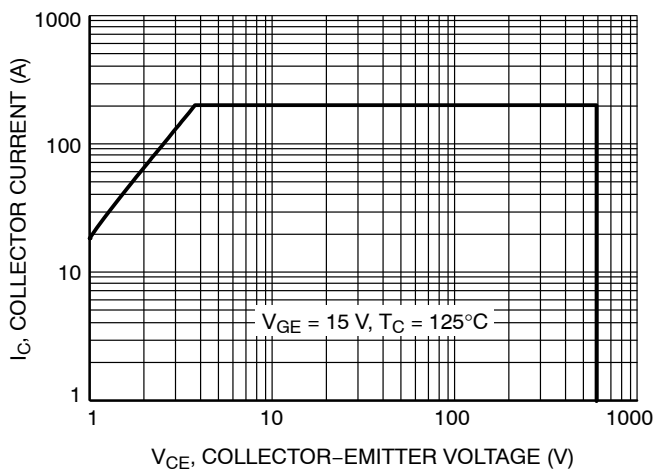
Figure 17. Reverse Bias Safe Operating Area

NGTG50N60FWG

TYPICAL CHARACTERISTICS

R_i (°C/W)	τ_i (sec)
0.02087	1.0E−4
0.05041	6.84E−5
0.07919	0.002
0.11425	0.03
0.19393	0.1
0.09951	2.0

50% Duty Cycle
20%
10%
5%
2%
1%
Single Pulse

$R_{\theta JC} = 0.56$

Junction R_1 R_2 R_n Case

$C_i = \tau_i / R_i$

C_1 C_2 C_n

Duty Factor = t_1/t_2
Peak $T_J = P_{DM} \times Z_{\theta JC} + T_C$
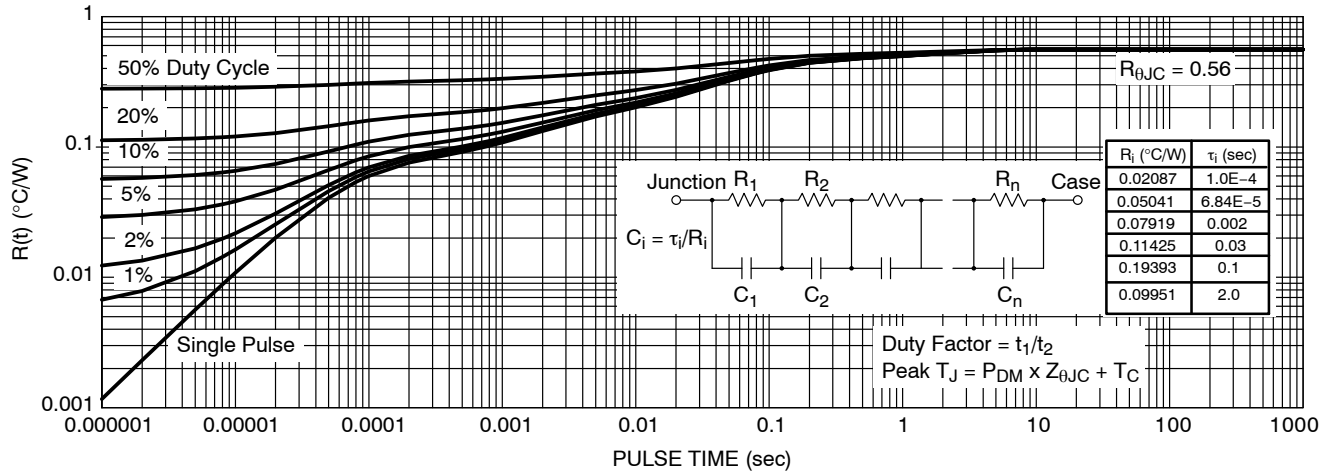
Figure 18. IGBT Transient Thermal Impedance
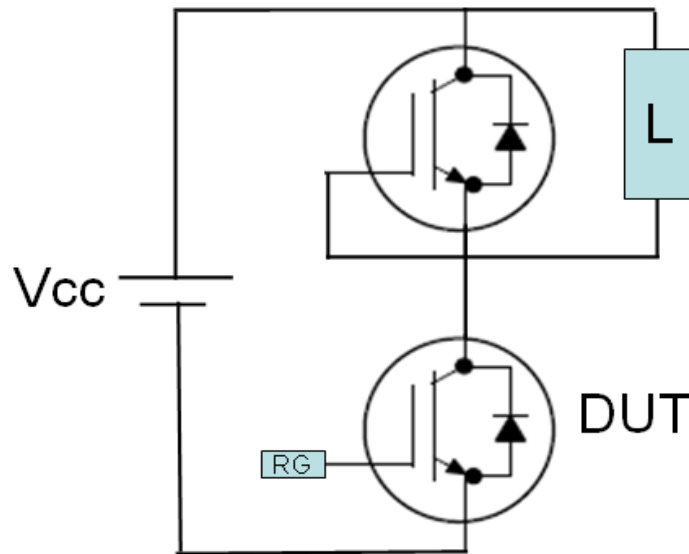
Figure 19. Test Circuit for Switching Characteristics
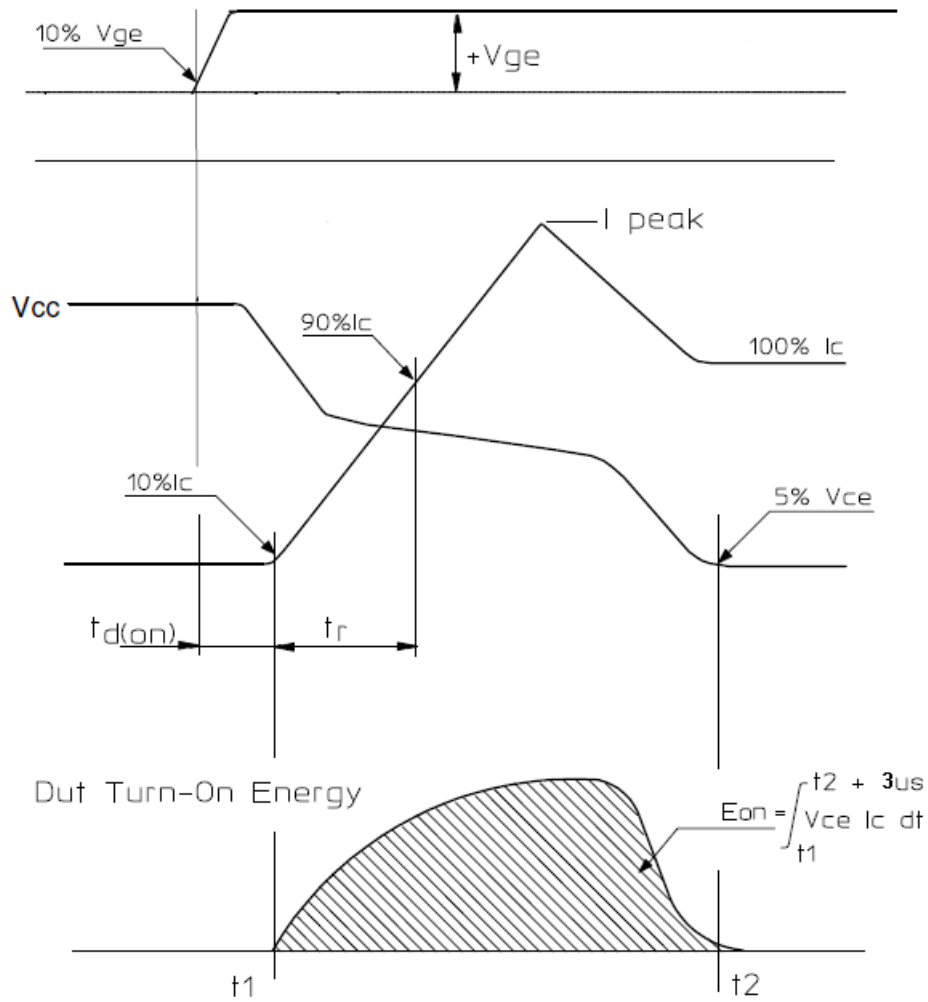
Figure 20. Definition of Turn On Waveform
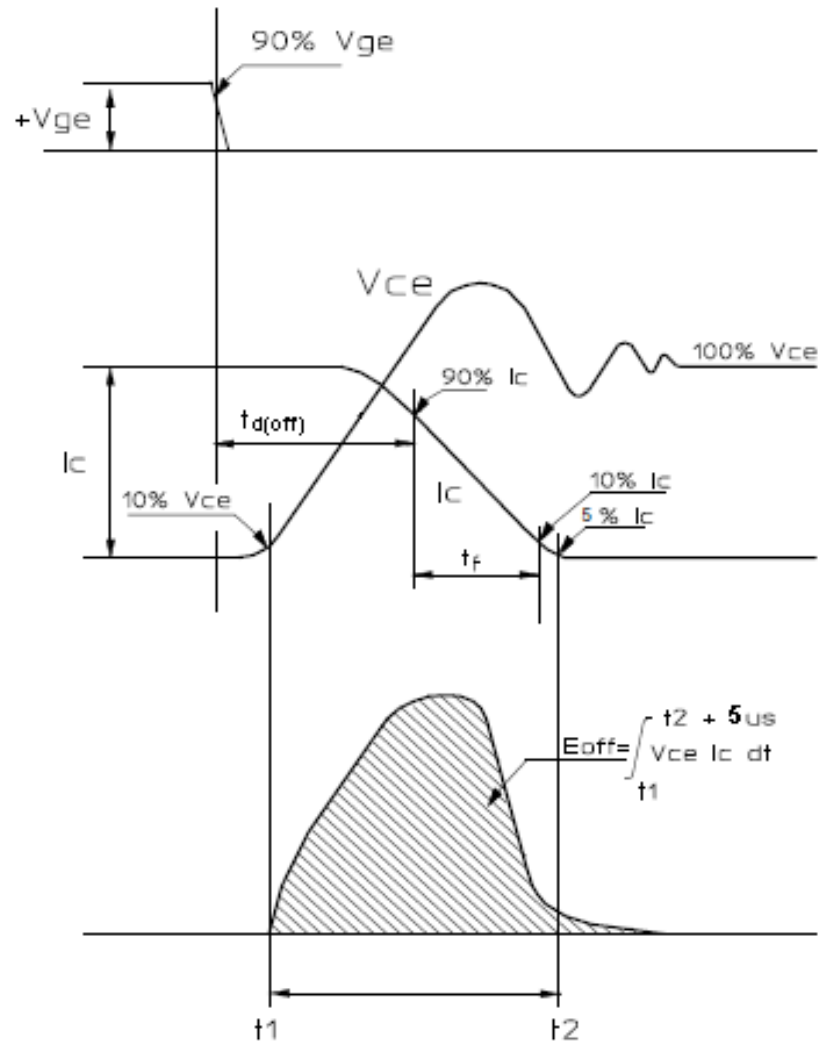
Figure 21. Definition of Turn Off Waveform

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®
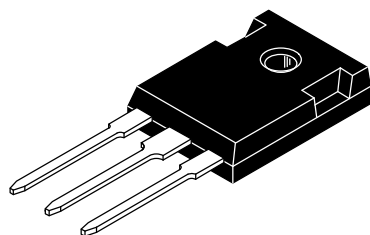
TO−247
CASE 340L−02
ISSUE F

DATE 26 OCT 2011
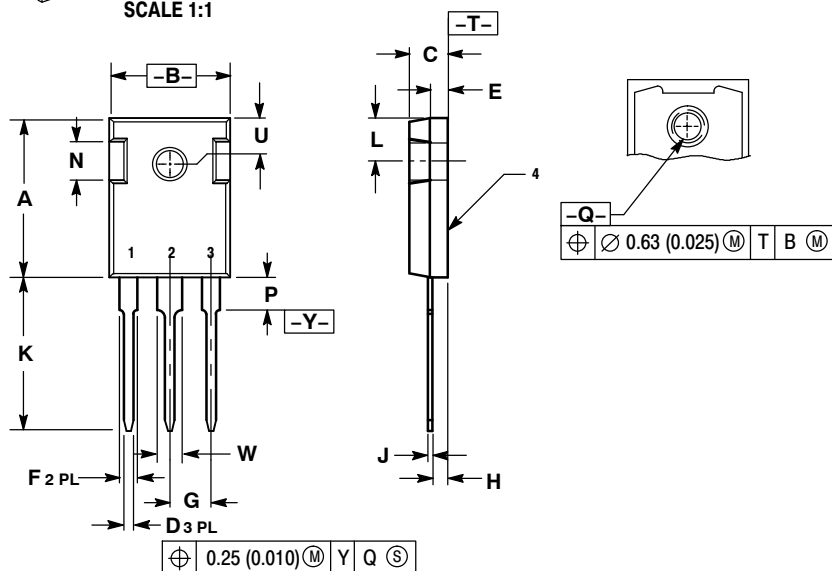
SCALE 1:1

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	8.30
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

⊕ | ∅ 0.63 (0.025) Ⓜ | T | B Ⓜ

⊕ | 0.25 (0.010) Ⓜ | Y | Q Ⓢ

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

GENERIC
MARKING DIAGRAM*
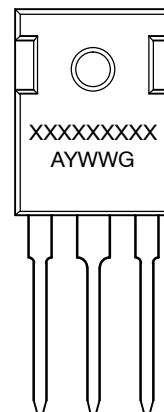
XXXXXXXXX
AYWWG

XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present.

DOCUMENT NUMBER:	98ASB15080C	
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO−247	PAGE 1 OF 2

ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80–21.46/0.819–0.845. DIM K WAS 19.81–20.32/0.780–0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

PUBLICATION ORDERING INFORMATION

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