

Dual JK-Master-Slave Flipflop with Set and Reset

FZJ 121
FZJ 125

Type	order numbers
FZJ 121	Q 67000-J 385
FZJ 125	Q 67000-J 386

Electrical characteristics

12 V-range

temperature range 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage at C	V_{IH}	$V_S = V_{SB}$	22	8.0			V
L-input voltage at C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.0	V
H-input voltage at J and K	V_{IH}	$V_S = V_{SB}$	22	8.0			V
L-input voltage at J and K	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			5.5	V
H-input voltage at $\bar{R}$ and $\bar{S}$	V_{IH}	$V_S = V_{SB}$	22	7.5			V
L-input voltage at $\bar{R}$ and $\bar{S}$	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $V_{IL} = 4.5 \text{ V}^1)$ $-I_{QL} = 0.1 \text{ mA}$	22	10.0	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $V_{IH} = 7.5 \text{ V}^1)$ $I_{QL} = 15 \text{ mA}$	22		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			2.0	5.0		V
L-signal	V_{nm}			2.3	5.0		V
H-input current at C	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	23			3.0	μA
H-input current at J, K, $\bar{R}$ and $\bar{S}$	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	23			1.0	μA
L-input current at C	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7 \text{ V}$	24		1.6	3.0	mA
L-input current at J, K, $\bar{R}$ and $\bar{S}$	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7 \text{ V}$	24		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$ $V_Q = 0 \text{ V}$	25	9.0	15.0	25.0	mA
Supply current	I_S	$V_S = V_{SA}$ $V_I = V_{IHA}$	23		15.0	24.0	mA

¹⁾ V_I applied to $\bar{R}$ and $\bar{S}$ resp.

Dual JK-Master-Slave Flipflop with Set and Reset

FZJ 121
FZJ 125

Delay times, $V_S=12\text{ V}$, $F_Q=1$, $T_A=25\text{ °C}$

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Maximum clock frequency f		duty cycle 1:1		0.2	0.5		MHz
Clock pulse duration	t_{pC}			0.6			s
Reset pulse duration	t_{pR}			1.0			s
Set pulse duration	t_{pS}	at 50%		1.0			s
Setup time	t_S			0			ns
Hold time	t_H			0			ns
Propagation delay from C to Q	t_{PLH}		31	160	290	520	ns
	t_{PHL}	$C_L=10\text{ pF}$ at 4.5 V	31	270	450	770	ns
from $\bar{R}$ or $\bar{S}$ to Q	t_{PLH}	above ground	30	70	165	330	ns
	t_{PHL}		30	180	330	580	ns
Transition time at Q	t_{TLH}	$C_L=10\text{ pF}$	31	200	340	570	ns
	t_{THL}		31	70	120	210	ns

Dual JK-Master-Slave Flipflop with Set and Reset

FZJ 121
FZJ 125

Electrical characteristics

15 V-range

temperature range 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage at C	V_{IH}	$V_S = V_{SB}$	22	8.0			V
L-input voltage at C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.0	V
H-input voltage at J and K	V_{IH}	$V_S = V_{SB}$	22	8.0			V
L-input voltage at J and K	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			5.5	V
H-input voltage at $\bar{R}$ and $\bar{S}$	V_{IH}	$V_S = V_{SB}$	22	7.5			V
L-input voltage at $\bar{R}$ and $\bar{S}$	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $V_{IL} = 4.5$ V ¹⁾ $-I_{QL} = 0.1$ mA	22	12.0	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $V_{IH} = 7.5$ V ¹⁾ $I_{QL} = 18$ mA	22		1.1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.0	8.0		V
L-signal	V_{nm}			2.3	5.0		V
H-input current at C	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	23			3.0	μ A
H-input current at J, K, $\bar{R}$ and $\bar{S}$	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	23			1.0	μ A
L-input current at C	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	24		2.0	3.6	mA
L-input current at J, K, $\bar{R}$ and $\bar{S}$	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	24		1.0	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$ $V_O = 0$ V	25	9.0	15.0	25.0	mA
Supply current	I_S	$V_S = V_{SA}$ $V_I = V_{IHA}$	23		20.0	32.0	mA

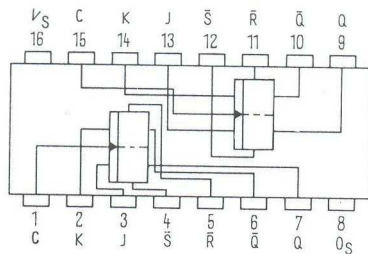
Delay times, $V_S = 15$ V, $F_Q = 1$, $T_A = 25$ °C

Propagation delay					
from C to Q	t_{PLH}	$C_L=10\text{ pF at }4.5\text{ V}$	31	330	ns
	t_{PHL}		31	470	ns
from $\bar{R}$ or $\bar{S}$ to Q	t_{PLH}	above ground	30	195	ns
	t_{PHL}		30	340	ns
Transition time	t_{TLH}	$C_L=10\text{ pF}$	31	410	ns
at Q	t_{THL}		31	75	ns

¹⁾ V_I applied to $\bar{R}$ and $\bar{S}$ resp.

Dual JK-Master-Slave Flipflop with Set and Reset

FZJ 121
FZJ 125



Pin configuration
top view
C = clock
J, K = input
Q, $\bar{Q}$ = outputs
 $\bar{R}$ = rest
 $\bar{S}$ = set

Logical data, each flipflop			upper limit A
Output load factor each output	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor at C at $\bar{R}$ and $\bar{S}$ at C, $\bar{R}$ and $\bar{S}$ remaining inputs	H-signal	F_{IH}	3
	H-signal	F_{IH}	1
	L-signal	F_{IL}	2
		F_I	1

Note: $\bar{R}$ and $\bar{S}$ are approx. 1.5 normalized loads dynamically

Truth table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

t_n = bit time before clock pulse
 t_{n+1} = bit time after clock pulse
L-level at $\bar{R}$ sets Q to L.
L-level at $\bar{S}$ sets Q to H.
 $\bar{R}$ and $\bar{S}$ operate independently of C.

Dual JK-Master-Slave Flipflop with Set and Reset

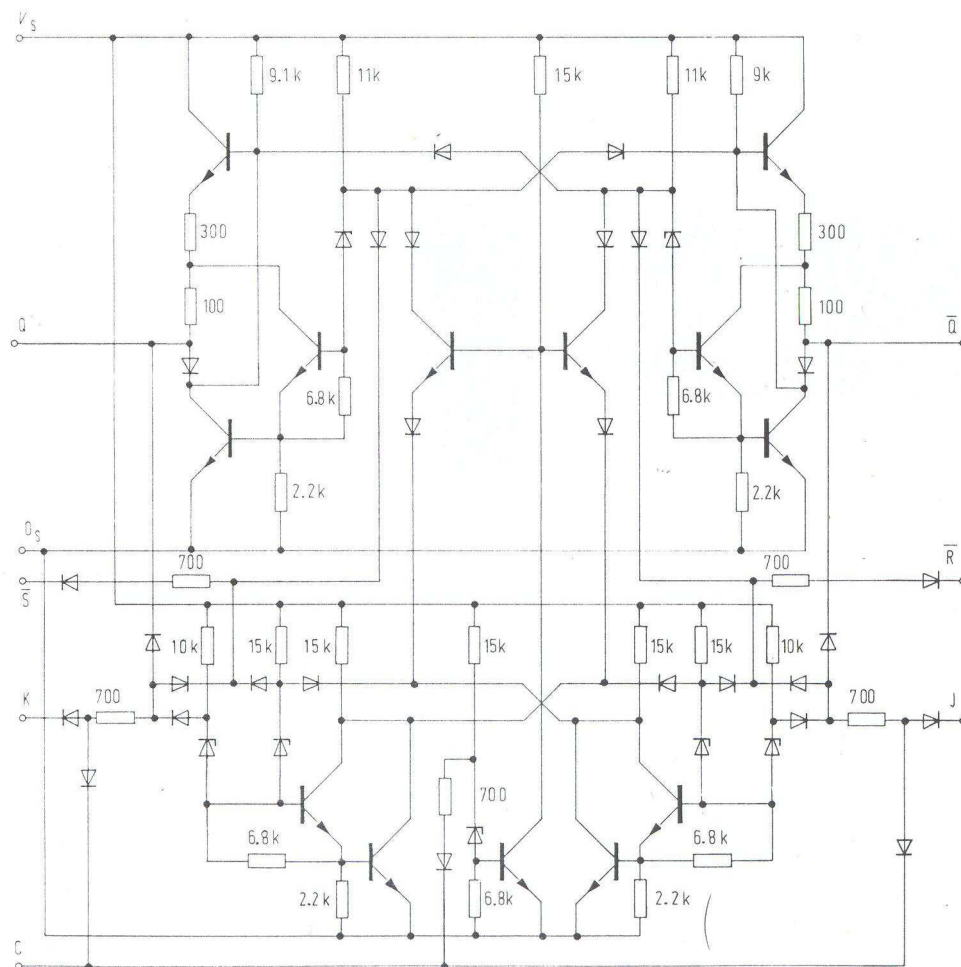
FZJ 121
FZJ 125

Clock pulse



- 1 isolate slave from master
- 2 enter signal from J and K into master
- 3 disable inputs J and K
- 4 transfer information from master to slave

Schematic



C = clock, J, K = inputs, Q, $\bar{Q}$ = outputs, $\bar{R}$ = reset, $\bar{S}$ = set

5.5 Counter and Register Circuits

5.5.1 Synchronous Counter with a 3:1 Division Ratio

Fig. 5.5.1 shows a synchronous divide-by-3-counter with the flipflop FZJ 121. The state of the counter is controlled by the Q and $\bar{Q}$ outputs and the J inputs. The connection between Q of FF1 and J of FF2 inhibits FF2 during every other clock pulse. The connection between $\bar{Q}$ of FF2 and J of FF1 blocks FF1 after the third pulse. The function table results as follows:

clock pulse	output Q_1	state* Q_2	corresp. decimal
1	L	L	0
2	H	L	1
3	L	H	2
4	L	L	0
$\vdots$	$\vdots$	$\vdots$	$\vdots$

* output state before
the clock pulse

The clock frequency of the synchronous counter is equal to the clock frequency of the flipflops as the clock inputs are connected in parallel.

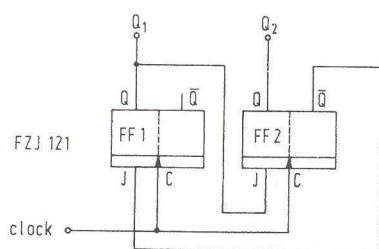


Fig. 5.5.1

5.5 Counter and Register Circuits

5.5.2 Synchronous Counter with a 4:1 Division Ratio

A synchronous divide-by-4-counter with the flipflop FZJ 121 is shown in fig. 5.5.2. The connection between Q of FF1 and J and K of FF2 inhibits FF2 during every other pulse. The following function table results:

clock pulse	output Q ₁	state* Q ₂	corresp. decimal
1	L	L	0
2	H	L	1
3	L	H	2
4	H	H	3
5	L	L	0
⋮	⋮	⋮	⋮

* output state before
the clock pulse

The clock frequency of the counter is equal to the clock frequency of the flipflops.

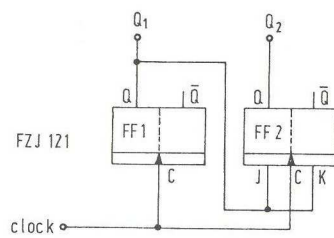


Fig. 5.5.2

5.5 Counter and Register Circuits

5.5.4 Reversible Decimal Counter with Preset

Fig. 5.5.4 shows a synchronous reversible counter which has been devised for a minimum number of components. The additional JK inputs that are required for the FZJ 121 flipflops are obtained by a combination of diodes BAW 76.

The operating mode is selected by the input mode control MC. At MC = H the counter counts up. The NAND-gates connected with Q_1 , Q_2 , and Q_3 are enabled and control the JK inputs of the following flipflops FZJ 121. The NAND-gates operated by the inverter FZH 201 are simultaneously inhibited. The counter counts down at MC = L; the JK conditions now being derived from the $\bar{Q}$ outputs. The logic state of MC can only be changed while the count input is low.

The truth table is as follows:

pulses at count input		mode control MC	carry C	outputs Q ₄ Q ₃ Q ₂ Q ₁							corresp. decimal
up											
1	H	L	L	L	L	L	L	H	L	11	0
2	H	L	L	L	L	L	H	L	L	10	1
3	H	L	L	L	L	H	L	L	L	9	2
4	H	L	L	L	L	H	H	L	L	8	3
5	H	L	L	L	H	L	L	L	L	7	4
6	H	L	L	L	H	L	H	L	L	6	5
7	H	L	L	L	H	H	L	L	L	5	6
8	H	L	L	L	H	H	H	L	L	4	7
9	H	L	H	H	L	L	L	L	L	3	8
10	H	H	H	H	L	L	H	H	L	2	9
11	H	L	L	L	L	L	L	H	L	1	0
			Q ₄	Q ₃	Q ₂	Q ₁	C	MC	pulses at		
			outputs				carry	mode	count		
								control	input		
down											

The carry pulse is generated by the gate FZH 231. This pulse controls not only the counting input of the following decade but inhibits also with $J = L$ the second and third stage being in state $Q_2 Q_3 = LL$. This is necessary during up-counting, since due to conditions $Q_1 = JK = H$ a state change of the second stage is possible, when the counter changes from $Q_4 Q_3 Q_2 Q_1 = HLLH$ to $LLLL$ (decimal 9 to 0). During counting down the same happens for the second and third stage, when the outputs change from $Q_4 Q_3 Q_2 Q_1 = LLLL$ to $LHLL$, which corresponds to a change from decimal 0 to 9.

Counter preset is possible by the gate FZH 201 via the RS-inputs of the flip-flop FZJ 121.

5.5 Counter and Register Circuits

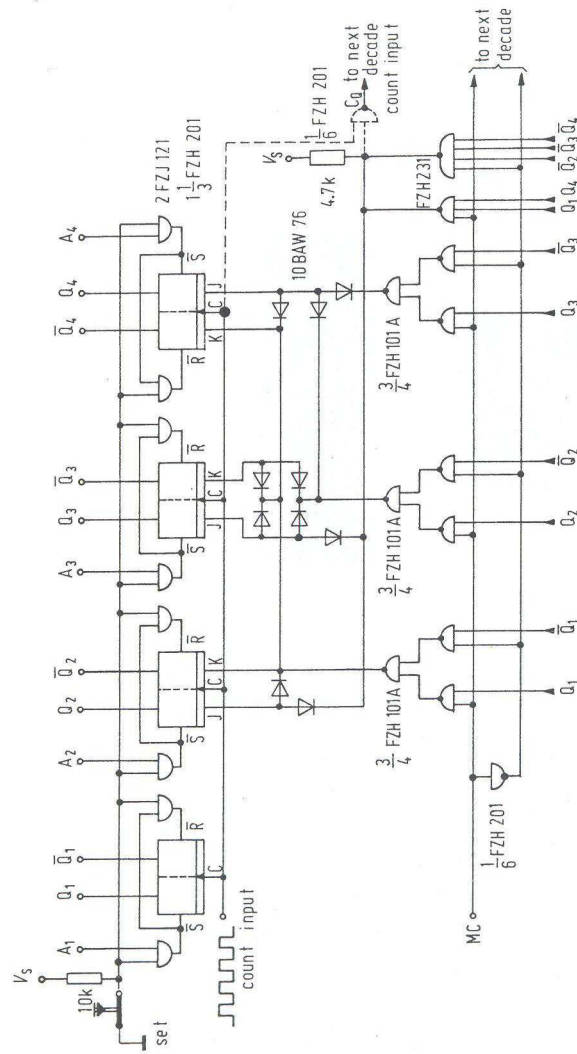


Fig. 5.5.4

5.5.6 Reversible Binary Counter with Preset

The operating mode is selected by the mode control input MC. For counting up $MC = H$. Thus the NAND-gates connected to outputs Q_1 , Q_2 and Q_3 are enabled and the NAND-gates driven by the inverter FLH 201 are inhibited. The JK information of the second flip-flop thus corresponds to the state at Q_1 . At the third stage it is $JK = Q_1 Q_2$ etc. Down counting occurs at $MC = L$; the JK-conditions now being derived from the $\bar{Q}$ outputs. The logic state of MC can only be changed while the count input is low.

pulses at count input	mode control MC	up				corresp. decimal	
		Q ₄	Q ₃	Q ₂	Q ₁		
1	H	L	L	L	L	17	0
2	H	L	L	L	H	16	1
3	H	L	L	H	L	15	2
4	H	L	L	H	H	14	3
5	H	L	H	L	L	13	4
6	H	L	H	L	H	12	5
7	H	L	H	H	L	11	6
8	H	L	H	H	H	10	7
9	H	H	L	L	L	9	8
10	H	H	L	L	H	8	9
11	H	H	L	H	L	7	10
12	H	H	L	H	H	6	11
13	H	H	H	L	L	5	12
14	H	H	H	L	H	4	13
15	H	H	H	H	L	3	14
16	H	H	H	H	H	2	15
17	H	L	L	L	L	1	0

down counting:

$$JK_n = \bar{Q}_1 \bar{Q}_2 \bar{Q}_3 \bar{Q}_4 \dots \bar{Q}_{n-1}$$

5.5 Counter and Register Circuits

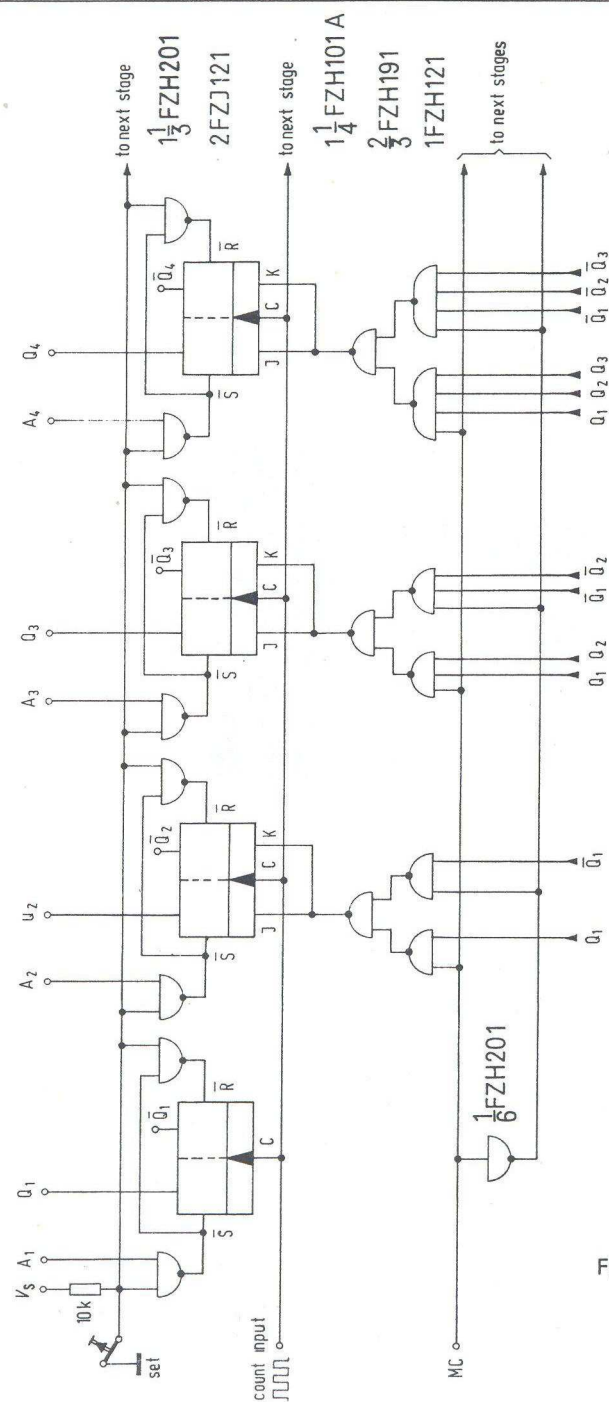


Fig. 5.5.6

5.5 Counter and Register Circuits

5.5.12 Bidirectional Shiftregister

The shiftregister shown next consists of 6 JK flipflops. Each clock pulse shifts the information loaded into the register by one bit to the right or to the left from its initial position. This kind of recirculation register is frequently used for the control of tooling machines.

When the supply voltage is turned on, the integrating network R_1/C_1 causes the first and the last flipflop to be set to an H-level and the remaining flipflop to an L-level.

The register shifts to the right if the input MC is supplied with an H-level. In this case one input each of the odd numbered gates is supplied with an H-signal. The output of the preceding flipflops are connected to the second input of these gates. When the output of the preceding flipflop is at an H-level, the output of gate 1, for example, will assume an L-level. By means of the succeeding NAND-gate and the inverter, the input conditions of the first flipflop will be $J = H$ and $K = L$.

The flipflop will remain at $Q_A = H$ at the following clock pulse due to this input condition. If the information at the second input of gate 1 changes to an L-level, an H-level will result at its output. Because there will also be on H-level at the output of the second gate, the input conditions of the first flipflop will now be $J = L$ and $K = H$. The flipflop will change to $Q_A = L$ at the next clock pulse due to this condition. The operation of the other flipflops can be determined in a similar way.

Left shift operation is achieved by an L-signal at MC. During left shift operation the information from the outputs is transferred to the inputs of the preceding flipflop by means of the even numbered gates. The odd numbered gates are blocked by an L-level.

Truth table for right shift operation:

	mode control	outputs of the flipflops					
	MC	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F
Initial state	H	H	L	L	L	L	H
1st clock	H	H	H	L	L	L	L
2nd clock	H	L	H	H	L	L	L
3rd clock	H	L	L	H	H	L	L
4th clock	H	L	L	L	H	H	L
5th clock	H	L	L	L	L	H	H

Truth table for left shift operation:

	mode control	outputs of the flipflops					
	MC	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F
Initial state	L	H	L	L	L	L	H
1st clock	L	L	L	L	L	H	H
2nd clock	L	L	L	H	H	H	L
3rd clock	L	L	L	H	H	L	L
4th clock	L	L	H	H	L	L	L
5th clock	L	H	H	L	L	L	L

Any desired program can be realised if the set and reset inputs $\bar{S}$ and $\bar{R}$ of the flipflops FZJ 121 are wired correspondingly.

5.5 Counter and Register Circuits

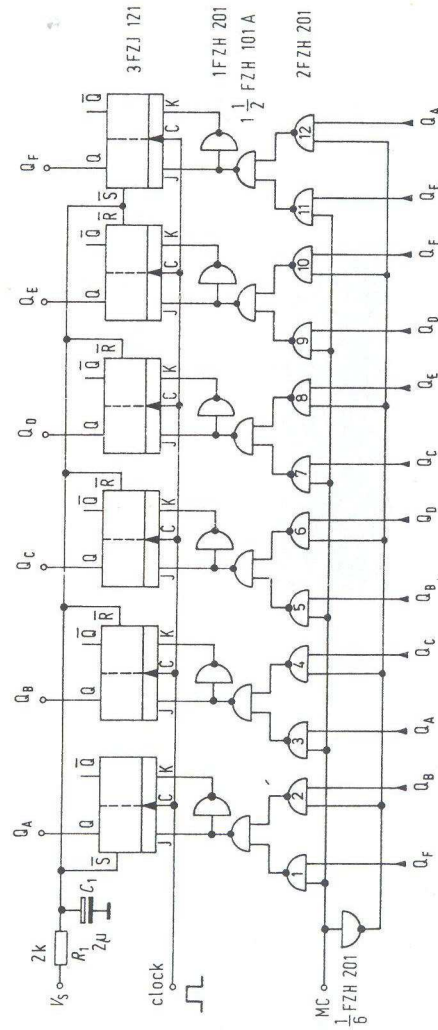


Fig. 5.5.12