CML Semiconductor Products

PRODUCT INFORMATION

FX365

μP Compatible CTCSS Encoder/Decoder

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Provisional Issue

Features/Applications

- CTCSS Encoder/Decoder
- Serial/Parallel μP Interface
- 38 Programmable Tones
- Separate Rx/Tx Audio Paths
- HP Filter for Rejection of CTCSS Tone and Prefiltering of Tx Audio
- Low Falsing with Noise Inputs
- Tx Phase Reversal Facility
- 'No Tone' Facility
- HF Filters on Inputs
- On-Chip Analogue Switching
- Low Power 5V CMOS
- Xtal Controlled Tones
- Meets EIA RS220(B)/MPT1306
- Choice of DIL or Surface Mount Package Styles

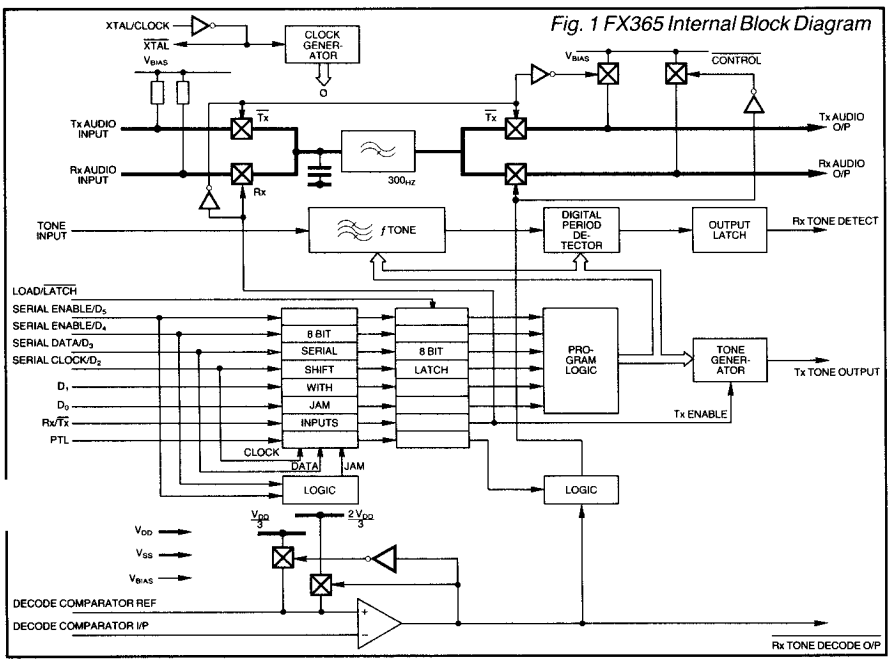


Fig. 1 FX365 Internal Block Diagram

FX365

Brief Description

The FX365 is a CMOS LSI device intended for use as a CTCSS Encoder/Decoder in radio communications systems. Designed specifically for microprocessor controlled multichannel equipment, the FX365 incorporates a number of advanced features which improve performance and facilitate system design. The tone frequency to be encoded or decoded, the transmit enable command and the monitor receiver audio command may all be entered via an 8-bit port and a load/latch pulse. Alternatively, the programming information may be entered via a serial data port and a data clock. The device has a new tone decoder design which reduces false decode outputs due to noise to insignificant levels.

The tone encoder has a phase reversal facility, the tone decoder and speech path high pass filter have separate inputs and both are protected against the effects of incident RF voltages. The speech path filter has low passband ripple, low output noise and a cut-off frequency of 300Hz regardless of the programmed CTCSS tone.

Separate Rx and Tx audio paths are provided for prefiltering of Tx audio and rejection of the CTCSS tone in Rx mode.

The FX365 uses a 1MHz crystal reference oscillator, a single 5-volt supply; and the choice of DIL or SMT packages makes it suitable for fixed or portable equipment.

Pin Number			Function
DIL FX365J	Quad Plastic FX365LG	PLCC FX365LS	
1	1	1	**V_{DD}:** Positive Supply.
2	2	2	**Xtal/Clock I/P:** Input to on-chip inverter used with a 1MHz Xtal or external clock source.
3	3	3	**$\overline{\text{Xtal}}$:** Output of on-chip inverter (clock output).
4	4	4	**Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch Rx/$\overline{\text{T}}$x, PTL, D_0–D_5. This pin is internally pulled to V_{DD}. A logic '1' applied to this input puts the 8 latches in 'transparent' mode. A logic '0' applied to this input puts the 8 latches in the 'latched' mode. In parallel mode data is loaded and latched by a logic 1→ 0 transition (see Fig. 4). In serial mode data is loaded and latched by a 0→1→0 strobe pulse on this pin (see Fig. 5).
5	5	5	**D_5/Serial Enable 1:** Data input D_5 (in parallel mode). A logic '1' applied to this input together with a logic '0' applied to D_4/SERIAL ENABLE 2 will put the device in 'Serial mode' (see Fig. 5). This pin internally pulled to V_{DD}.
6	6	6	**D_4/Serial Enable 2:** Data input D_4 (in parallel mode). A logic '0' applied to this input together with a logic '1' on pin 5 will place the device in 'serial mode' (see Fig. 5). This pin internally pulled to V_{DD}.
7	7	7	**D_3/Serial Data:** Data input D_3 (in parallel mode). In serial mode this pin becomes the serial data input for D_5–D_0, Rx/$\overline{\text{T}}$x, PTL (see Fig. 5). D_5 is clocked first and PTL last. This pin internally pulled to V_{DD}.
8	8	8	**D_2/Serial Clock:** Data D_2 (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see Fig. 5). This pin is internally pulled to V_{DD}.
9	9	9	**D_1:** Data D_1 (in parallel mode). This pin internally pulled to V_{DD}.
10	10	10	**D_0:** Data D_0 (in parallel mode). This pin internally pulled to V_{DD}.
11	11	11	**V_{SS}:** Negative supply.
12	12	12	**Decode Comparator Ref (I/P):** This pin is internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1MΩ resistors depending on the logical state of the TONE DECODE O/P pin. TONE DEC O/P=1 will bias this input to $2V_{DD}/3$, a logic '0' will bias this input to $V_{DD}/3$. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions.
13	13	13	**$\overline{\text{Rx Tone Decoder (O/P)}}$:** Gated output of the decode comparator. This output is used to gate the Rx Audio path. A logic '0' on this pin indicates a successful decode and indicates that the 'decode comparator input' pin is more positive than the 'decode comparator ref' input (see Table 2).

Pin Number			Function
DIL FX365J	Quad Plastic FX365LG	PLCC FX365LS	
14	14	14	**Decode Comparator Input:** This is the inverting input of the decode comparator. This pin is to be connected to the Rx TONE DETECT pin via an external integrator (see Figs. 2 & 3).
15	15	15	**Rx Tone Detect (O/P):** In Rx mode this pin will go to logic '1' during a successful decode (see Table 2). This pin is normally connected to the Decode Comparator input via the external integrator circuitry, as shown in Figs. 2 & 3.
16	16	16	**Tx Tone O/P:** A low impedance emitter follower stage for sourcing the CTCSS sinewave under the control of the Rx/$\overline{Tx}$ pin. This O/P when not transmitting a tone may be biased to $\frac{V_{DD}}{2} - 0.7V$ or O/C (see Table 2).
17	17	17	**Rx/$\overline{Tx}$:** This input (in parallel mode) selects Rx or Tx modes (see Fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.
18	18	18	**PTL:** In parallel Rx mode this pin operates as a 'press to listen' function by enabling the Rx audio path thus overriding the tone squelch function. In parallel Tx mode this pin reverses the phase of the transmitted CTCSS tone (squelch tail elimination). In serial mode this function is serially loaded (see Fig. 3). The phase reversal function should be applied by timing circuit to ensure correct system operation.
19	19	19	**Rx Audio Out:** This is the high pass filtered "Receive" audio output pin. This pin outputs audio when Rx TONE DECODE = 0, or PTL = 1 or NOTONE is programmed (see Table 2). In Tx mode this pin is biased to $\frac{V_{DD}}{2}$.
20	20	20	**Tx Audio Out:** This is the high pass filtered "Transmit" audio output pin. In Tx mode this pin outputs audio present at the 'Tx AUDIO INPUT' pin. In Rx mode this pin is biased to $\frac{V_{DD}}{2}$.
21	21	21	**Bias:** This pin is the output of an internally generated $\frac{V_{DD}}{2}$ bias level and would normally be externally decoupled to V_{SS} via C_6.
22	22	22	**Tx Audio I/P:** This is the Tx Audio input pin. In Tx mode audio may be prefiltered, using the Tx audio path, thus helping to avoid talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. The Tx audio path may also be used to prefilter speech when using scramblers which introduce noise in the low frequency band. This pin is internally biased to $\frac{V_{DD}}{2}$.
23	23	23	**Rx Audio Input:** This is the input to the audio high pass filter in Rx mode. This pin is internally biased to $\frac{V_{DD}}{2}$.
24	24	24	**Tone Input:** This is the input to the CTCSS tone detector and is internally biased to $\frac{V_{DD}}{2}$.

External Component Connections

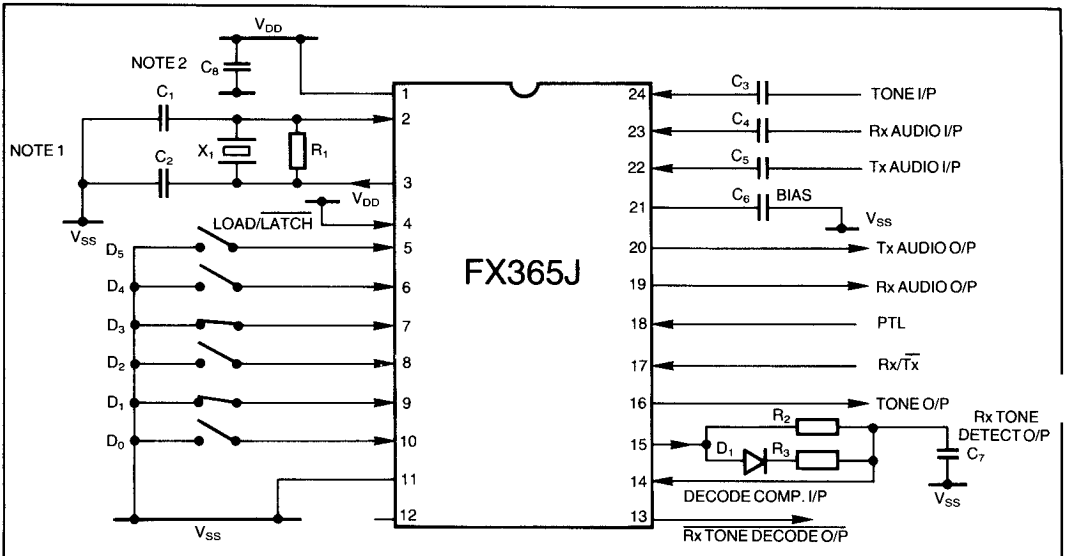


Fig. 2 Parallel Wired Application

Component	Unit Value	Note
R_1	1M	1
R_2	820k	
R_3	330k	
C_1	68p	1
C_2	33p	1
C_3	0.1μ	
C_4	0.1μ	

Component	Unit Value	Note
C_5	0.1μ	
C_6	1.0μ	
C_7	0.1μ	
C_8	1.0μ	2
D_1	small signal	
X_1	1MHz	1

NOTES:

Tolerances: Resistors ±10%. Capacitors ±20%

1. *Xtal circuitry shown is in accordance with CML. Application Note D/XT/1 April 1986.*
2. *C_8 is used for power supply decoupling. Depending on application further filtering may be required.*

Table 1 Component References and Values

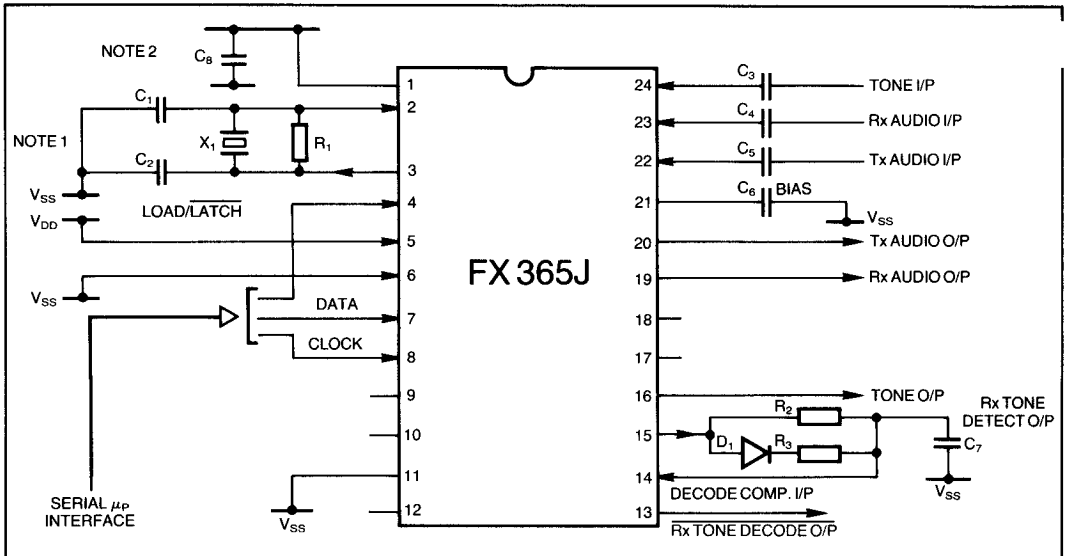


Fig. 3 Serial Microprocessor Application

Truth Tables

Input Pin – Condition				Output Pin – Condition		Result/Function					Notes
D_0–D_5	Rx/$\overline{Tx}$	PTL	Decode Comp Input	Rx Tone Detect	$\overline{Tone\ Decode}$	Tone Transmitter Enabled	Tx Tone Phase Reversed	Tx Audio Path Enabled	Tone Decoder Enabled	Rx Audio Path Enabled	
Tone	0	0	x	0	1	Yes	No	Yes	No	No (bias)	1a
Tone	0	1	x	0	1	Yes	Yes	Yes	No	No (bias)	1b
No tone	0	x	x	0	1	No (bias)	x	Yes	No	No (bias)	2
Tone	1	0	0	0	1	No (o/c)	x	No	Yes	No (bias)	3a
Tone	1	1	0	0	1	No (o/c)	x	No	Yes	Yes	3b
Tone	1	x	1	1	0	No (o/c)	x	No	Yes	Yes	4
No tone	1	x	x	x	0	No (o/c)	x	No	Yes	Yes	5

Notes:

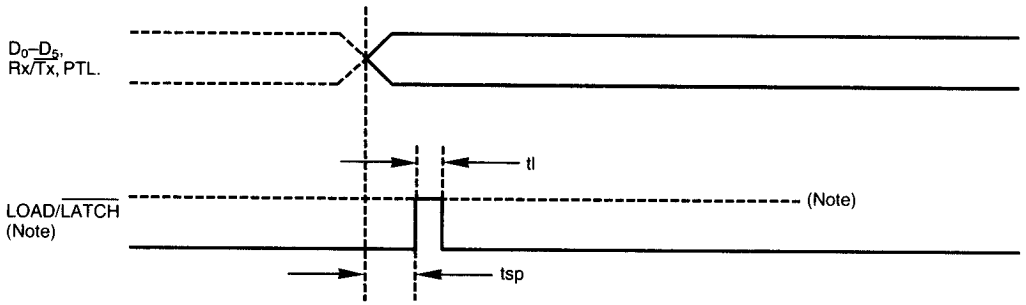
1a. Normal tone transmit condition.
1b. Tone transmit with phase reversed.
2. 'NOTONE' programmed in Tx mode, tone transmit O/P set to $V_{DD}/2 - 0.7V$. Tx audio path enabled.
3a. Normal decode standby.
3b. Normal decode standby with PTL used to enable audio.
4. Normal 'decode of correct CTCSS tone' condition, PTL has no effect.
5. 'NOTONE' programmed in Rx mode, tone transmit O/P (o/c), Rx audio path enabled.

Table 2 Truth table defining combinations of input/output conditions.

Nominal Freq. Hz	FX365 Frequency	$\triangle f_o$%	Programme Inputs D_0	D_1	D_2	D_3	D_4	D_5
67.0	67.05	+.07	1	1	1	1	1	1
71.9	71.90	0.0	1	1	1	1	1	0
74.4	74.35	−.07	0	1	1	1	1	1
77.0	76.96	−.05	1	1	1	1	0	0
79.7	79.77	+.09	1	0	1	1	1	1
82.5	82.59	+.10	0	1	1	1	1	0
85.4	85.38	−.02	0	0	1	1	1	1
88.5	88.61	+.13	0	1	1	1	0	0
91.5	91.58	+.09	1	1	0	1	1	1
94.8	94.76	−.04	1	0	1	1	1	0
97.4	97.29	−0.11	0	1	0	1	1	1
100.0	99.96	−.04	1	0	1	1	0	0
103.5	103.43	−.07	0	0	1	1	1	0
107.2	107.15	−.05	0	0	1	1	0	0
110.9	110.77	−.12	1	1	0	1	1	0
114.8	114.64	−.14	1	1	0	1	0	0
118.8	118.80	0.0	0	1	0	1	1	0
123.0	122.80	−.17	0	1	0	1	0	0
127.3	127.08	−.17	1	0	0	1	1	0
131.8	131.67	−.10	1	0	0	1	0	0
136.5	136.61	+.08	0	0	0	1	1	0
141.3	141.32	+.02	0	0	0	1	0	0
146.2	146.37	+.12	1	1	1	0	1	0
151.4	151.09	−.20	1	1	1	0	0	0
156.7	156.88	+.11	0	1	1	0	1	0
162.2	162.31	+.07	0	1	1	0	0	0
167.9	168.14	+.14	1	0	1	0	1	0
173.8	173.48	−.19	1	0	1	0	0	0
179.9	180.15	+.14	0	0	1	0	1	0
186.2	186.29	+.05	0	0	1	0	0	0
192.8	192.86	+.03	1	1	0	0	1	0
203.5	203.65	+.07	1	1	0	0	0	0
210.7	210.17	−.25	0	1	0	0	1	0
218.1	218.58	+.22	0	1	0	0	0	0
225.7	226.12	+.18	1	0	0	0	1	0
233.6	234.19	+.25	1	0	0	0	0	0
241.8	241.08	−.30	0	0	0	0	1	0
250.3	250.28	−.01	0	0	0	0	0	0
Notone	Notone	—	0	0	0	0	1	1
Serial Input Mode			x	x	Clock	Data	0	1

Table 3 Tone programming Truth table

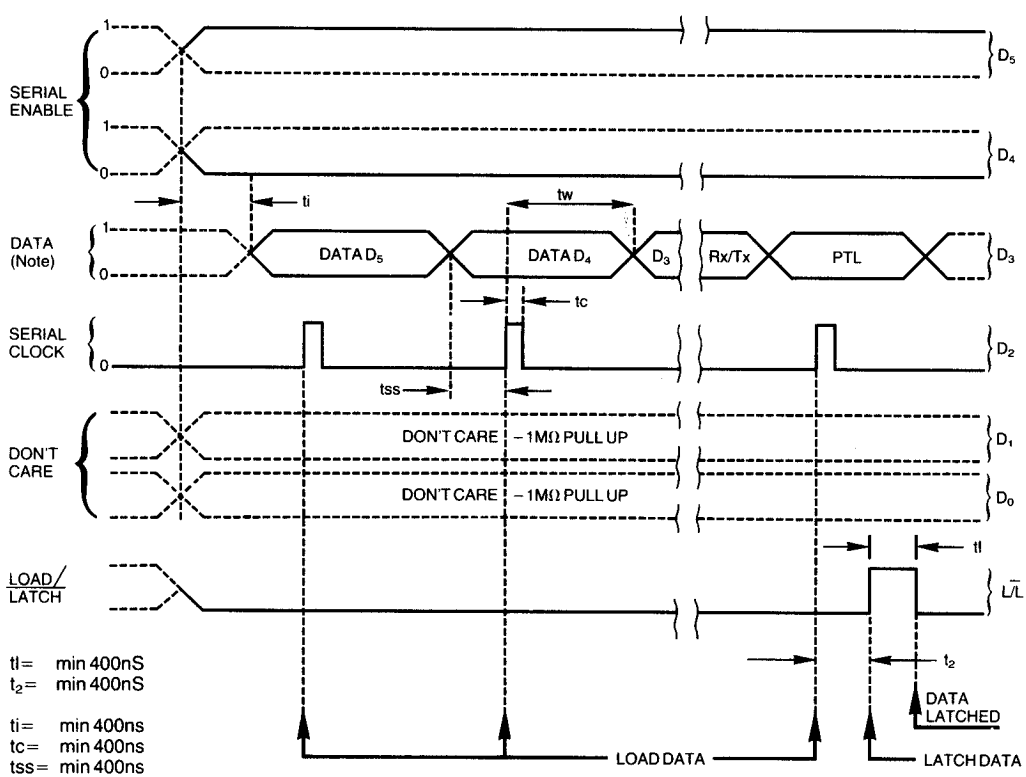
Parallel and Serial Mode Timing Diagrams



Note: For wired, non microprocessor, applications load/latch should be connected to V_{DD}

tl min=400ns
tsp min=400ns

Fig. 4 Parallel mode timing diagram



tl= min 400nS
t_2= min 400nS

ti= min 400ns
tc= min 400ns
tss= min 400ns
tw= min 400ns

tl= min 400ns
t_2= min 400ns

Note 1: Serial bit 1 through bit 8=D_5, D_4, D_3, D_2, D_1, D_0, Rx/Tx and PTL respectively.
Load bit 1 first, bit 8 last.

Fig. 5 Serial mode timing diagram

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS}=0V)		−0.3V to (V_{DD}+0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX365J	−30°C to +85°C
	FX365LG/LS	−30°C to +70°C
Storage temperature range:	FX365J	−55°C to +125°C
	FX365LG/LS	−40°C to +85°C
Maximum device dissipation		800mW
Derating		10mW/°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
V_{DD} = 5.0V. T_{AMB} = 25°C. 0dB ref: = 300mVrms. Composite Signal = 0dB 1kHz Tone, −12dB Noise (band-limited 6kHz aussian white noise), −20dB f_o CTCSS Tone.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Characteristics					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
(Tx)		–	3.5	–	mA
(Rx)		–	3.5	–	mA
Tone Input Impedance		–	1.0	–	MΩ
Audio Input Impedance		–	1.0	–	MΩ
Audio Output Impedance		–	1.0	–	kΩ
Digital Input Impedance	1	–	1.0	–	MΩ
Input Logic "1"	1	3.5	–	–	V
Input Logic "0"	1	–	–	1.5	V
Logic "1" Output 1' source = 0.1mA	2	4.0	–	–	V
Logic "0" Output 1' sink = 0.1 mA	2	–	–	1.0	V
Dynamic Characteristics					
Decoder					
Decode Input Signal Level	3	−20	–	–	dB
Decode Response Time	3, 6	–	–	250	ms
De-Response Time	3, 6	–	–	250	ms
Decode Selectivity	3	±0.5	–	±3.0	%f_o
Encoder					
Tone Output Level (relative 775mVrms)		−3.0	0	–	dB
Tone Frequency Accuracy (f_o error)		−0.3	–	+0.3	%f_o
Risetime to 90% (nominal output)					
f_o > 100Hz	***4***	–	***55.0***	–	***ms***
f_o < 100Hz	***4***	–	***70.0***	–	***ms***
Tone Output Load Current		–	–	5.0	mA
Total Harmonic Distortion		–	2.0	5.0	%
Output Level Variation Between Tones		–	0.1	–	dB
Audio Filter					
Total Harmonic Distortion	5	–	2.0	5.0	%
Output Noise Level					
Input a.c. Short Cct, Audio Switch Enabled		–	***−49.0***	***−45.0***	***dB***
Cut-Off frequency		–	300	–	Hz
Bandpass Ripple (300Hz −3000Hz)	5	−1.0	–	+1.0	dB
Stopband Attenuation <250Hz	5	36.0	40.0	–	dB
Passband Gain (ref. 1kHz)		–	0	–	dB
Audio Switch					
Isolation	5	–	60.0	–	dB
Serial/Parallel Inputs					
Parallel Set-Up Time (t_{SP})	7	400	–	–	ns
Load/Latch Pulse Width (t_L)	7	400	–	–	ns
Serial Clock Pulse Width (t_C)	7	400	–	–	ns
Serial Set-Up Time (t_{SS})	7	400	–	–	ns
Serial Clock Frequency	7	–	1.0	–	MHz

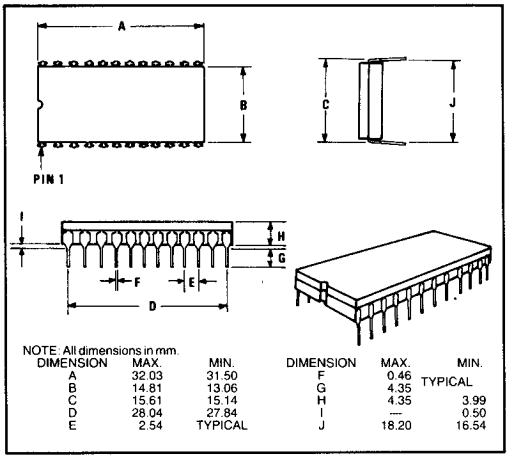
Notes

1. Refers to Rx/$\overline{Tx}$, PTL, Decode Comparator Input, D_0, D_1, D_2, D_3, D_4, D_5.
2. All logic outputs.
3. Composite Signal Test Condition.
4. Any programme tone and RL = 600Ω. CL = 15pF. Includes response to a phase reversal instruction.
5. 1kHz reference = 0dB.
6. f_o > 100Hz, (for 100Hz >f_o>67Hz: t = (100/f_o Hz) x 250ms).
7. See Figures 4 and 5.

Packaging Outlines

The FX365J, the cerdip package, is illustrated in figure 6. The 'LG' version is shown in figure 7, and the 'LS' version in figure 8. To allow complete identification, the FX365 LG and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number anti-clockwise when viewed from the top (indent side).

Fig. 6 **FX365J** *Cerdip DIL Package*



NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.	DIMENSION	MAX.	MIN.
A	32.03	31.50	F	0.46	TYPICAL
B	14.81	13.06	G	4.35	
C	15.61	15.14	H	4.35	3.99
D	28.04	27.84	I	—	0.50
E	2.54	TYPICAL	J	18.20	16.54

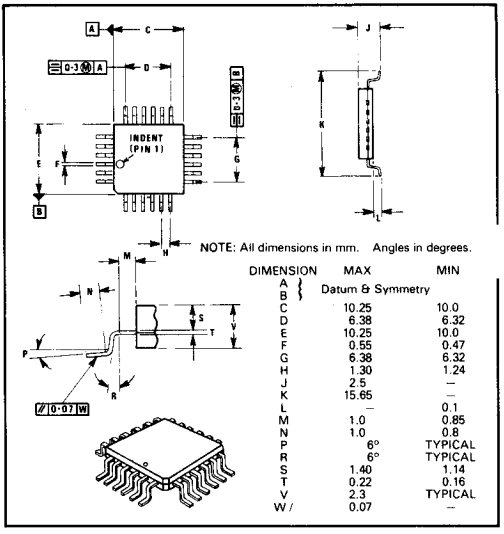
Ordering Information

FX365J	**24-pin cerdip DIL**
FX365LG	**24-pin quad plastic encapsulated, bent and cropped**
FX365LS	**24-lead plastic leaded chip carrier**

Handling Precautions

The FX365J/LG/LS is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

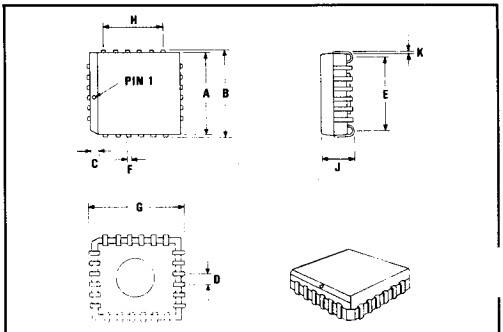
Fig. 7 **FX365LG** *Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX	MIN
A, B	Datum & Symmetry	
C	10.25	10.0
D	6.38	6.32
E	10.25	10.0
F	0.55	0.47
G	6.38	6.32
H	1.30	1.24
J	2.5	—
K	15.65	—
L	—	0.1
M	1.0	0.85
N	1.0	0.8
P	6°	TYPICAL
R	6°	TYPICAL
S	1.40	1.14
T	0.22	0.16
V	2.3	TYPICAL
W	0.07	—

Fig. 8 **FX365LS** *Package*



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.	DIMENSION	MAX.	TYP.	MIN.
A	10.40		9.70	F	0.55		0.45
B	11.05		10.60	G	11.05		10.60
C		1.15 x 45°		H		6.35	
D		1.27		J	3.70		3.25
E		9.30		K	0.27		0.17