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PRE-PUBLICATION PRODUCT INFORMATION EXTRACT

FX-209 Adaptive Delta Modulation Encoder or Decoder.

The FX-209 contains all the active analogue and digital circuitry of an adaptive delta modulation encoder or decoder, leaving the user to connect the passive resistors and capacitors to suit his application.

This Nitride PMOS device can in many applications replace conventional analogue-to-digital converters (ADC) and their corresponding digital-to-analogue converters (DAC) with advantage.

The conventional ADC is a pulse code modulator. It accepts a continuous band-limited signal, samples it, and converts each sample into a binary word. This means that for n bit binary words the samples have been quantized to any of l levels, where $l = 2^n$. The binary words are then sequentially transmitted, in the case of a telecommunications application, or they may be used locally in some digital process, such as a digital filter. There are three characteristics of this type of ADC which in some applications can give rise to difficulties.

1. The necessity of maintaining word synchronism, i.e. the ability of the receiver to correctly identify each code word. If this is not done the DAC will decode words composed of two adjacent words, resulting in gross distortion.

2. The need to provide a filter with a sharp cut-off after the DAC to prevent aliasing effects.

3. In situations where some of the binary words at the input to the DAC are in error, due to a noisy transmission channel for example, the signal-to-noise ratio snr of the decoded signal is exponentially related to the number of words in error. This means that a small error rate results in a large reduction in snr.

The FX-209 adaptive delta modulator, ADM, greatly alleviates these difficulties encountered with conventional ADCs and DACs. Before describing the FX-209, the basic behaviour of the linear and adaptive delta modulators are briefly explained.

Linear delta modulation (LDM)

The linear delta modulator is shown in Figure 1. The continuous input signal x(t) to be encoded is compared with the feedback signal y(t) to yield the binary signal q(t). This signal is converted into a synchronous binary signal L(t) with the aid of a D flip flop and an external clock. L(t) is transmitted (or processed, if for example the delta modulator forms part of an instrument), and it is also locally decoded back into a continuous signal y(t) by means of a simple R1 C1 integrator, see Figures 1(a) and 2. The action of the encoder is to cause y(t) to track x(t).

Notice that at any clock instant the polarity of the output bit is dependent on the sign of the error $x(t) - y(t)$, and this is the information transmitted. This means that word synchronisation, essential with conventional ADCs, is not required. However, the bit rate is not reduced because the clock operates at a higher value than in a conventional ADC. This results in a simplification in the requirements of the final filter after the decoder, as at these high clock rates aliasing is not a problem.

The delta modulator decoder is very simple, see Figure 1 (b). It is the local decoder used in the encoder, which in the absence of transmission errors recovers $y(t)$, followed by a low pass filter to remove the sharp changes in this waveform thereby producing $\hat{x}(t)$, a close replica of $x(t)$. The size of a single transmission error produces an error in $y(t)$ of approximately twice the step height γ, see Figure 2, but this error in $y(t)$ can propogate for a duration depending on the time constant of the R1 C1 integrator. By comparison the errors in conventional ADCs can be very much greater although they do not propogate. However, for speech signals, linear and syllabically companded delta modulation systems are vastly superior to pulse code modulation systems (which of course comprise an ADC and a DAC) in the presence of high transmission error rates.

Adaptive delta modulation (ADM)

The tracking ability of the delta modulator can be greatly enhanced if the changes γ in the feedback signal per clock instant adapts to the variations of the input signal.

The choice of adaptation strategy depends on the type of signal being encoded, and the FX-209 is particularly suitable for encloding speech signals. It is found that a desirable adaptation procedure is for γ to vary in a manner dependent on the envelope of the speech signal, rather than its instantaneous value. Figure shows a syllabically companded delta modulator. The titles 'companded' and 'adaptive' may be treated synonymously. The R1 C1 integrator is included as before to convert the pulses (whose duration are equal to a clock period) in the waveform $h(t)$ into the continuous signal $y(t)$ as previously described.

Although $L(t)$ is a binary waveform, $h(t)$ the signal at the output of the multiplier, is a multilevel one, whose magnitude depends on $V_c(t)$ and whose polarity is identical to $L(t)$.

The magnitude H of the pulses in $h(t)$ is

$$H = A\, V_c(t)\, \mathrm{sgn}\{L(t)\}$$

where A is a gain factor. The sequence detector observes the present and previous values of $L(t)$, say Lr, Lr-1 and Lr-2, and the logic circuitry produces a waveform $g(t)$ which either increases or decreases the charge on capacitor C2. A suitable encoding algorithm is one which makes $g(t)$ a logical one if the encoder is experiencing a partial overload, i.e. if the logical equation

$$Lr\ Lr\text{-}1\ Lr\text{-}2 + \overline{Lr}\ \overline{Lr\text{-}1}\ \overline{Lr\text{-}2} = 1$$

is satisfied. The time constant R2 C2 (>>R1 C1) is chosen as a

function of the envelope of the input signal. In the case of speech a suitable choice of R2 C2 is 5 to 20 mSecs, although sometimes 100 mSecs may be preferred.

Observe that if the envelope of x(t) increases g(t) will charge up C2 and h(t) will be composed of large pulses, and vice versa if the envelope of x(t) is small. It is because the amplitude of h(t) changes slowly relative to the clock rate that this type of delta modulator is relatively resistant to transmission errors.

The L(t) signal is decoded at the receiver by applying it to the local decoder (same form as the one used in the encoder, see Figure 3) followed by a low pass filter to remove out-of-band noise.

FX-209 device.

The system diagram of the FX-209 used as an adaptive delta modulator is shown in Figure 4. It resembles the syllabically companded delta modulator shown in Figure 3, except that an idle channel loop containing resistor R5 and adaptation algorithm Z1, Z2, Z3 have been added. The arrows in Figure 4 refer to information flow.

The idle channel feedback path between pins 14 and 13 reduces the idle channel noise which occurs in the decoded signal when the input signal x(t) is zero. Ideally, when x(t) = 0, L(t) should be composed of alternate positive and negative levels, i.e. a logical pattern .... 101010.... The final low pass filter F_o having a cut-off frequency well below the high frequency oscillations in L(t), produces a zero output voltage. In practice, the idle channel pattern will diverge from the alternating pattern and a small signal will emerge from the filter F_o. The time constant R5 C'in, (R5>>R4) is chosen so as to make the pattern of logical ones and zeros close to the ideal. By arranging for R5 C'in >> f_{c_l} the lowest frequency to be encoded, the idle channel loop does not interfere with the encoding of the speech signals.

R4 and R5 are selected to provde the correct input bias such that the input signal can be varied over the widest amplitude range without waveform distortion occurring. For d.c. operation, or when FX-209 acts as a decoder, R5 and C'in are removed.

The R1 C1 integrator controls the overload characteristic shown in Figure 5. This characteristic shows the highest amplitude E_{sm} as an input sinusoid can have without causing the delta modulator to be overloaded. The overload condition is represented by

$$E_{sm} = \frac{2.2}{\sqrt{1 + \left(\frac{f}{f_1}\right)^2}} \qquad \text{where} \quad f_1 = \frac{1}{2\pi\ R1\ C1}$$

f_1 is the break frequency of the R1 C1 integrator.

The theoretical and measured curves are shown in Figure 5.

for R1 = 100KΩ, C1 = 2,200pf.

If the signal x(t) to be encoded has a flat spectrum, then an R1 C1 integrator should be connected prior to C'in, and a corresponding differentiating network introduced between the FX-209 decoder and the filter F_o. The R1 C1 values used in Figure 5 are suitable for speech encoding.

The time constant R2 C2 is related to the envelope of the input signal. In the case of speech signals, R2 C2 may be set as a function of syllabic (≙ 100mSecs) or pitch (≙ 5mSecs) durations.

Having selected R2 C2, R3 is chosen by applying sinewave and observing the locally decoded waveform on pin 11, and the symmetry of the pulses H at pin 10. The choice of R3 is significant for large amplitude sinusoids. The lower R3 the better the symmetry of H and the decoded waveform in overload but lower amplitudes will overload the encoder. The compromise depends on the application. It is important to ensure that the FX-209 decoder (see Figure 7) have the same resistor and capacitor values to ensure the similarity between the signals on pin 11 of the FX-209 encoder and decoder.

By adjusting Z1, Z2 and Z3 to either logical zero (ground) or logical one (open-circuit) the logical signal g(t) can be altered for a given binary output signal L(t) according to table 1. The significance of the symbols D and P in this table is as follows. g(t) goes positive (earth) on the next negative going clock edge after D consecutive logical ones or logical zeros in the L(t) signal. g(t) returns to a negative potential on the Pth positive clock edge after a change of binary level in the L(t) signal. For the purpose of explanation, Figure 6 is presented showing stylised g(t) waveforms for some D and P values and an arbitrary signal L(t). Observe that L(t) changes level on a positive going clock edge.

Decoding

The FX-209 connected as a delta modulator decoder is shown in Figure 7. The idle channel loop is disconnected, and the binary signal L(t) is connected directly to the input comparator in order to remove the effects of amplitude noise and distortion introduced into the transmission channel. y(t) has been connected to pin 12 to utilise the buffer amplifier connected internally between pins 12 and 13. This arrangement is satisfactory, except when y(t) is very small. When it is important to faithfully decode small signals, connect y(t) directly to the filter, and provide a bias of -6 volts on pin 12. The values of resistors, capacitors, Z1, Z2, Z3, should be the same as those used in the encoder.

Typical performance curves.

These curves are for the FX-209 encoder and decoder connected as shown in Figures 4 and 7, with a source follower connected to the buffered output (pin 11). The FX-209 have the following external parameters Z1, Z2, Z3 grounded, R1 = 100KΩ, R2 = 220KΩ, R3 = 220KΩ, R4 = 270KΩ, R5 = 1.2MΩ, R_L = 10KΩ, C1 = 2200pf, C2 = 0.47μF, C'in = 0.047μF.

Figure 8 shows the linearity of the delta modulation system (encoder followed by decoder) for a sinusoidal input of 800Hz and a clock rate of 64KHz.

The decoded voltage as a function of frequency is shown in Figure 9. The flat portion demonstrates the linearity over the speech band, while the small rise in the curves at the higher frequencies indicate the system is overloaded. The signal-to-noise (snr) is measured using the arrangement of Figure 10. The input signal x(t) is encoded and decoded to yield $y_b(t)$, which is a.c. coupled into the source follower. With the switches in position 1, x(t) is a sinusoid. The signal at the output of the source follower is low pass filtered by a filter having a cut-off frequency of 3,400Hz. The signal-to-noise ratio is measured by the Distortion Factor Meter.

With the switches in position 2, x(t) is a narrow band White Gaussian noise source. The snr of $y_b(t)$ is measured by the Quantization Distortion Tester.

The variation of snr as a function of frequency for various peak-to-peak values of input sinusoid and a clock frequency of 64KHz, is shown in Figure 11.

In Figure 12 the broad hump characteristic of snr versus input power when encoding a 800Hz tone and employing a 64KHz clock is presented.

An 800Hz tone having a p to p amplitude of 2 volts has a snr versus clock frequency f_p performance as depicted in Figure 13. The system increases its snr by 9dB per octave increase in f_p over most of its working range.

The behaviour of the FX-209 when encoding White Gaussian noise signals is shown in Figure 14. This test-signal gives results similar to those obtained with speech signals. The wide dynamic range is evident and the correspondence with Figure 13 is apparent.

The FX-209 as a linear delta modulator.

The FX-209 can be adapted to perform as a linear delta modulator by leaving pins 6 and 8 unconnected, and applying -5 volts to pin 9. Using the Z1, Z2, Z3 resistor and capacitor values previously stated, the snr versus input power for a White Gaussian signal is shown in Figure 15 for f_p = 64KHz. The characteristic improvement in snr of 6dB per octave increase in input power is obtained.

FX-209 as a double integration adaptive delta modulator.

The snr can be improved if the R_1 C_1 integrator between pins 10 and 12 is replaced by the double integrator arrangement shown in figure 16. This network also determined the overload characteristic and has a transfer function,

$$V(jw) = \frac{I + jw\, C_1' r}{jw\, C_1 R_1 + (1 + jw\, C_1' (R + r))(1 + jw\, C_1 R_1)}$$

If $R_1 \gg R_1$ and $C_1 \gg C_1$

$$V(jw) \doteq \left(\frac{1}{1 + jw\, C_1 R_1}\right) \left(\frac{1 + jw\, C_1' r}{1 + jw\, C_1' (R_1' + r)}\right)$$

$$= H_1 (jw).\ H_1' (jw)$$

where H_1 (jw) and H_1' (jw) are the transfer functions of the first and second integrators shown in figure 16.

The first integrator introduces a pole at the frequency f_1, while the second integrator produces a pole at f_1' and a zero at f_o, where

$$f_1 = \frac{1}{2\pi R_1 C_1}$$

$$f_1' = \frac{1}{2\pi C_1' (R_1' + r)}$$

$$f_o = \frac{1}{2\pi C_1' r}$$

When encoding speech signals, the following inequality is recommended:-

$$f_{c1} \leqslant f_1 < f_1' < f_{c2} < f_o \ll f_p$$

where f_c and f_c are the lowest and highest frequencies in the speech signal respectively, and f_p is the clock frequency.

The resistor r, which results in the Bode plot of V(jw) returning to a fall of 6dB per octave increase in frequency for frequencies above f_o, is essential if the encoder is to be stable.

Generally the circuit of figure 16 is also used at the decoder, although the resistor r may be omitted as the decoder, being an open loop system, is not subjected to stability problems. If r is removed R_1' has its value increased by r. A capacitor C_3 may be connected between pins 11 and 1 to form a final pole in the spectral shaping network. This pole is formed by the output resistance of the buffer amplifier connected internally between pins 12 and 11, and C_3.

The position of the pole depends on the application, but near the top end of the message band is often a good position.

For: $R_1 = 10K\Omega$, $R_1' = 68K\Omega$, $r = 22K\Omega$, $C_1 = 0.022\mu F$, $C_1' = 1{,}000pf$, and a capacitor $C_3 = 0.022\mu F$ at the decoder, the curves of snr versus input power for $f_p = 64KHz$ and 32KHz are shown in Figure 17. The experimental arrangement is the one shown in figure 10 with the switches in position 2. Also displayed on figure 17 are the performance curves for the single integration a.d.m. system, whose snr at $f_p = 64KHz$ is substantially the same as the double integration a.d.m. system at $f_p = 32KHz$. There is however, more distortion in this double integration a.d.m. at high input signal levels.

Effect of logic control parameters on snr.

The effect of the logic control parameters Z_1, Z_2, Z_3, on snr for the FX-209 double integration a.d.m. system having the parameters stated in the last section is shown in figure 18. The best results are achieved when Z_1, Z_2, Z_3 are all logical zeros.

FX-209 ABRIDGED OPERATING NOTES

Supply voltage range		-10V to -16V
Supply current		approx -10mA @ -12V

(Note: Supply polarities expressed in PMOS terminology, Vdd is -ve. Device may be operated with positive or negative grounded supplies).

Clock frequency range		2kHz to 125kHz
Clock threshold		-1.5V to -5V according to supply
Clock rise-time		level triggered, rise-time non-critical
Logic output		open drain switch, R'on 1k-ohm max output current -10mA max.
Multiplex Input		apply positive (ground) to open circuit logic output.
Z1, Z2, Z3 inputs		logical '0' = positive logical '1' = negative or open circuit
Buffer output (pin 11)		decoded signal centred about negative bias level, Z'out approx 30k-ohms.
Temperature range	operating	-30 to +85°C.
	storage	-55 to +125°C.

Further Reading

"Delta Modulation Systems", Dr.R.Steele, Pentech Press, London WC1N 2HY
Dr. Steele is consultant to Consumer Microcircuits Ltd.

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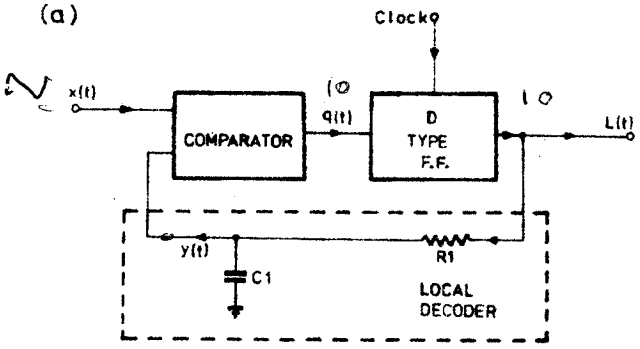
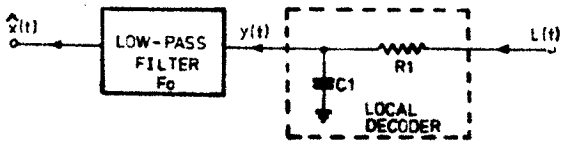
LINEAR DELTA MODULATION SYSTEM

(a)



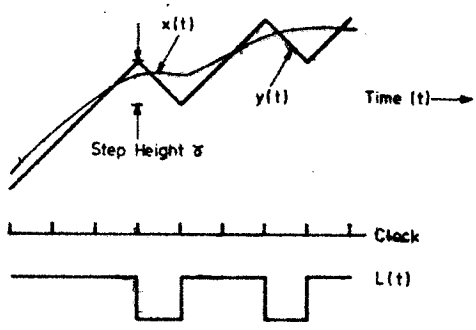
ENCODER

(b)



DECODER

FIG. 1



ENCODE

DECODE

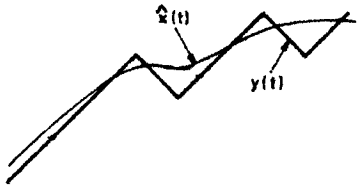
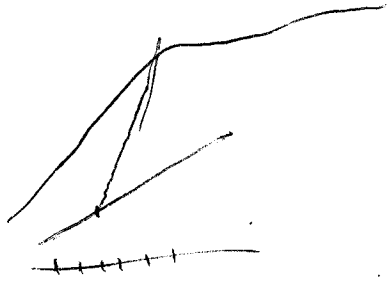
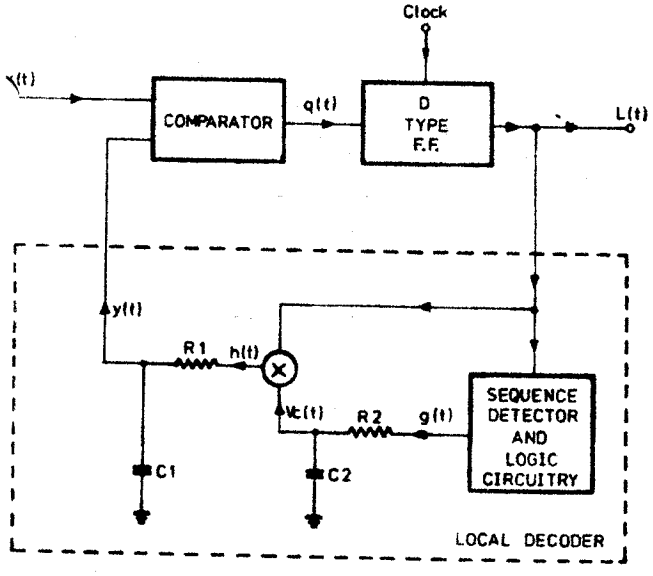


FIG. 2



ADAPTIVE DELTA MODULATION SYSTEM



FX 209 AS DELTA MODULATOR

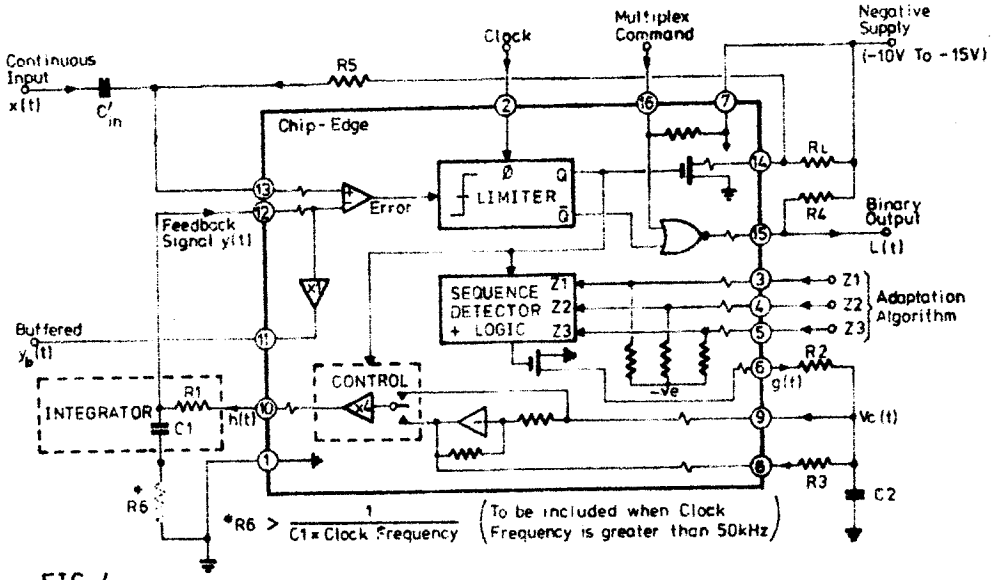


FIG. 4

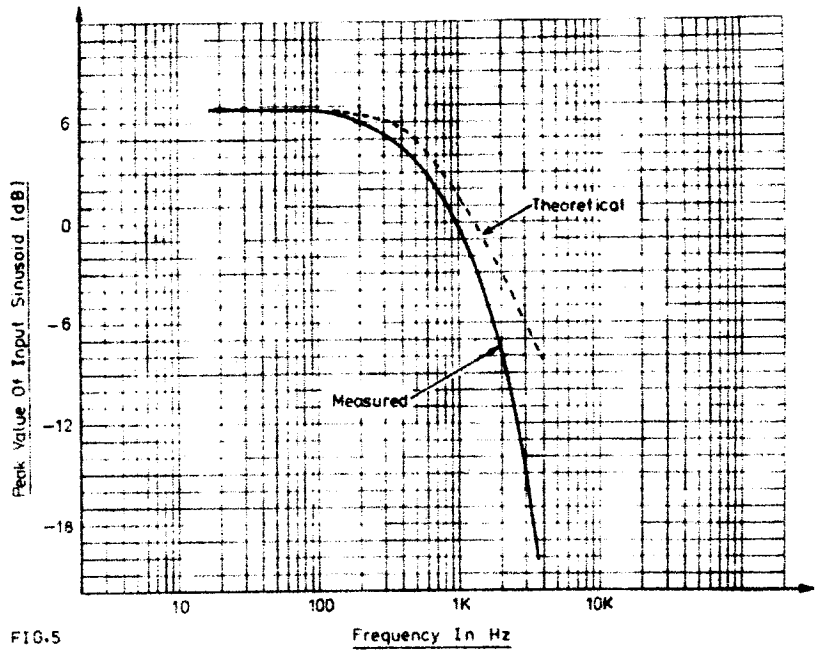
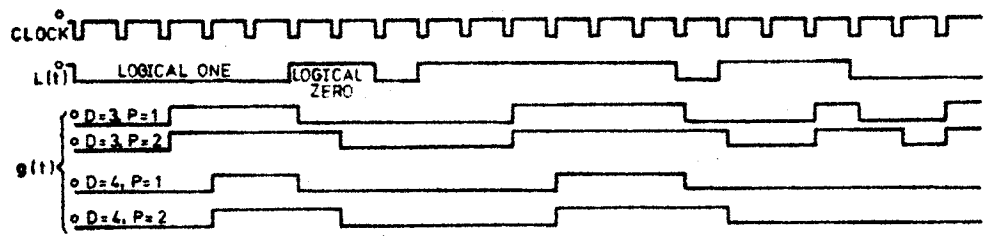


FIG.5

EXAMPLES OF WAVEFORMS FOR VARIOUS ADAPTION ALGORITHMS



N.B. g(t) appearing at pin 6 is generated by an open drain type output. Logic 1 = O.C. Logic 2 = S.C.

TABLE. 1

Z1	Z2	Z3	D	P	Z1	Z2	Z3	D	P
0	0	0	3	1	1	0	0	4	4
0	0	1	3	2	1	0	1	5	1
0	1	0	4	1	1	1	0	5	2
0	1	1	4	2	1	1	1	5	4

FIG. 6

FX 209 AS DELTA MODULATOR DECODER

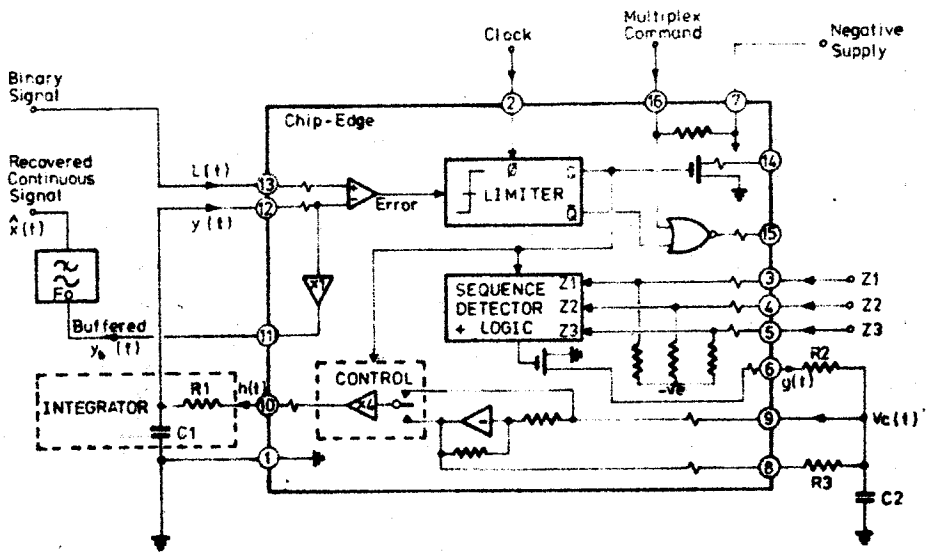


FIG. 7

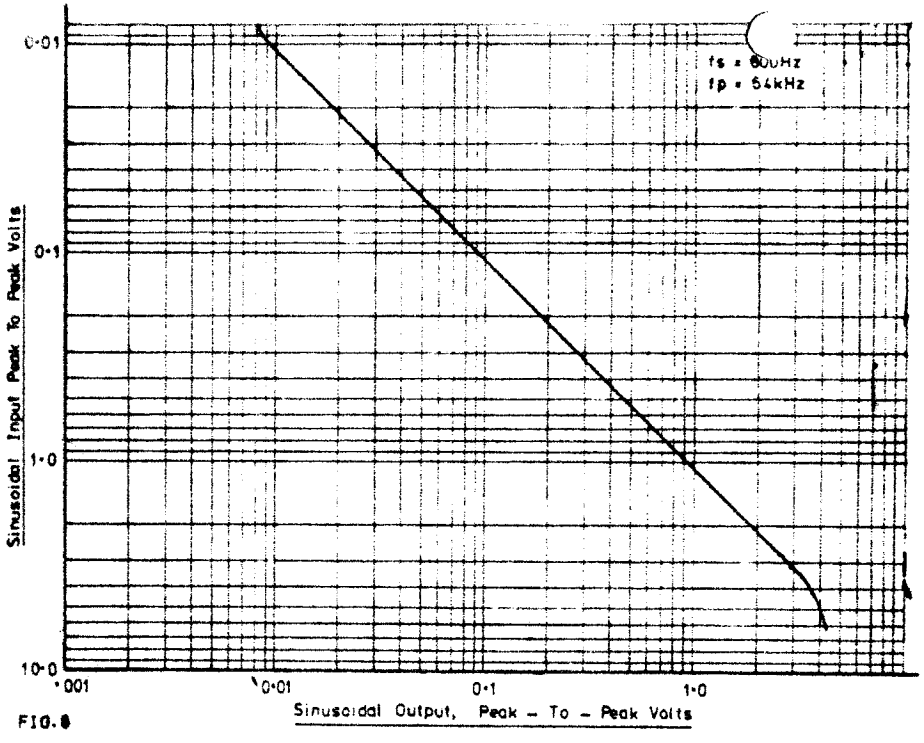


FIG.8

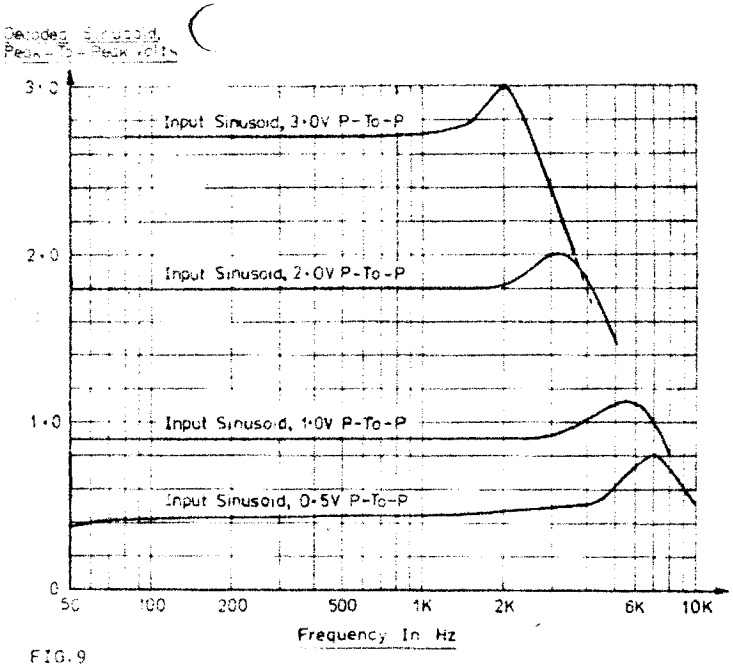
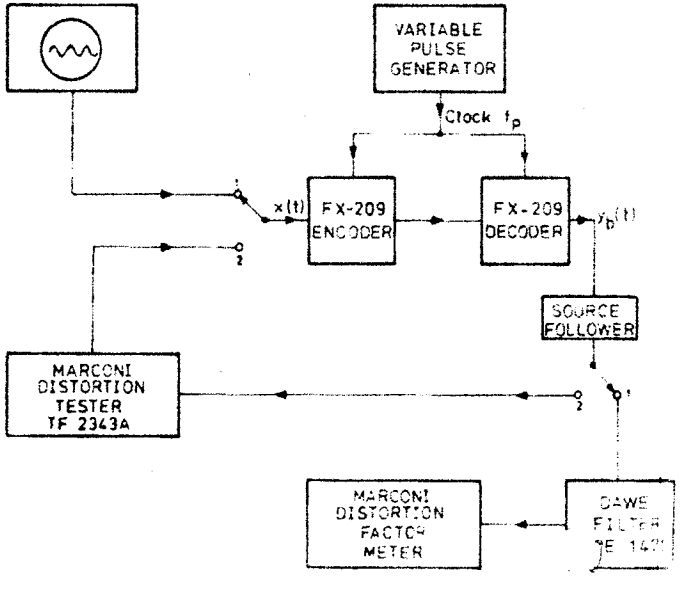
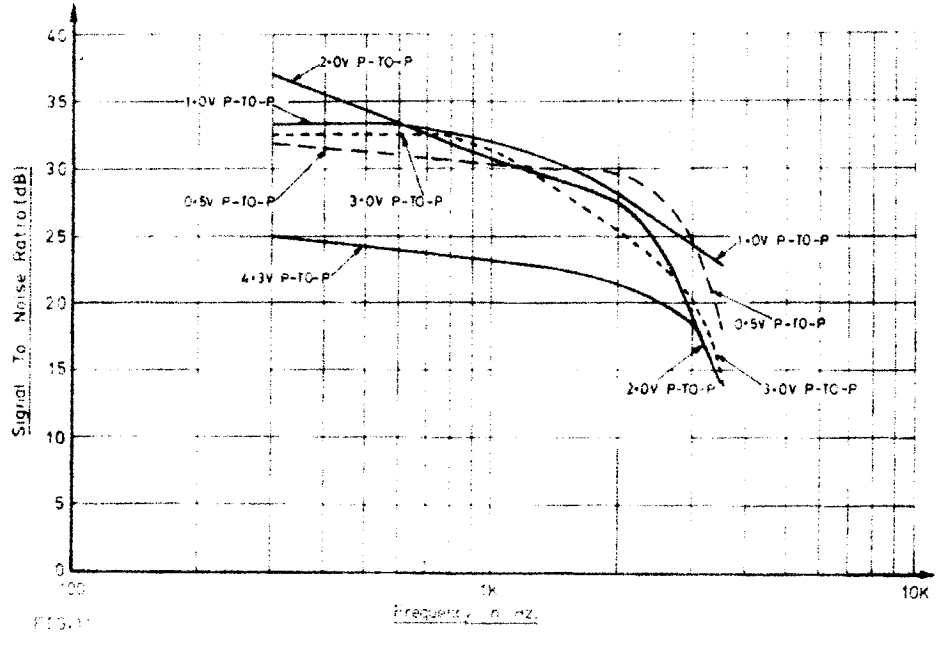


FIG.9

TEST ARRANGEMENT FOR MEASURING SIGNAL-TO-NOISE RATIO





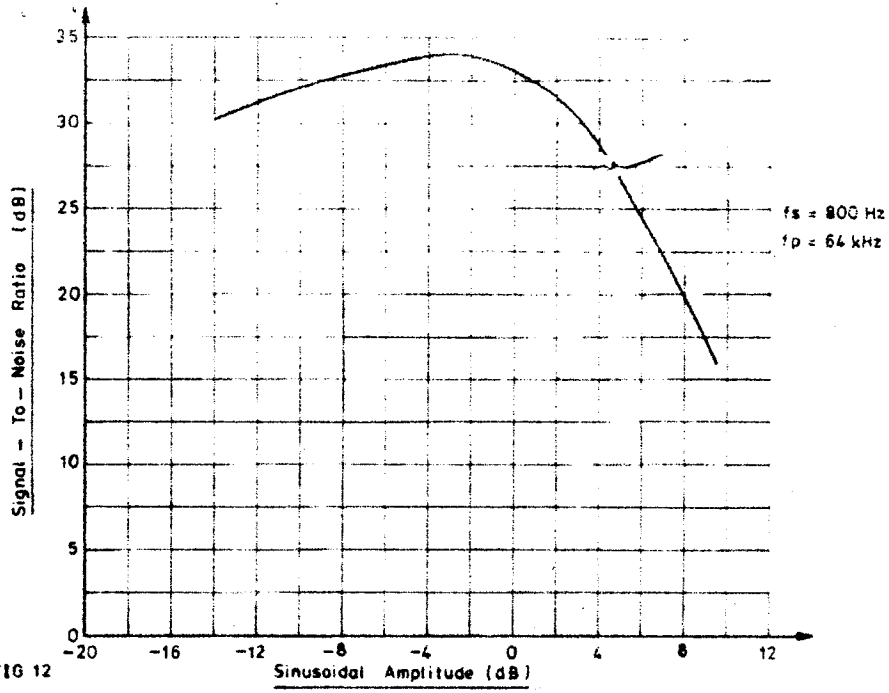


FIG 12

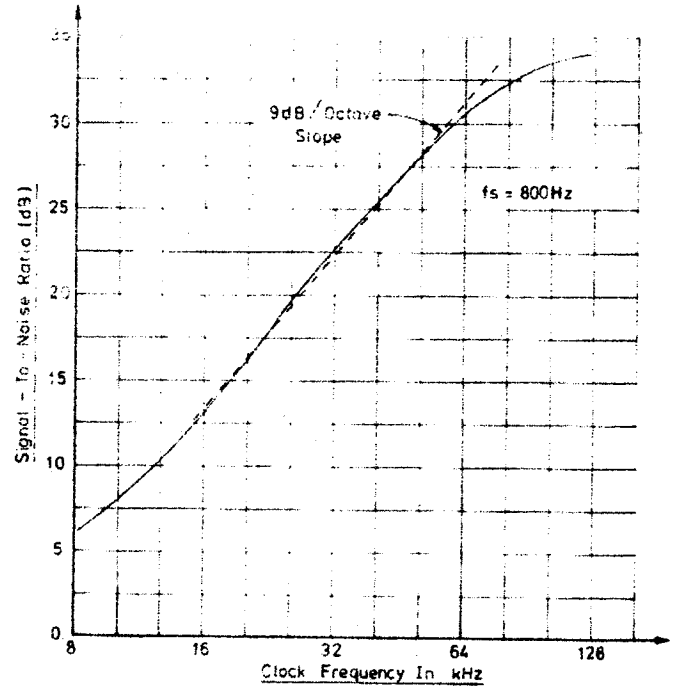
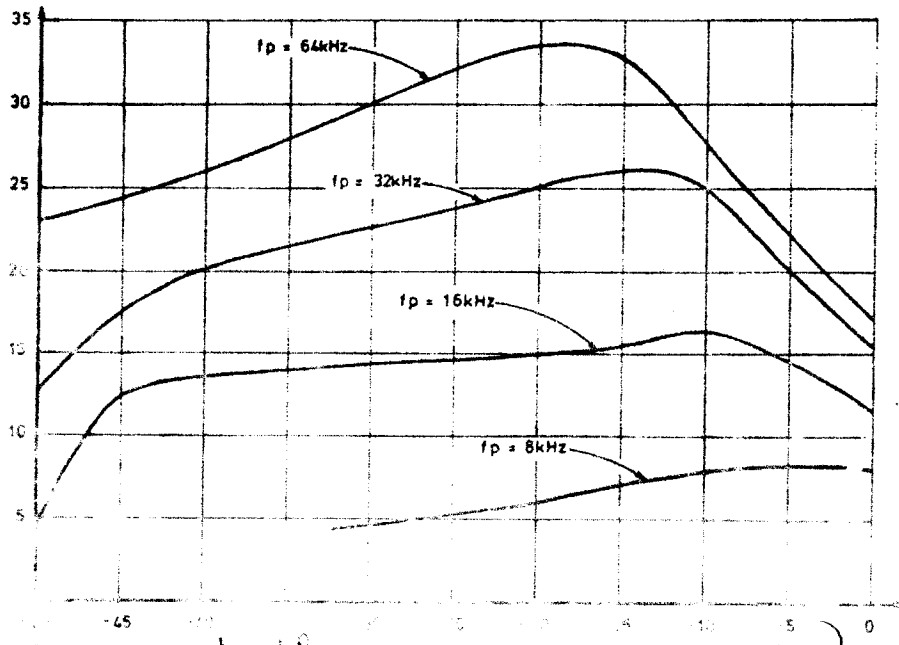
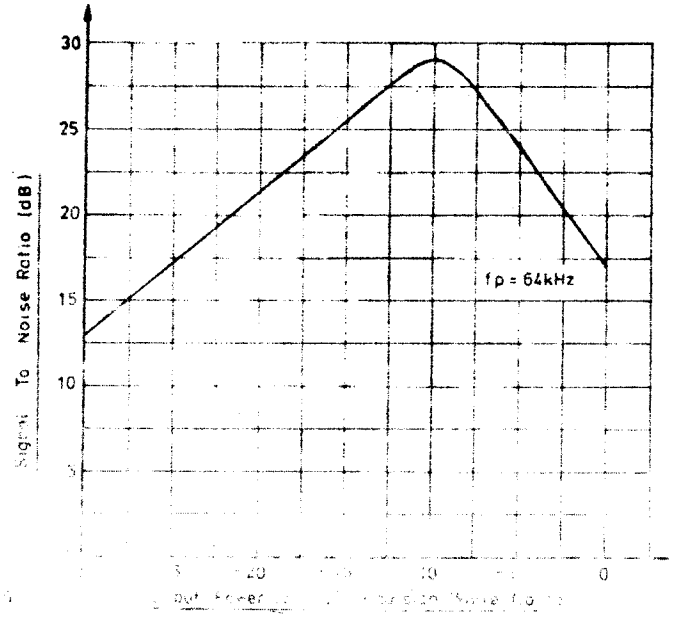


FIG 13





Input Power Gaussian White Noise

DOUBLE INTEGRATOR ARRANGEMENT

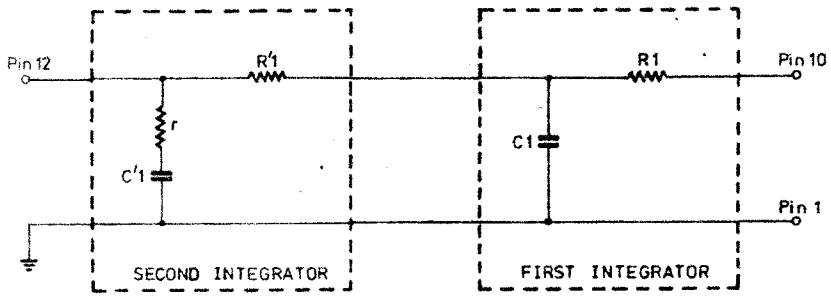


FIG 16

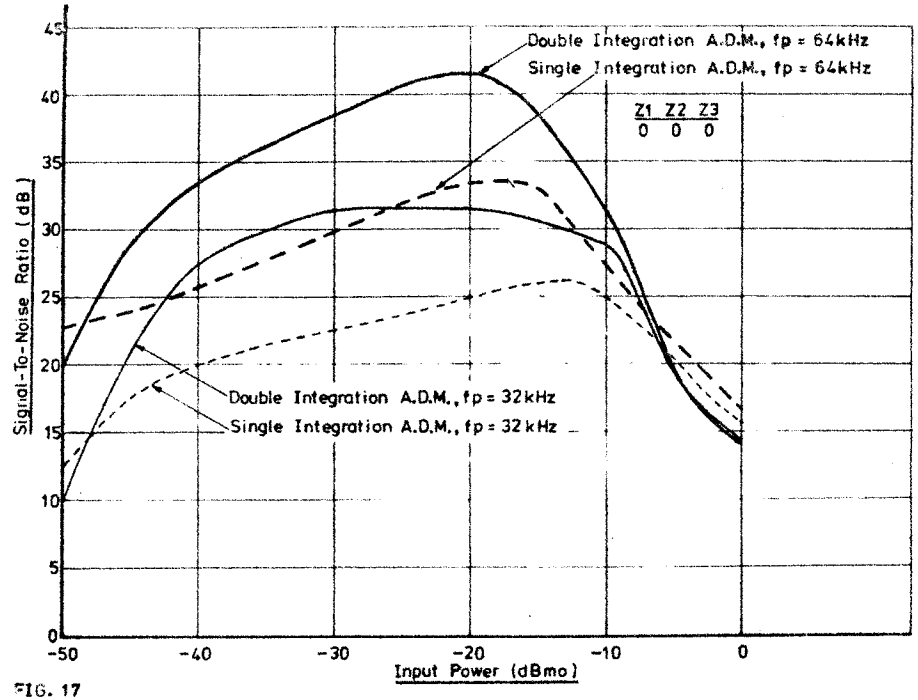
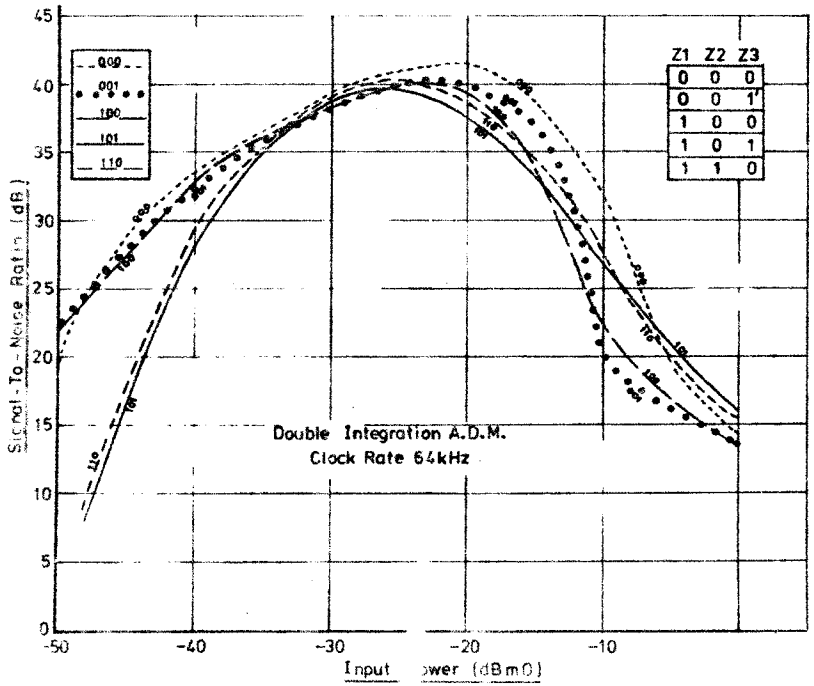


FIG. 17



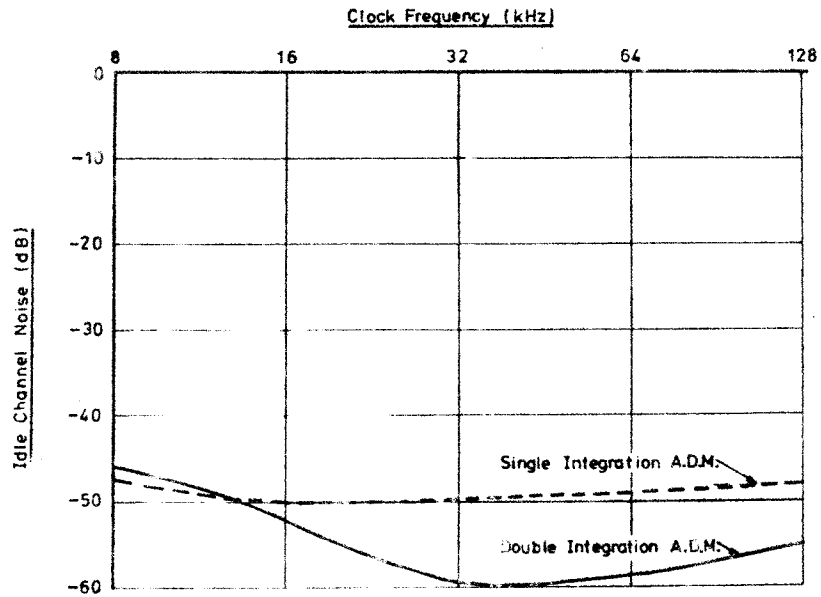


FIG. 19