FTE150N10N-1

N-Channel MOSFET

Lead Free Package and Finish

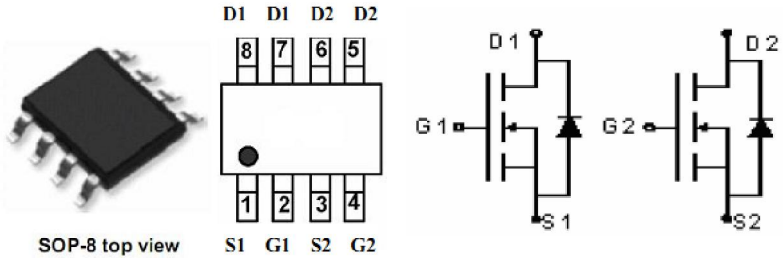
Applications:

- Adaptor
- Charger
- SMPS

V_{DSS}	$R_{DS(ON)}$ (Typ.VGS=10V)	I_D
100V	113mΩ	4A

Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves



Ordering Information

PART NUMBER	PACKAGE	BRAND
FTE150N10N-1	SOP-8	***IPS***

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	FTE150N10N-1	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current	4	A
	Continuous Drain Current TC = 100 °C	3	A
I_{DM} [a1]	Pulsed Drain Current	16	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS} [a2]	Avalanche Energy	28.8	mJ
I_{AS} [a2]	Avalanche Current	7.6	A
P_D	Power Dissipation	2	W
	Derating Factor above 25°C	0.016	W/℃
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃
T_L	MaximumTemperature for Soldering	300	℃

Thermal Resistance

Symbol	Parameter	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	62.5	℃/W

OFF Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	--	--	V	V_{GS}=0V, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	V_{DS}=100V, V_{GS}=0V T_J=25℃
		--	--	100		V_{DS}=80V, V_{GS}=0V T_J=125℃
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	V_{GS}=+20V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}= -20V

ON Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	StaticDrain-to-Source On-Resistance(NOTE *3)	--	113	150	mΩ	V_{GS}=10V, I_D=4A
			135	190	mΩ	V_{GS}=4.5V, I_D=3A
$V_{GS(TH)}$	Gate Threshold Voltage	1.8	2.4	2.9	V	V_{DS}=V_{GS},I_D=250μA

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_g	Gate resistance		3.4		Ω	V_{GS}= 0V,V_{DS} = 0V f =1.0MHz
C_{iss}	Input Capacitance	--	556.5	--	pF	V_{GS}= 0V,V_{DS} = 50V f =1.0MHz
C_{oss}	Output Capacitance	--	34.7	--		
C_{rss}	Reverse Transfer Capacitance	--	18.7	--		
Q_g(10V)	Total Gate Charge	--	11.5	--	nC	I_D=4A,V_{DD}=50V V_{GS} = 10V
Q_g(4.5V)			5.8			
Q_{gs}	Gate-to-Source Charge	--	2.2	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	2.6	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	8.5	--	ns	V_{DD}=50V, I_D=4A, V_G=10V R_G=3Ω
t_{rise}	Rise Time	--	6.3	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	29.2	--		
t_{fall}	Fall Time	--	3.2	--		

Source-Drain Diode Characteristics Tc=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	4	A	T_C=25℃
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	16	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_{SD}=4A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	59.2	--	ns	I_F= I_S di/dt=100A/us
Q_{rr}	Reverse Recovery Charge	--	107.7	--	nC	

Notes:

*1. Repetitive rating; pulse width limited by maximum junction temperature.

*2. L=1.0mH, I_D=7.6A, Start T_J=25℃

Characteristics Curve：

Figure 1.Maximum Effective Thermal Impedance，Junction-to- Ambient

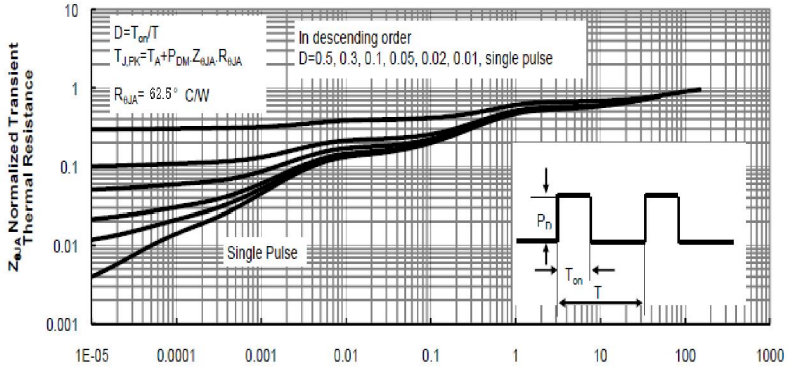


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

Figure 2.Typical Output Characteristics

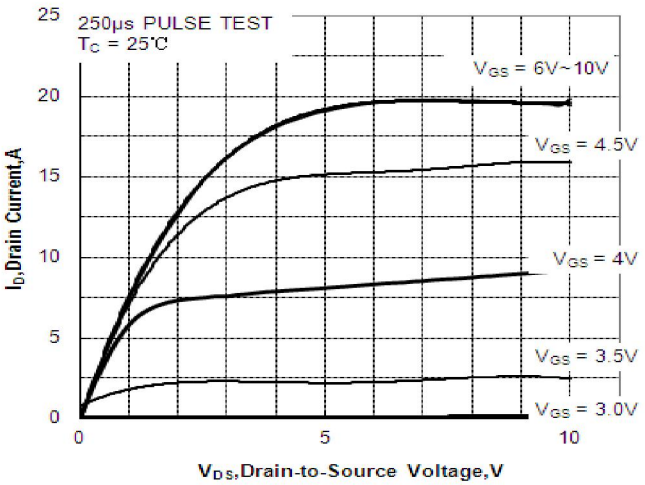


Figure 3. Typical Transfer Characteristics

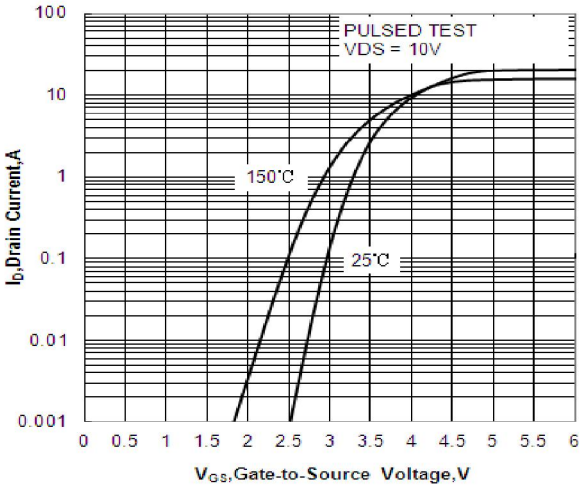


Figure 4. Typical Body Diode Transfer Characteristics

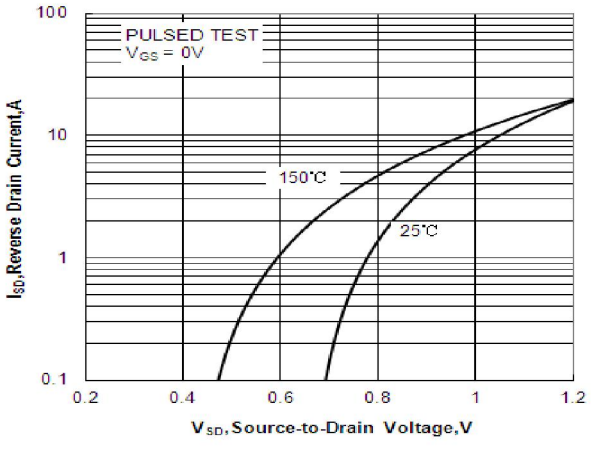


Figure 5. Typical on Resistance VS Drain Current

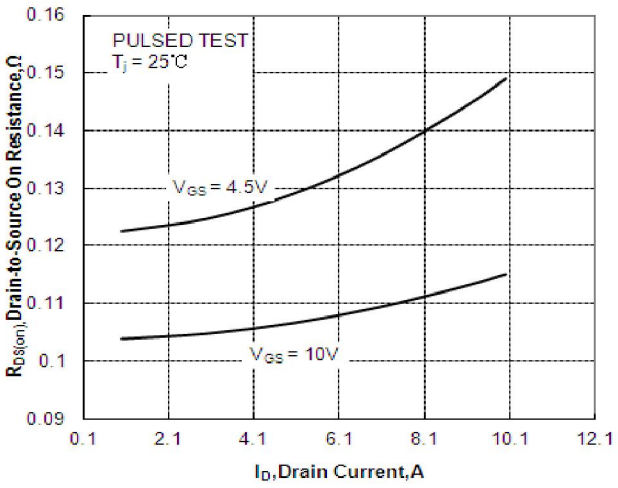


Figure6. Capacitance VS Drain-to-Source Voltage

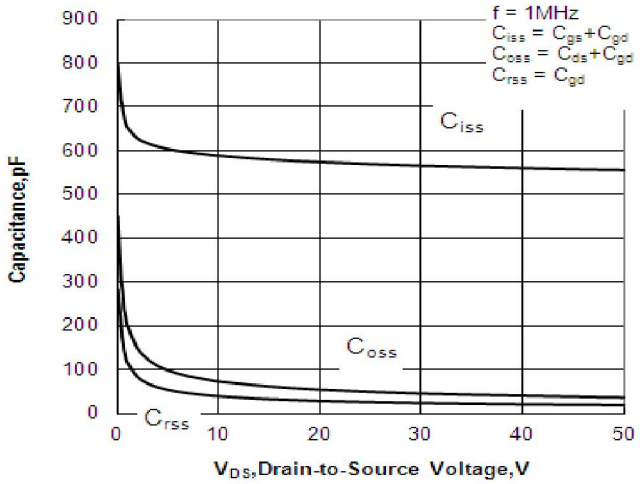


Figure 7. Gate Charge VS Gate-to-Source Voltage

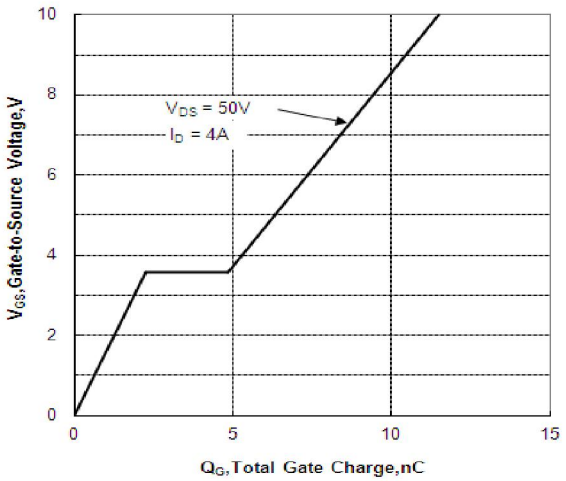


Figure 8. Breakdown Voltage VS Temperature

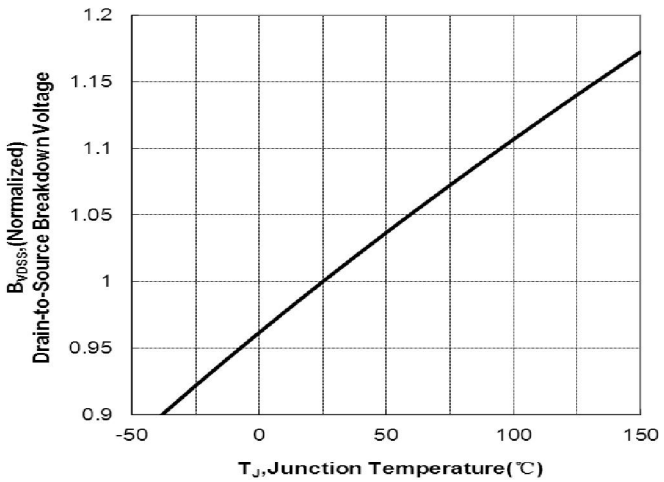


Figure 9. on-Resistance VS Temperature

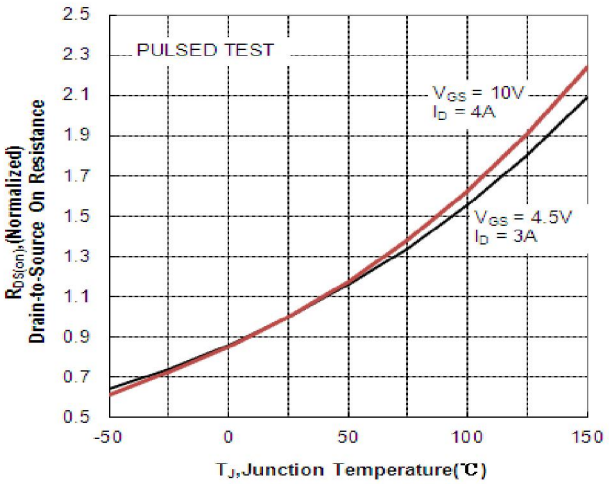


Figure 10. Resistance vs Gate-to-Source Voltage

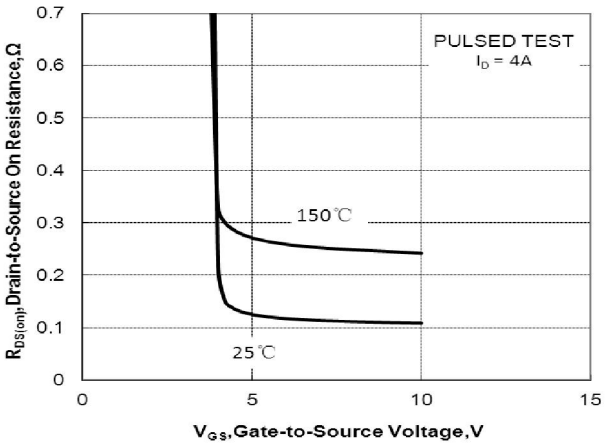


Figure 11. Typical Threshold Voltage vs Junction Temperature

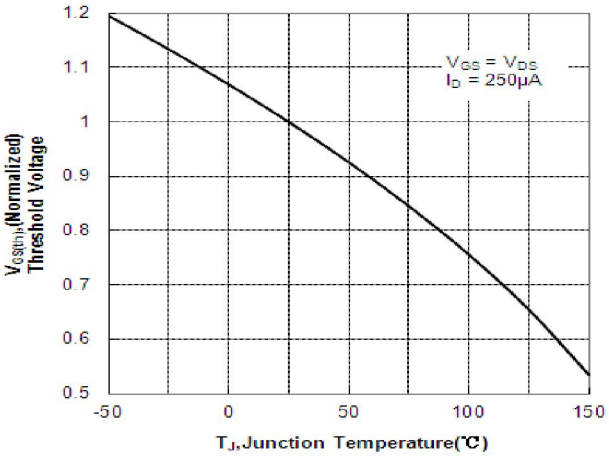
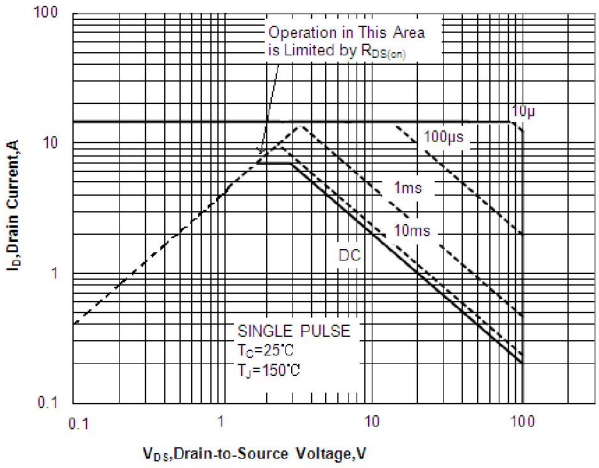


Figure 12. Safe Operating Area



Test Circuits and Waveforms

Figure 13. Gate Charge Test Circuit

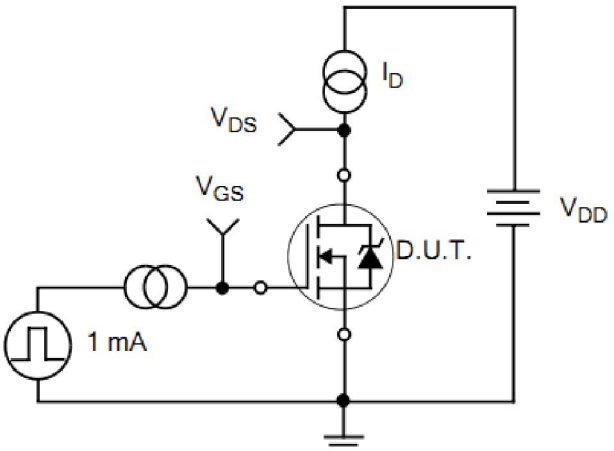


Figure 14. Gate Charge Waveforms

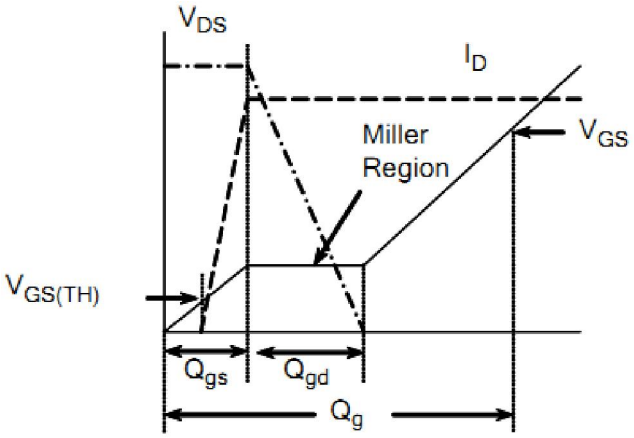


Figure 15. Resistive Switching Test Circuit

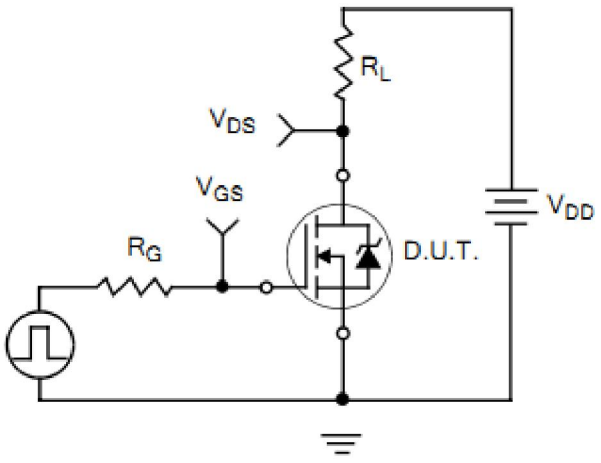


Figure 16. Resistive Switching Waveforms

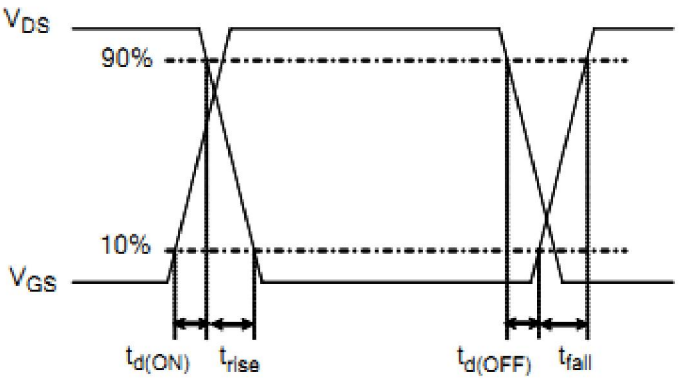


Figure 17. Diode Reverse Recovery Test Circuit

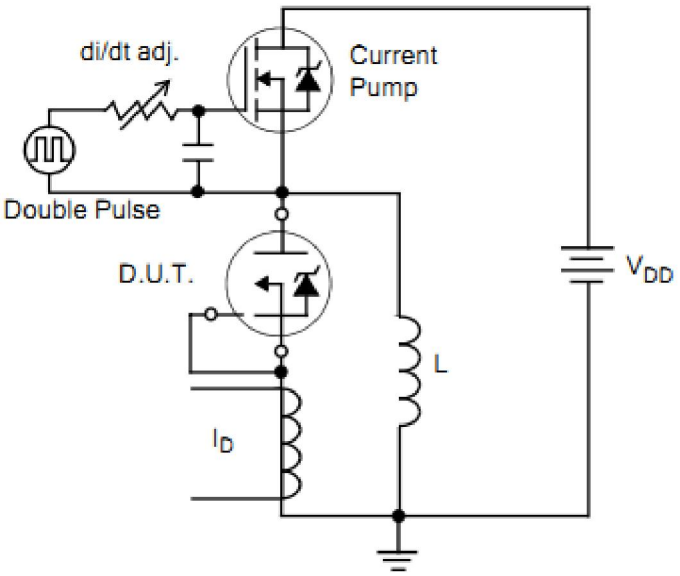


Figure 18. Diode Reverse Recovery Waveform

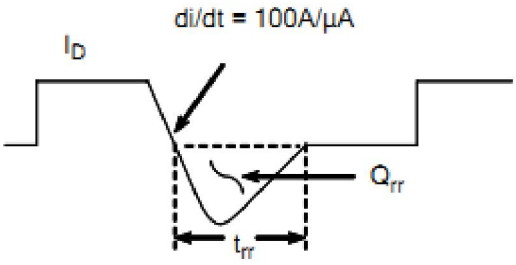


Figure19.Unclamped Inductive Switching Test Circuit

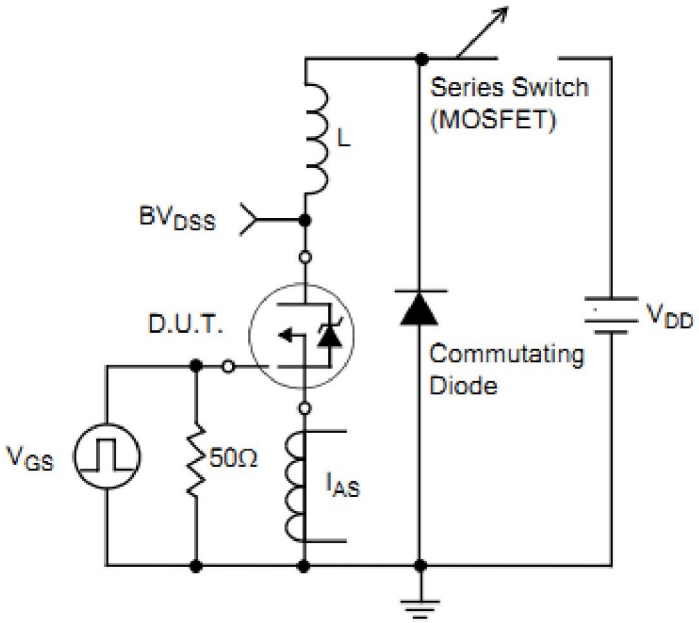
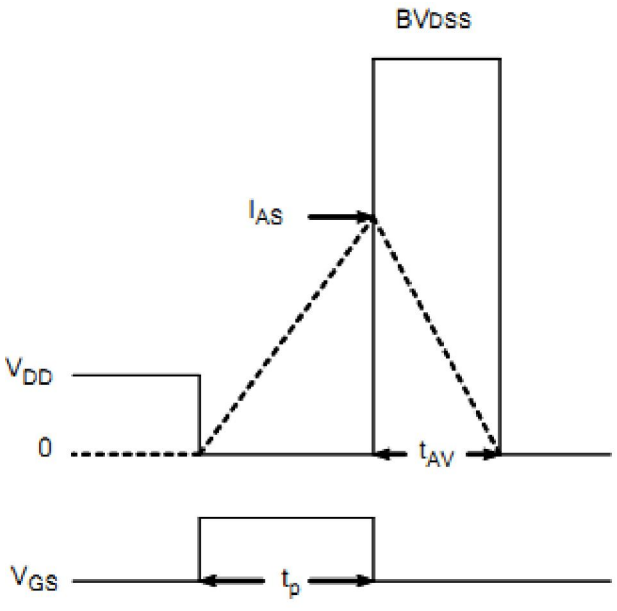


Figure20.Unclamped Inductive Switching Waveform



$$E_{AS} \quad \frac{I_{AS}^{2} L}{2}$$

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