FTB1404

N-Channel MOSFET

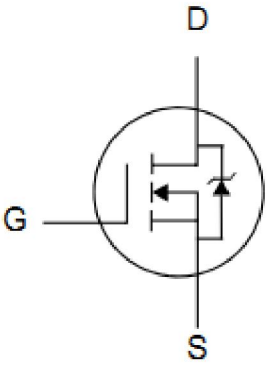
Lead Free Package and Finish

Applications:
- Adaptor
- Charger
- SMPS

V_{DSS}	$R_{DS(ON)}$(Typ.)	I_D (Silicon limited current)
40V	3.8mΩ	202A

Features:
- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves

Packages
Not to Scale



Ordering Information

PART NUMBER	PACKAGE	BRAND
FTB1404	TO-263	***IPS***

Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter	FTB1404	Units
V_{DSS}	Drain-to-Source Voltage	40	V
I_D	Continuous Drain Current	202	A
	Continuous Drain Current T_C =100℃	143	A
I_{DM}	Pulsed Drain Current (NOTE *1)	808	A
P_D	Power Dissipation	271	W
	Derating Factor above 25℃	2.16	W/℃
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy(NOTE *2)	519	mJ
T_L	Maximum Temperature for Soldering	300	℃
T_J and T_{STG}	Operating Junction and Storage Temperature Range	150，-55 to150	

Thermal Resistance

Symbol	Parameter	Max	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	0.46	℃/W	Water cooled heatsink, P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.

OFF Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	40	--	--	V	V_{GS}=0V, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	V_{DS}=40V, V_{GS}=0V T_J=25℃
		--	--	100		V_{DS}=32V, V_{GS}=0V T_J=125℃
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	V_{GS}=+20V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}= -20V

ON Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	StaticDrain-to-Source On-Resistance	--	3.8	5	mΩ	V_{GS}=10V, I_D=81A
$V_{GS(TH)}$	Gate Threshold Voltage	2	--	4	V	V_{DS}=V_{GS},I_D=250μA
Pulse width ≤300μs; duty cycle≤ 2%						

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	5431	--	pF	V_{GS}= 0V,V_{DS} = 25V f =1.0MHz
C_{oss}	Output Capacitance	--	1542	--		
C_{rss}	Reverse Transfer Capacitance	--	170	--		
Q_g	Total Gate Charge	--	103.6	--	nC	I_D=81A,V_{DD}=32V V_{GS} = 10V
Q_{gs}	Gate-to-Source Charge	--	20	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	33.2	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	29.1	--	ns	V_{DD}=20V, I_D=81A, V_{GS}=10V R_G=2.5Ω
t_{rise}	Rise Time	--	27.5	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	85.3	--		
t_{fall}	Fall Time	--	35.7	--		

Source-Drain Diode Characteristics Tc=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	202	A	T_C=25℃
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	808	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_{SD}=95A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	1708	--	ns	I_S= 10A
Q_{rr}	Reverse Recovery Charge	--	4.36	--	uC	di/dt=100A/us
Pulse width ≤300μs; duty cycle ≤ 2%						

Notes:

*1. Repetitive rating; pulse width limited by maximum junction temperature.

*2. L=0.12mH, I_D=95A, Start T_J=25℃

Characteristics Curve：

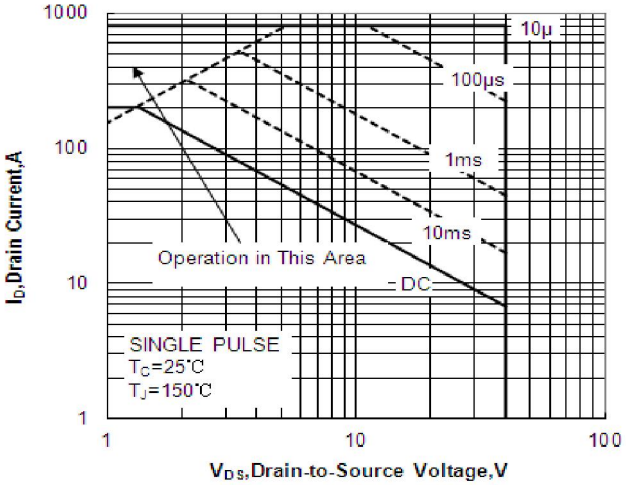


Figure1 Maximum Forward Bias Safe Operating Area

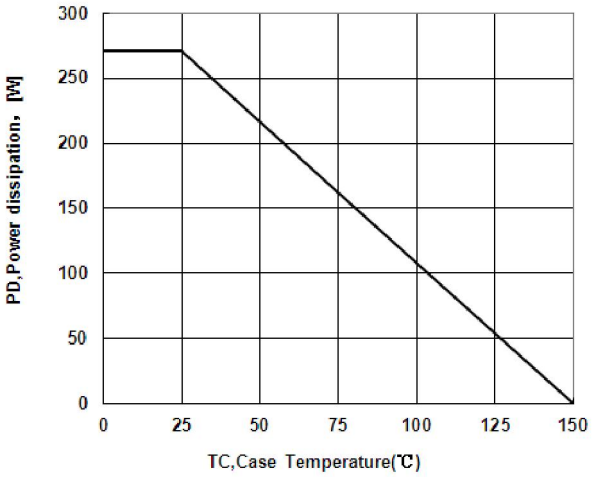


Figure 2 Maximum Power Dissipation vs Case Temperature

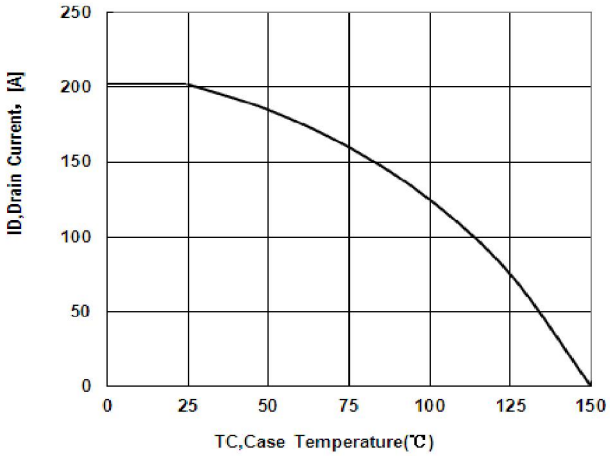


Figure 3 Maximum Continuous Drain Current vs Case Temperature

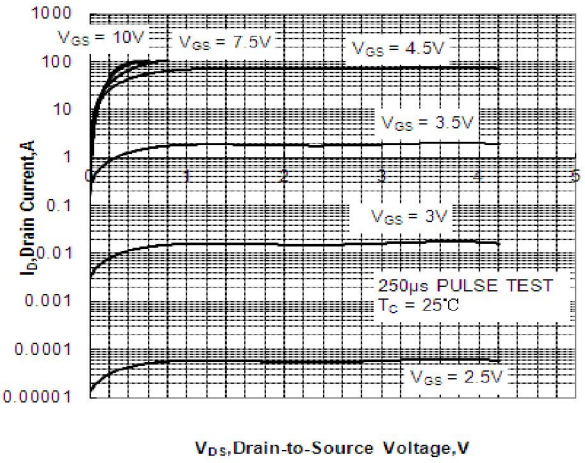


Figure 4 Typical Output Characteristics

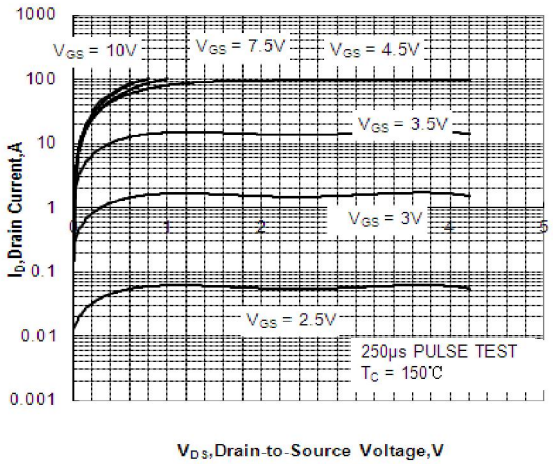


Figure 5 Typical Output Characteristics

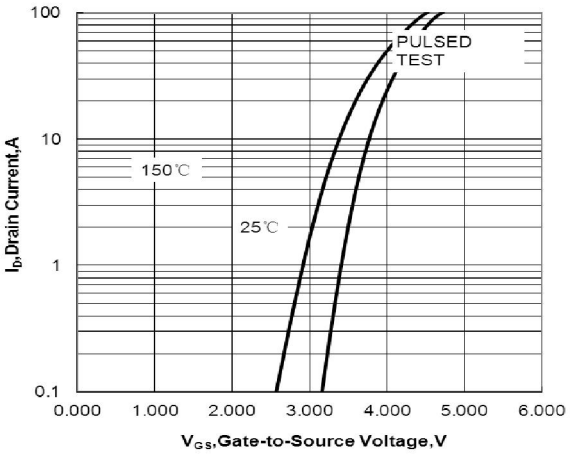


Figure 6 Typical Transfer Characteristics

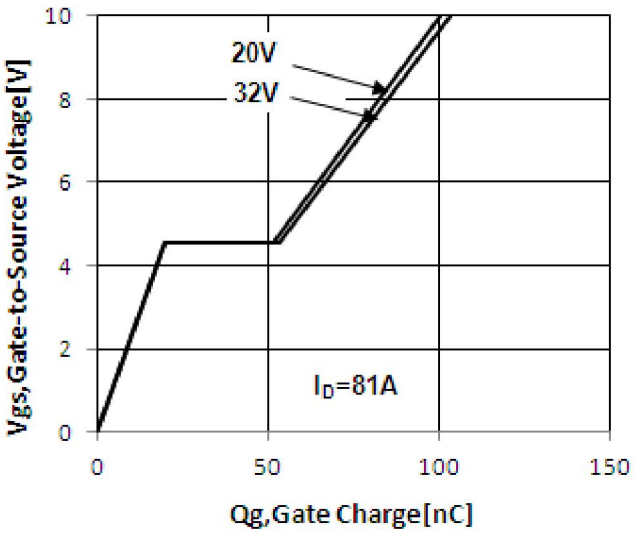


Figure 7 Typical Gate Charge vs Gate to Source Voltage

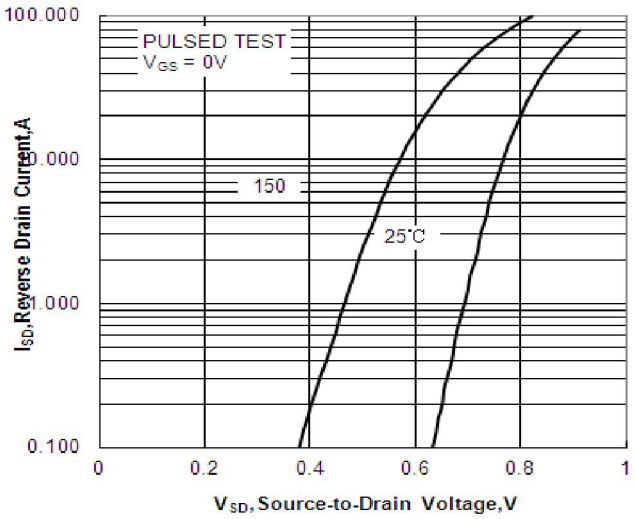


Figure 8 Typical Body Diode Transfer Characteristics

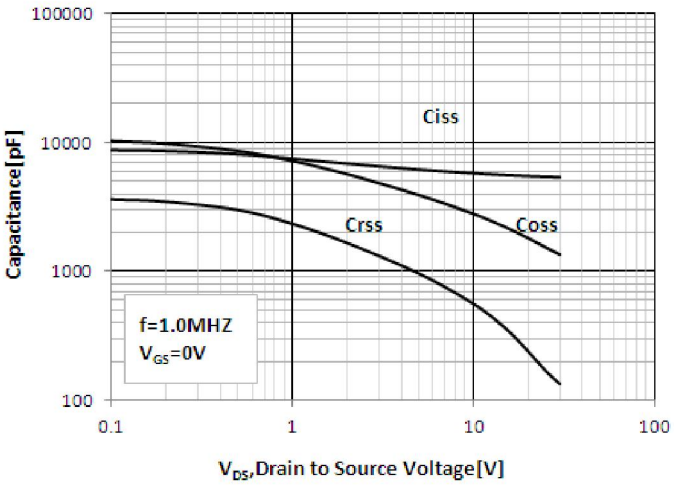


Figure 9 Typical Capacitance vs Drain to Source Voltage

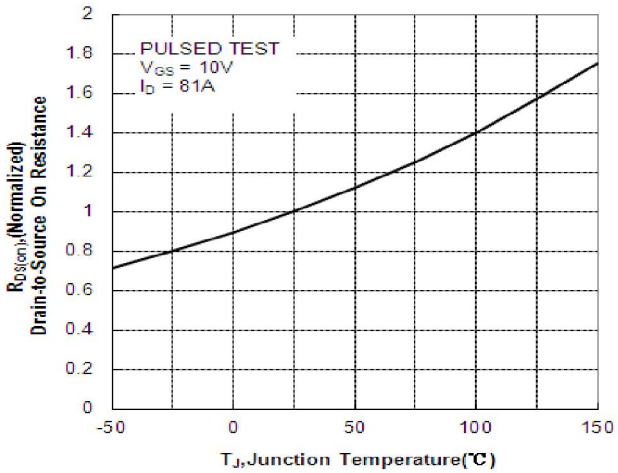
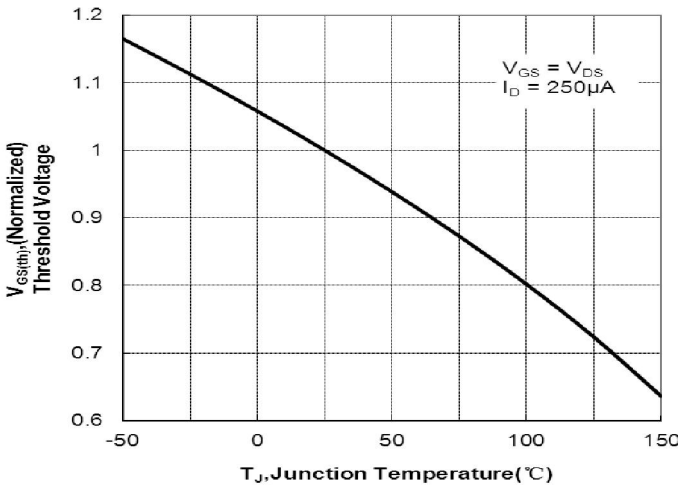
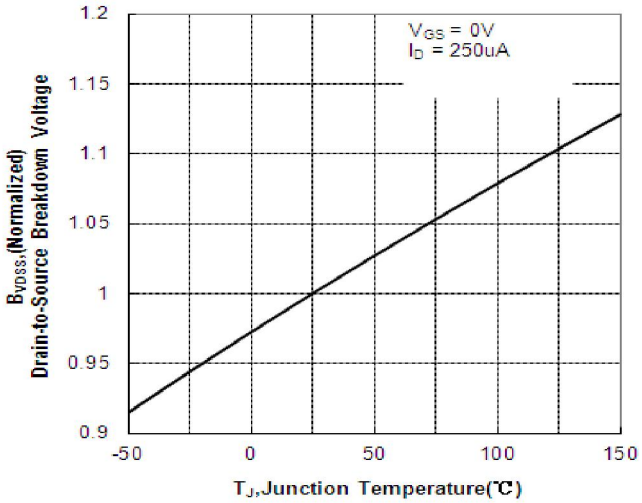


Figure 10 Typical Drian to Source on Resistance vs Junction Temperature





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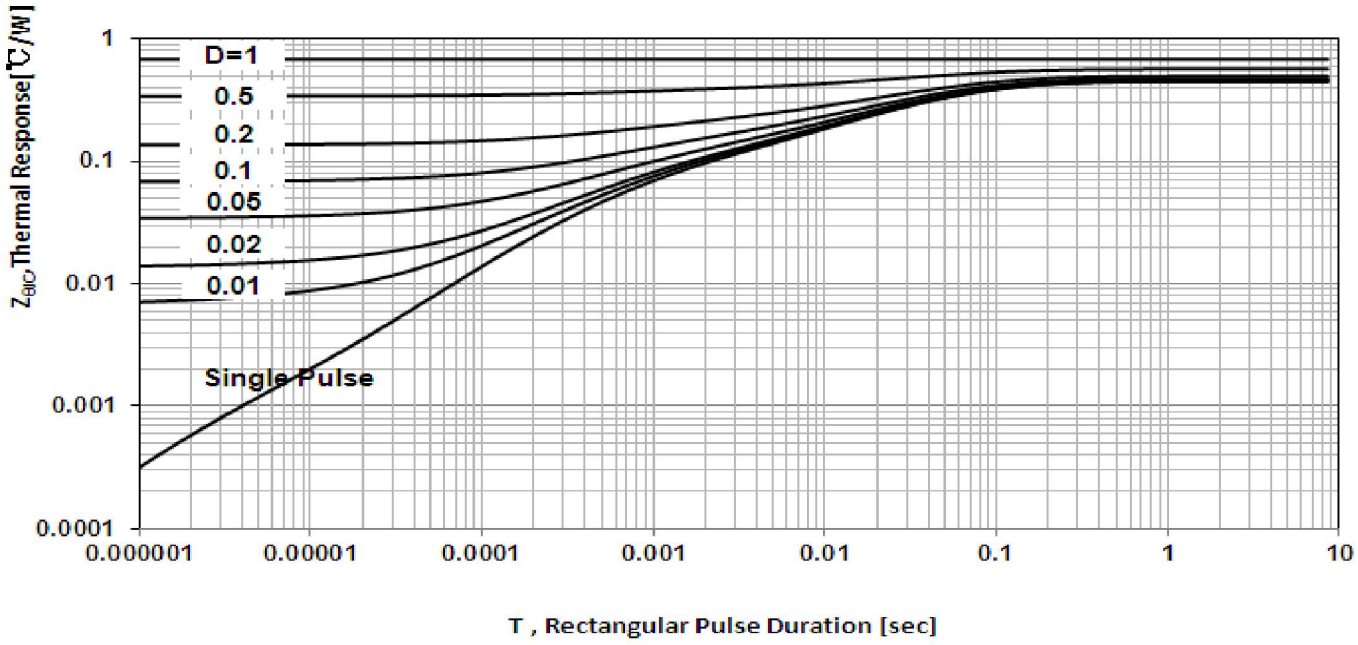


Figure 13 Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test Circuits and Waveforms

Figure 14. Gate Charge Test Circuit

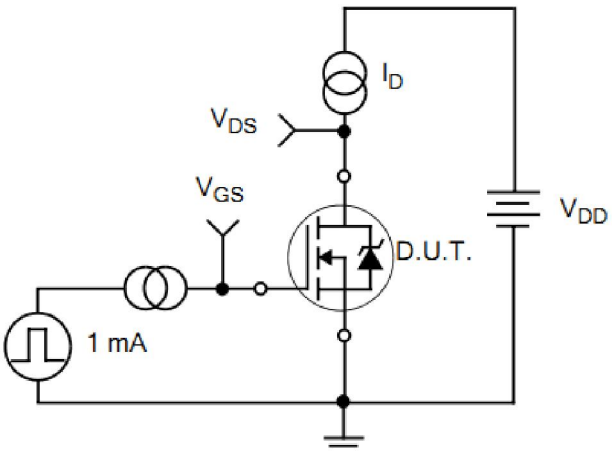


Figure 15. Gate Charge Waveforms

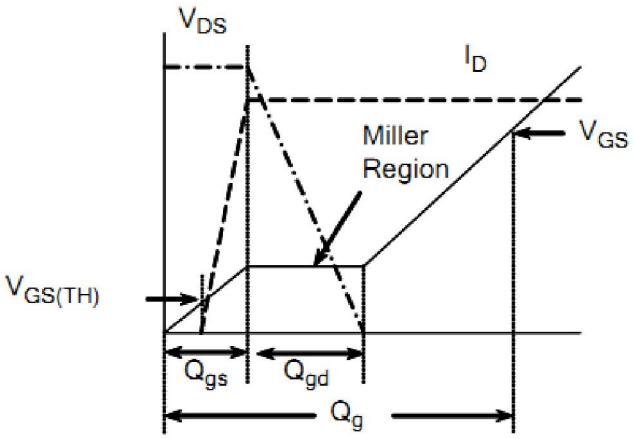


Figure 16. Resistive Switching Test Circuit

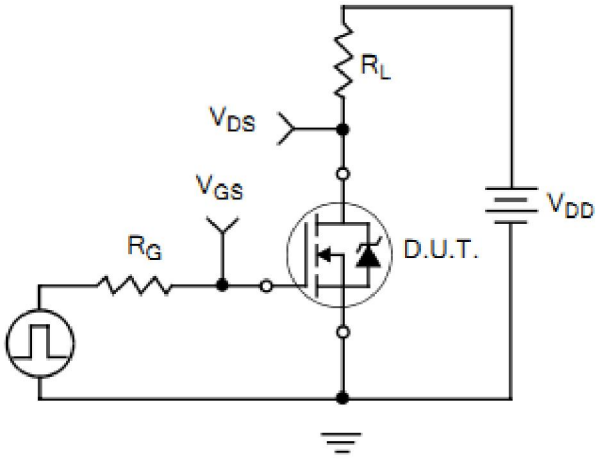


Figure 17. Resistive Switching Waveforms

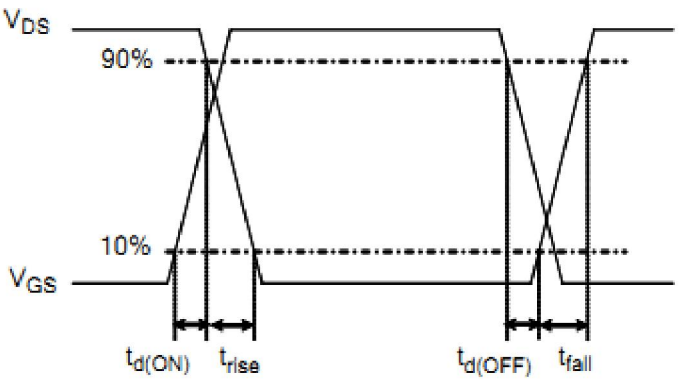


Figure 18. Diode Reverse Recovery Test Circuit

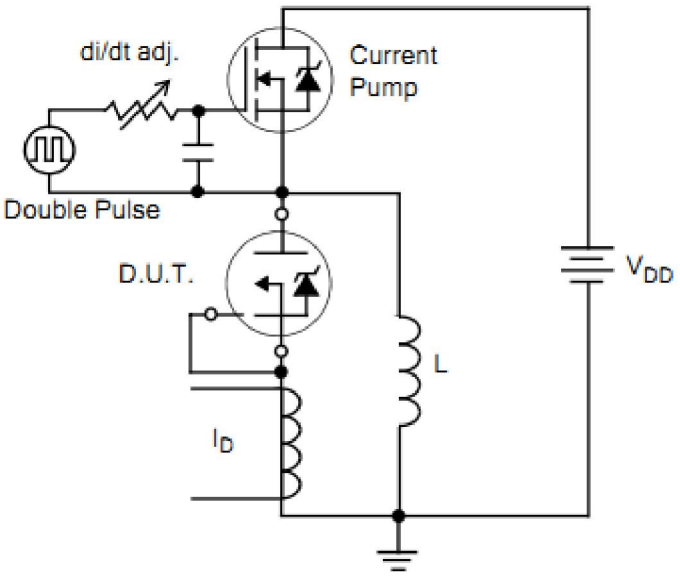


Figure 19. Diode Reverse Recovery Waveform

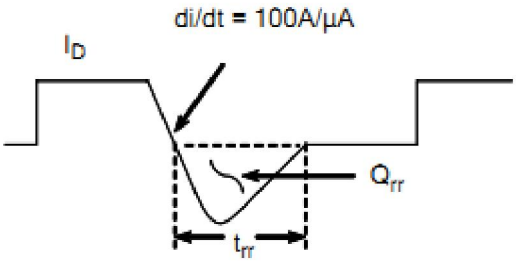


Figure20.Unclamped Inductive Switching Test Circuit

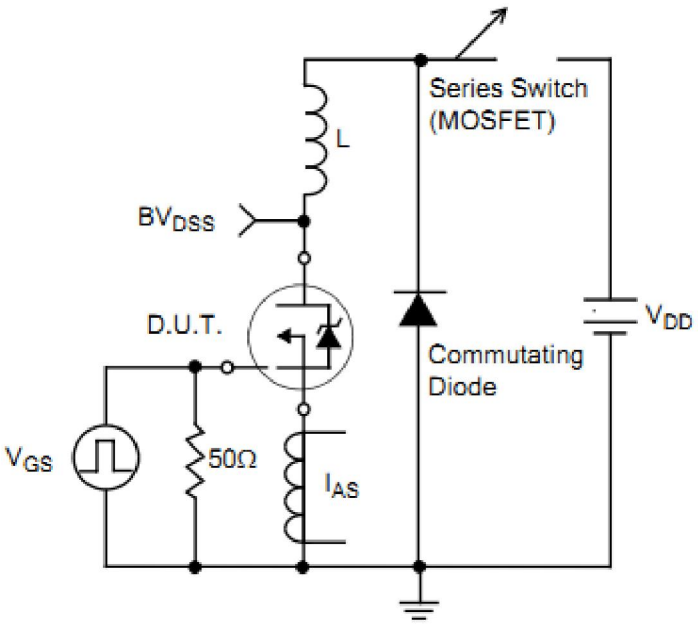
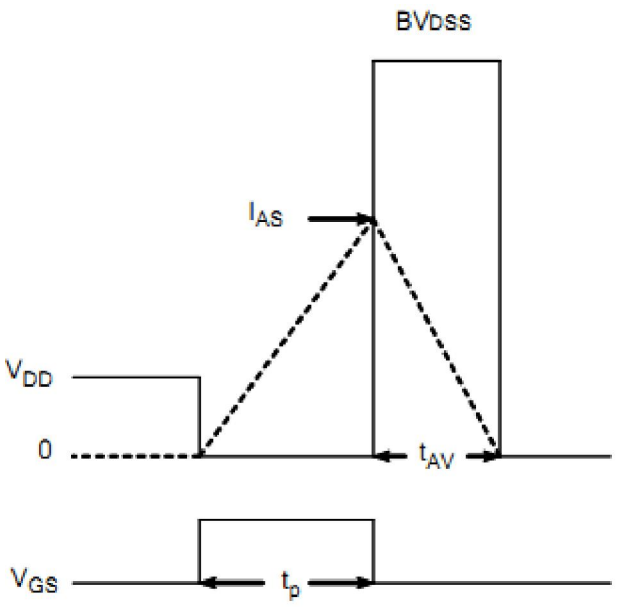


Figure21.Unclamped Inductive Switching Waveform



$$E_{AS} \quad \frac{I_{AS}{}^2 L}{2}$$

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