Product Data Sheet

Doc# : D-FT5202-0902 (Version : 1.0)
DDCN# : 201001002

Date: 21-Jan-10

FT5202

Capacitive Touch Panel controller

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Index

Product Data Sheet

FocalTech

Doc# : D-FT5202-0902 (Version : 1.0)

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1. Description

FT5202 series ICs are single chip capacitive touch panel controller ICs with a built-in 8 bit Micro-controller unit (MCU). It adopts the mutual capacitance approach, which supports true multi-touch capabilities. In conjunction with a mutual capacitive touch panel, FT5202 facilitates user friendly input functions, which can be used for portable devices, such as cellular phones, digital cameras, and notebook personal computers.

2. Typical Applications

FT5202 accommodates a wide range of applications from with a set of buttons up to a 2D touch sensing device.

- Mobile phones, smart phones, PDAs
- Portable MP3 and MP4 media players
- Navigation systems, GPS
- Digital cameras
- Game consoles
- Car applications
- POS (Point of Sales) devices

3. Features

- Mutual capacitive sensing techniques
- True multi-touch with up to 5 points of absolution X and Y coordinates
- Immune to RF interferences
- Auto calibration: Insensitive to capacitance and environmental variations
- Supporting up to 16 transmit lines and 10 receive lines
- Supporting up to 7” touch screen (from 2.8” to 7”)
- Fully programmable scan sequences with individually adjustable receive lines and transmit lines to support various of applications
- Scan rate larger than 80Hz
- Touch resolution of 100 dots per inch (dpi) or higher -- depending on the panel size
- I2C interfaces
- Operating voltage: 2.8V ~ 3.6V

- Capable of driving single channel (transmit/receive) resistance: ~ 15K Ω
- Capable of supporting single channel (transmit/receive) capacitance: 50 pF
- The optimal sensing mutual capacitor: 1pF~2pF
- The accuracy of the ADC is 12bit
- Built-in MCU with 20KB of program SRAM, 4KB of data SRAM and 256B internal data space
- 11 internal interrupt sources and 2 external interrupt sources
- 3 operating modes
  Active
  Monitor
  Hibernate
- Operating temperature range: -40°C ~ +85°C
- System can be booted from both sources:
  Internal non-volatile memory
  An external host processor

4. Functional Description

4.1. Architectural Overview

Figure 4-1 shows the overall architecture for FT5202.

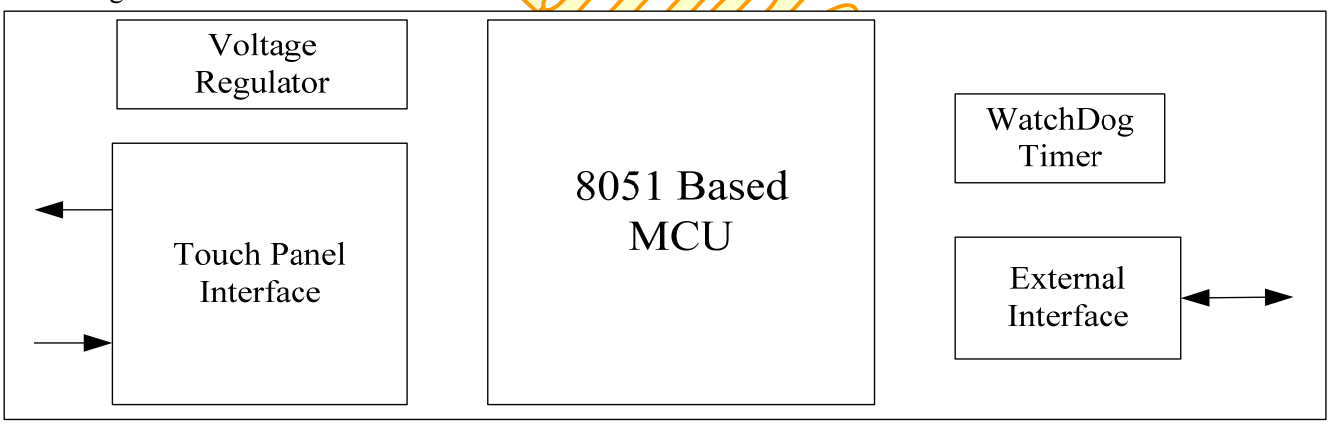


Figure 4-1 FT5202system architecture diagram

FT5202 can be divided into the following functional groups:

- Touch panel interface circuits

  The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. So, it supports both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces, which will be explained in detail in a later section.

- 8051 based MCU

  This MCU is 8051 compatible with some enhancements. For example, larger program and data memories are supported. In addition, a Multiplier Accumulator (MAC) unit is implemented to speed up the touch detection algorithms. Furthermore, a One Time Programmable (OTP) is implemented to store programs and some key parameters.

  Complex signal processing algorithms are implemented with firmware running on this MCU to further process the received signals in order to detect the touches reliably. Communication protocol software is also implemented on this MCU to exchange data and control information with the host processor.

  The MCU executes the program stored in the on chip program memory (SRAM). Upon power-up, the program can be downloaded (booted) from the following two sources:

  On chip OTP
  The FLASH connected to the host processor

  The detailed boot procedure will be discussed later.

- External Interface

  I2C: an interface for data exchange with host

  INT: an interrupt signal to inform the host processor that touch data is ready for read

  WAKE: an interrupt signal for the host to change F5202 from Hibernate to Active mode

- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input 3.3V supply

4.2. MCU

This section describes some critical features and operations supported by the 8051 compatible MCU. Figure 4-2 shows the overall structure of the MCU block. In addition to the 8051 compatible MCU core, we have added the following circuits:

MAC: A 16x8 multiplier with a 32 bit accumulator

Program memory: 20KB SRAM

Data memory: 4KB SRAM

Real time clock (RTC): A 32KHz RC oscillator

Timer: A number of timers are available to generate different clocks

Master clock: A 27MHz RC oscillator

Clock Manager: To control various clocks under different operation conditions of the system

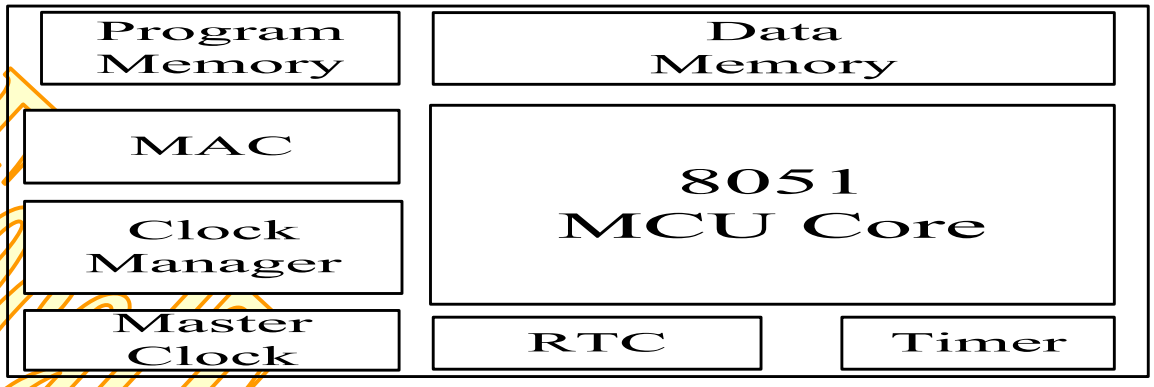


Figure 4-2 MCU block diagram

4.3. Operation Modes

FT5202 operates in the following three modes:

Active

Monitor

Hibernate

Active mode**:** When in this mode, FT5202 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT5202 to speed up or to slow down. The minimum scan period is 12 ms per frame.

Monitor mode**:** When in this mode, FT5202 scans the panel at a reduced speed. The default scan rate is 30 frames per second and the host processor can increase or decrease this rate. When in this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5202shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

Hibernate mode**:** In this mode, the chip is placed in a power down mode. It shall only respond to the "WAKE" signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

4.4. Boot

Upon power up, FT5202 shall load the program onto the program memory and start executing the program. This is called the boot procedure. The program can be booted with the following three methods:

- From an internal non-volatile memory
- From the Host through a serial interface

The user can select one of the above boot methods by configuring MSET0_N pins. The following table shows the configuration of these pins and the corresponding boot method.

MSET0_N	Boot #	Boot method
1	0	From OTP to program SRAM with the DMA method
0	1	From a host processor to program SRAM via I2C

4.5. Host Interface

Figure 4-3 shows the interface between a host processor and FT5202. The interface for other FT5202 series chips is identical. This interface consists of the following three sets of signals:

- Serial interface
- Interrupt from FT5202 to the host
- Wake up signal from the host to FT5202

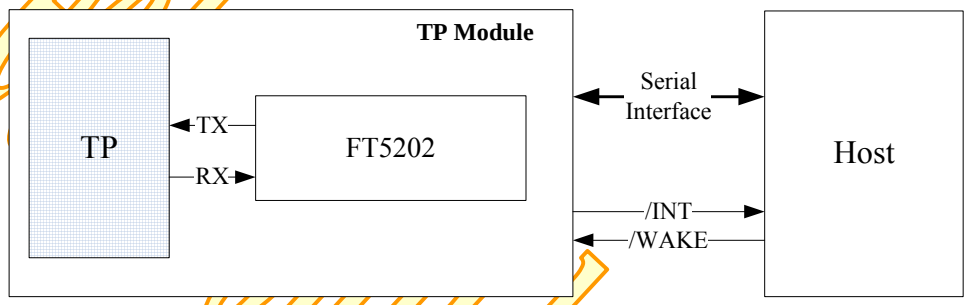


Figure 4-3 Host interface diagram

The serial interfaces of FT5202 is I2C. The details of this interface are described in detail in Section 4.6. The interrupt signal, /INT, is used for FT5202 to inform that host that data are ready for the host to receive. The /WAKE signal is used for the host to wake up FT5202 from the Hibernate mode. Upon exiting the Hibernate mode, FT5202 shall enter the Active mode.

4.6. Serial Interface

FT5202 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 4-4.

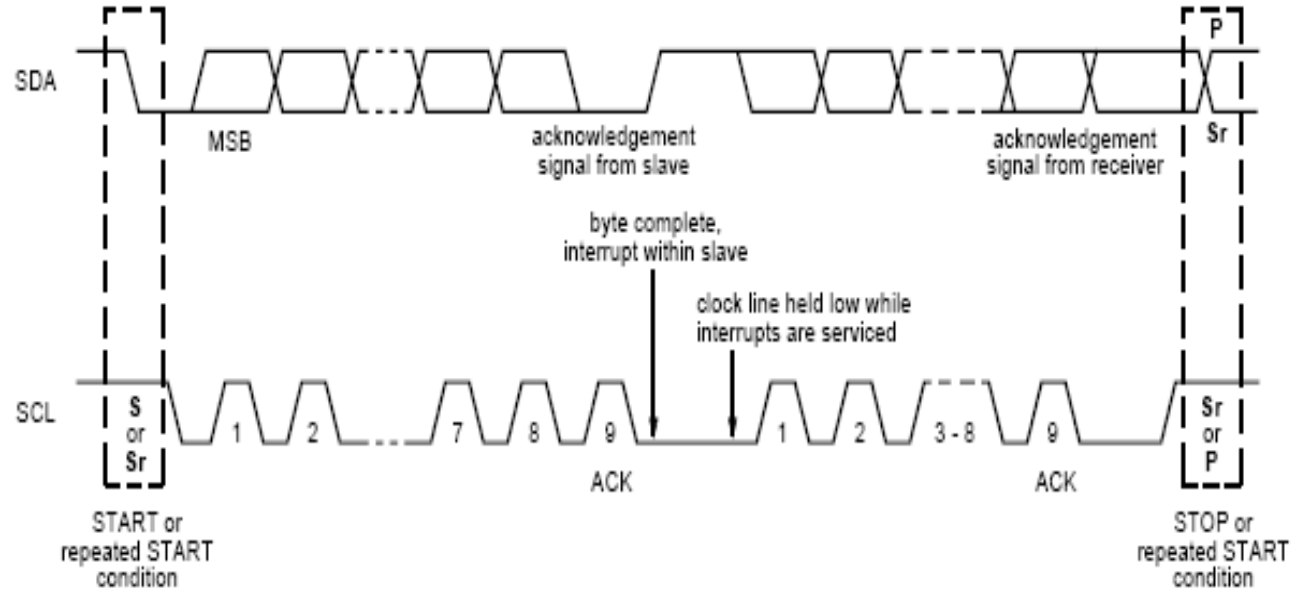


Figure 4-4 I2C serial data transfer format

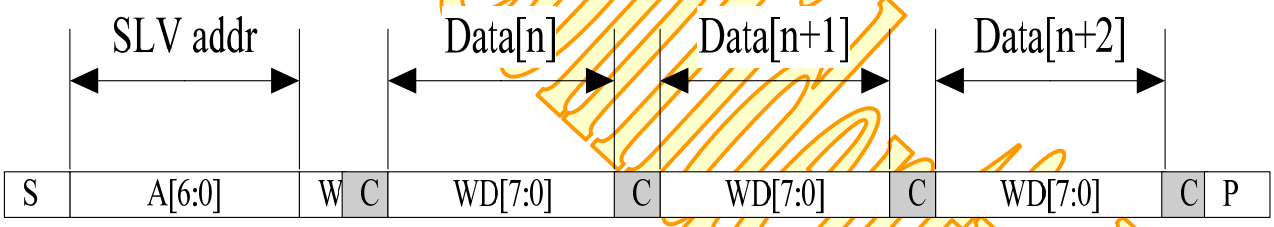


Figure 4-5 I2C master write, slave read

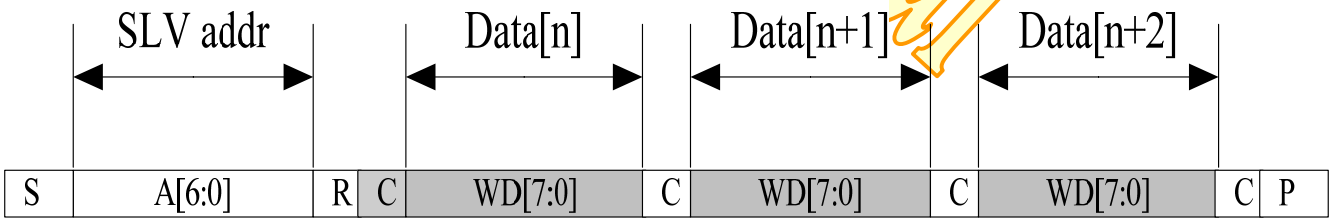


Figure 4-6 I2C master read, slave write

Table 4-1 lists the meanings of the mnemonics used in the above figures.

Table 4-1 Mnemonics description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:4]: 3'b011 A[3:0]: data bits are identical to those of I2CCON[7:4] register.
W	1'b0: Write
R	1'b1: Read
C	ACK
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics

parameter	Unit	MIN	MUX
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\
Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

5. Electrical Specifications

5.1. Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDDA1 - VSSA1	V	-0.3 ~ +3.6	1, 2
Power Supply Voltage 2	VDDA2 – VSSA2	V	-0.3 ~ +3.6	1, 3
Power Supply Voltage 3	VPP	V	-0.3 ~ +8	1
Input Voltage	Vt	V	-0.3 ~VDDA + 0.3	1
Operating Temperature	Topr	℃	-40 ~ +85	1, 4
Storage Temperature	Tstg	℃	-55 ~ +110	1

Notes:

1. If used beyond the absolute maximum ratings, FT5202 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDDA1(high)≥VSSA1 (low)
3. Make sure VDDA2(high)≥VSSA2 (low)
4. The DC/AC characteristics of die and wafer products are guaranteed at 85℃

5.2. DC Characteristics

Table 5-2 DC Characteristics (VDDA=VDDA1=VDDA2=2.6~3.3V, Ta=-40~85℃)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.8 x VDDA	--	VDDA	
Input low -level voltage	VIL	V		-0.3	--	0.2 x VDDA	
Output high -level voltage	VOH	V	IOH=-0.1mA	0.8 x VDDA	--	--	
Output low -level voltage	VOL	V	IOH=0.1mA	--	--	0.2 x VDDA	
I/O leakage current	ILI	μA	Vin=0~VDDA	-1	--	1	
Current consumption （Normal operation mode）	Iopr	mA	VDDA1=VDDA2 = 2.8V Ta=25℃	--	3	4.5	
Current consumption （Monitor mode）	Imon	mA	VDDA1=VDDA2 = 2.8V Ta=25℃	--	2.4	--	

Current consumption （Sleep mode）	Islp	mA	VDDA1=VDDA2 = 2.8V Ta=25℃	--	0.03	--	
Step-up output voltage	V8X	V	VDDA1=VDDA2 = 2.8V	18	20	--	
Input voltage	VDDA2	V		2.8	--	3.6	

5.3. AC Characteristics

Table 5-3 AC Characteristics of oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDDA2 = 2.8V 25℃	25	27	29	
OSC clock 2	fosc2	KHz	VDDA2 = 2.8V Ta=25℃	29	32	35	

Table 5-4 AC Characteristics of TX & RX

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
TX acceptable clock	ftx	KHz		100	150	270	
TX output rise time	Ttxr	nS		--	20	--	
TX output fall time	Ttxf	nS		--	20	--	
RX input voltage	Trxi	V		1.2	--	1.5	

Notes:

DC/AC electrical characteristics of bare die and wafer products are guaranteed at +85℃.

5.4. I/O Ports Circuits

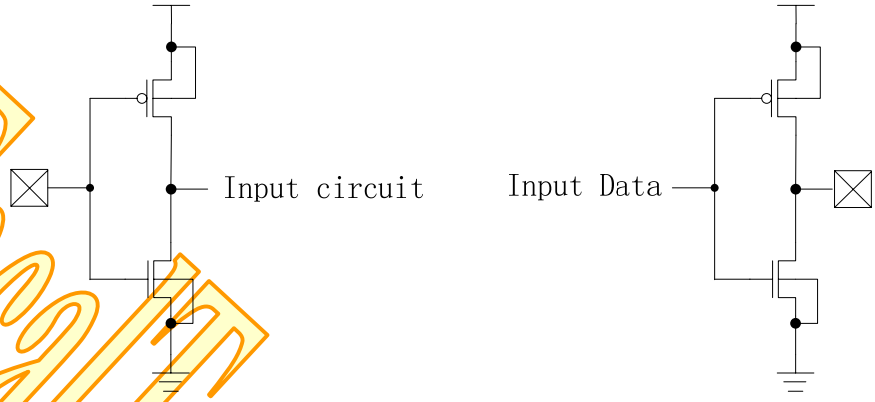


Figure 5-1 Input & Output port circuits

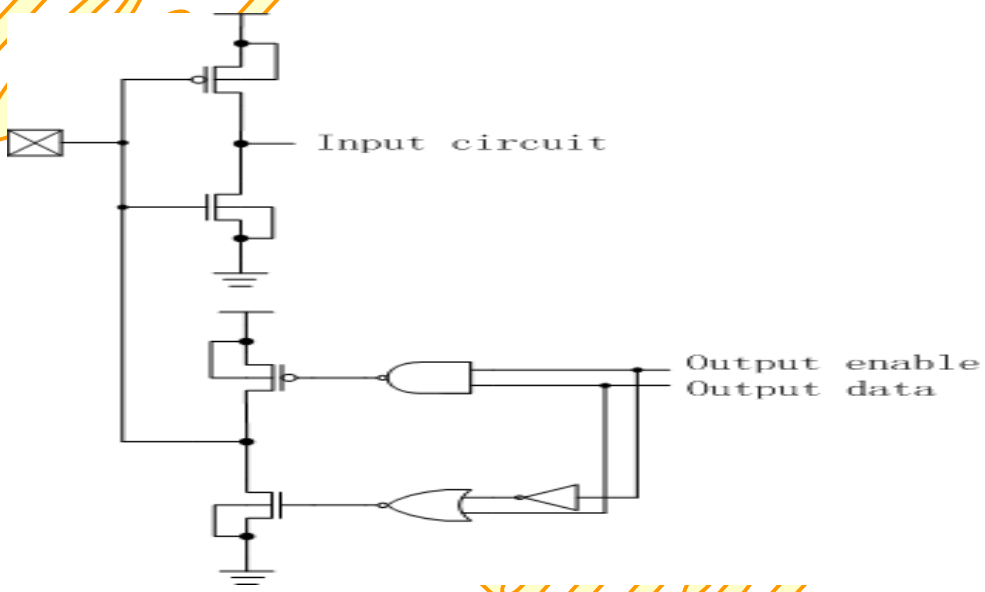


Figure 5-2 In/out port circuit

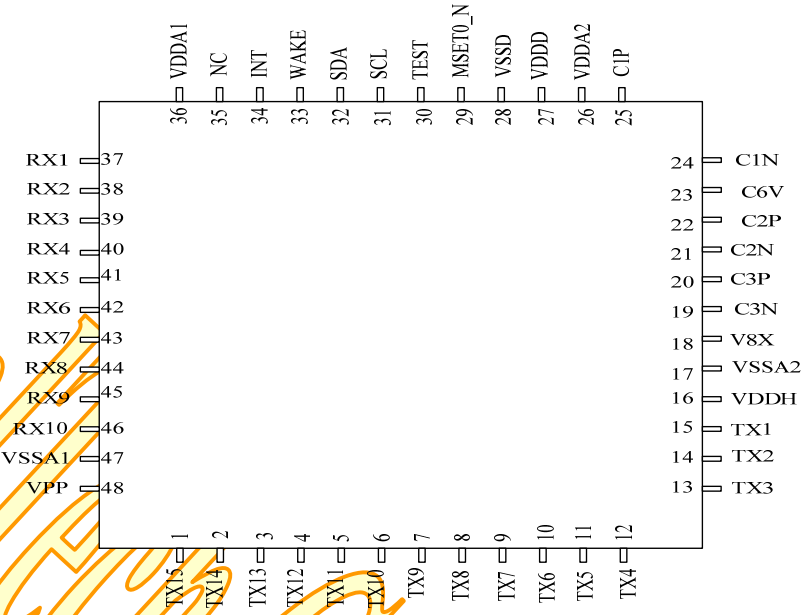
6. Pin Configurations

6.1. Pin List of FT5202 (QFN48L-6x6)

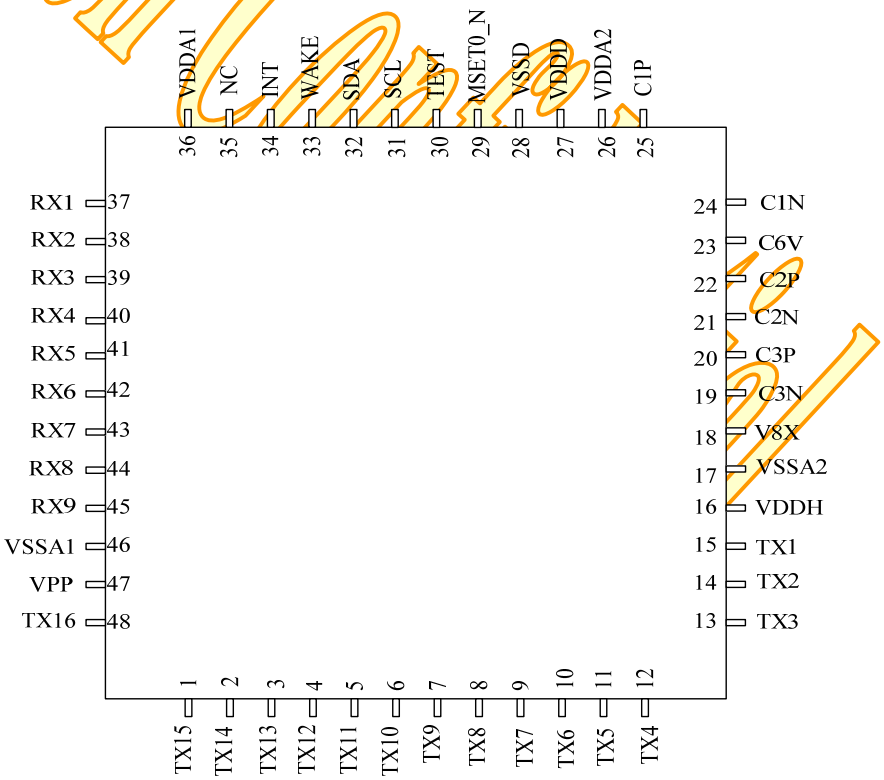
Name	Pin Number		Type	Description
	DE1	DE2		
TX16		48	O	Transmit output pin
TX15	1	1	O	Transmit output pin
TX14	2	2	O	Transmit output pin

TX13	3	3	O	Transmit output pin
TX12	4	4	O	Transmit output pin
TX11	5	5	O	Transmit output pin
TX10	6	6	O	Transmit output pin
TX9	7	7	O	Transmit output pin
TX8	8	8	O	Transmit output pin
TX7	9	9	O	Transmit output pin
TX6	10	10	O	Transmit output pin
TX5	11	11	O	Transmit output pin
TX4	12	12	O	Transmit output pin
TX3	13	13	O	Transmit output pin
TX2	14	14	O	Transmit output pin
TX1	15	15	O	Transmit output pin
VDDH	16	16	PWR	High voltage power supply (12 – 18V) from the charge pump LDO，generated internal. A 1 μ F ceramic to ground is required.
VSSA2	17	17	GND	Analog ground
V8X	18	18	I/O	Charge pump output at 8 times of the input voltage. A 1 μ F ceramic capacitor to ground is required.
C3N	19	19	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C3P
C3P	20	20	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C3N
C2N	21	21	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C2P
C2P	22	22	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C2N
C6V	23	23	I/O	Charge pump output at twice of the input voltage. A 1 μ F ceramic capacitor to ground is required.
C1N	24	24	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C1P
C1P	25	25	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C1N
VDDA2	26	26	PWR	Analog power supply

VDDD	27	27	PWR	Digital power supply, generated internal. A 1 μ F ceramic capacitor to ground is required.
VSSD	28	28	GND	Digital ground
MSET0_N	29	29	I	Boot select: 0: From I2C 1: From OTP
TEST	30	30	I	Test mode enabled at high and normal mode when low
SCL	31	31	I/O	I2C clock input
SDA	32	32	I/O	I2C data input and output
WAKE	33	33	I	External interrupt from the host
INT	34	34	O	External interrupt to the host
NC	35	35	I/O	Not connected
VDDA1	36	36	PWR	Analog power supply
RX1	37	37	I	Receiver input pins
RX2	38	38	I	Receiver input pins
RX3	39	39	I	Receiver input pins
RX4	40	40	I	Receiver input pins
RX5	41	41	I	Receiver input pins
RX6	42	42	I	Receiver input pins
RX7	43	43	I	Receiver input pins
RX8	44	44	I	Receiver input pins
RX9	45	45	I	Receiver input pins
RX10	46		I	Receiver input pins
VSSA1	47	46	GND	Analog ground
VPP	48	47	PWR	OTP Program power supply, 7.5V when programming. VSS/VDD/Floating when not programming



FT5202DE1 Package Diagram



FT5202DE2 Package Diagram

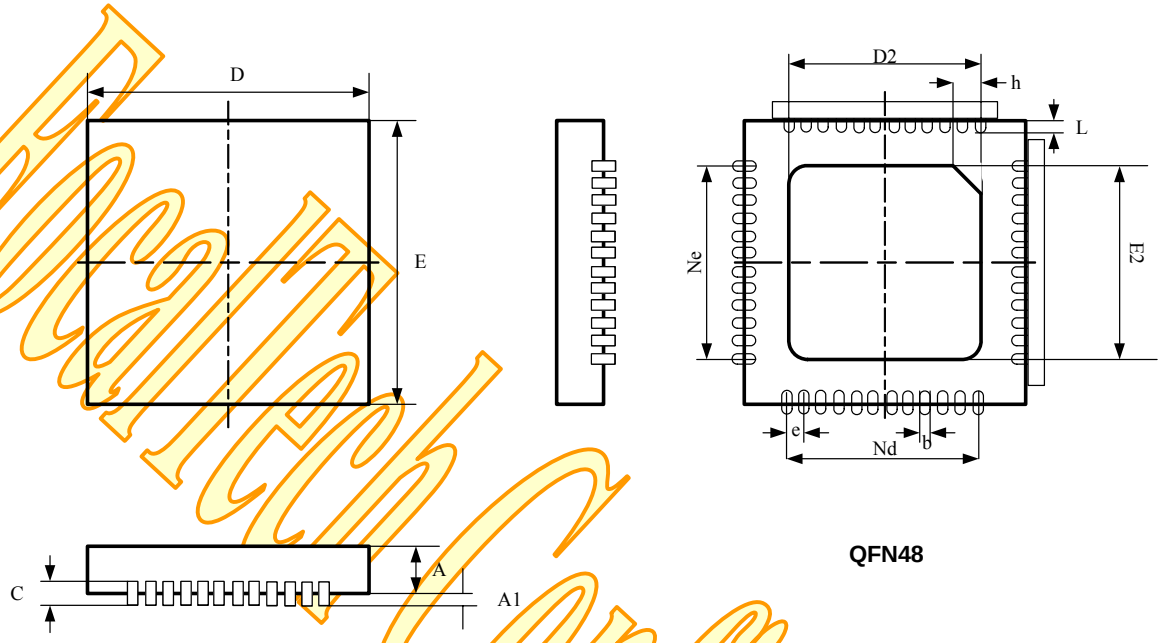
6.2. Pin List of FT5202 (BGA49L – 5x5)

BGA PIN Name	BGA Pin Number	Type	Description
VPP	A2	PWR	OTP Program power supply, 7.5V when programming. VSS/VDD/Floating when not programming
TX<16>	A1	O	Transmit output pin
TX<15>	B1	O	Transmit output pin
TX<14>	C1	O	Transmit output pin
TX<13>	C2	O	Transmit output pin
TX<12>	C3	O	Transmit output pin
TX<11>	D1	O	Transmit output pin
TX<10>	D2	O	Transmit output pin
TX<9>	D3	O	Transmit output pin
TX<8>	E1	O	Transmit output pin
TX<7>	E2	O	Transmit output pin
TX<6>	E3	O	Transmit output pin
TX<5>	F1	O	Transmit output pin
TX<4>	F2	O	Transmit output pin
TX<3>	F3	O	Transmit output pin
TX<2>	G1	O	Transmit output pin
TX<1>	G2	O	Transmit output pin
VDDH	G3	PWR	High voltage power supply (12 – 18V) from the charge pump LDO, generated internal. A 1μF ceramic to ground is required.
VSSA2	E4	GND	Analog ground
V8X	F4	I/O	Charge pump output at 8 times of the input voltage. A 1μF ceramic capacitor to ground is required.
C3N	G4	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C3P
C3P	G5	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C3N
C2N	F5	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C2P
C2P	E5	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C2N
C6V	G6	I/O	Charge pump output at twice of the input voltage. A 1μF ceramic capacitor to ground is required.
C1N	F6	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C1P

C1P	G7	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C1N
VDDA2	F7	PWR	Analog power supply
IOVCC	E6	PWR	I/O power supply.
VDDD	E7	PWR	Digital power supply, generated internal. A 1μF ceramic capacitor to ground is required.
VSSD	D4	GND	Digital ground
MSET0_N	D5	I	Boot select: 0: From I2C 1: From OTP
TEST	C4	I	Test mode enabled at high and normal mode when low
SCL	D6	I/O	I2C clock input
SDA	D7	I/O	I2C data input and output
WAKE	C5	I	External interrupt from the host
INT	C6	O	External interrupt to the host
NC	C7	I/O	Not connected
VDDA1	B7	PWR	Analog power supply
RX<1>	A7	I	Receiver input pins
RX<2>	A6	I	Receiver input pins
RX<3>	B6	I	Receiver input pins
RX<4>	A5	I	Receiver input pins
RX<5>	B5	I	Receiver input pins
RX<6>	A4	I	Receiver input pins
RX<7>	B4	I	Receiver input pins
RX<8>	A3	I	Receiver input pins
RX<9>	B3	I	Receiver input pins
VSSA1	B2	GND	Analog ground

7. Package information

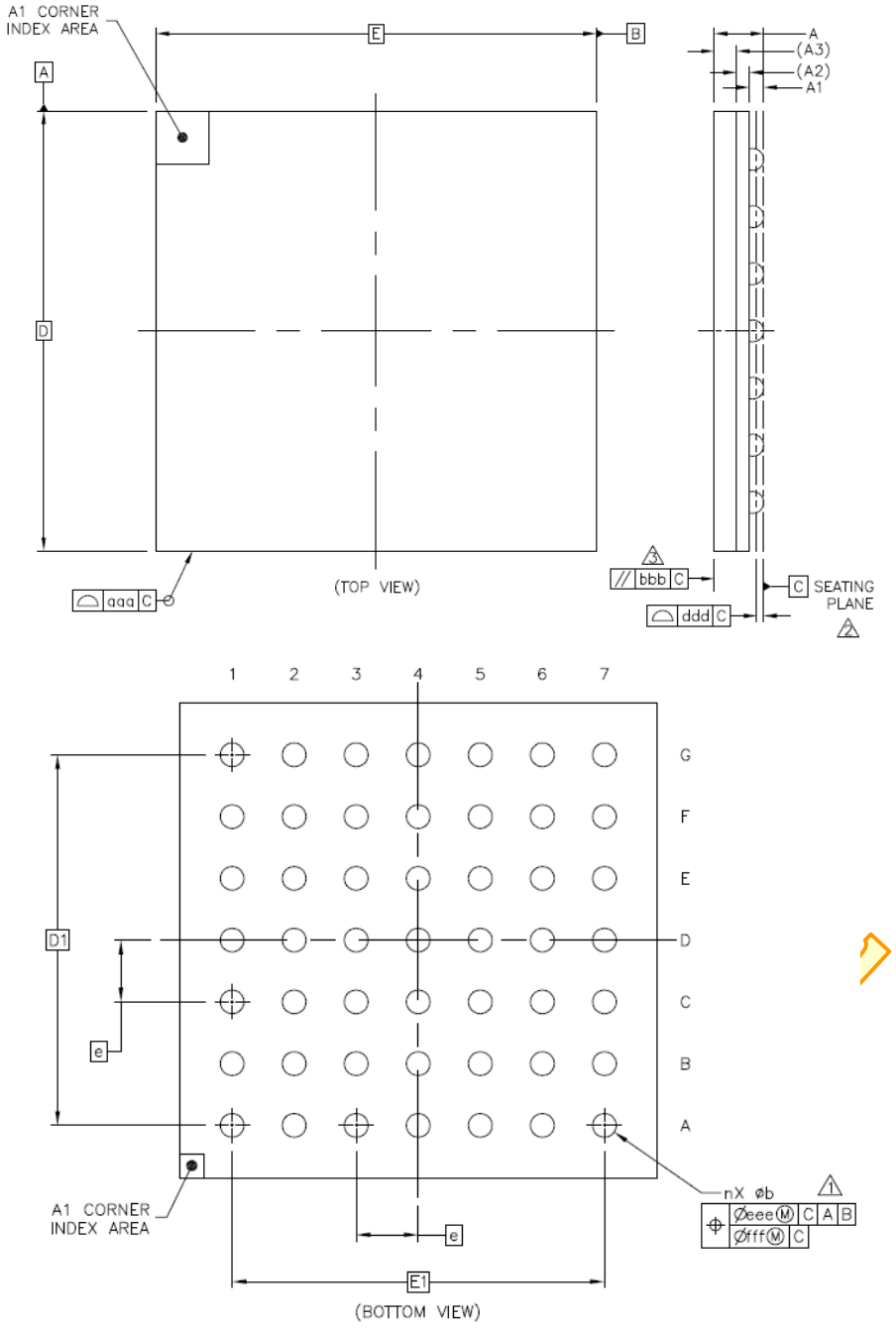
7.1. Package information of QFN-6x6-48L Package



QFN48

SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.70	0.75	0.80	Ne	4.40BSC		
A1	----	0.01	0.05	Nd	4.40BSC		
b	0.18	0.22	0.28	E	5.90	6.00	6.10
c	0.15	0.20	0.25	E2	4.10REF		
D	5.90	6.00	6.10	L	0.35	0.40	0.45
D2	4.10REF			h	0.30	0.35	0.40
e	0.40 BSC			L/F (MIL)	177*177		

7.2. Package information of BGA-5x5- 49LPackage



Notes:

1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C.
2. Datum C (seating plane) is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of mark on top surface of package.

	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	----	----	0.6
STAND OFF	A1	0.12	----	0.2
SUBSTRATE THICKNESS	A2	----	----	0.15
MOLD THICKNESS	A3	0.25 REF		
BODY SIZE	D	5 BSC		
	E	5 BSC		
BALL DIAMETER		0.25		
BALL OPENING		0.25		
BALL WIDTH	b	0.2	----	0.3
BALL PITCH	e	0.65		
BALL COUNT	n	49		
EDGE BALL CENTER TO CENTER	D1	3.9 BSC		
	E1	3.9 BSC		
BODY CENTER TO CONTACT BALL	SD	---- BSC		
	SE	---- BSC		
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.1		
COPLANARITY	ddd	0.08		
BALL OFFSET (PACKAGE)	eee	0.15		
BALL OFFSET (BALL)	fff	0.05		

7.3. Order Information

Package Type	**QFN**
	48 Pin (6 * 6)
	0.75 - P0.4
Product Name	**FT5202DE1**

Note:

1). The last two letters in the product name indicate the package type and lead pitch and thickness.

2). The second last letter indicates the package type.

D : QFN-6*6 、W : BGA-5*5

3). The last letter indicates the lead pitch and thickness.

E : 0.75 - P0.4 、H : 0.6 -P0.65

T : Track Code

F : "F" for Lead Free process.

Y : Year Code

WW : Week Code

SV : Lot Code

Product Name	Package Type	# TX Pins	# RX Pins
FT5202DE1	QFN-48L	15	10
FT5202DE2	QFN-48L	16	9
FT5202WH2	BGA-49L	16	9

REVISION TABLE

Version	Revisions	Date
0.1	First draft	2010-01-19

END OF DATABOOK