DUAL CHANNEL1.5 MHZ, 600MA SYNCHRONOUS STEP-DOWN CONVERTER

FSP3112

FEATURES

- High Efficiency : Up to 96%
- 1.5MHz Constant Frequency Operation
- 600mA Output Current at V_{IN}=3.0V
- Very Low Quiescent Current of 500μA
- No Schottky Diode Required
- Low $R_{DS(ON)}$ Internal Switches: 0.35Ω
- 0.6V reference allows low Output Voltage
- Current Mode Operation for excellent line and load transient Response
- Short-Circuit &Thermal Fault Protection
- ＜1μA Shutdown Current
- Power-on Reset Output
- Externally Synchronized Oscillator
- Small Thermally Enhanced MSOP10 and DFN10 Packages

GENERAL DESCRIPTION

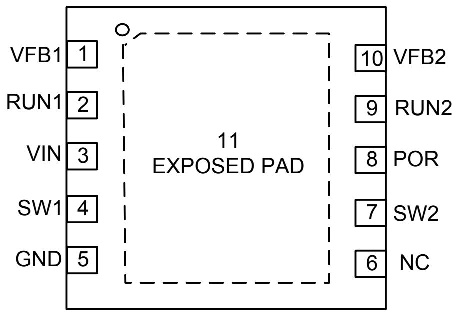
The FSP3112 is a dual channel high efficiency monolithic synchronous step down current mode DC-DC converter operating at 1.5MHz constant frequency. The device integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode for each of the channels. The FSP3112 can operate from a 2.5V to 5.5V input voltage and is ideal for powering portable equipment that runs from a single cell lithium-Ion (Li+) battery. It can supply 600mA output current for each channel and can also run at 100% duty cycle for low dropout operation, extending battery life in portable system. For FSP3112, Pulse Skipping Mode operation at light loads provides very low output ripple voltage for noise sensitive applications.

APPLICATIONS

- Portable Media Players
- Digital Still Cameras
- Cellular Telephones
- PDAs
- Wireless and DSL modems

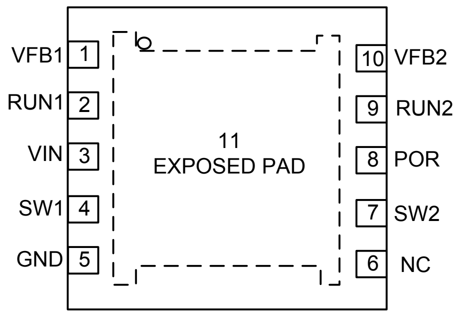
PIN CONFIGURATION

(Top View)



10-Lead (3mm ×3mm) Plastic DFN
Exposed Pad is PGND (Pin 11)
Must be connected to GND.

(Top View)

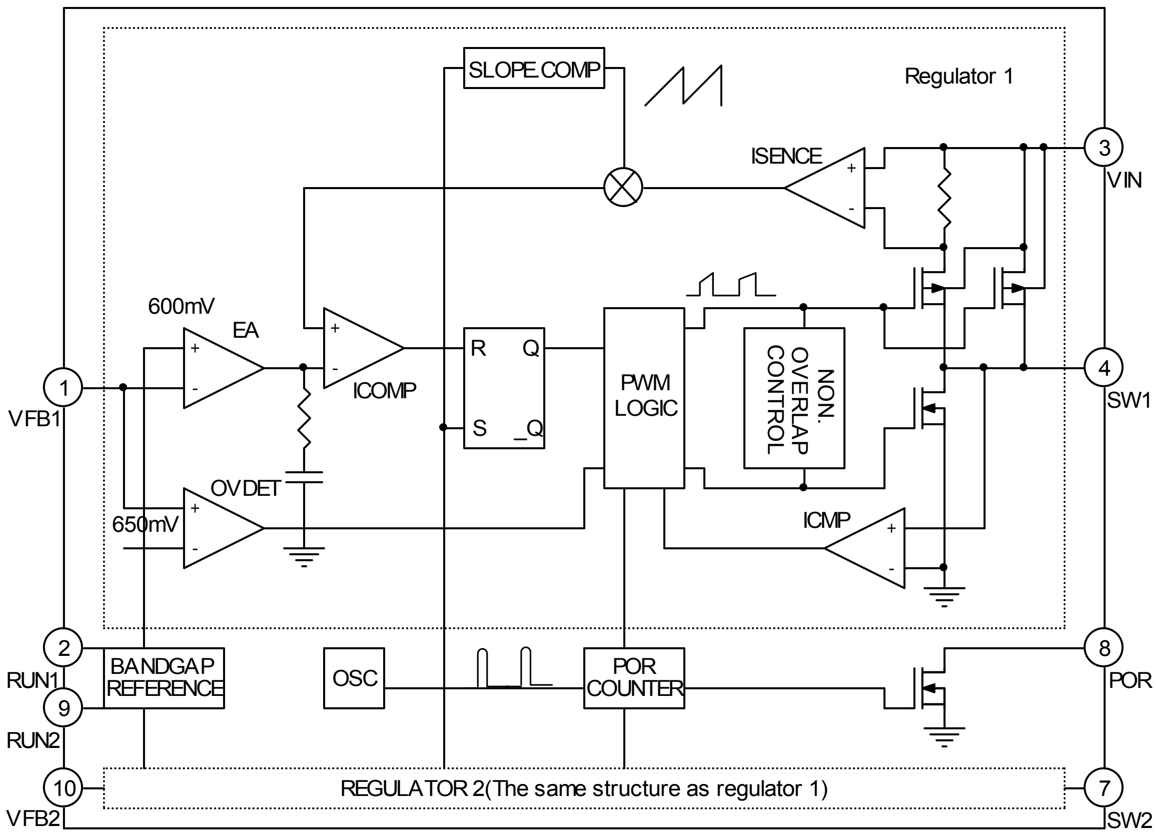


10-Lead Plastic MSOP
Exposed Pad is PGND (Pin 11)
Must be connected to GND.

■ PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1	VFB1	Channel 1 output feedback. It receives the feedback voltage from the external resistive divider across the output.
2	RUN1	Channel 1 Enable
3	VIN	Power Supply
4	SW1	Channel 1 power switch output
5	GND	Ground
6	NC	No Connection
7	SW2	Channel 2 power switch output.
8	POR	Power On Reset.
9	RUN2	Enable Pin of Channel 2.
10	VFB2	Channel 2 output feedback. It receives the feedback voltage from the external resistive divider across the output.
11	EXPOSED PAD	Power Ground. It must be connect to ground properly.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Parameter	Rating	Unit
Input Supply Voltage	-0.3 to +6	V
RUN1, RUN2	-0.3 to V_{IN}+0.3	V
VFB1, VFB2 Voltages	-0.3 to V_{IN}+0.3	V
SW1, SW2 Voltages	-0.3 to V_{IN}+0.3	V
POR Voltages	-0.3 to +6	V
Peak SW1,SW2 Sink and Source Current	1.5	A
Operating Temperature Range	-40 to +85	℃
Junction Temperature (Note 2)	+125	℃
Storage Temperature Range	-65 to 150	℃
Lead Temperature (soldering, 10 sec.)	+300	℃

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J=T_A+P_D\times\theta_{JA}$

■ ELECTRICAL CHARACTERISTICS (NOTE 3)

($V_{IN}=V_{RUN}$=3.6V, T_A=25℃, Test circuit of Figure 1, Unless otherwise noted)

Parameter	Condition	Min.	Typ.	Max.	Unit
Input DC Supply Current Active Mode Shutdown Mode	$V_{FB1}=V_{FB2}$=0.5V, RUN=0V, V_{IN}=4.2V		500 0.3	800 2	μA
Input Voltage Range		2.5		5.5	V
Regulated Feedback Voltage	T_A=+25℃, Channel 1 or 2	0.5880	0.6000	0.6120	V
	T_A=0℃≤T_A≤85℃, Channel 1 or 2	0.5865	0.6000	0.6135	V
	T_A=-40℃≤T_A≤85℃, Channel 1 or 2	0.5850	0.6000	0.6150	V
Feedback Pin Input Current	V_{FB}=0.65V			±30	nA
Reference Voltage Line Regulation	V_{IN}=2.5V to 5.5V		0.11	0.40	%/V
Output Voltage Line Regulation	V_{IN}=2.5V to 5.5V, V_{OUT}=1.8V, I_{OUT}=10mA		0.11	0.40	%/V
Output Voltage Load Regulation	V_{IN}=3.6V, I_{OUT}=0 to 600mA,		0.0015		%/mA
Maximum Output Current	V_{IN}=3.0V	600			mA
Oscillator Frequency	$V_{FB\ 1/2}$= 0.6V	1.2	1.5	1.8	MHz
$R_{DS(ON)}$ of P-CH MOSFET	I_{SW}=300mA		0.35	0.45	Ω
$R_{DS(ON)}$ of N-CH MOSFET	I_{SW}=-300mA		0.28	0.45	Ω
Peak Inductor Current	V_{IN}=3V,$V_{FB1}=V_{FB2}$=0.5V, Duty cycle<35%		1.2		A
SW Leakage	V_{RUN}=0V, V_{SW}=0V or 5V, V_{IN}=5V		±0.01	±1	μA
RUN Threshold	-40℃≤T_A≤85℃	0.3	0.45	1.50	V
RUN Leakage Current			±0.1	±1	μA
Power-On Reset Threshold (POR)	V_{FBX} Ramping Up		8.5		%
	V_{FBX} Ramping Down,		-8.5		%
	Power-On Reset Delay		175		mS
	Power-On Reset On-Resistance		100		Ω

Note 3: 100% production test at +25℃. Specifications over the temperature range are guaranteed by design and characterization.

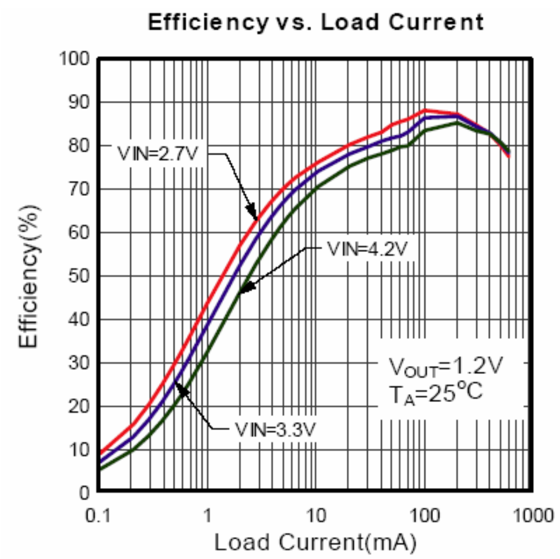
■ THERMAL RESISTANCE (NOTE 4)

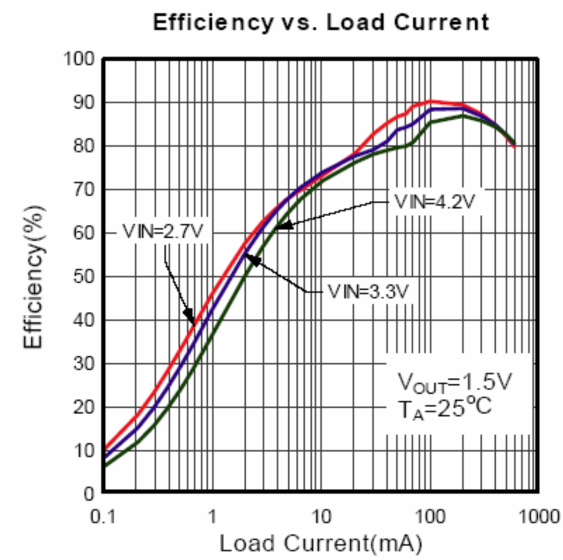
Package	θ_{JA} (℃/W)	θ_{JC} (℃/W)
MSOP-10 (EXPOSE PAD)	45	10
DFN-10 (EXPOSE PAD)	45	10

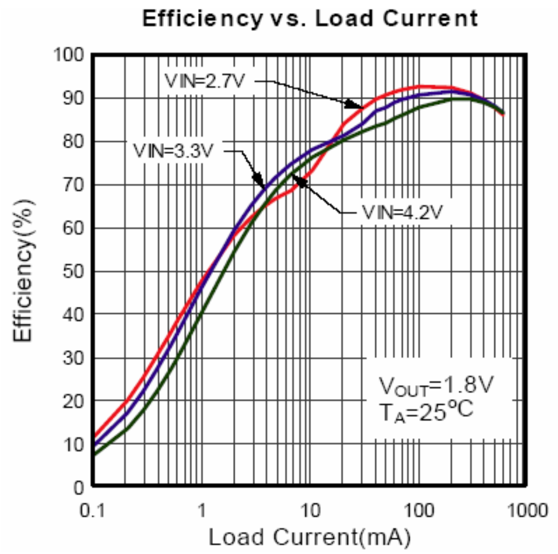
Note 4: Thermal Resistance is specified with approximately 1 square of 1 oz cooper.

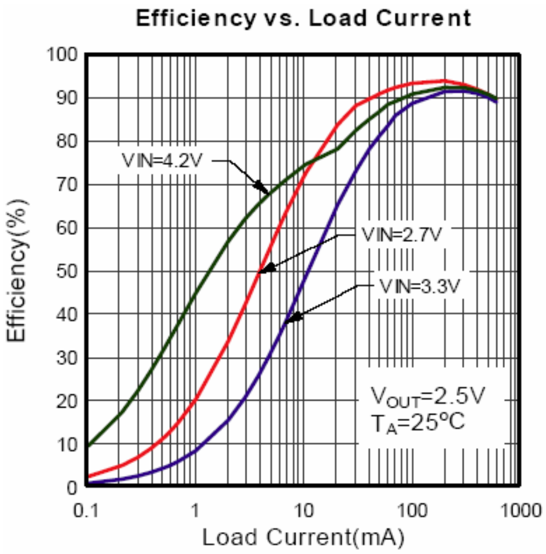
■ TYPICAL PERFORMANCE CHARACTERISTICS

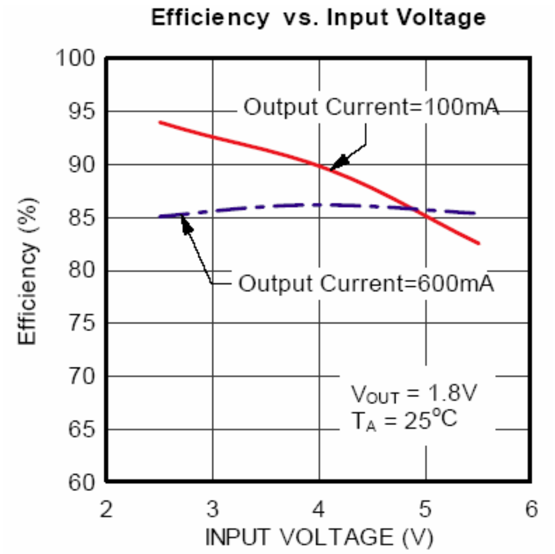
(Test Figure 1 below unless otherwise specified)

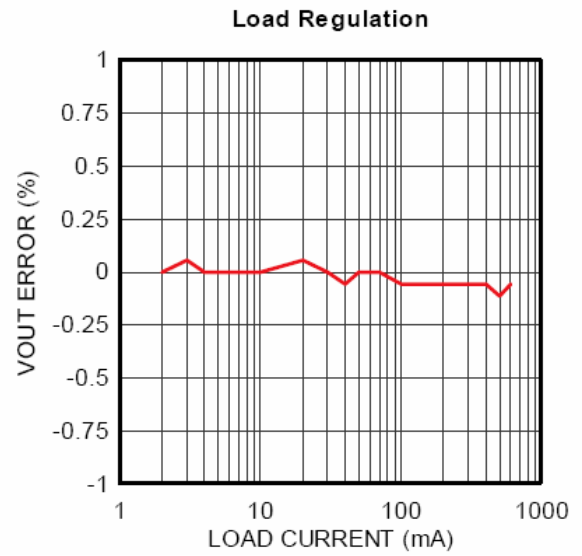




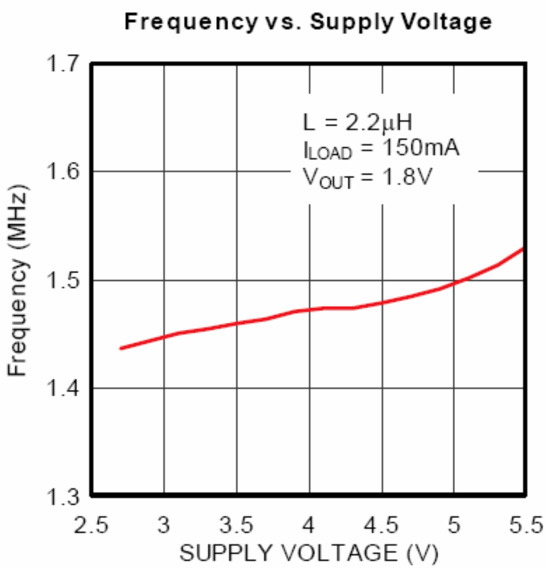


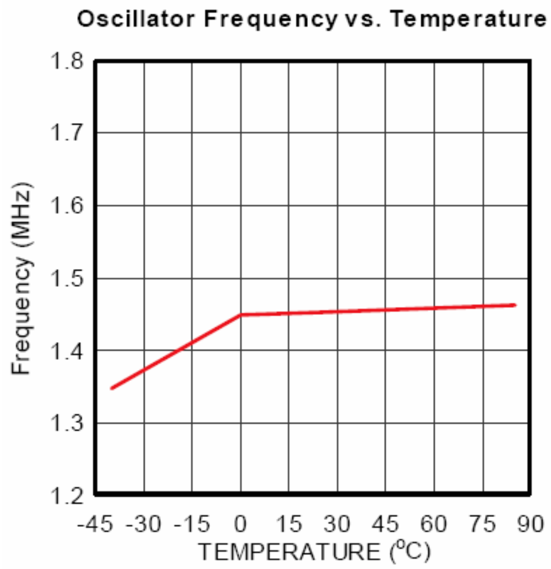


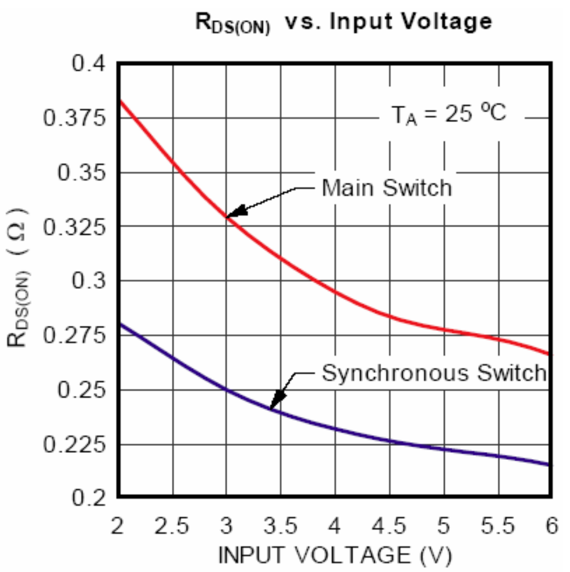


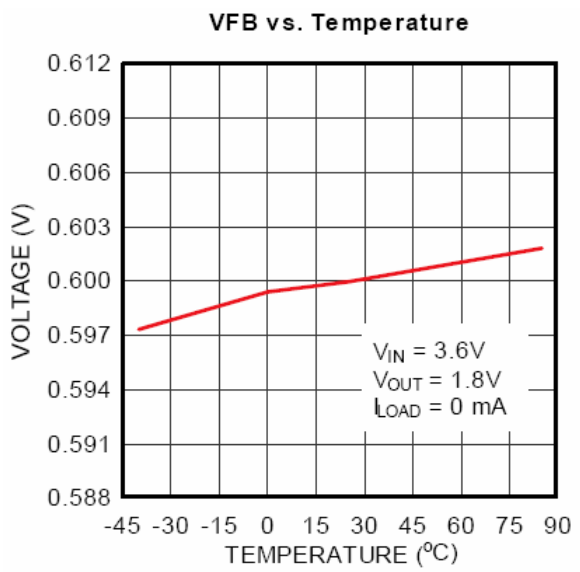


■ TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

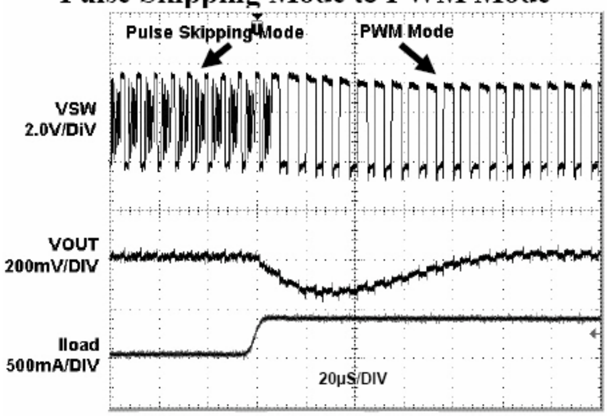






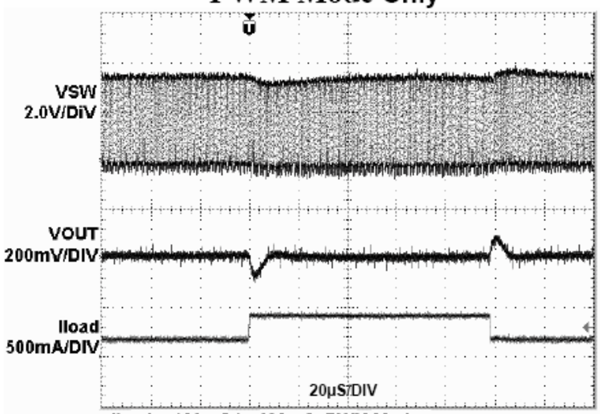


Load Transient Response
Pulse Skipping Mode to PWM Mode



Iload = 26mA to 400mA, Pulse Skipping Mode
L=2.2uH, Cin=10uF, Cout=10uF, Vin=3.6V, Vout=1.8V

Load Transient Response
PWM Mode Only



Iload = 180mA to 400mA, PWM Mode
L=2.2uH, Cin=10uF, Cout=10uF, Vin=3.6V, Vout=1.8V

OPERATION

FSP3112 is a monolithic switching mode Step-Down DC-DC converter. It utilizes internal MOSFETs to achieve high efficiency and can generate very low output voltage by using internal reference at 0.6V. It operates at a fixed switching frequency, and uses the slope compensated current mode architecture. This Step-Down DC-DC Converter suppliers 600mA output current at VIN=3V with input voltage range from 2.5V to 5.5V. For FSP3112 with the Pulse Skipping Mode feature, users can optimize ripple at light load for noise sensitive applications.

CURRENT MODE PWM CONTROL

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for excellent load and line responses and protection of the internal main switch (P-Ch MOSFET) and synchronous rectifier (N-Ch MOSFET). During normal operation, the internal P-Ch MOSFET is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. The current comparator, I_{COMP}, limits the peak inductor current. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until either the inductor current starts to reverse, as indicated by the current reversal comparator, I_{ZERO}, or the beginning of the next clock cycle. The OVDET comparator controls output transient overshoots by turning the main switch off and keeping it off until the faults is no longer present.

PULSE SKIPPING MODE OPERATION

The FSP3112 can automatically switch to Pulse Skipping Mode operation at light load to improve efficiency. In the Pulse Skipping Mode, the inductor current may reach zero or reverse on each pulse. The PWM control loop will automatically skip pulses to maintain output regulation. The bottom MOSFET is turned off by the current reversal comparator, I_{ZERO}, and the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for the switching regulator.

DROPOUT OPERATION

When the input voltage decreases toward the value of the output voltage, the FSP3112 allows the main switch to remain on for more than one switching cycle and increases the duty cycle until it reaches 100%.
The duty cycle D of a step-down converter is defined as:

$$D=T_{ON}\times f_{OSC}\times 100\% \approx \frac{V_{OUT}}{V_{IN}}\times 100\%$$

Where T_{ON} is the main switch on time and f_{OSC} is the oscillator frequency.
The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor. At low input supply voltage, the $R_{DS(ON)}$ of the P-Channel MOSFET increase, and the efficiency of the converter decreases. Caution must be exercised to ensure the heat dissipated not to exceed the maximum junction temperature of the IC.

MAXIMUM LOAD CURRENT

The FSP3112 will operate with input supply voltages as low as 2.5V, however, the maximum load current decreases at lower input due to large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub harmonic oscillations at duty cycles greater than 50%. Conversely the current limit increases as the duty cycle decreases.

■ APPLICATION INFORMATION

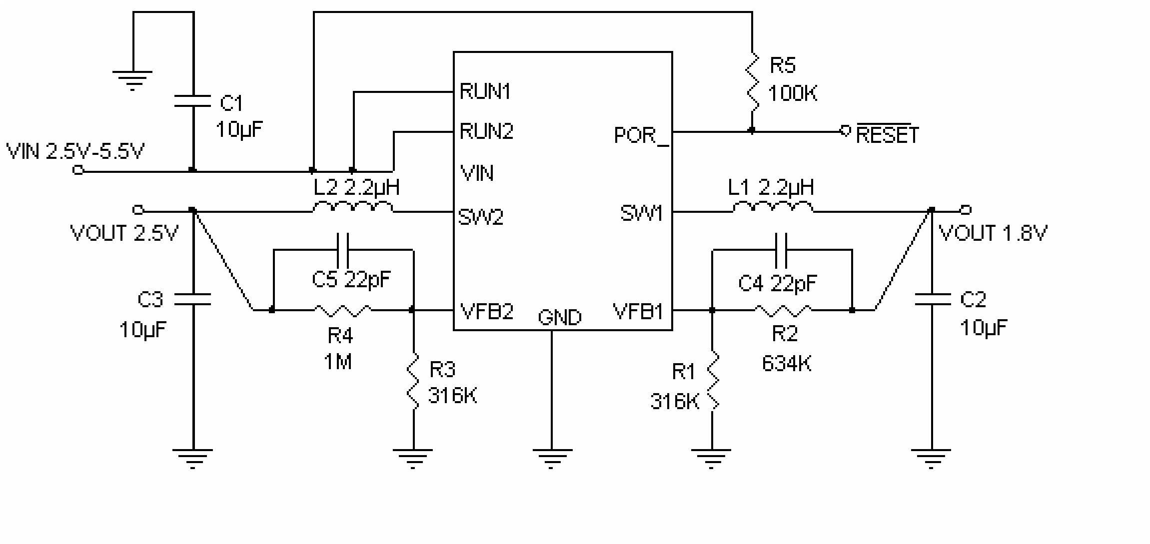


Fig.1 FSP3112 Typical Application Circuit

SETTING THE OUTPUT VOLTAGE

The external resistor sets the output voltage according to the following equation:

$$V_{OUT} = 0.6V\left(1 + \frac{R2}{R1}\right)$$

Table 1 ----Resistor select for output voltage setting

V_{OUT}	R1(R3)	R2(R4)
1.2V	316K	316K
1.5V	316K	474K
1.8V	316K	634K
2.5V	316K	1001K

INDUCTOR SELECTION

For most designs, the FSP3112 operates with inductors of 1μH to 4.7μH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor Ripple Current. Large value inductors lower ripple current and small value inductors result in high ripple currents. Choose inductor ripple current approximately 35% of the maximum load current 600mA, or ΔI_L=210mA.

For output voltages above 2.0V, when light-load efficiency is important, the minimum recommended inductor is 2.2μH. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. For higher efficiency at heavy loads (above 200mA), or minimal load regulation (but some transient overshoot), the resistance should be kept below 100mΩ. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (600mA+105mA). Table2 lists some typical surface mount inductors that meet targent applications for the FSP3112.

Part #	L (μH)	Max DCR (mΩ)	Rated D.C. Current (A)	Size W×L×H (mm)
Sumida CR43	14 2.2 3.3 4.7	56.2 71.2 86.2 108.7	2.52 1.75 1.44 1.15	4.5×4.0×3.5
Sumida CDRH4D18	1.5 2.2 3.3 4.7	75 110 162	1.32 1.04 0.84	4.7×4.7×2.0
Toko D312C	1.5 2.2 3.3 4.7	120 140 180 240	1.29 1.14 0.98 0.79	3.6×3.6×1.2

INPUT CAPACITOR SELECTION

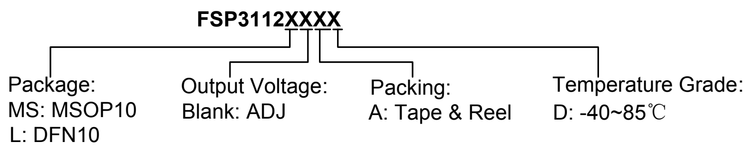
The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for minimum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 4.7μF ceramic capacitor for most applications is sufficient.

OUTPUT CAPACITOR SELECTION

The output capacitor is requires to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current. The output ripple V_{OUT} is determined by:

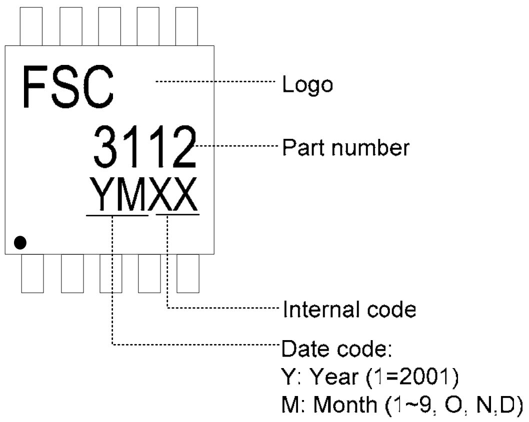
$$\Delta V_{OUT} \le \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C3} \right)$$

■ ORDERING INFORMATION

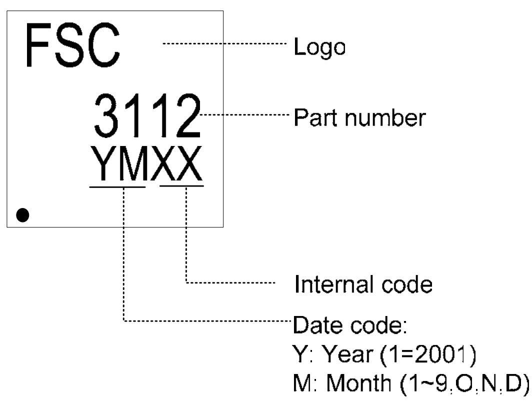


■ MARKING INFORMATION

(1) MSOP10

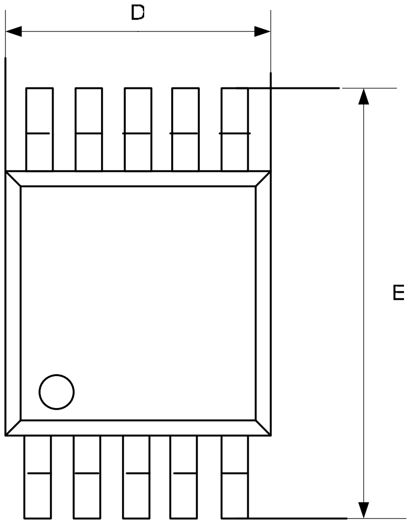


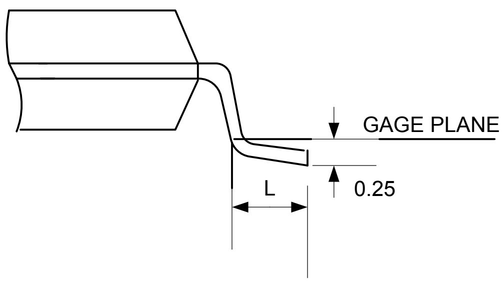
(2) DFN10



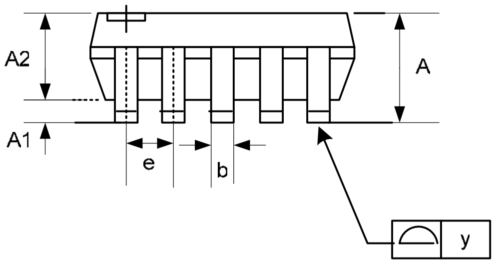
■ PACKAGE INFORMATION

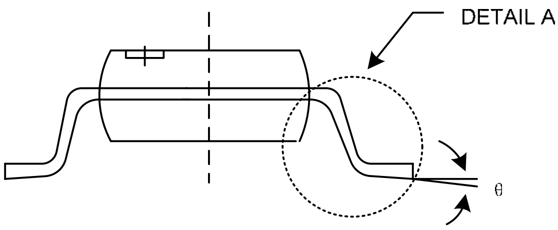
(1) MSOP10





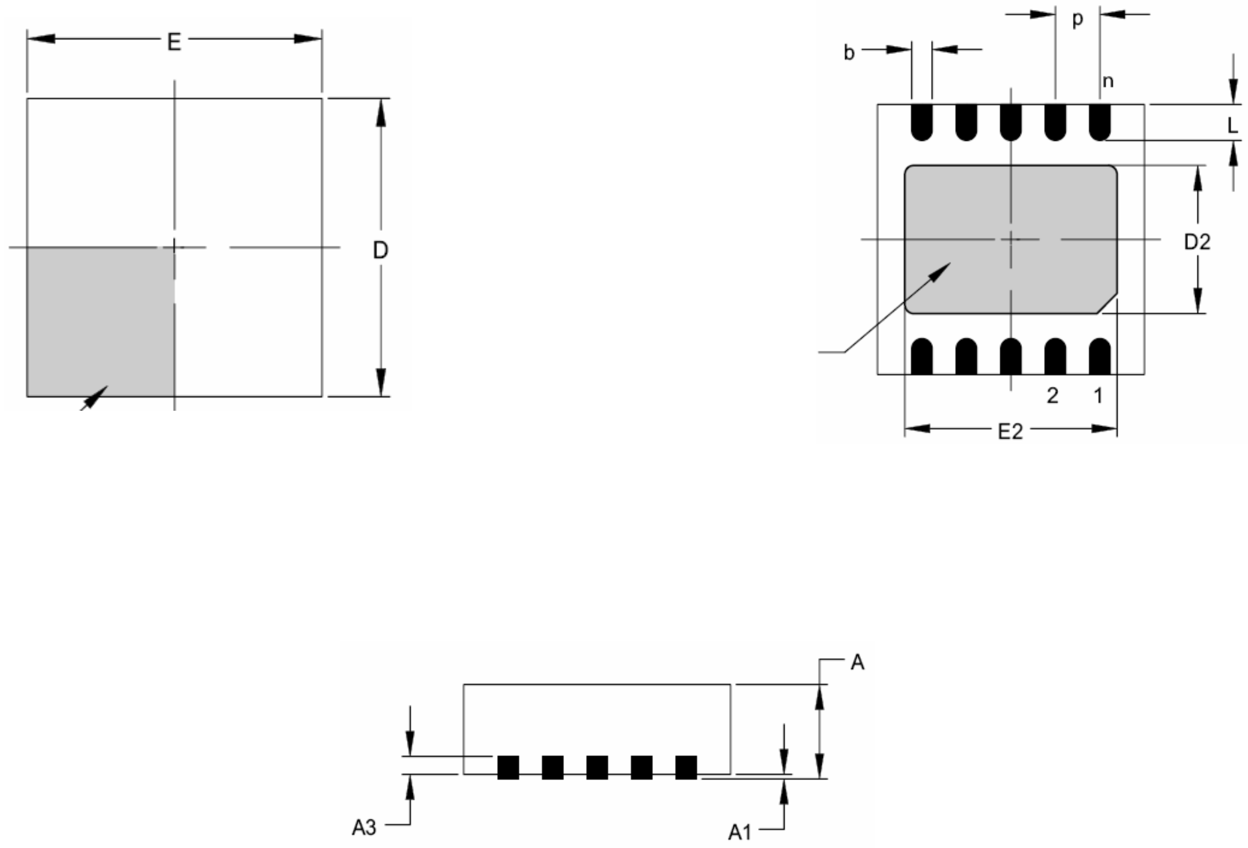
DETAIL A





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A		1.10		0.0433
A1	0.05	0.15	0.0020	0.0060
A2	0.75	0.95	0.0295	0.0374
b	0.17	0.27	0.0067	0.0106
D	2.90	3.10	0.1142	0.1220
E	4.80	5.00	0.1890	0.1970
e	0.50BSC.		0.0197BSC.	
L	0.40	0.70	0.0157	0.0276
y		0.10		0.0039
θ	0°	6°	0°	6°

2) DFN10



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20REF			0.008REF		
E	2.85	3.00	3.15	0.112	0.118	0.124
E2	1.39		2.45	0.055		0.096
D	2.85	3.00	3.15	0.112	0.118	0.124
D2	1.20		1.75	0.047		0.069
b	0.18	0.25	0.30	0.008	0.010	0.015
L	0.30	0.40	0.50	0.012	0.016	0.020
p	0.50BSC			0.020BSC		