FSGM300N

Green-Mode Power Switch

ON Semiconductor®

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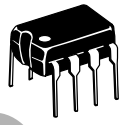


PDIP−8
CASE 626−05

Description

The FSGM300N is an integrated Pulse Width Modulation (PWM) controller and SENSEFET® specifically designed for offline Switch−Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed−frequency oscillator, Under−Voltage Lockout (UVLO), Leading−Edge Blanking (LEB), optimized gate driver, internal soft−start, temperature−compensated precise current sources for loop compensation, and self−protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSGM series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform suited for cost−effective design of a flyback converter.

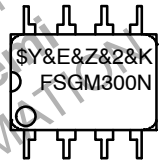
Features

- Advanced Burst−Mode Operation for Low Standby Power
- Random Frequency Fluctuation for Low EMI
- Pulse−by−Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over−Voltage Protection (OVP), Abnormal Over−Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output−Short Protection (OSP), and Under−Voltage Lockout (UVLO) with Hysteresis
- Auto−Restart Mode
- Internal Startup Circuit
- Internal High−Voltage SENSEFET: 650 V
- Built−in Soft−Start: 15 ms
- This is a Pb−Free Device

Applications

- Power Supply for LCD Monitor, STB and DVD Combination

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&E	‘= Designates Space
&Z	= Assembly Plant Code
&2	= 2−Digit Date Code Format
&K	= 2−Digit Lot Run Tracebility Code
FSGM300N	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION

Part Number	Package	Operating Junction Temperature	Current Limit	$R_{DS(ON)}$ (Max.)	Output Power Table (Note 2)				Replaces Device	Shipping
					230V_{AC} ± 15% (Note 3)		85 – 265 V_{AC}			
					Adapter (Note 4)	Open Frame (Note 5)	Adapter (Note 4)	Open Frame (Note 5)		
FSGM300N	8−DIP	−40°C ~ +125°C	1.60 A	2.2 Ω	26 W	40 W	20 W	30 W	FSFM300N	3000 / Tube

1. Pb−free package per JEDEC J−STD−020B.
2. The junction temperature can limit the maximum output power.
3. 230 V_{AC} or 100 / 115 V_{AC} with voltage doubler.
4. Typical continuous power in a non−ventilated enclosed adapter measured at 50°C ambient temperature.
5. Maximum practical continuous power in an open−frame design at 50°C ambient temperature.

Application Circuit

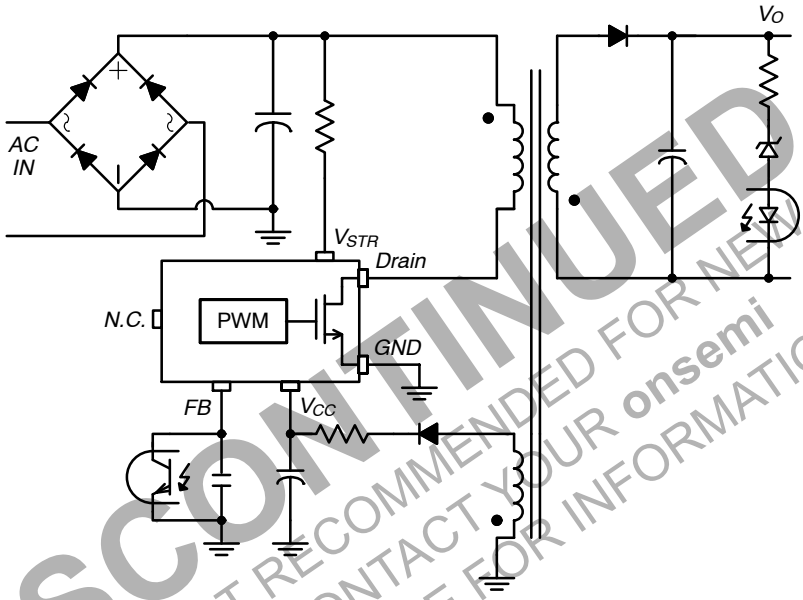

Figure 1. Typical Application Circuit

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Internal Block Diagram

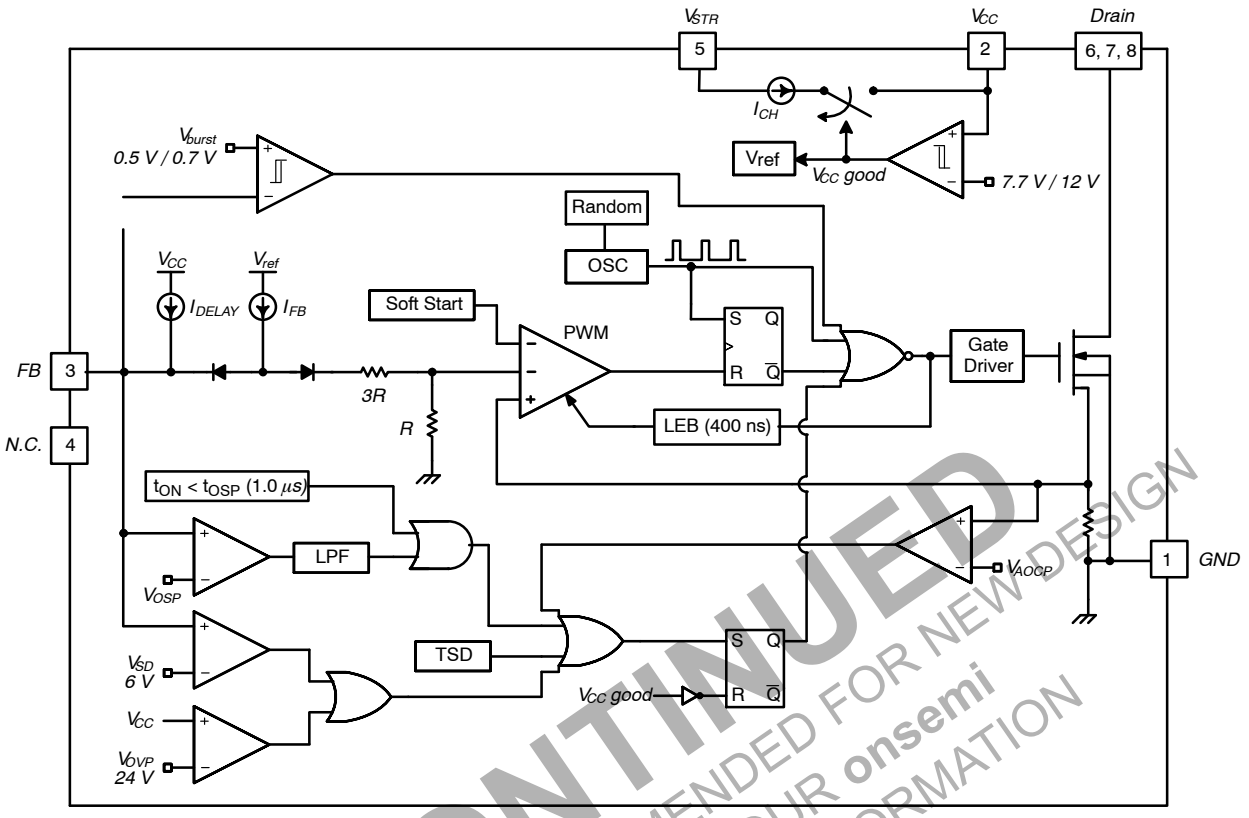

Figure 2. Internal Block Diagram

Pin Configuration

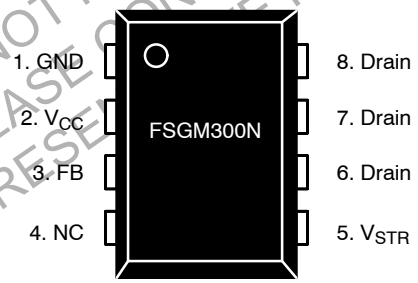

Figure 3. Pin Configuration (Top View)

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PIN DEFINITIONS

Pin No.	Name	Description
1	GND	*Ground*. This pin is the control ground and the SENSEFET source.
2	V_{CC}	*Power Supply*. This pin is the positive supply input, w hich provides the internal operating current for both startup and steady−state operation.
3	FB	*Feedback*. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto−coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6 V, the overload protection triggers, which shuts down the power switch.
4	N.C.	No connection.
5	V_{STR}	*Startup*. This pin is connected directly, or through a resistor, to the high−voltage DC link. At startup, the internal high−voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12 V, the internal current source (I_{CH}) is disabled.
6, 7, 8	Drain	*SENSEFET Drain*. High−voltage power SENSEFET drain connection.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{STR}	V_{STR} Pin Voltage		−	650	V
V_{DS}	Drain Pin Voltage		−	650	V
V_{CC}	V_{CC} Pin Voltage		−	26	V
V_{FB}	Feedback Pin Voltage		−0.3	8.0	V
I_{DM}	Drain Current Pulsed		−	4	A
I_{DS}	Continuous Switching Drain Current (Note 6)	T_C = 25°C	−	1.90	A
		T_C = 100°C	−	1.27	A
E_{AS}	Single Pulsed Avalanche Energy (Note 7)		−	190	mJ
P_D	Total Power Dissipation (T_C = 25°C) (Note 8)		−	1.5	W
T_J	Maximum Junction Temperature		−	150	°C
	Operating Junction Temperature (Note 9)		−40	+125	°C
T_{STG}	Storage Temperature		−55	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114	2	−	kV
		Charged Device Model, JESD22−C101	2	−	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty (D_{MAX} = 0.83) and junction temperature *(see Figure 4)*.
7. L = 45 mH, starting T_J = 25°C.
8. Infinite cooling condition *(refer to the SEMI G30−88)*.
9. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

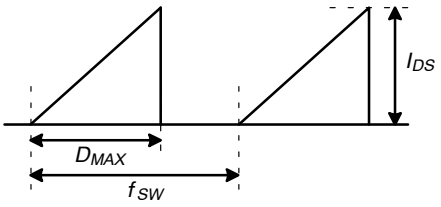

Figure 4. Repetitive Peak Switching Current

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THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
θ_{JA}	Junction−to−Ambient Thermal Impedance (Note 10)	80	°C/W
θ_{JC}	Junction−to−Case Thermal Impedance (Note 11)	20	°C/W
Ψ_{JT}	Junction−to−Top Thermal Impedance (Note 12)	35	°C/W

10. Infinite cooling condition *(refer to the SEMI G30−88)*.
11. Free standing with no heat−sink under natural convection.
12. Measured on the package top surface.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SENSEFET SECTION						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{CC} = 0 V, I_D = 250 μA	650	−	−	V
I_{DSS}	Zero−Gate−Voltage Drain Current	V_{DS} = 520 V, T_A = 125°C	−	−	250	μA
$R_{DS(ON)}$	Drain−Source On−State Resistance	V_{GS} = 10 V, I_D = 1 A	−	1.8	2.2	Ω
C_{ISS}	Input Capacitance (Note 13)	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz	−	515	−	pF
C_{OSS}	Output Capacitance (Note 13)	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz	−	75	−	pF
t_r	Rise Time	V_{DS} = 325 V, I_D = 4 A, R_G = 25 Ω	−	26	−	ns
t_f	Fall Time	V_{DS} = 325 V, I_D = 4 A, R_G = 25 Ω	−	25	−	ns
$t_{d(on)}$	Turn−On Delay Time	V_{DS} = 325 V, I_D = 4 A, R_G = 25 Ω	−	14	−	ns
$t_{d(off)}$	Turn−Off Delay Time	V_{DS} = 325 V, I_D = 4 A, R_G = 25 Ω	−	32	−	ns
CONTROL SECTION						
f_S	Switching Frequency (Note 13)	V_{CC} = 14 V, V_{FB} = 4 V	61	67	73	kHz
Δf_S	Switching Frequency Variation (Note 13)	−25°C < T_J < 125°C	−	±5	±10	%
D_{MAX}	Maximum Duty Ratio	V_{CC} = 14 V, V_{FB} = 4 V	71	77	83	%
D_{MIN}	Minimum Duty Ratio	V_{CC} = 14 V, V_{FB} = 0 V	−	−	0	%
I_{FB}	Feedback Source Current	V_{FB} = 0	120	150	180	μA
V_{START}	UVLO Threshold Voltage	V_{FB} = 0 V, V_{CC} Sweep	11	12	13	V
V_{STOP}		After Turn−on, V_{FB} = 0 V	7.0	7.7	8.5	V
V_{OP}	V_{CC} Operating Range		13	−	22.5	V
$t_{S/S}$	Internal Soft−Start Time	V_{STR} = 40 V, V_{CC} Sweep	−	15	−	ms
BURST−MODE SECTION						
V_{BURH}	Burst−Mode Voltage	V_{CC} = 14 V, V_{FB} Sweep	0.6	0.7	0.8	V
V_{BURL}			0.4	0.5	0.6	V
Hys			−	200	−	mV

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
PROTECTION SECTION							
I_{LIM}	Peak Drain Current Limit		di/dt = 300 mA/μs	1.44	1.60	1.76	A
V_{SD}	Shutdown Feedback Voltage		V_{CC} = 14 V, V_{FB} Sweep	5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{CC} = 14 V, V_{FB} = 4 V	2.0	2.7	3.4	μA
t_{LEB}	Leading−Edge Blanking Time (Note 13, 15)			–	400	–	ns
V_{OVP}	Over−Voltage Protection		V_{CC} Sweep	22.5	24.0	25.5	V
t_{OSP}	Output Short Protection (Note 13)	Threshold Time	OSP Triggered when $t_{ON} < t_{OSP}$ & $V_{FB} > V_{OSP}$ (Lasts Longer than t_{OSP_FB})	0.7	1.0	1.3	μs
V_{OSP}		Threshold V_{FB}		1.4	1.6	1.8	V
t_{OSP_FB}		V_{FB} Blanking Time		2.0	2.5	3.0	μs
T_{SD}	Thermal Shutdown Temperature (Note 13)		Shutdown Temperature	125	135	145	°C
Hys			Hysteresis	–	40	–	°C
TOTAL DEVICE SECTION							
I_{OP}	Operating Supply Current, (Control Part in Burst Mode)		V_{CC} = 14 V, V_{FB} = 0 V	1.0	1.5	2.0	mA
I_{OPS}	Operating Switching Current, (Control Part and SENSEFET Part)		V_{CC} = 14 V, V_{FB} = 2 V	2.1	2.5	2.9	mA
I_{START}	Start Current		V_{CC} = 11 V (Before V_{CC} Reaches V_{START})	400	500	600	μA
I_{CH}	Startup Charging Current		V_{CC} = V_{FB} = 0 V, V_{STR} = 40 V	0.95	1.10	1.50	mA
V_{STR}	Minimum V_{STR} Supply Voltage		V_{CC} = V_{FB} = 0 V, V_{STR} Sweep	–	26	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

13. Although these parameters are guaranteed, they are not 100% tested in production.
14. Average value.
15. t_{LEB} includes gate turn−on time.

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Table 1. COMPARISON OF FSFM300N AND FSGM300N

Function	FSFM300N	FSGM300N	Advantages of FSFM300N
Random Frequency Fluctuation		Built−in	Low EMI
Operating Current	3 mA	1.4 mA	Very low stand−by power
Protections	OLP OVP AOCP TSD	OLP OVP OSP AOCP TSD with Hysteresis	Enhanced protections and high reliability
Power Balance	Long T_{CLD}	Very Short T_{CLD}	The difference of input power between the low and high input voltage is quite small

TYPICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

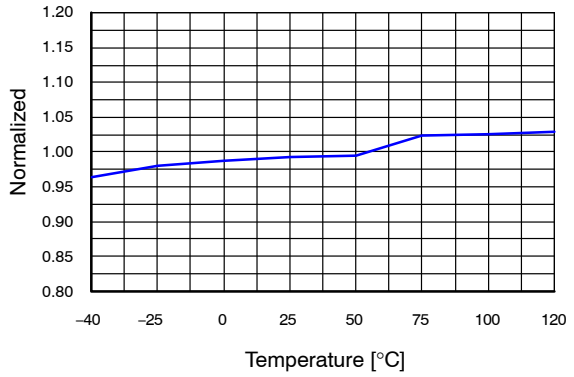

Figure 5. Operating Supply Current (I_{OP}) vs. T_A

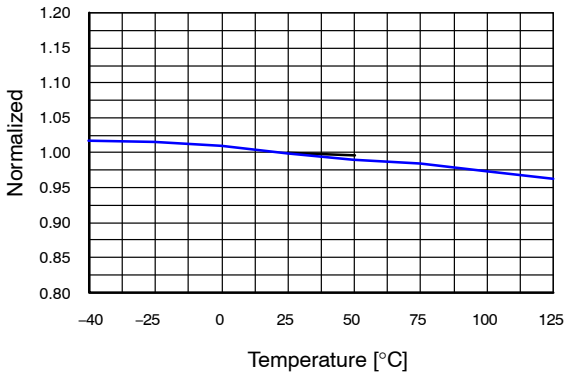

Figure 6. Operating Switching Current (I_{OPS}) vs. T_A

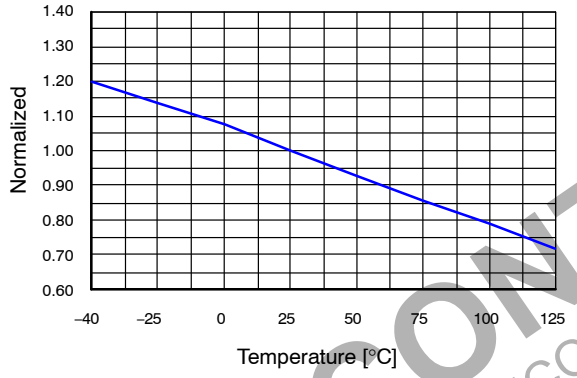

Figure 7. Startup Charging Current (I_{CH}) vs. T_A

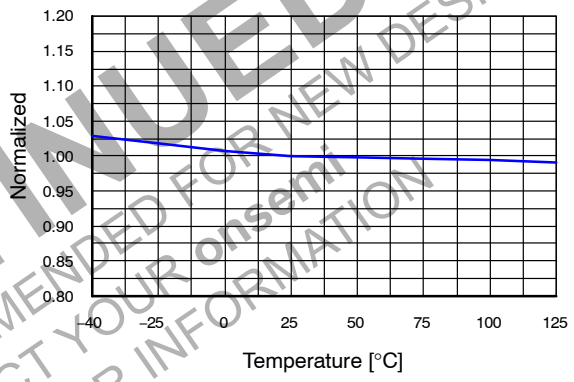

Figure 8. Peak Drain Current Limit (I_{LIM}) vs. T_A

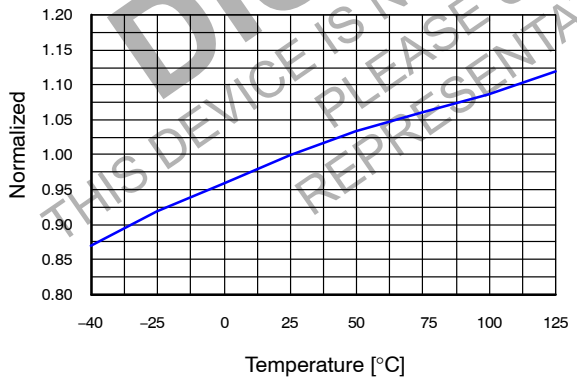

Figure 9. Feedback Source Current (I_{FB}) vs. T_A

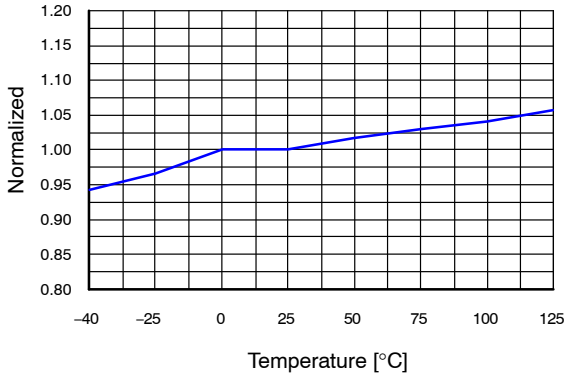

Figure 10. Shutdown Delay Current (I_{DELAY}) vs. T_A

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TYPICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

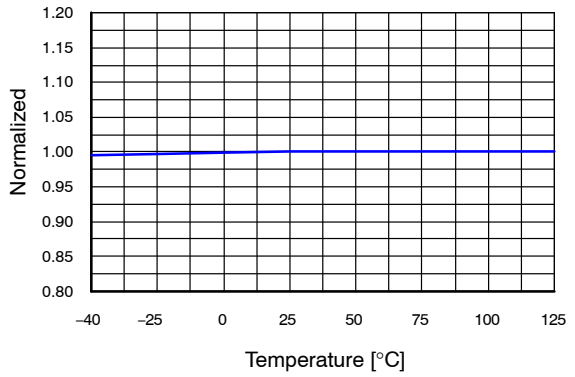

Figure 11. UVLO Threshold Voltage (V_{START}) vs. T_A

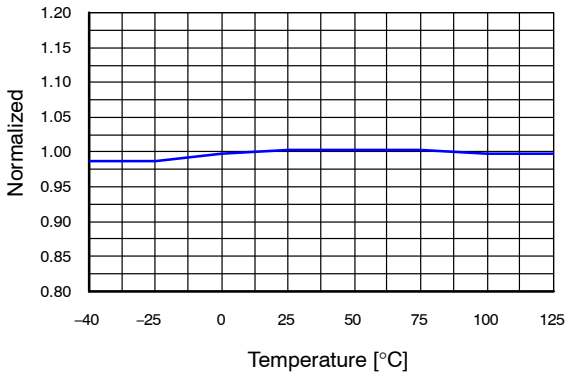

Figure 12. UVLO Threshold Voltage (V_{STOP}) vs. T_A

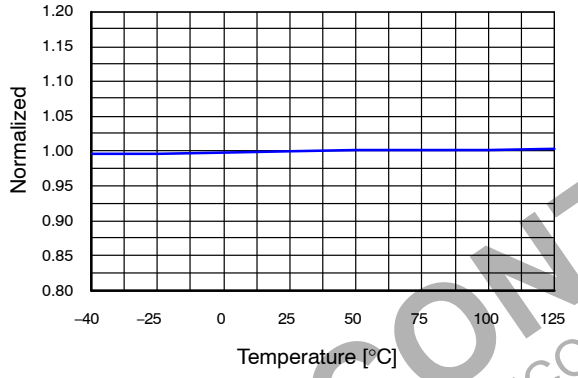

Figure 13. Shutdown Feedback Voltage (V_{SD}) vs. T_A

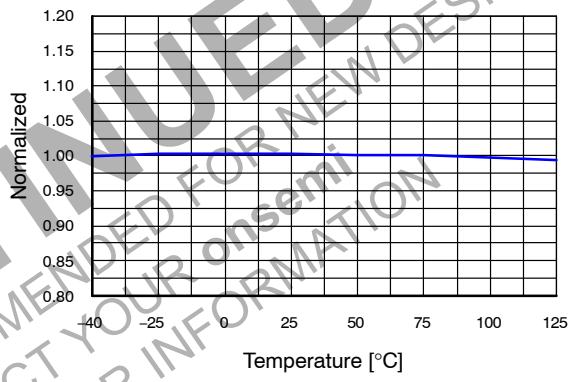

Figure 14. Over−Voltage Protection (V_{OVP}) vs. T_A

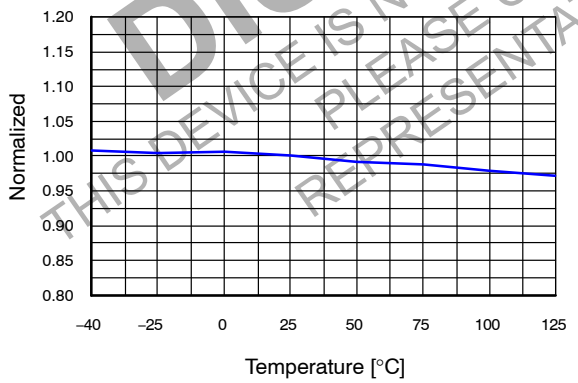

Figure 15. Switching Frequency (f_S) vs. T_A

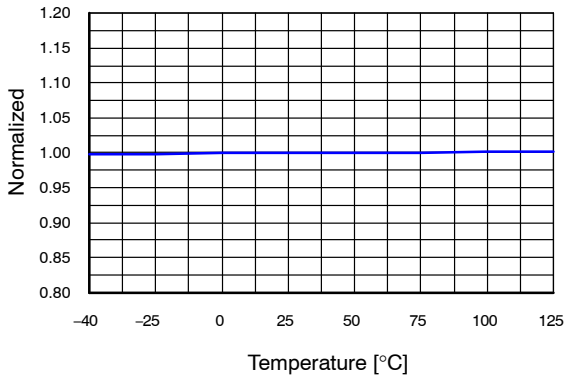

Figure 16. Maximum Duty Ratio (D_{MAX}) vs. T_A

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FUNCTIONAL DESCRIPTION

Startup

At startup, an internal high−voltage current source supplies the internal bias and charges the external capacitor (C_{Vcc}) connected to the V_{CC} pin, as illustrated in Figure 17. When V_{CC} reaches 12 V, the FSGM300N begins switching and the internal high−voltage current source is disabled. The FSGM300N continues normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 7.7 V.

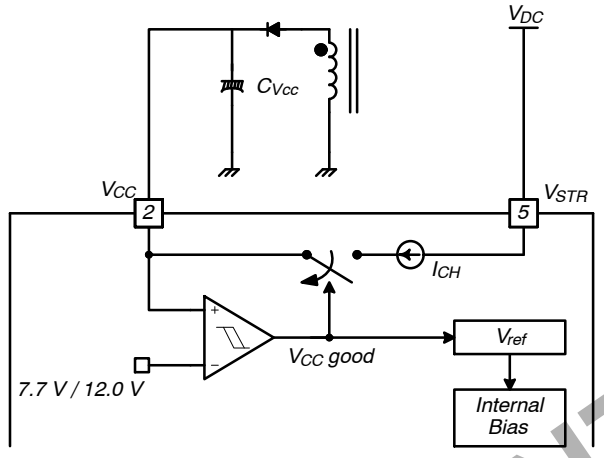

Figure 17. Startup Block

Soft−Start

The FSGM300N has an internal soft−start circuit that increases PWM comparator inverting input voltage, together with the SENSEFET current, slow ly after it starts. The typical soft−start time is 15 ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This helps prevent transformer saturation and reduces stress on the secondary diode during startup.

Feedback Control

This device employs current−mode control, as show n in Figure 18. An opto−coupler (such as the FOD817) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5 V, the opto−coupler LED current increases, pulling down the feedback voltage and reducing drain current. This typically occurs when the input voltage is increased or the output load is decreased.

Pulse−by−Pulse Current Limit

Because current−mode control is employed, the peak current through the SENSEFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 18. Assuming that the 150 μA current source flows only through the internal resistor (3R + R = 16 kΩ), the cathode voltage of diode D2 is about 2.4 V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.4 V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current through the SENSEFET is limited.

Leading−Edge Blanking (LEB)

At the instant the internal SENSEFET is turned on, a high−current spike usually occurs through the SENSEFET, caused by primary−side capacitance and secondary−side rectifier reverse recovery. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSGM300N employs a leading−edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for t_{LEB} (400 ns) after the SenseFET is turned on.

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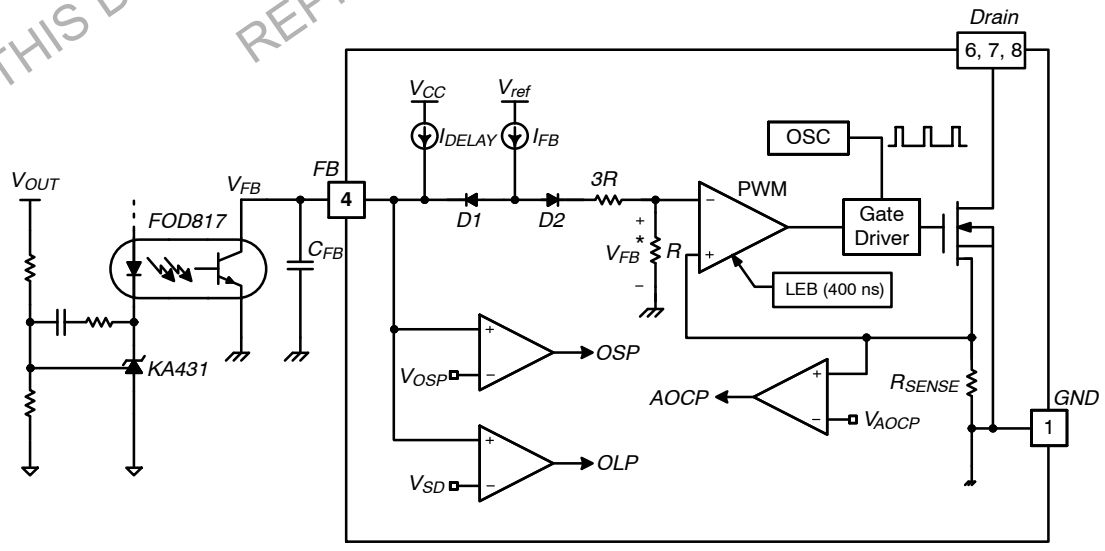

Figure 18. Pulse Width Modulation Circuit

Protection Circuits

The FSGM300N has several self−protective functions, such as Overload Protection (OLP), Abnormal Over−Current Protection (AOCP), Output−Short Protection (OSP), Over−Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto−restart. Once the fault condition is detected, switching is terminated and the SENSEFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the Under−Voltage Lockout (UVLO) stop voltage of 7.7 V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 12.0 V, the FSGM300N resumes normal operation. If the fault condition is not removed, the SENSEFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto−restart can alternately enable and disable the switching of the power SENSEFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

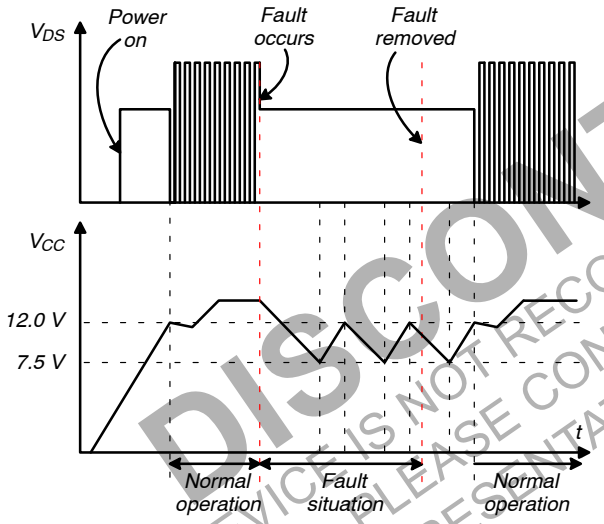

Figure 19. Auto−Restart Protection Waveforms

Overload Protection (OLP)

Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse−by−pulse current limit capability, the maximum peak current through the SENSEFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum pow er, the output voltage (V_{OUT}) decreases below the set voltage. This reduces the current through the opto−coupler LED, which also reduces the opto−coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.4 V, D1 is blocked and the 2.7 μA current source starts to charge C_{FB} slowly up. In this condition, V_{FB} continues increasing until it reaches 6.0 V, when the switching operation is terminated, as show n in Figure 20. The delay time for shutdown is the time required to charge C_{FB} from 2.4 V to 6.0 V with 2.7 μA. A 25 ~ 50 ms delay is typical for most applications. This protection is implemented in auto−restart mode.

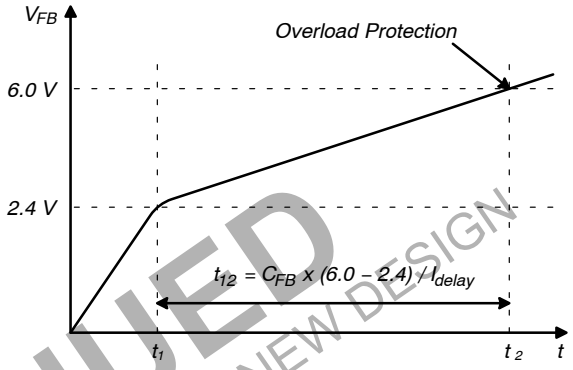

Figure 20. Overload Protection

Abnormal Over−Current Protection (AOCP)

When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SENSEFET during the minimum turn−on time. Even though the FSGM300N has overload protection, it is not enough to protect the FSGM300N in that abnormal case; since severe current stress is imposed on the SENSEFET until OLP is triggered. The FSGM300N internal AOCP circuit is shown in Figure 21. When the gate turn−on signal is applied to the power SENSEFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the S−R latch, resulting in the shutdown of the SMPS.

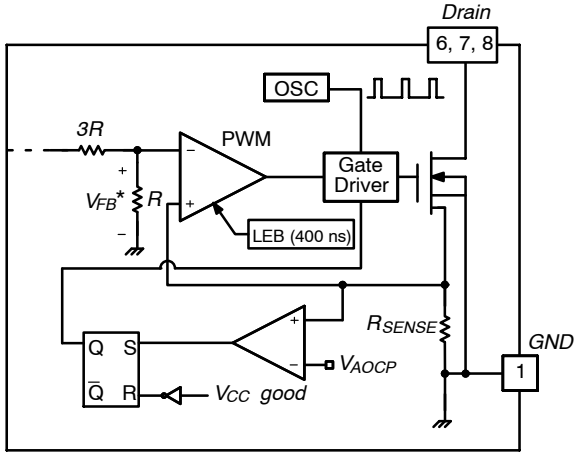

Figure 21. Abnormal Over−Current Protection

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Output−Short Protection (OSP)

If the output is shorted, steep current with extremely high di/dt can flow through the SENSEFET during the minimum turn−on time. Such a steep current brings high−voltage stress on the drain of the SENSEFET when turned off. To protect the device from this abnormal condition, OSP is included. It is comprised of detecting V_{FB} and SENSEFET turn−on time. When the V_{FB} is higher than 1.6 V and the SENSEFET turn−on time is lower than 1.0 μs, the FSGM300N recognizes this condition as an abnormal error and shuts down PWM switching until V_{CC} reaches V_{START} again. An abnormal condition output short is shown in Figure 22.

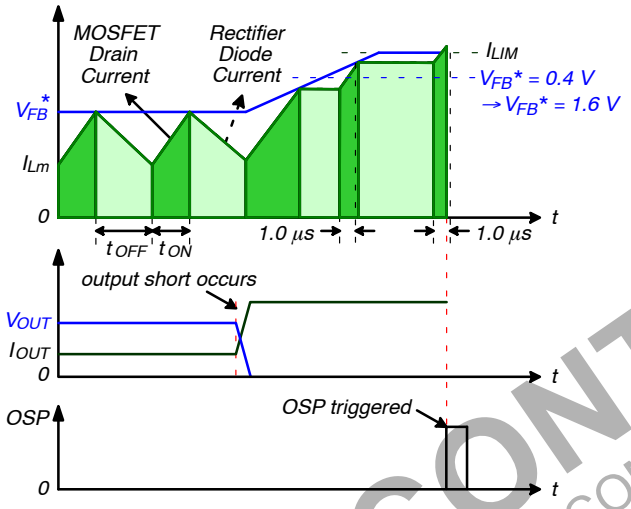

Figure 22. Output−Short Protection

Over−Voltage Protection (OVP)

If the secondary−side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto−coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the V_{CC} is proportional to the output voltage and the FSGM300N uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.0 V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.0 V.

Thermal Shutdown (TSD)

The SENSEFET and the control IC on a die in one package makes it easier for the control IC to detect the over temperature of the SENSEFET. If the temperature exceeds ~135°C, the thermal shutdown is triggered and stops operation. The FSGM300N operates in auto−restart mode until the temperature decreases to around 95°C, when normal operation resumes.

Soft Burst−Mode Operation

To minimize power dissipation in standby mode, the FSGM300N enters burst−mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 23, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (500 mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (700 mV), switching resumes. The feedback voltage then falls and the process repeats. Burst−mode operation alternately enables and disables switching of the SENSEFET, thereby reducing switching loss in standby mode.

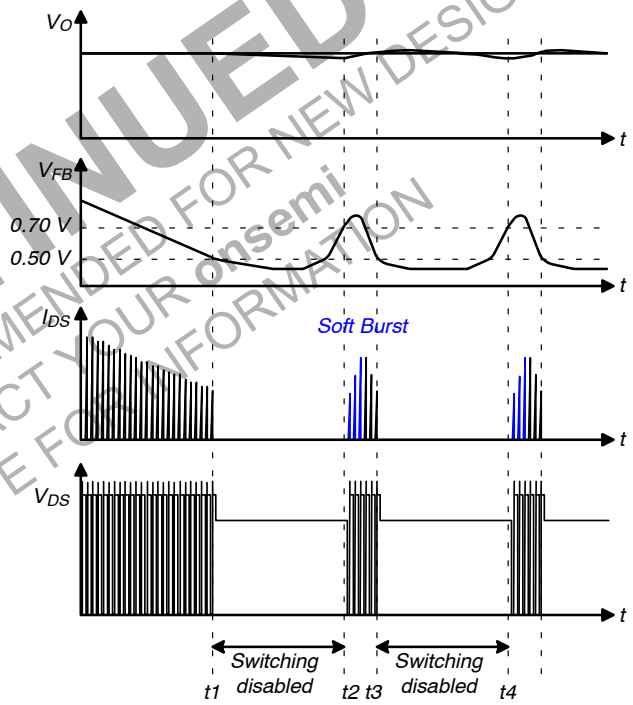

Figure 23. Burst−Mode Operation

Random Frequency Fluctuation (RFF)

Fluctuating switching frequency of an SMPS can reduce EMI by spreading the energy over a wide frequency range. The amount of EMI reduction is directly related to the switching frequency variation, which is limited internally. The switching frequency is determined randomly by external feedback voltage and internal free−running oscillator at every switching instant. This Random Frequency Fluctuation scatters the EMI noise around typical switching frequency (67 kHz) effectively and can reduce the cost of the input filter included to meet the EMI requirements (e.g. EN55022).

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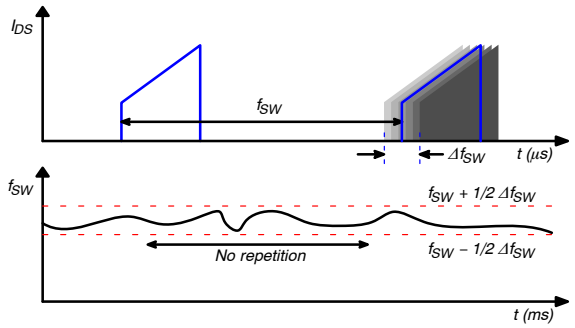

Figure 24. Random Frequency Fluctuation

TYPICAL APPLICATION CIRCUIT

Table 2. TYPICAL APPLICATION CIRCUIT

Application	Input Voltage	Rated Output	Rated Power
LCD Monitor Power Supply	85 ~ 265 V_{AC}	5.0 V (2 A) 14.0 V (1.2 A)	26.8 W

Key Design Notes:

1. The delay time for overload protection is designed to be about 30 ms with C105 (22 nF). OLP time between 25 ms (18 nF) and 50 ms (39 nF) is recommended.
2. The SMD−type capacitor (C106) must be placed as close as possible to the V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improve ESD and surge immunity. Capacitance between 100 nF and 220 nF is recommended.

Schematic

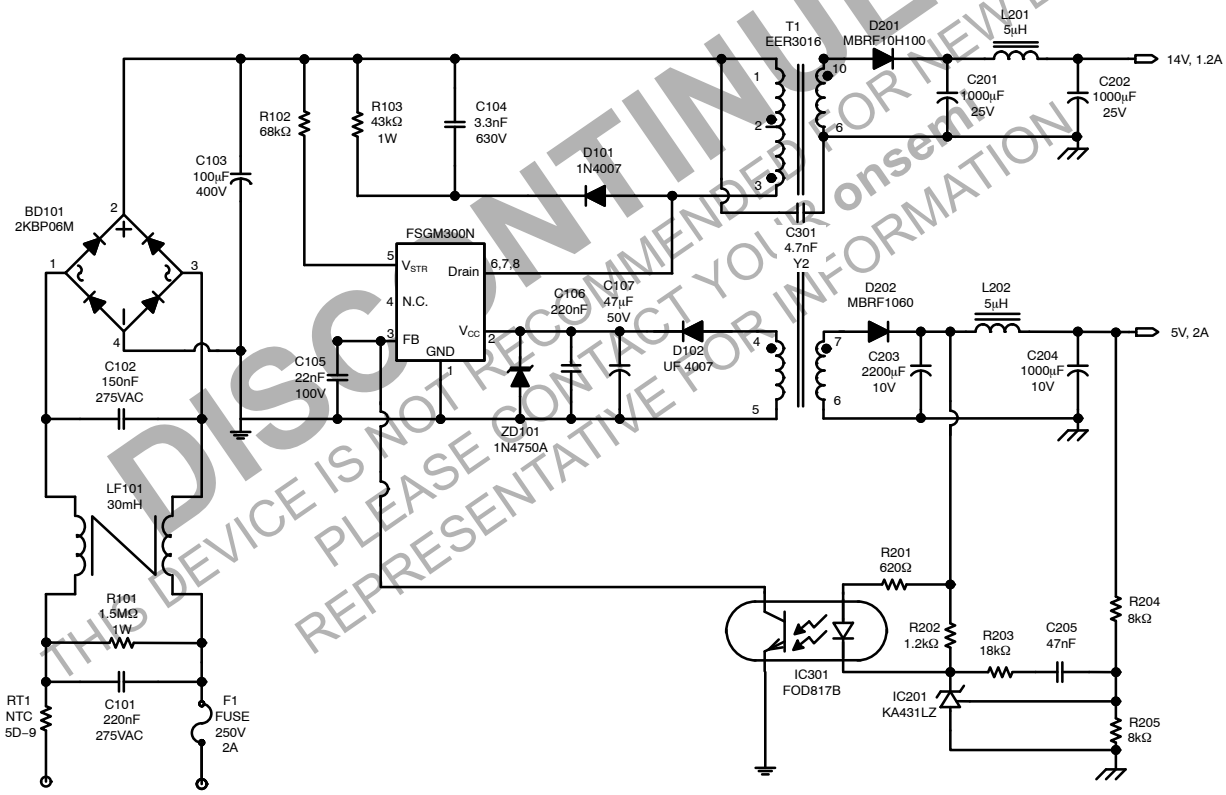

Figure 25. Schematic of Demonstration Board

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Transformer

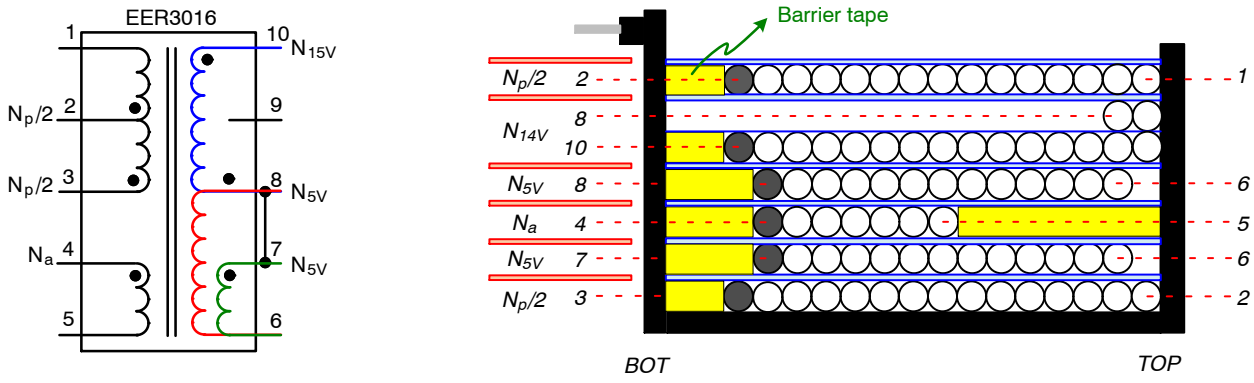

Figure 26. Schematic of Transformer

Winding Specification

Table 3. WINDING SPECIFICATION

	Pin (S → F)	Wire	Turns	Winding Method	Barrier Tape		
					TOP	BOT	Ts
$N_p/2$	3 → 2	0.25 φ x 1	21	Solenoid Winding		2.0 mm	1
Insulation: Polyester Tape t = 0.025 mm, 2 Layers							
N_{5V}	7 → 6	0.4 φ x 2 (TIW)	3	Solenoid Winding		3.0 mm	1
Insulation: Polyester Tape t = 0.025 mm, 2 Layers							
N_a	4 → 5	0.2 φ x 1	7	Solenoid Winding	4.0 mm	3.0 mm	1
Insulation: Polyester Tape t = 0.025 mm, 2 Layers							
N_{5V}	8 → 6	0.4 φ x 2 (TIW)	3	Solenoid Winding		3.0 mm	1
Insulation: Polyester Tape t = 0.025 mm, 2 Layers							
N_{14V}	10 → 8	0.4 φ x 2 (TIW)	5	Solenoid Winding		2.0 mm	1
Insulation: Polyester Tape t = 0.025 mm, 2 Layers							
$N_p/2$	2 → 1	0.25 φ x 1	21	Solenoid Winding		2.0 mm	1
Insulation: Polyester Tape t = 0.025 mm, 2 Layers							

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Electrical Characteristics

Table 4. ELECTRICAL CHARACTERISTICS

	Pin	Specification	Remark
Inductance	1 – 3	900 μH ±7%	67 kHz, 1 V
Leakage	1 – 3	15 μH Maximum	Short All Other Pins

Core & Bobbin

- Core: EER3016 (Ae = 109.7 mm^2)
- Bobbin: EER3016

Bill of Materials

Table 5. Bill of Materials

Part #	Value	Note
Fuse		
F101	250 V 2 A	
NTC		
NTC101	5D−9	DSC
Resistor		
R101	1.5 MΩ, J	1 W
R102	68 kΩ, J	1/2 W
R103	43 kΩ, J	1 W
R201	620 Ω, F	1/4 W, 1%
R202	1.2 kΩ, F	1/4 W, 1%
R203	18 kΩ, F	1/4 W, 1%
R204	8 kΩ, F	1/4 W, 1%
R205	8 kΩ, F	1/4 W, 1%
IC		
FSGM300N	FSGM300N	ON Semiconductor
IC201	KA431LZ	ON Semiconductor
IC301	FOD817B	ON Semiconductor
Diode		
D101	1N4007	Vishay
D102	UF4007	Vishay
ZD101	1N4750	Vishay
D201	MBRF10H100	ON Semiconductor
D202	MBRF1060	ON Semiconductor
BD101	2KBP06	Vishay

Part #	Value	Note
Capacitor		
C101	220 nF / 275 V	Box (Pilkor)
C102	150 nF / 275 V	Box (Pilkor)
C103	100 μF / 400 V	Electrolytic (SamYoung)
C104	3.3 nF / 630 V	Film (Sehwa)
C105	27 nF / 100 V	Film (Sehwa)
C106	220 nF	SMD (2012)
C107	47 μF / 50 V	Electrolytic (SamYoung)
C201	1000 μF / 25 V	Electrolytic (SamYoung)
C202	1000 μF / 25 V	Electrolytic (SamYoung)
C203	2200 μF / 10 V	Electrolytic (SamYoung)
C204	1000 μF / 16 V	Electrolytic (SamYoung)
C205	47 nF / 100 V	Film (Sehwa)
C301	4.7 nF / Y2	Y−cap (Samhwa)
Inductor		
LF101	30 mH	Line filter 0.5Ø
L201	5 μH	5 A Rating
L202	5 μH	5 A Rating
Transformer		
T101	900 μH	

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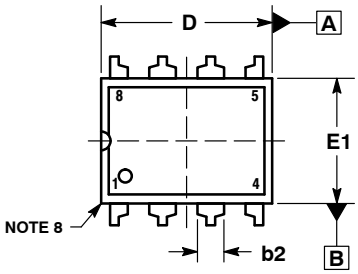
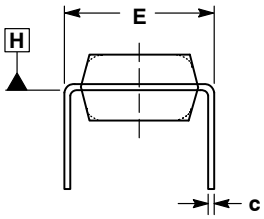
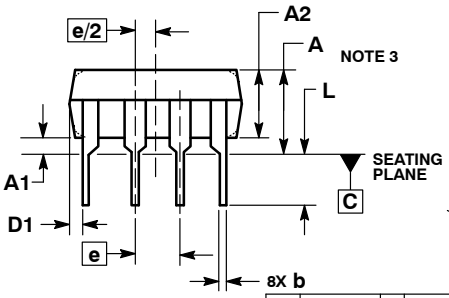


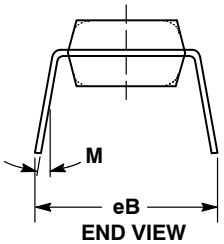
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



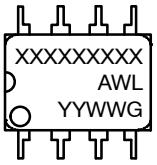
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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