



# FSC-BT616V

**Car Spec Grade Bluetooth 5.1 specifications Wireless MCU Module**

**Datasheet**

**Version 1.2**

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## Revision History

Version	Date	Notes	
1.0	2020/04/14	Initial Version	Fish
1.1	2020/11/05	Update the pin definition to correspond to the chip	Fish
1.2	2021/11/04	Modify Bluetooth Version: Upgrade from BT5 to BT5.1 Change storage temperature: -40°C to +125°C	Marsh

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## 1. INTRODUCTION

### Overview

FSC-BT616V is a wireless microcontroller (MCU) targeting Bluetooth 5.1 low energy applications.

Very low active RF and MCU current and low-power mode current consumption provide excellent battery lifetime and allow for operation on small coin cell batteries and in energy-harvesting applications.

FSC-BT616V contains a 32-bit ARM® Cortex®-M3 core that runs at 48 MHz as the main processor and a rich peripheral feature set that includes a unique ultra-low power sensor controller. This sensor controller is ideal for interfacing external sensors and for collecting analog and digital data autonomously while the rest of the system is in sleep mode. Thus, FSC-BT616V is great for a wide range of applications where long battery lifetime, small form factor, and ease of use is important.

It supports GAP, ATT/GATT, SMP, L2CAP profiles. It integrates Baseband controller in a small package (Integrated chip antenna), so the designers can have better flexibilities for the product shapes.

### Features

- 2.4-GHz RF Transceiver Compatible With Bluetooth low energy (BLE) 5.1 Specifications
- Qualified for Automotive Applications
- Link Budget of 102 dB for BLE
- Integrate MCU to execute Bluetooth protocol stack.
- Postage stamp sized form factor

- Excellent Receiver Sensitivity (-95 dBm for Bluetooth low energy 1Mbps), Selectivity, and Blocking Performance
- Low power
- Class 1.5 support(up to +5 dBm)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 921.6Kbps
- UART, I2C, SPI, 12-bit ADC (200ks/S) data connection interfaces.
- Support the OTA upgrade.
- Bluetooth stack profiles support: LE HID, and all BLE protocols.
- Support eight capacitance sensor button
- Integrated temperature sensor
- Operating temperature: -40°C to +105°C
- Device HBM ESD Classification Level 2
- Device CDM ESD Classification Level C3

### Application

- Automotive Applications
  - Car Access
  - Keyless Entry
  - Passive Entry/Passive Start (PEPS) Systems
  - Car Sharing
  - Piloted Parking
  - Wireless Onboard Diagnostics (OBD)
  - Cable Replacement
  - Remote Control
  - Sensors
- Industrial
  - Logistics
  - Production and Manufacturing Automation
  - Asset Tracking and Management
  - HMI and Remote Display
  - Access Control

Module picture as below showing

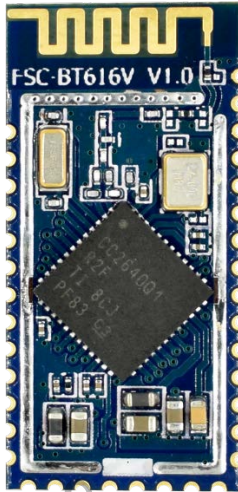


Figure 1: FSC-BT616V Picture

## 2. General Specification

**Table 1:** General Specifications

Categories	Features	Implementation
Wireless Specification	Chip	TI CC2640R2F-Q1
	Bluetooth Version	Bluetooth low energy (BLE) 5.1 Specifications
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+5 dBm (Maximum)
	Receive Sensitivity	-95 dBm (Typical)
	Raw Data Rates (Air)	2 Mbps(Bluetooth 5.1)
	Modulation	GFSK
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
	GPIO	5, 6, 7, 8 data bit character
		22(maximum – configurable) lines
		O/P drive strength (4 mA)
		Pull-up resistor (33 KΩ) control
	I2C Interface	Read pin-level
		1 (configurable from GPIO total). Up to 400 kbps
		Up to 2 SSI interfaces with a frequency of up to 4 MHz
	SS1 Interface	Support both master and slave mode
		SPI, MICROWIRE, TI
		Analog input voltage range: 1.8V ~ 3.8V
	ADC Interface	Supports single 12-bit SAR ADC conversion
		8 channels (configured from GPIO total)
		Up to 200MSPS conversion
	PWM	4 General-Purpose Timer Modules
		Four General-Purpose Timer Modules
		(Eight 16-Bit or Four 32-Bit Timers, PWM Each)
Profiles	Class Bluetooth	No Support
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
		BT5.1 Specifications
		MFI Support
Maximum Connections	Classic Bluetooth	No Support
	Bluetooth Low Energy	1Clients(TBD)
FW upgrade		Over the Air
		Xds
Supply Voltage	Supply	1.8V ~ 3.8V
Power Consumption		Max Peak Current(TX Power @ +5dBm TX): 20mA
		Standby Doze (Wait event) - ~1mA (TBD)
		Deep Sleep - 2uA(RTC Running and RAM/CPU Retention) (TBD)

Physical	Dimensions	13mm X 26.9mm X 2.0mm; Pad Pitch 1.5mm	
Environmental	Operating	-40°C to +105°C	
	Storage	-40°C to +125°C	
Miscellaneous	Lead Free	Lead-free and RoHS compliant	
	Warranty	One Year	
Humidity		10% ~ 90% non-condensing	
MSL grade:		MSL 3	
ESD grade:	Human Body Model	All pins: ±2000V	
	Charged device model	RF pins/ Non-RF pins: ±500V; XOCS pin: ±250V	

### 3. HARDWARE SPECIFICATION

#### 3.1 Block Diagram and PIN Diagram

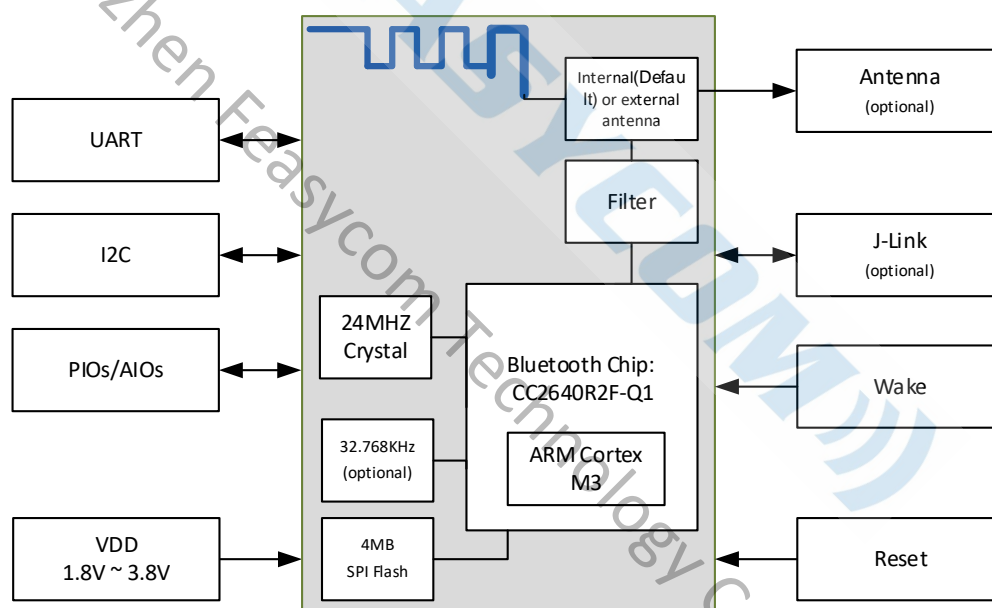


Figure 2: Block Diagram



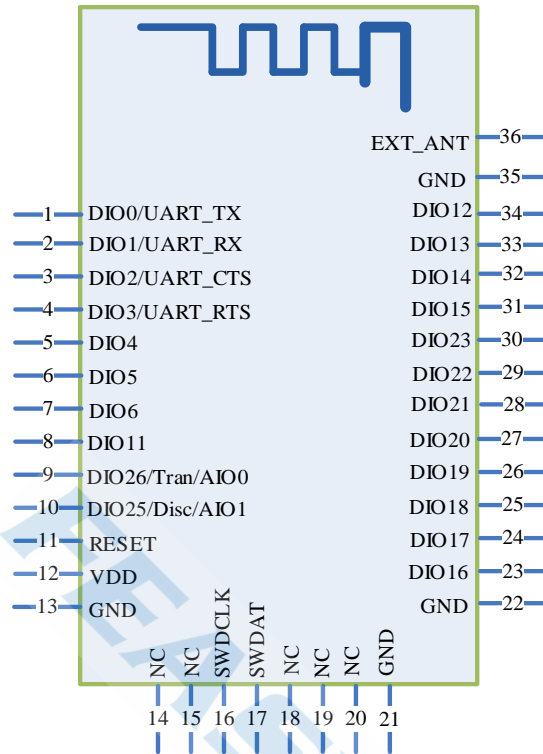


Figure 3: FSC-BT616V PIN Diagram (Top View)

### 3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	DIO0/UART_TX	O	UART data output	Note 1
2	DIO1/UART_RX	I	UART data input	Note 1
3	DIO2/UART_CTS	I/O	UART clear to send active low Alternative Function: Programmable input/output line	Note 1
4	DIO3/UART_RTS	I/O	UART request to send active low Alternative Function: Programmable input/output line	Note 1
5	DIO4	I/O	Programmable input/output line	
6	DIO5	I/O	Programmable input/output line	
7	DIO6	I/O	Programmable input/output line	
8	DIO11	I/O	Programmable input/output line	
9	DIO26/Tran/AIO0	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU change UART transmission mode.	Note 1
10	DIO25/Disc/AIO1	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU disconnect bluetooth.	Note 1
11	RESET	I	External reset input: Active LOW, with an internal pull-up. Set this pin low reset to initial state.	

12	VDD	Vdd	Power supply voltage 1.8V ~ 3.8V	
13	GND	Vss	Power Ground	
14	NC	NC		
15	NC	NC		
16	SWDCLK	I/O	Debugging through the clk line(Default)	Note 1
17	SWDAT	I/O	Debugging through the data line(Default)	Note 1
18	NC	NC		
19	NC	NC		
20	NC	NC		
21	GND	Vss	Power Ground	
22	GND	Vss	Power Ground	
23	DIO16	I/O	Programmable input/output line * The I/O port for reuse.	Note 6
24	DIO17	I/O	Programmable input/output line * The I/O port for reuse.	Note 6
25	DIO18	I/O	Programmable input/output line * The I/O port for reuse.	Note 6
26	DIO19	I/O	Programmable input/output line * The I/O port for reuse.	Note 6
27	DIO20	I/O	Programmable input/output line	
28	DIO21	I/O	Programmable input/output line	
29	DIO22	I/O	Programmable input/output line Alternative Function: I2C CLK line (Default)	Note 1,3
30	DIO23	I/O	Programmable input/output line Alternative Function: I2C DATA line (Default)	Note 1,3
31	DIO15	I/O	Programmable input/output line	Note 1
32	DIO14	I/O	Programmable input/output line Alternative Function: LED(Default)	Note 1,4
33	DIO13	I/O	Programmable input/output line Alternative Function: BT Status(Default)	Note 1,2
34	DIO12	I/O	Programmable input/output line	Note 1
35	GND	Vss	RF Ground	
36	EXT_ANT	O	RF signal output	Note 5

#### Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	BT Status(Default)-- Disconnected: Low Level; Connected: High Level.
Note 3	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 4	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 5	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the OR resistance to block out the on-board antenna; Or contact Feasycom for modification.

Note 6	This I / O port is shared with the internal SPI Flash chip. We do not recommend using this pin, floating processing. This pin is only available when the module is not equipped with air-upgrade function.
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## 4. PHYSICAL INTERFACE

### 4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

### 4.2 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Low voltage reset (LVR) or Software Reset(SYSRESETREQ, CPU Reset, CHIPRST).

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

### 4.3 General Purpose Analog IO

- 12-bit SAR ADC engine with up to 200KSPS conversion rate
- Conversion range: VSSA to VDDA (1.8 to 3.8 V)
- Temperature sensor

Twelve 12-bit 1 μs multi-channel ADC is integrated in the device.

The conversion range is between 1.8 V < VDD < 3.8 V. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages. The ADC can be triggered from the events generated by the general-purpose timers and the advanced-control timers with internal connection.

The temperature sensor can be used to generate a voltage that varies linearly with temperature. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.

### 4.4 General Purpose Digital IO

There are 22 general purpose digital IOs defined in the module. All these GPIOs can be configured by software to

realize various functions, such as button controls, LED drives or interrupt signals to host controller, etc. Do not connect them if not use.

The I/O type of each I/O pins can be configured by software individually as Input or Push-pull output mode. After the chip is reset, the I/O mode of all pins is input mode with no pull-up and pull-down enable. Each I/O pin has an individual pull-up and pull-down resistor which is about 30 kΩ ~ 50 kΩ for VDD and Vss.

## 4.5 RF Interface

For This Module, the default mode for antenna is internal ,it also has the interface for external antenna. If you need to use an external antenna, by modifying the module on the OR resistance to block out the on-board antenna; Or contact Feasycom for modification.

The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 5.1; 125-Kbps to 2-Mbps over the air data rate.
- TX output power of +5dBm.
- Receiver to achieve maximum sensitivity -95dBm @ 1 Mbps BLE.

## 4.6 Serial Interfaces

### 4.6.1 UART

FSC-BT616V provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART\_RX and UART\_TX transfer data between the two devices. The remaining two signals, UART\_CTS and UART\_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT616V deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

**Table 3:** Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)

	Maximum	921600bps(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /1.5/2
Bits per channel		5/6/7/8

When connecting the module to a host, please make sure to follow .

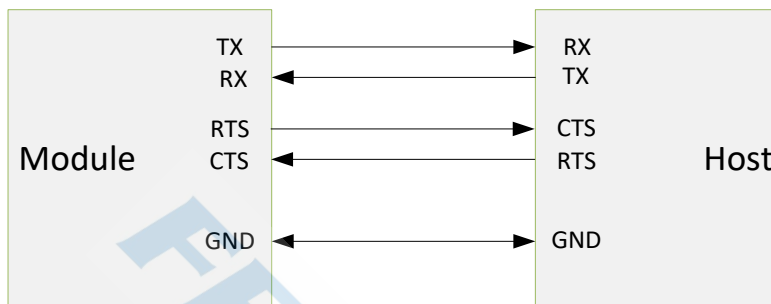


Figure 4: UART Connection

#### 4.6.2 I<sup>2</sup>C Interface

- Up to two I<sup>2</sup>C bus interfaces can support both master and slave mode with a frequency up to 400KHZ.
- Provide arbitration function, optional PEC(packet error checking) generation and checking.
- Supports 7 –bit and 10 –bit addressing mode and general call addressing mode.

The I<sup>2</sup>C interface is an internal circuit allowing communication with an external I<sup>2</sup>C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I<sup>2</sup>C module provides two data transfer rates: 100 kHz of standard mode or 400kHz of the fast mode. The I<sup>2</sup>C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I<sup>2</sup>C bus at the same time. A CRC-8 calculator is also provided in I<sup>2</sup>C interface to perform packet error checking for I<sup>2</sup>C data.

#### 4.7 SSI Interface

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and Texas Instruments synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

#### 4.8 PWM Interface

Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers or as a PWM module.

## 5. ELECTRICAL CHARACTERISTICS

### 5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100ms period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100ms period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

**Table 4:** Absolute Maximum Rating

Parameter	Min	Max	Unit
$V_{DD}-V_{SS}$ - DC Power Supply	-0.3	+4.1	V
$V_{IN}$ - Voltage on any digital pin	-0.3	$V_{DD}+0.3$ (max 4.1)	V
$V_{IN}$ - Voltage on ADC input (Voltage scaling enabled)	-0.3	$V_{DD}$	V
$V_{IN}$ - Voltage on ADC input (Voltage scaling disabled, $V_{DD}$ as reference)	-0.3	$V_{DD} / 2.9$	V
Input RF level		5	dBm
$T_{ST}$ - Storage Temperature	-40	+125	°C
$I_{IO}$ - Maximum Current sunk by a I/O pin		8	mA
$I_{IO}$ - Maximum Current sourced by a I/O pin		8	mA

### 5.2 Recommended Operating Conditions

**Table 5:** Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
$V_{DD}-V_{SS}$ - DC Power Supply	1.8	3.3	3.8	V
$T_A$ - Operating Temperature	-40	25	+105	°C
$I_{IO}$ - Maximum Current sunk by a I/O pin	2	4	6	mA
$I_{IO}$ - Maximum Current sourced by a I/O pin	2	4	6	mA

### 5.3 Input/output Terminal Characteristics

**Table 6:** DC Characteristics

Parameter	Min	Type	Max	Unit
<b><math>V_{DD} = 1.8V</math>, <math>T_A = 25^{\circ}C</math></b>				
$V_{OH}$ - High Level Output Voltage, $I_{IO}=8mA$ IOCURR = 2, high-drive GPIOs only	1.32	1.54	-	V

$V_{OL}$ - Low Level Output Voltage, $I_{IO}=8mA$ IOCURRE = 2, high-drive GPIOs only	-	0.26	0.32	V
$V_{OH}$ - High Level Output Voltage, $I_{IO}=4mA$ , IOCURRE = 1	1.32	1.58	-	V
$V_{OL}$ - Low Level Output Voltage, $I_{IO}=4mA$ , IOCURRE = 1	-	0.21	0.32	V
GPIO pullup current - Input mode, pullup enabled, $V_{pad} = 0V$	-	71.7	-	$\mu A$
GPIO pulldown current - Input mode, pulldown enabled, $V_{pad} = VDD$	-	21.1	-	$\mu A$
GPIO high/low input transition, no hysteresis - IH = 0, transition between reading 0 and reading 1	-	0.88	-	V
GPIO low-to-high input transition, with hysteresis - IH = 1, transition voltage for input read as 0 $\rightarrow$ 1	-	1.07	-	V
GPIO high-to-low input transition, with hysteresis - IH = 1, transition voltage for input read as 1 $\rightarrow$ 0	-	0.74	-	V
GPIO input hysteresis - IH = 1, difference between 0 $\rightarrow$ 1 and 1 $\rightarrow$ 0 points	-	0.33	-	V
<b><math>V_{DD} = 3.0V, T_A = 25^\circ C</math></b>				
$V_{OH}$ - High Level Output Voltage, $I_{IO}=8mA$ IOCURRE = 2, high-drive GPIOs only	-	2.68	-	V
$V_{OL}$ - Low Level Output Voltage, $I_{IO}=8mA$ IOCURRE = 2, high-drive GPIOs only	-	0.33	-	V
$V_{OH}$ - High Level Output Voltage, $I_{IO}=4mA$ , IOCURRE = 1	-	2.72	-	V
$V_{OL}$ - Low Level Output Voltage, $I_{IO}=4mA$ , IOCURRE = 1	-	0.28	-	V
<b><math>V_{DD} = 3.8V, T_A = 25^\circ C</math></b>				
GPIO pullup current - Input mode, pullup enabled, $V_{pad} = 0V$	-	277	-	$\mu A$
GPIO pulldown current - Input mode, pulldown enabled, $V_{pad} = VDD$	-	113	-	$\mu A$
GPIO high/low input transition, no hysteresis - IH = 0, transition between reading 0 and reading 1	-	1.67	-	V
GPIO low-to-high input transition, with hysteresis - IH = 1, transition voltage for input read as 0 $\rightarrow$ 1	-	1.94	-	V
GPIO high-to-low input transition, with hysteresis - IH = 1, transition voltage for input read as 1 $\rightarrow$ 0	-	1.54	-	V
GPIO input hysteresis - IH = 1, difference between 0 $\rightarrow$ 1 and 1 $\rightarrow$ 0 points	-	0.40	-	V
<b><math>T_A = 25^\circ C</math></b>				
$V_{IH}$ - Lowest GPIO input voltage reliably interpreted as a High	-	-	0.8	VDD
$V_{IL}$ - Lowest GPIO input voltage reliably interpreted as a LOW	0.2	-	-	VDD

## 5.4 Analog Characteristics

**Table 7:** Specifications of 12-bit SARADC(voltage scaling enabled, unless otherwise noted.<sup>(1)</sup>)



Parameter	Min	Type	Max	Unit
V <sub>DDA</sub> - Operation Voltage	0	-	VDD	V
R <sub>ADC</sub> - Resolution	-	-	12	bit
F <sub>SPS</sub> - Sampling Rate	-	-	200	KSPS
Offset (Internal 4.3-V equivalent reference <sup>(2)</sup> )	-	2	-	LSB
Gain error (Internal 4.3-V equivalent reference <sup>(2)</sup> )	-	2.4	-	LSB
DNL(3) Differential nonlinearity	-	>-1	-	LSB
INL(4) Integral nonlinearity	-	±3	-	LSB
<b>ENOB - Effective number of bits</b>				
Internal 4.3-V equivalent reference(2), 200ksps, 9.6-kHz input tone	-	9.8	-	bits
VDD as reference, 200 ksps, 9.6-kHz input tone	-	10	-	bits
Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200ksps, 300-Hz input tone	-	11.1	-	bits
<b>THD - Total harmonic distortion</b>				
Internal 4.3-V equivalent reference <sup>(2)</sup> , 200 ksps, 9.6-kHz input tone	-	-65	-	dB
VDD as reference, 200ksps, 9.6-kHz input tone	-	-69	-	dB
Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200ksps, 300-Hz input tone	-	-71	-	dB
<b>SINAD, SNDR - Signal-to-noise and distortion ratio</b>				
Internal 4.3-V equivalent reference <sup>(2)</sup> , 200ksps, 9.6-kHz input tone	-	60	-	dB
VDD as reference, 200ksps, 9.6-kHz input tone	-	63	-	dB
Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200ksps, 300-Hz input tone	-	69	-	dB
<b>SFDR - Spurious-free dynamic range</b>				
Internal 4.3-V equivalent reference <sup>(2)</sup> , 200ksps, 9.6-kHz input tone	-	67	-	dB
VDD as reference, 200ksps, 9.6-kHz input tone	-	72	-	dB
Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200ksps, 300-Hz input tone	-	73	-	dB
Conversion time - Serial conversion, time-to-output, 24-MHz clock	-	50	-	Clock-cycles
Current consumption - Internal 4.3-V equivalent reference <sup>(2)</sup>	-	0.66	-	mA
Current consumption - VDD as reference	-	0.75	-	mA
Reference voltage - VDD as reference (Also known as RELATIVE) (input voltage scaling enabled)	-	VDD	-	V
Input impedance - 200 ksps, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time	-	>1	-	MΩ

(1) Using IEEE Std 1241™-2010 for terminology and test methods.

(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.

(3) No missing codes. Positive DNL typically varies from +0.3 to +3.5, depending on device.

(4) For a typical example.



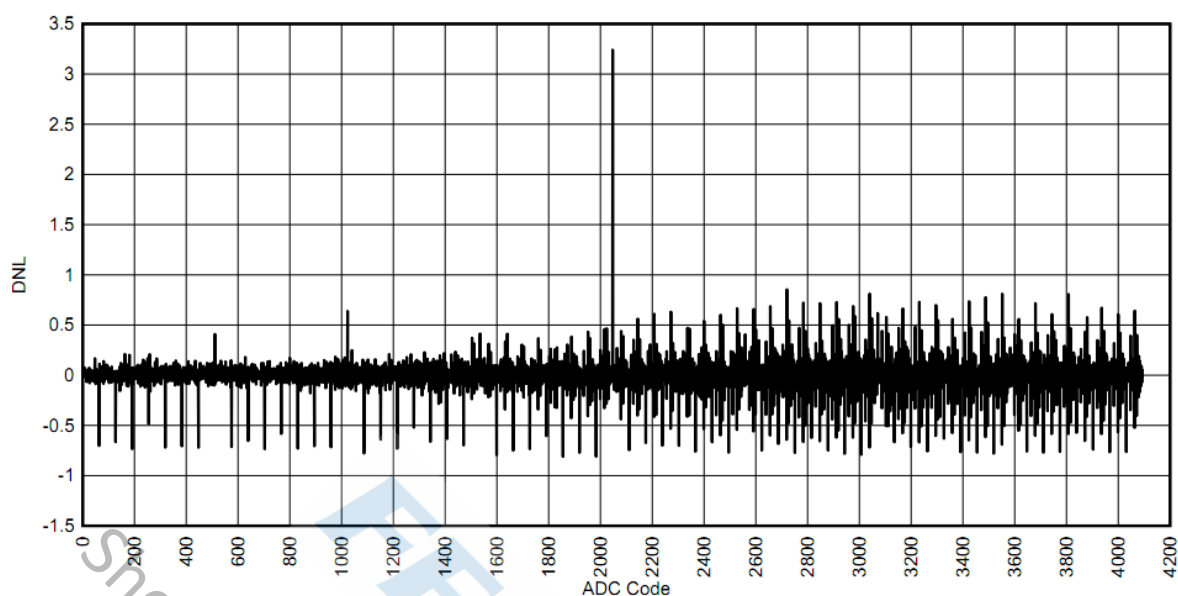


Figure 5: SoC ADC DNL vs ADC Code (Internal Reference)

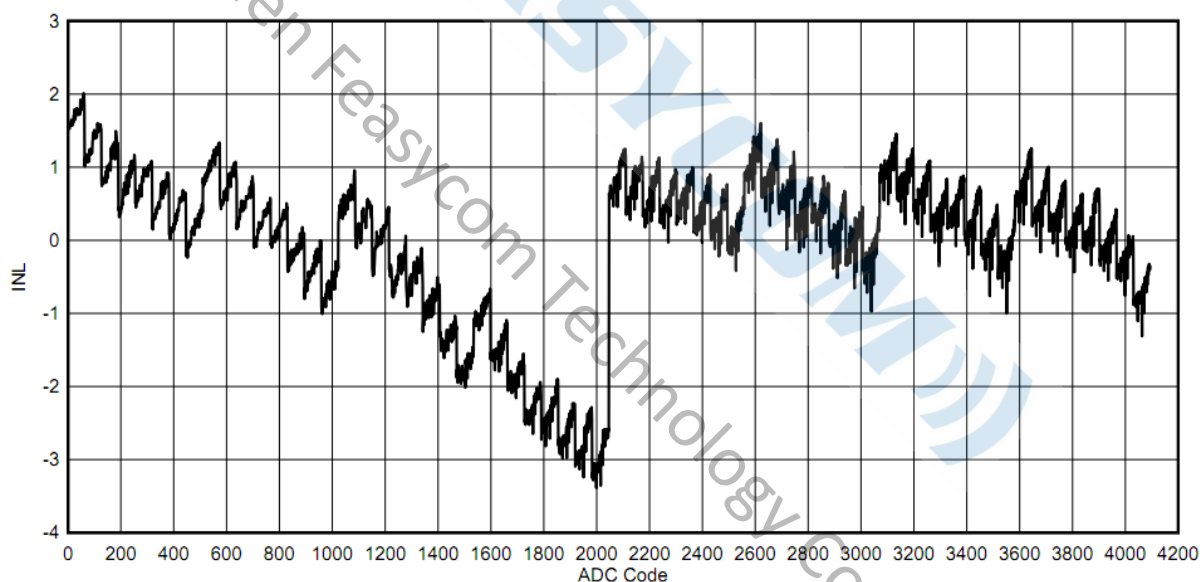


Figure 6: SoC ADC INL vs ADC Code (Internal Reference)

## 5.5 Temperature Sensor

Table 8: Temperature Sensor (reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$ , unless otherwise noted)

Parameter	Min	Type	Max	Unit
Resolution	-	4	-	$^\circ\text{C}$
Range	-40	-	+105	$^\circ\text{C}$
Accuracy	-	$\pm 5$	-	$^\circ\text{C}$

Supply voltage coefficient <sup>(1)</sup>	-	3.2	-	°C / V
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(1) Automatically compensated when using supplied driver libraries.

## 5.6 Battery Monitor

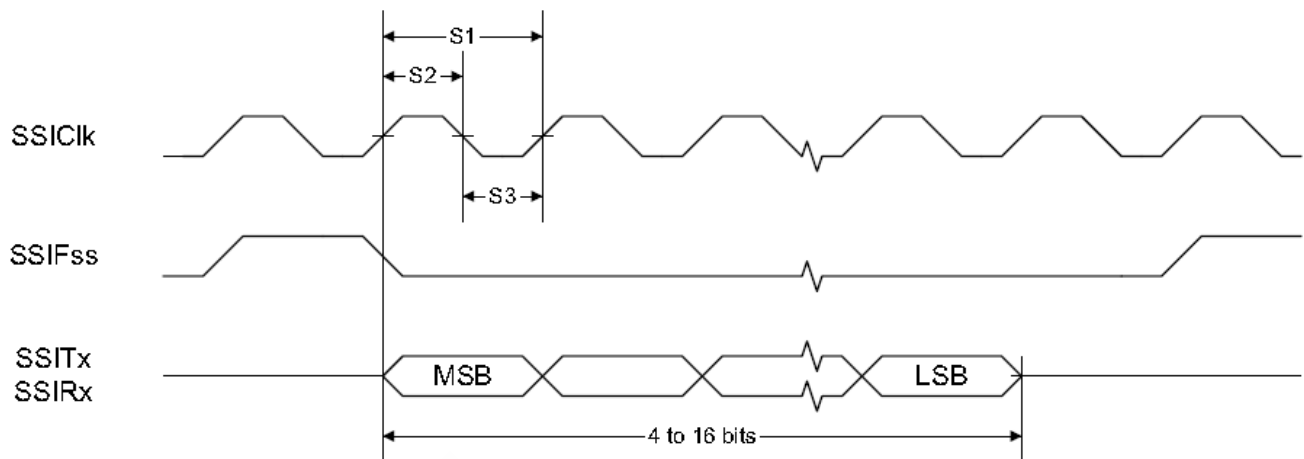
**Table 9:** Battery Monitor (reference design with Tc = 25°C, VDD = 3.0 V, unless otherwise noted)

Parameter	Min	Type	Max	Unit
Resolution	-	50	-	mV
Range	1.8	-	3.8	V
Accuracy	-	13	-	mV

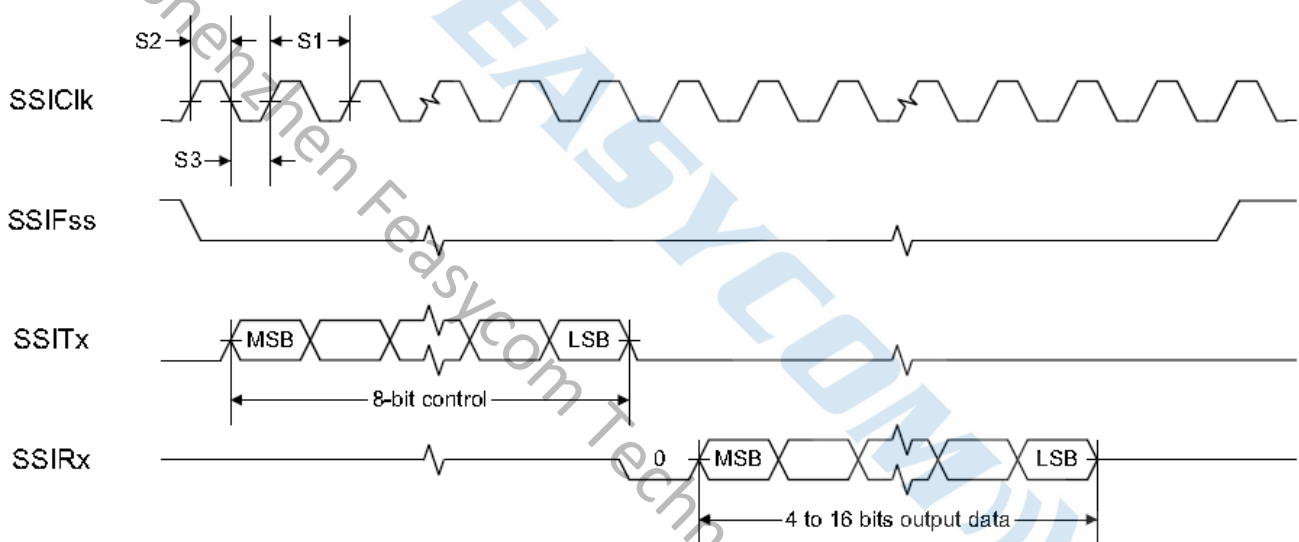
## 5.7 Synchronous Serial Interface (SSI)

**Table 10:** Synchronous Serial Interface (SSI) (Tc = 25°C, VDD = 3.0 V, unless otherwise noted.)

Parameter	Min	Type	Max	Unit
S1 t <sub>clk_per</sub> (SSIClk period) - Device operating as SLAVE	12	-	65024	System clocks
S2 t <sub>clk_high</sub> (SSIClk high time) - Device operating as SLAVE	-	0.5	-	t <sub>clk_per</sub>
S3 t <sub>clk_low</sub> (SSIClk low time) - Device operating as SLAVE	-	0.5	-	t <sub>clk_per</sub>
S1 (TX only) t <sub>clk_per</sub> (SSIClk period) - One-way communication to SLAVE Device operating as MASTER	4	-	65024	System clocks
S1 (TX and RX) t <sub>clk_per</sub> (SSIClk period) - Normal duplex operation Device operating as MASTER	8	-	65024	System clocks
S2 t <sub>clk_high</sub> (SSIClk high time) - Device operating as MASTER	-	0.5	-	t <sub>clk_per</sub>
S3 t <sub>clk_low</sub> (SSIClk low time) - Device operating as MASTER	-	0.5	-	t <sub>clk_per</sub>



**Figure 7:** SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement



**Figure 8:** SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

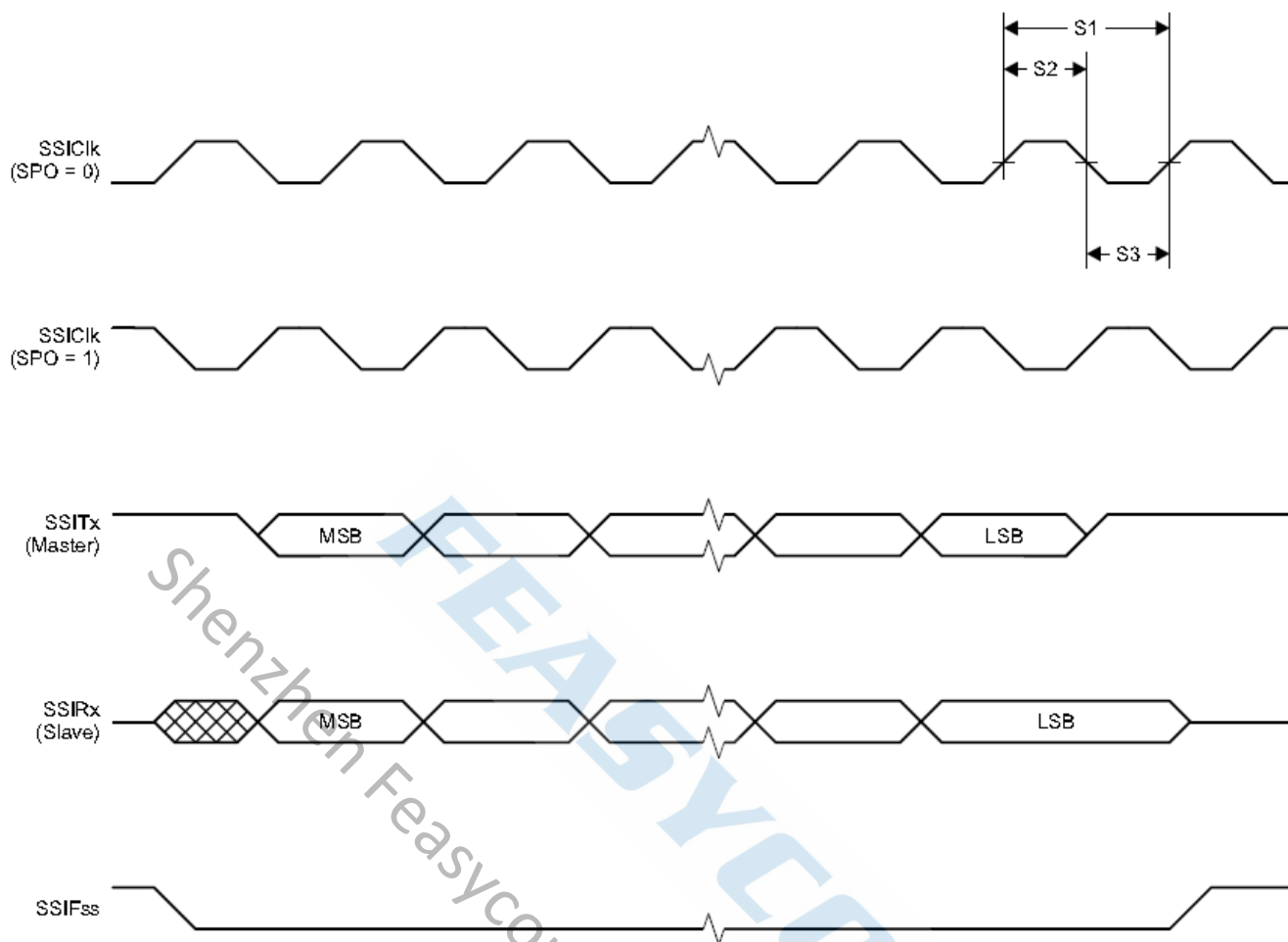


Figure 9: SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

## 5.8 Switching Characteristics

Table 11: Switching Characteristics

Parameter	Min	Typ	Max	Unit
<b>WAKEUP AND TIMING</b>				
Idle → Active	-	14	-	uS
Standby → Active	-	151	-	uS
Shutdown → Active	-	1015	-	uS

## 5.9 Power consumptions

**Table 12:** Power consumptions

Parameter	Test Conditions	Type	Unit
Discoverable	24MHz Off , 32.768KHz On	~42	uA
	Advert interval 500mS , Uart Off		
	24MHz Off , 32.768KHz On	~1.18	mA
	Advert interval 500mS , Uart On		
LE Connection	Connection Interval 18mS	~49	uA
	24MHz Off , 32.768KHz On		
	Uart Off	1.47	mA
	Connection Interval 18mS		
	24MHz On , 32.768KHz On		
	Uart On		

## 6. MSL & ESD

**Table 13:** MSL and ESD

Parameter	Test Conditions	Value
MSL grade:	MSL 3 <sup>(1)</sup>	
ESD grade:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001 <sup>(2)</sup>	All pins ±2000V
	Charged device model (CDM), per JESD22-C101 <sup>(3)</sup>	XOCS ±250V
		All other pins ±500V

(1)The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the Picture below and follow instructions specified by IPC/JEDEC J-STD-033.

**Note:** The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the Picture below, the modules must be removed from the shipping tray.

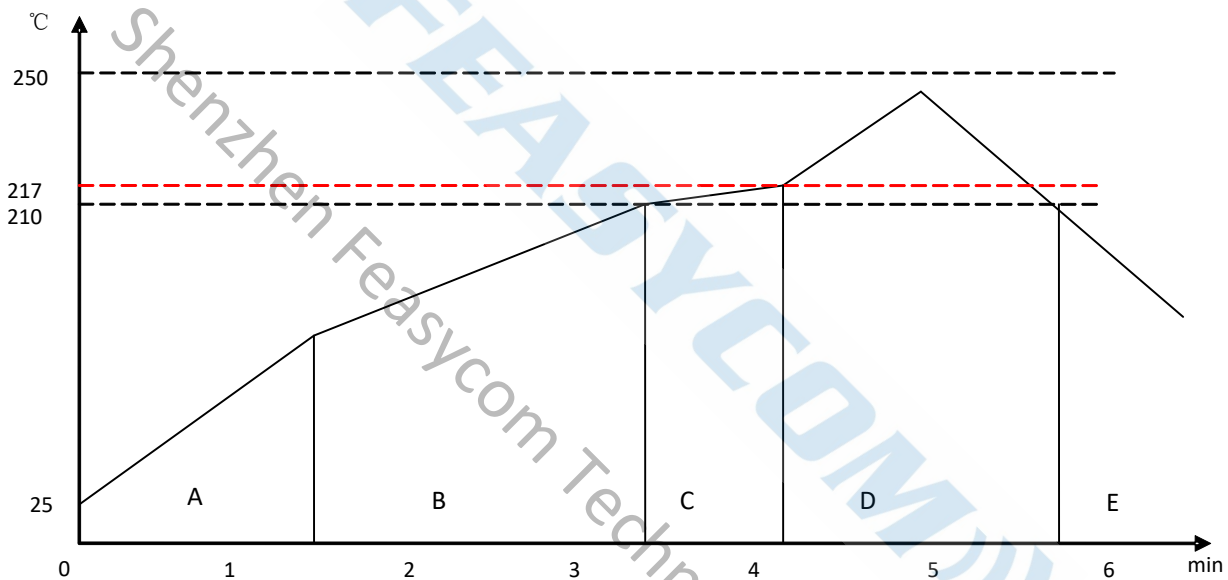
Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

**Table 14:** Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @	Floor Life Limit	Saturated @	Floor Life Limit	Saturated @	Floor Life Limit
	30°C/85%	+ 72 hours @ 30°C/60%	30°C/85%	+ 72 hours @ 30°C/60%	30°C/85%	+ 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

**Figure 10:** Typical Lead-free Re-flow

**Pre-heat zone (A)** — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

**Equilibrium Zone 1 (B)** — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

**Equilibrium Zone 2 (C) (optional)** — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

**Reflow Zone (D)** — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature ( $T_p$ ) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

**Cooling Zone (E)** — The cooling rate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

## 8. MECHANICAL DETAILS

### 8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0 mm(H) Tolerance:  $\pm 0.1\text{mm}$
- Module size: 13mm X 26.9mm Tolerance:  $\pm 0.2\text{mm}$
- Pad size: 1mmX0.8mm Tolerance:  $\pm 0.1\text{mm}$
- Pad pitch: 1.5mm Tolerance:  $\pm 0.1\text{mm}$

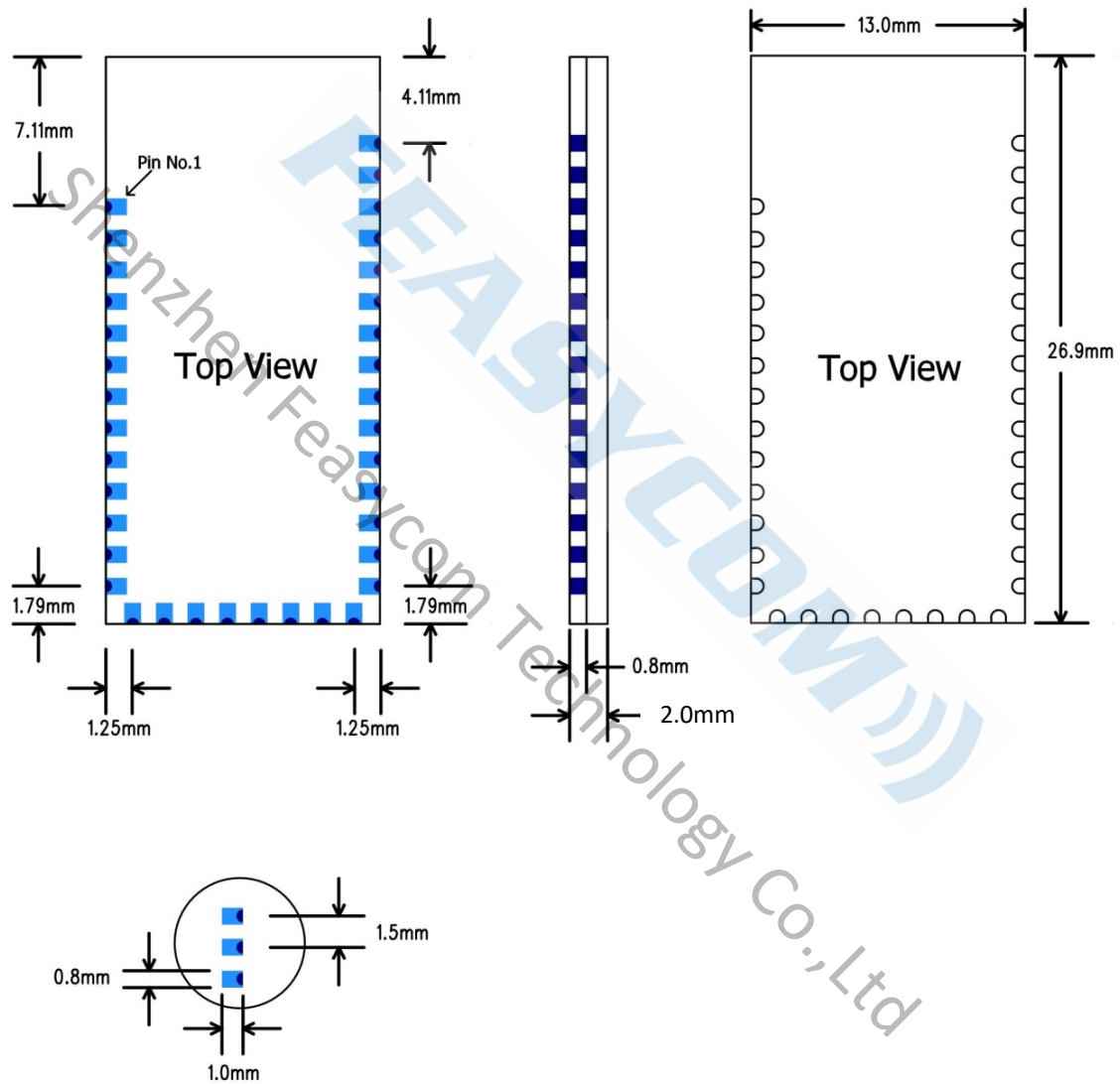


Figure 11: FSC-BT616V footprint

## 8.2 Host PCB Land Pattern and Antenna Keep-out for FSC-BT616V

Please check the picture below for Pad Structure and Keep Out Area:

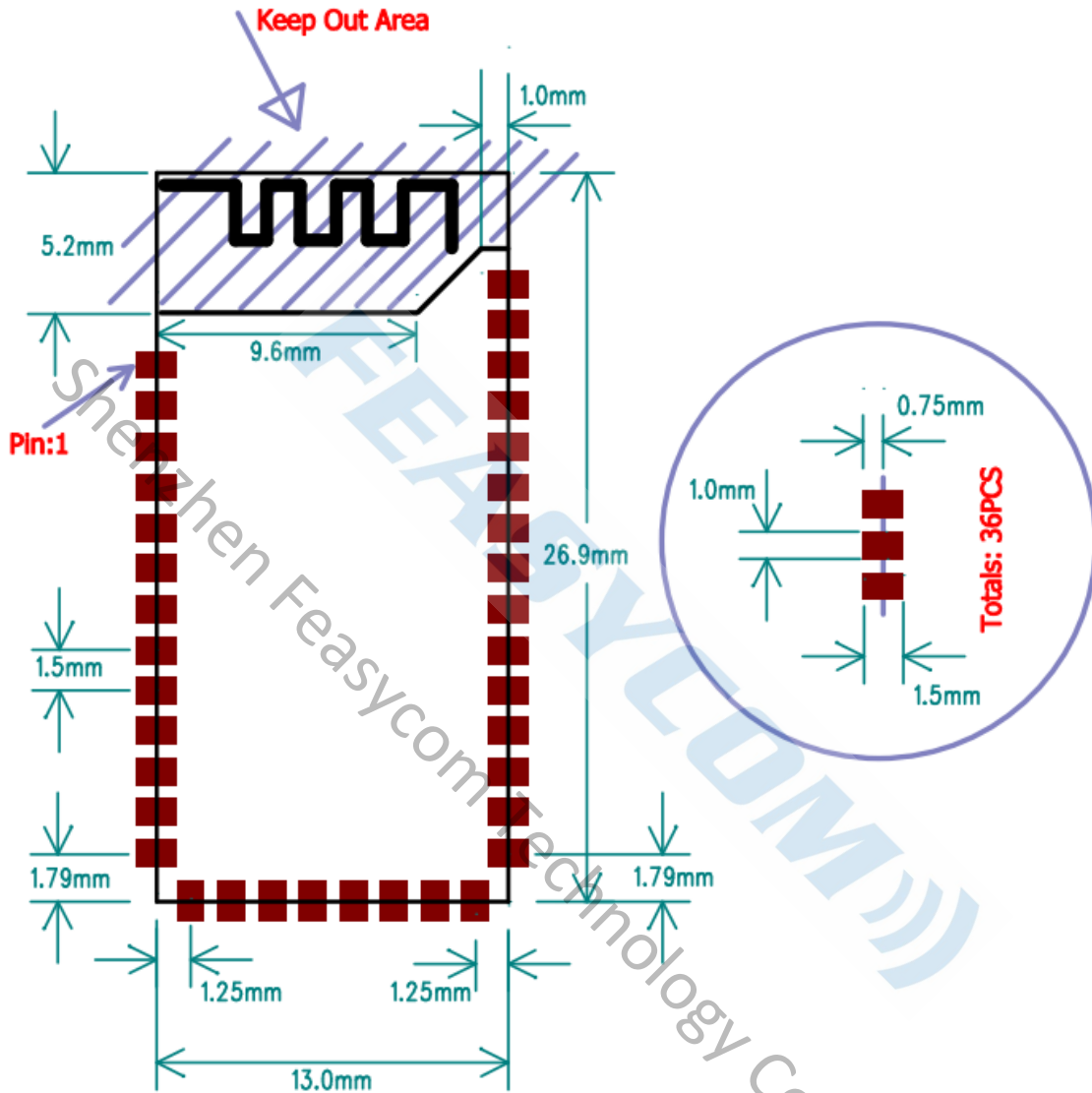


Figure 12: Host PCB-Top View

## 9. HARDWARE INTEGRATION SUGGESTIONS

### 9.1 Soldering Recommendations

FSC-BT616V is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

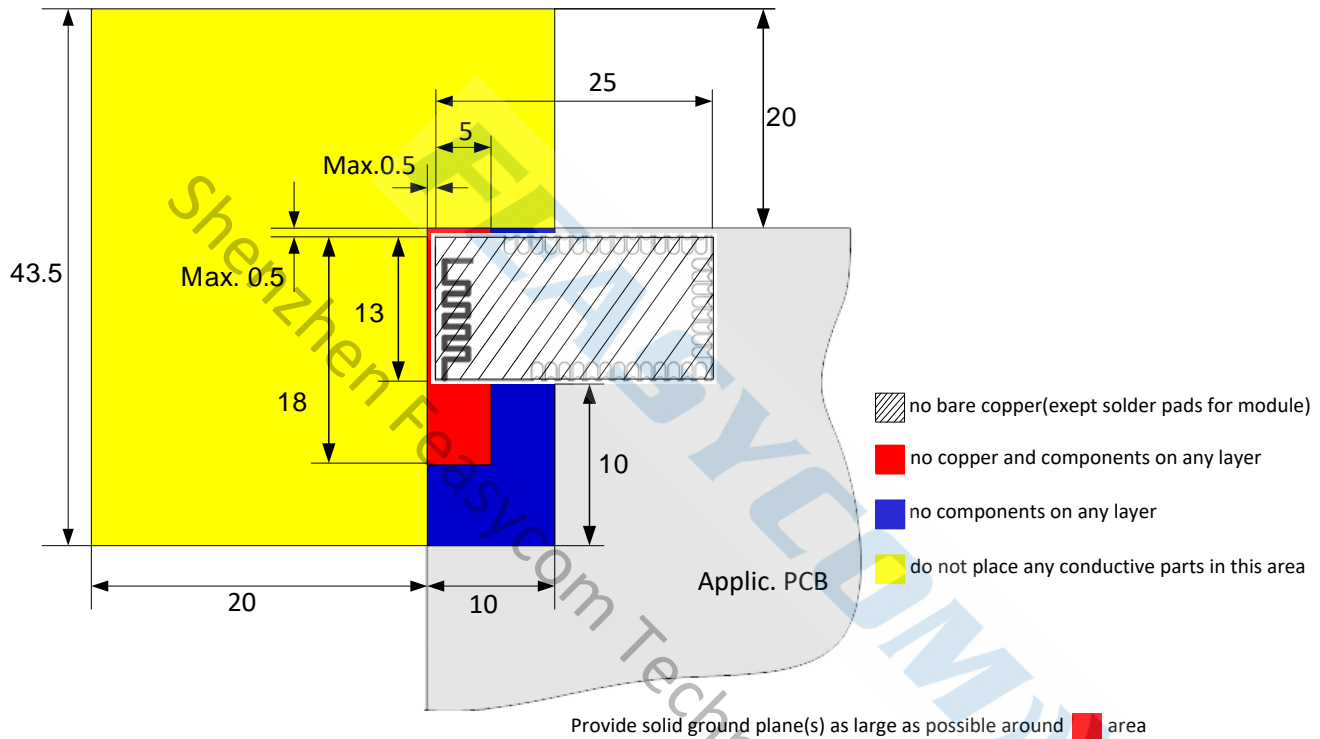
Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.



## 9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.



**Figure 13:** FSC-BT616V Restricted Area (Unit: mm)

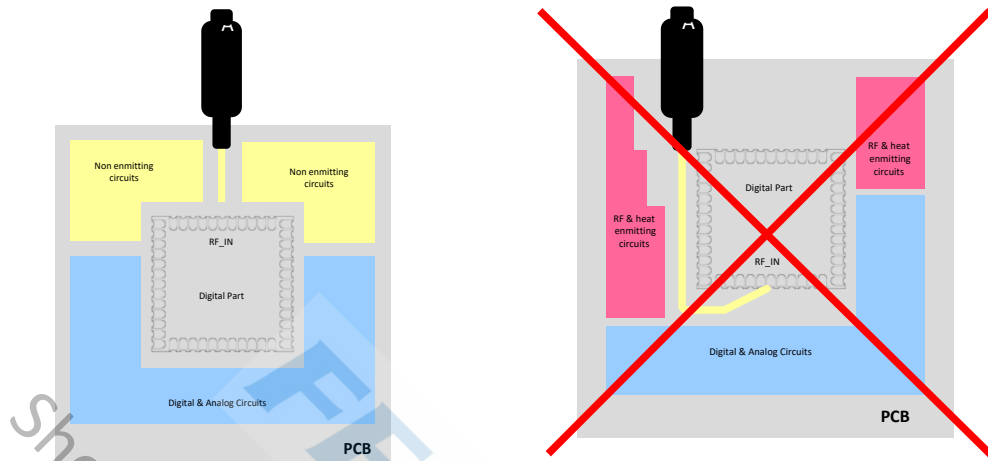
Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

## 9.3 Layout Guidelines(External Antenna)

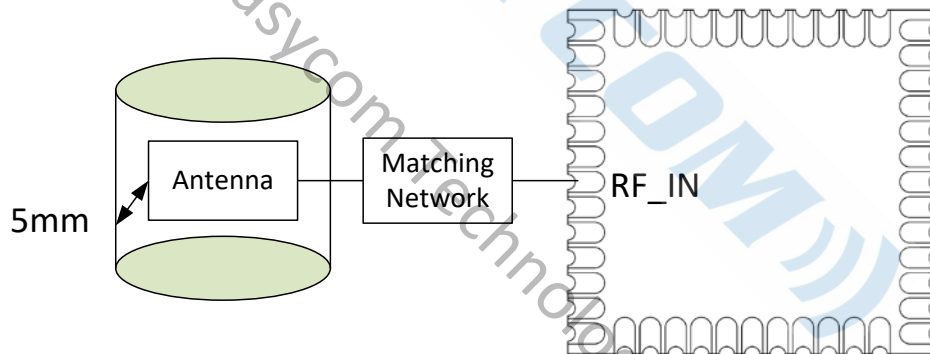
Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be  $50\Omega$  and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in picture below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.



**Figure 14:** Placement the Module on a System Board

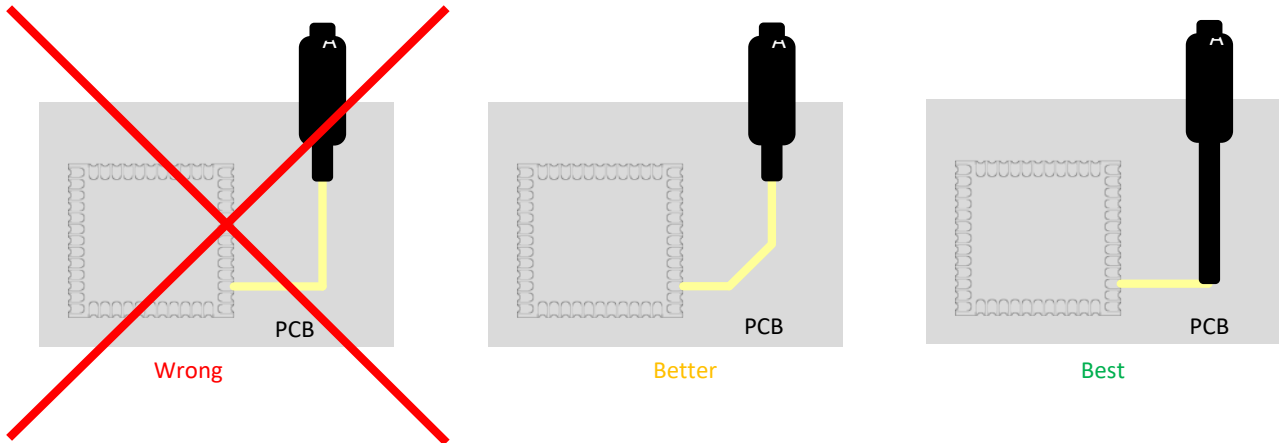
### 9.3.1 Antenna Connection and Grounding Plane Design



**Figure 15:** Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.



**Figure 16:** Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

## 10. PRODUCT PACKAGING INFORMATION

### 10.1 Default Packing

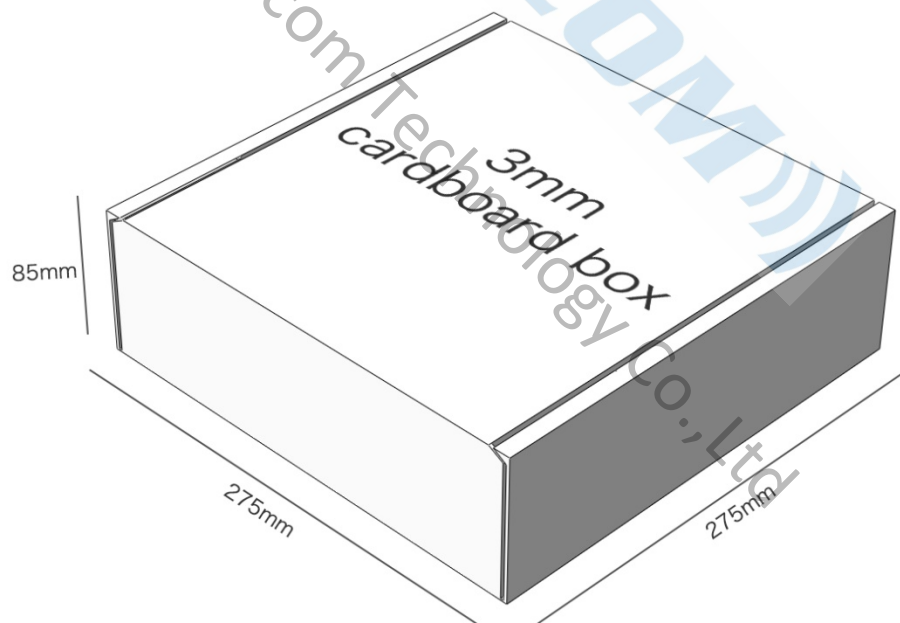
- Tray vacuum
- Tray Dimension: 180mm \* 195mm





Figure 17: Tray vacuum

## 10.2 Packing box(Optional)



\* If require any other packing, must be confirmed with customer

\* Package: 1000PCS Per Carton (Min Carton Package)

Figure 18: Packing Box

## 11. APPLICATION SCHEMATIC

