High Performance SPDT Analog Switch with Over-Voltage Tolerance

FSA3051

X2DFN6 1x1, 0.35P
(TMLP)
CASE 716AA

Description

The FSA3051 is a 6 Ω, bi-directional, low-power, two port, high-speed, Single Pole / Double Throw (SPDT) analog switch. It features an extremely low on capacitance (C_{ON}) of 7.7 pF and wide bandwidth of 1.0 GHz.

The FSA3051 contains special circuitry on the switch I/O pins for applications where the V_{CC} supply is powered-off (V_{CC} = 0 V), which allows the device to withstand an over-voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the select (S) pin is lower than the supply voltage (V_{CC}). This feature is especially valuable to ultra-portable applications, such as cell phones, allowing for direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

Features

- Low On Capacitance: 7.7 pF Typical
- Low On Resistance: 6 Ω Typical
- Low Power Consumption: 1 μA Maximum
  - 15 μA Maximum I_{CCT} over an Expanded Voltage Range (V_{IN} = 1.8 V, V_{CC} = 5.5 V)
- Wide −3 db Bandwidth: 1.0 GHz
- Packaged in Ultra Small 6-Lead TMLP
- Broad V_{CC} Operating Range: 1.6 V to 5.5 V
- Over-Voltage Tolerance (OVT) on all Data Ports up to 6 V without External Components

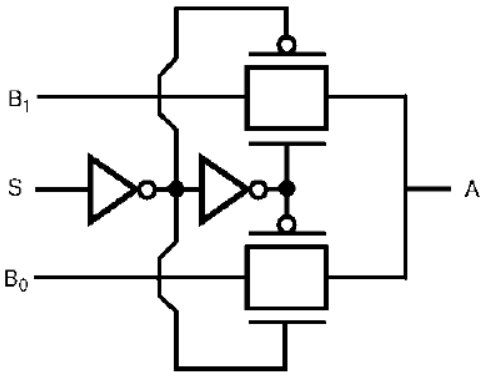
Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

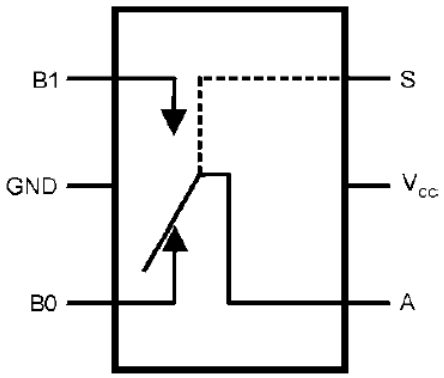
MARKING DIAGRAM

NT = Specific Device Code
&K = 2-Digits Lot Run Traceability Code
&2 = 3-Digit Plant Code
&Z = Assembly Plant Code

ANALOG SYMBOLS



Logic Symbol



Analog Symbol

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

PIN ASSIGNMENTS

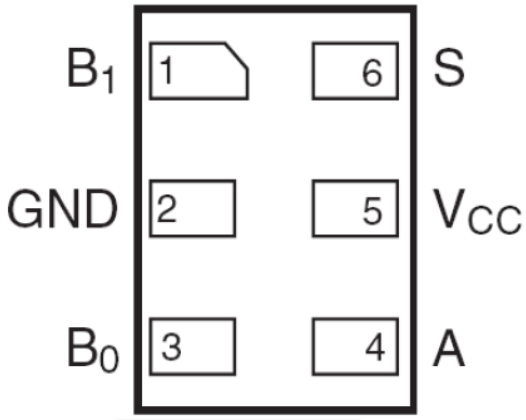


Figure 1. 6-Lead TMLP (Top-Through View)

PIN DEFINITIONS

UMLP Pin#	Name	Description
1	B_1	Data Port
2	GND	Ground
3	B_0	Data Port
4	A	Data Port
5	V_{CC}	Supply Voltage
6	S	Switch Select

TRUTH TABLE

S	Function
LOW	B_0 connected to A
HIGH	B_1 connected to A

1. LOW ≤ V_{IL}
2. HIGH ≥ V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.0	V
V_{CNTRL}	DC Input Voltage (Note 3)		−0.5	VCC	V
V_{SW}	DC Switch I/O Voltage (Note 3)		−0.50	6.00	V
I_{IK}	DC Input Diode Current		−50	−	mA
I_{OUT}	DC Output Current		−	50	mA
T_{STG}	Storage Temperature		−65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)		−	1	Level
ESD	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	2	−	kV
		I/O to GND	2	−	
		Power to GND	2	−	
	Charged Device Model, JEDEC: JESD22-C101		1	−	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	1.6	5.5	V
V_{CNTRL}	Control Input Voltage (S) (Note 4)	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	−0.5	5.5	V
T_A	Operating Temperature	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. The control input must be held HIGH or LOW and it must not float.

DC CHARACTERISTICS (All typical value are at T_A = 25 °C unless otherwise specified.)

Symbol	Characteristic	Condition	V_{CC} (V)	T_A = −40°C to 85°C			Unit
				Min	Typ	Max	
V_{IK}	Clamp Diode Voltage	I_{IN} = −18 mA	3.0	−	−	−1.2	V
V_{IH}	Input Voltage High		1.8 to 4.3	1.3	−	−	V
			4.3 to 5.5	1.7	−	−	
V_{IL}	Input Voltage Low		1.8 to 4.3	−	−	0.5	V
			4.3 to 5.5	−	−	0.7	
I_{IN}	Control Input Leakage	V_{CNTRL} = 0 to V_{CC}	1.8	−1	−	1	μA
			5.5	−1	−	1	
I_{OZ}	Off State Leakage	V_{SW} = 0 V to V_{CC}	1.8	−2	−	2	μA
		V_{SW} = 0 V to 3.6 V	5.5	−2	−	2	
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW} = 0 V to 4.3 V, V_{CC} = 0 V, Figure 3	0	−2	−	2	μA
R_{ON}	Switch On Resistance (Note 5)	V_{SW} = 0.4 V, I_{ON} = −8 mA, Figure 2	3.0	−	4	10	Ω
		V_{SW} = 1.8 V, I_{ON} = −8 mA, Figure 2	3.0	−	6	10	
R_{ON}	Switch On Resistance (Note 5)	V_{SW} = 0.4 V, I_{ON} = −8 mA, Figure 2	1.8	−	6	10	Ω
		V_{SW} = 1.8 V, I_{ON} = −8 mA, Figure 2	1.8	−	14	25	
ΔR_{ON}	On Resistance Match Between Channels (Note 5, 6)	V_{SW} = 0.4 V, I_{ON} = −8 mA	3.0	−	35	−	mΩ
			1.8	−	40	−	
I_{CC}	Quiescent Supply Current	V_{CNTRL} = 0 or V_{CC}, I_{OUT} = 0	5.5	−	−	1	μA
I_{CCT}	Increase in I_{CC} Current per Control Voltage and V_{CC}	V_{CNTRL} = 1.8 V	3.0	−	−	10	μA
		V_{CNTRL} = 2.6 V	5.5	−	−	10	
		V_{CNTRL} = 1.8 V	5.5	−	−	15	

5. Measured by the voltage drop between A and Bn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or Bn ports).
6. $\Delta R_{ON} = R_{ON}$ maximum − R_{ON} minimum measured at identical V_{CC}, temperature, and voltage levels.
7. Guaranteed by characterization.

AC CHARACTERISTICS (Note 8) (All typical value are at T_A = 25 °C unless otherwise specified.)

Symbol	Characteristic	Condition	V_{CC} (V)	T_A = −40°C to 85°C			Unit
				Min	Typ	Max	
t_{ON}	Turn-On Time S to Output	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 0.8 V, Figure 4, Figure 5	3.0 to 3.6	−	34	−	ns
			1.8	−	110	−	
t_{OFF}	Turn-Off Time S to Output	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 0.8 V, Figure 4, Figure 5	3.0 to 3.6	−	23	−	ns
			1.8	−	50	−	
t_{PD}	Propagation Delay	C_L = 5 pF, R_L = 50 Ω, Figure 6, Figure 6	3.3	−	0.2	−	ns
			1.8	−	0.3	−	
t_{BBM}	Break-Before-Make	R_L = 50 Ω, C_L = 5 pF, V_{SW1} = V_{SW2} = 0.8 V, Figure 7	3.0 to 3.6	15	−	50	ns
			1.8	−	−	100	
O_{IRR}	Off Isolation	R_L = 50 Ω, f = 240 MHz, Figure 9	1.8	−	−20	−	dB
			3.0 to 3.6	−	−23	−	
Xtalk	Crosstalk	R_L = 50 Ω, f = 240 MHz, Figure 10	1.8	−	−18	−	dB
			3.0 to 3.6	−	−23	−	dB
BW	−3 db Bandwidth	R_L = 50 Ω, C_L = 0 pF, V_{SW} = 0.4 V	1.8	−	810	−	MHz
		R_L = 50 Ω, C_L = 0 pF, Figure 8	3.0 to 3.6	−	1	−	GHz
		R_L = 50 Ω, C_L = 5 pF, Figure 8		−	750	−	MHz

8. Guaranteed by characterization. Not production tested.

CAPACITANCE (Note 9)

Symbol	Characteristic	Condition	V_{CC} (V)	T_A = −40°C to 85°C			Unit
				Min	Typ	Max	
C_{IN}	Control Pin Input Capacitance		0	−	1.5	−	pF
C_{ON}	A Port On Capacitance	f = 1 MHz,	3.0	−	7.7	−	
		f = 240 MHz, Figure 12	3.3	−	7.7	−	
		f = 1 MHz,	1.8	−	10.0	−	
		f = 240 MHz, Figure 12	1.8	−	5.0	−	
C_{OFF}	Bn Port Off Capacitance	f = 1 MHz	3.0	−	3.3	−	
		f = 240 MHz, Figure 11	3.3	−	3.3	−	
		f = 1 MHz	1.8	−	5.0	−	
		f = 240 MHz, Figure 11	1.8	−	4.0	−	

9. Not production tested.

TEST DIAGRAMS

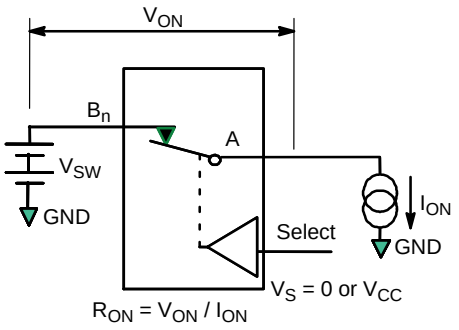
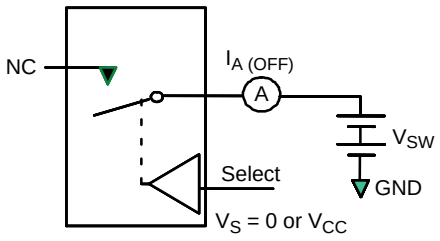
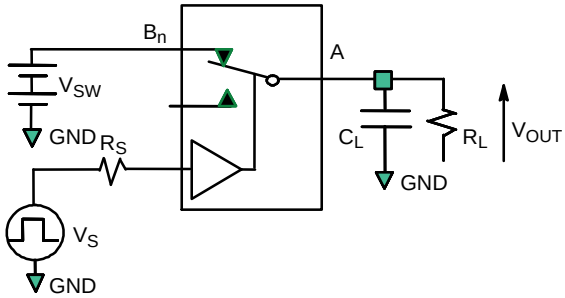


Figure 2. On Resistance



**Each switch port is tested separately

Figure 3. Off Leakage



R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 4. AC Test Circuit Load

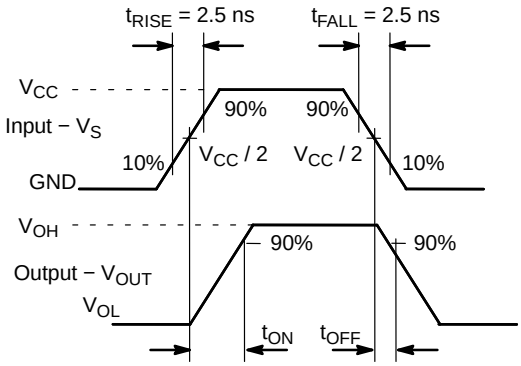


Figure 5. Turn-On / Turn-Off Waveforms

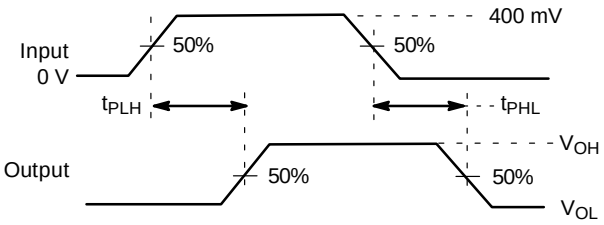
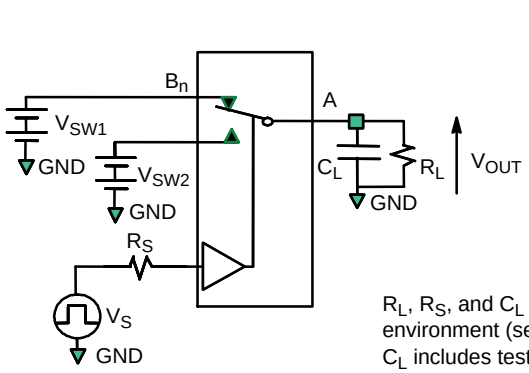
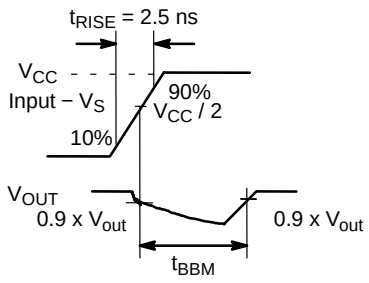


Figure 6. Propagation Delay ($t_R t_F$ – 500 ps)





R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 7. Break-Before-Make Interval Timing

TEST DIAGRAMS (CONTINUED)

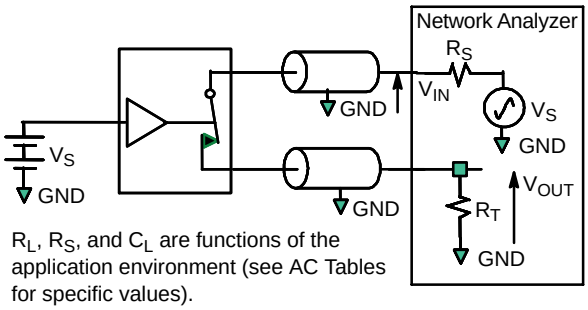


Figure 8. Bandwidth

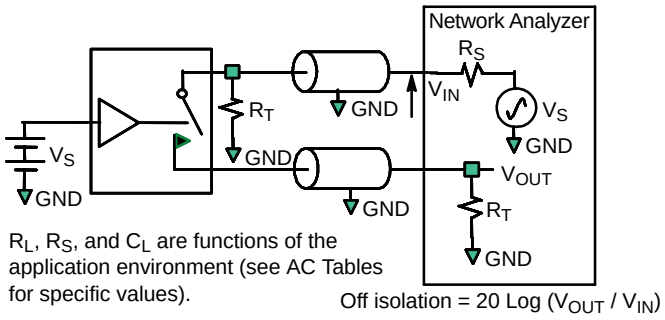


Figure 9. Channel Off Isolation

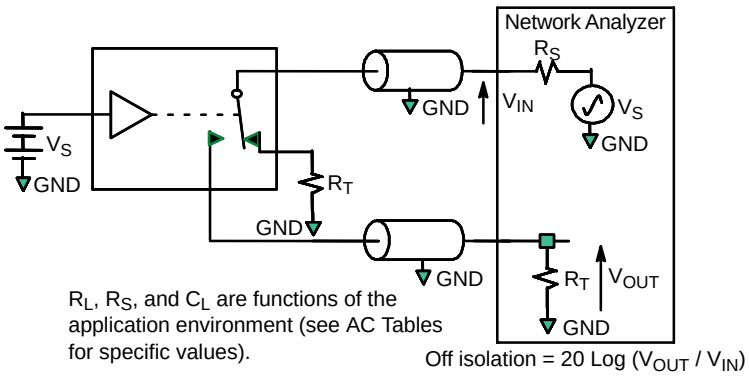


Figure 10. Channel-to-Channel Crosstalk

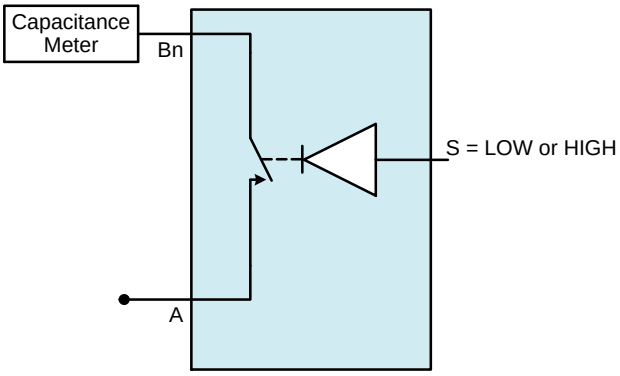


Figure 11. Channel Off Capacitance

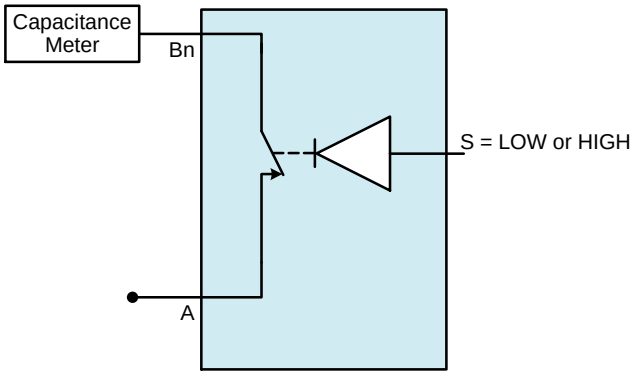


Figure 12. Channel On Capacitance

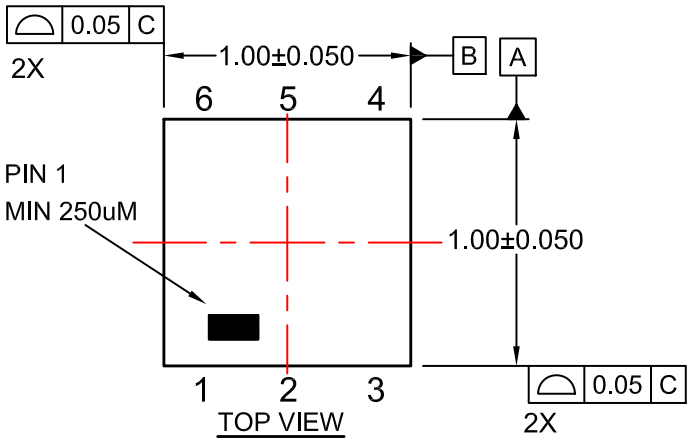
ORDERING INFORMATION

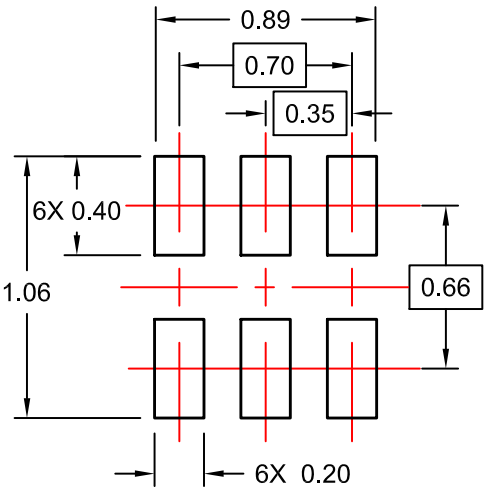
Part Number	Top Mark	Operating Temperature Range	Package Type	Shipping†
FSA3051TMX	NT	−40 to +85 °C	X2DFN6 1x1, 0.35P 6-Lead, Dual, Ultra-ultrathin Molded Leadless Package (TMLP), 1.0 x 1.0 mm. Top left unit orientation in carrier tape (Pb-Free, Halide Free)	10000 / Tape & Reel

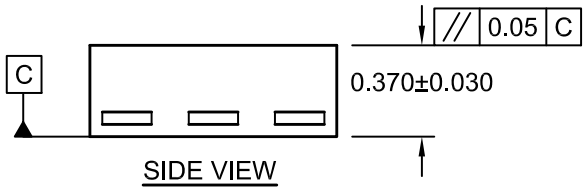
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

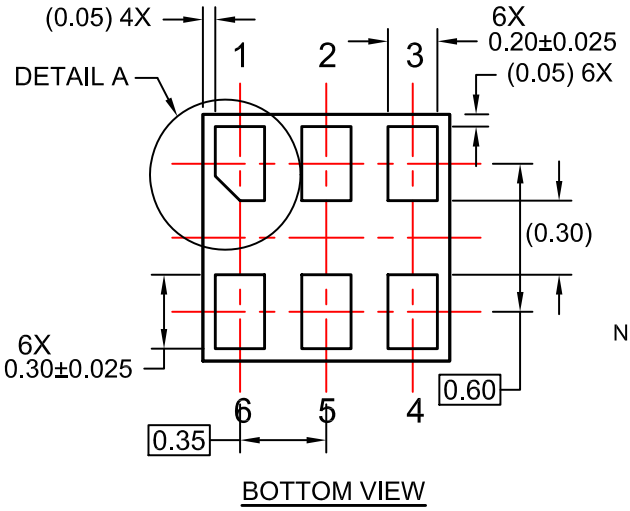
X2DFN6 1x1, 0.35P
CASE 716AA
ISSUE O

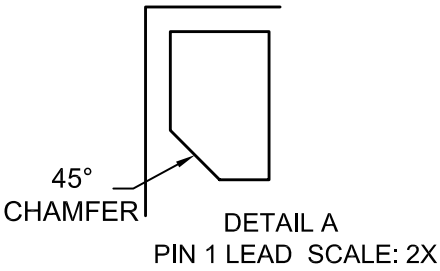
DATE 30 NOV 2016



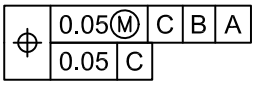








NOTES:
A. NO JEDEC STANDARD APPLIES
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009



DOCUMENT NUMBER:	**98AON13695G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**X2DFN6 1x1, 0.35P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales