AMERICAN MICROSYSTEMS, INC.

FS6261-01

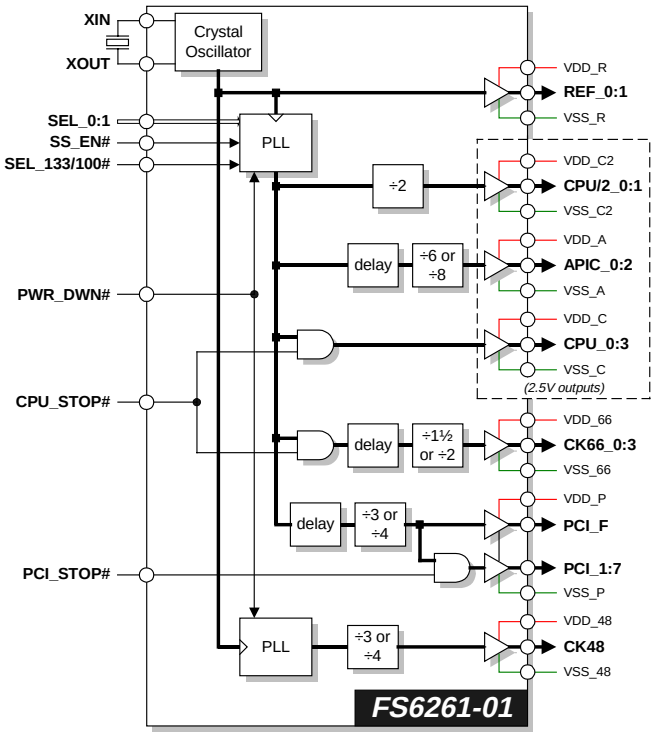
Motherboard Clock Generator IC

January 2000

1.0 Features

- Generates clocks required for Intel® i820 based desktop and workstation systems, including:
  - Four enabled 2.5V 133/100MHz CPU Front Side Bus (FSB) clocks
  - Two 2.5V CPU/2 clocks for synchronous memory
  - Seven enabled 3.3V PCI bus clocks and one free-running PCI clock
  - Four enabled 3.3V 66MHz AGP clocks
  - Three 2.5V 16.67MHz APIC bus clocks
  - Two 3.3V 14.318MHz REF clocks
  - One 3.3V 48MHz USB clock
- CPU clock cycle – cycle jitter < 150ps p-p
- Non-linear spread-spectrum modulation (-0.5% at 31.5kHz)
- Supports test mode and tristate output control
- Separate CPU-enable, PCI-enable and power-down inputs with glitch-free stop clock controls on all clocks for clock control and power management

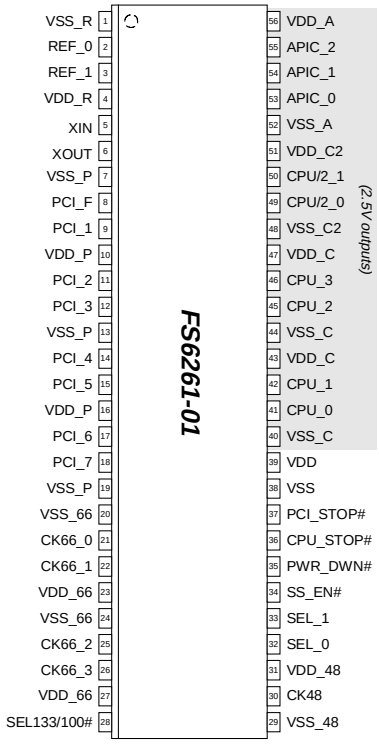
Figure 1: Block Diagram



2.0 Description

The FS6261-01 is a CMOS clock generator IC designed for high-speed motherboard applications. Two different frequencies can be selected for the CPU clocks via two SEL pins. Glitch-free stop clock control of the CPU, AGP (66MHz) and PCI clocks is provided. A low current power-down mode is available for mobile applications. Separate clock buffers provide for a 2.5V voltage range on the CPU_0:3, CPU/2_0:1 and APIC_0:2 clocks.

Figure 2: Pin Configuration



56-pin SSOP

Table 1: CPU/PCI Frequency Selection

SEL_133/100#	SEL_1	SEL_0	CPU (MHz)	PCI (MHz)
0	0	0	tristate	tristate
0	0	1	(reserved)	(reserved)
0	1	0	100	33.33
0	1	1	100	33.33
1	0	0	XIN/2	XIN/6
1	0	1	(reserved)	(reserved)
1	1	0	133	33.33
1	1	1	133	33.33

Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active-low pin

PIN	TYPE	NAME	DESCRIPTION
53, 54, 55	DO	APIC_0:2	Three low-skew (<250ps @ 1.25V) 2.5V 16.67MHz clock outputs for APIC bus timing. APIC clocks are synchronous with CPU clocks but lag the CPU clocks by 1.5 to 4ns.
30	DO	CK48	One 3.3V 48MHz clock output for Universal Serial Bus (USB) timing
21, 22, 25, 26	DO	CK66_0:3	Four 3.3V 66MHz AGP clock outputs. CK66 clocks are synchronous with CPU clocks but lag the CPU clocks by 0 to 1.5ns.
41, 42, 45, 46	DO	CPU_0:3	Four low-skew 2.5V 133/100MHz CPU clock outputs for host frequencies
49, 50	DO	CPU/2_0:1	Two low-skew 2.5V clock outputs at half the CPU clock frequencies (66/50MHz)
36	DI^U	CPU_STOP#	CPU_0:3 and CK66_0:3 clock output enable. Asynchronous, active-low disable stops all CPU and CK66 clocks in the low state.
9, 11, 12, 14, 15, 17, 18	DO	PCI_1:7	Seven 3.3V PCI clock outputs. PCI clocks are synchronous with CPU clocks but lag the CK66 clocks by 1.5 to 4ns.
8	DO	PCI_F	One free-running 3.3V PCI clock output
37	DI^U	PCI_STOP#	PCI_1:7 clock output enable. Asynchronous, active-low disable stops all PCI clocks in the low state.
35	DI^U	PWR_DWN#	Asynchronous active-low power-down signal shuts down oscillator, all PLLs, puts all clocks in low state. Clock re-enable latency of ≤ 3ms.
2, 3	DO	REF_0:1	Two buffered outputs of the 14.318MHz reference clock
32, 33	DI^U	SEL_0:1	Two frequency select inputs (see Table 4)
28	DI	SEL_133/100#	Selects 133MHz or 100MHz CPU frequency (pull-up/pull-down *must* be provided externally)
34	DI^U	SS_EN#	Spread spectrum enable. Active-low enable turns on the spread spectrum feature; a logic-high turns off the spread spectrum modulation.
39	P	VDD	3.3V ± 10%
31	P	VDD_48	Power supply for 3.3V CK48 clock output
23, 27	P	VDD_66	Power supply for 3.3V CK66_0:3 clock outputs
56	P	VDD_A	Power supply for 2.5V APIC_0:2 clock outputs
43, 47	P	VDD_C	Power supply for 2.5V CPU_0:3 clock outputs
51	P	VDD_C2	Power supply for 2.5V CPU/2_0:1 clock outputs
10, 16	P	VDD_P	Power supply for 3.3V PCI_1:7 and PCI_F clock outputs
4	P	VDD_R	Power supply for 3.3V REF_0:1 clock outputs
38	P	VSS	Ground
29	P	VSS_48	Ground for CK48 clock outputs
20, 24	P	VSS_66	Ground for CK66_0:3 clock outputs
52	P	VSS_A	Ground for APIC_0:2 clock outputs
40, 44	P	VSS_C	Ground for CPU_0:3 clock outputs
48	P	VSS_C2	Ground for CPU/2_0:1 clock outputs
7, 13, 19	P	VSS_P	Ground for PCI_1:7 and PCI_F clock outputs
1	P	VSS_R	Ground for REF_0:1 clock outputs
5	AI	XIN	14.318MHz crystal oscillator input. XIN can be driven by an external frequency source.
6	AO	XOUT	14.318MHz crystal oscillator output

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Table 3: Actual Clock Frequencies

Note: Spread spectrum disabled

CLOCK	TARGET (MHz)	ACTUAL (MHz)	DEVIATION (ppm)
APIC_0:2	16.67 (with CPU = 133.3)	16.6634	-195.92
	16.67 (with CPU = 100.0)	16.6661	-36.657
CPU_0:3	133.33	133.3072	-195.92
	100.00	99.9963	-36.657
CPU/2_0:1	66.67	66.6536	-195.92
	50.00	49.9982	-36.657
PCI_1:7, PCI_F	33.33 (with CPU = 133.3)	33.3268	-195.92
	33.33 (with CPU = 100.0)	33.3321	-36.657
CK66_0:3	66.67 (with CPU = 133.3)	66.6536	-195.92
	66.67 (with CPU = 100.0)	66.6642	-36.657
CK48 (1)	48	48.0080	+167

(1) 48MHz USB clock is required to be 167ppm off from 48.000MHz to conform to USB requirements.

3.0 Programming Information

Table 4: Function/Clock Enable Configuration

CONTROL INPUTS						CLOCK OUTPUTS (MHz)							
SEL_ 133/100#	SEL_1	SEL_0	PWR_ DWN#	CPU_ STOP#	PCI_ STOP#	REF_0:1	CPU_0:3	CPU/2_ 0:1	PCI_F	PCI_1:7	APIC_ 0:2	CK48	CK66_ 0:3
0	0	0	1	X	X	tristate	tristate	tristate	tristate	tristate	tristate	tristate	tristate
0	0	1	1	1	1	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)
0	1	0	1	1	1	14.318	100	50	33.33	33.33	16.67	tristate	66.67
0	1	1	1	1	1	14.318	100	50	33.33	33.33	16.67	48	66.67
1	0	0	1	1	1	XIN	XIN÷2	XIN÷4	XIN÷8	XIN÷8	XIN÷16	XIN÷2	XIN÷4
1	0	1	1	1	1	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)
1	1	0	1	1	1	14.318	133.33	66.67	33.33	33.33	16.67	tristate	66.67
1	1	1	1	1	1	14.318	133.33	66.67	33.33	33.33	16.67	48	66.67
X	X	X	0	X	X	low	low	low	low	low	low	low	low
SEL_0:1 and SEL_133/100# ≠ 0 or SEL_0:1 ≠ 01			1	0	0	14.318	low	running	33.33	low	16.67	48	low
			1	0	1	14.318	low	running	33.33	33.33	16.67	48	low
			1	1	0	14.318	running	running	33.33	low	16.67	48	66.67
			1	1	1	14.318	running	running	33.33	33.33	16.67	48	66.67

3.1 SEL_1, SEL_0

These two input pins can either tristate the output drivers, select the Test Mode frequency, or choose the CPU frequencies. Both the SEL_1 and SEL_0 pins have pull-ups that default the CPU output frequency to either 100MHz or 133MHz, depending on the state of the SEL_133/100# pin. These pins should be fixed at a logic state before power-up occurs.

3.2 SEL_133/100#

This pin is an active-low LVTTL input that switches between a 133MHz or a 100MHz system (CPU) clock. A pull-up or pull-down must be provided externally and this pin should be fixed at a logic state before power-up occurs.

4.0 Clock Latency

All clock outputs are stopped in the low state, and are started so that the first high pulse is a full pulse width. All clocks complete a full period on transitions between running (enabled) and stopped (disabled) to ensure glitch-free stop clock control.

All enabled clocks will continue to run while disabled clocks are stopped. The clock enable signals are assumed to be asynchronous inputs relative to clock outputs. Enable signals are synchronized to their respective clocks by this device. The CPU and PCI clocks will transition between running and stopped according to Table 5.

4.1 Power-Up Latency

Power-up latency is defined as the time from the moment when PWR_DWN# goes inactive (a rising edge) to when the first valid clocks are driven from the device. Upon release of PWR_DWN#, external circuitry should allow a minimum of 3ms for the PLLs to lock before enabling any clocks.

4.1.1 PWR_DWN#

The PWR_DWN# signal is an asynchronous, active-low LVTTL input that puts the device in a low power inactive state without removing power from the device. All internal clocks are turned off, and all clock outputs are held low. Powering down occurs in less than two PCI clocks from the falling edge of PWR_DWN# to when all clock outputs are forced low. The REF and CK48 clocks are brought low as soon as possible.

4.2 Clock Enable Latency

Clock enable latency is defined in the number of rising edges of free-running PCI clocks between when the enable signal becomes active (a rising edge) to when the first valid clock is driven from the device.

4.2.1 CPU_STOP#

The CPU_STOP# pin is an active-low LVTTL input pin that disables the CPU_0:3 and CK66_0:3 clocks for low power operation. CPU_STOP# can be asserted asynchronously, and the stop clock control is glitch-free, in that the CPU clock must complete a full cycle before the clock is stopped low. One rising edge of the PCI_F clock is allowed before the CPU and CK66 clocks are enabled or disabled.

4.2.2 PCI_STOP#

The PCI_STOP# pin is an active-low LVTTL input pin that disables the PCI_1:7 clocks for low power operation, except for the PCI_F clock. The PCI_F is a free-running clock, and will continue to run even if all other PCI clocks have stopped. PCI_STOP# can be asserted asynchronously, and the stop-clock control is glitch-free, in that the PCI clock must complete a full cycle before the clock is stopped low. Only one rising edge of the PCI_F clock is allowed after the PCI_STOP# signal is enabled/disabled.

Table 5: Latency Table

SIGNAL	SIGNAL STATE		PCI CLOCK ENABLE LATENCY
CPU_STOP#	0	disabled	1
	1	enabled	1
PCI_STOP#	0	disabled	1
	1	enabled	1
PWR_DWN#	0	Power OFF	2 (max.)
	1	Power ON	3ms

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Figure 2: CPU_STOP# Timing

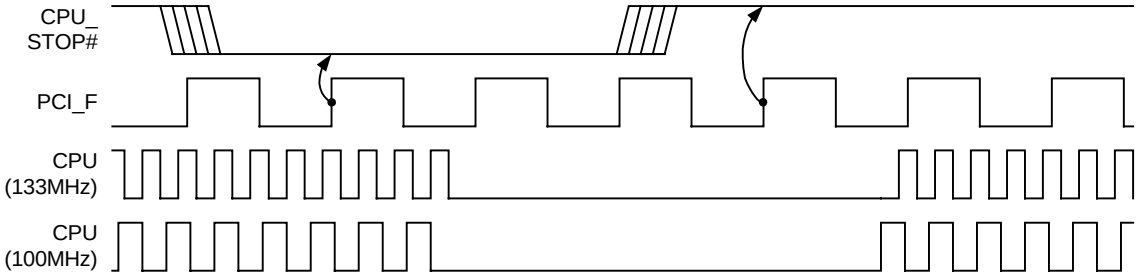


Figure 3: PCI_STOP# Timing

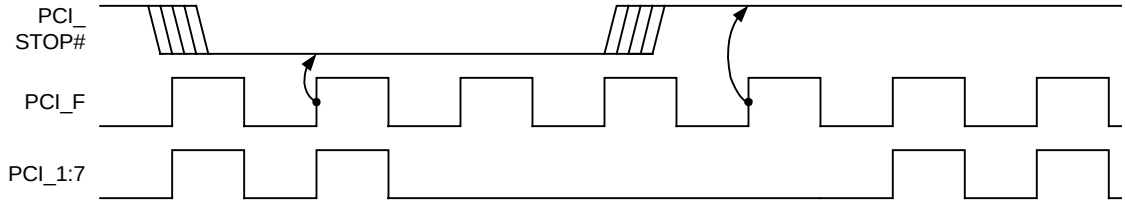
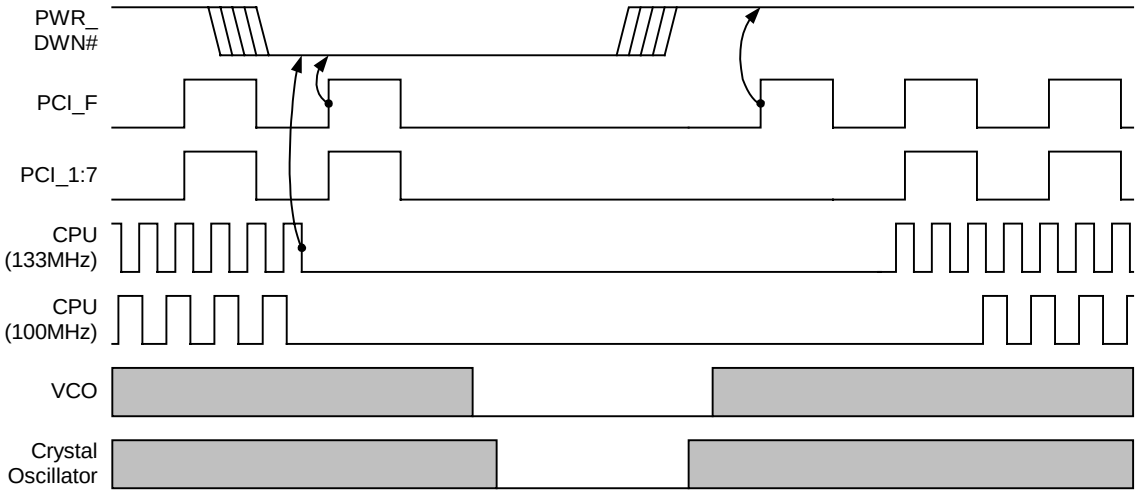


Figure 4: PWR_DWN# Timing

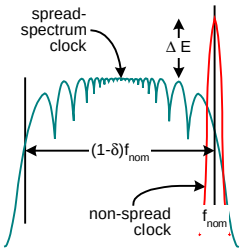


Shaded regions in the Crystal Oscillator and VCO waveforms indicate that the clock is valid and the Crystal Oscillator and VCO are active.

5.0 Spread Spectrum Modulation

To limit peak EMI emissions, high-speed motherboard designs now require the reduction of the peak harmonic energy contained in the system bus frequencies. A reduction in the peak energy of a specific frequency can be accomplished by spreading the energy over a limited range of frequencies through a technique known as spread spectrum clocking. In this technique, a generated clock frequency is dithered in a tightly controlled sweep near the clock frequency using a predetermined modulation profile and period.

Figure 5: Spectral Energy Distribution



The amount of EMI reduction is directly related to three parameters: the modulation percentage, the frequency of the modulation, and the modulation profile.

5.1 Modulation Percentage

The modulation percentage δ, is typically 0.5% of the center frequency (denoted here as f_{nom}). The modulation percentage determines the range of frequencies the spectral energy is distributed over. For a 100MHz clock frequency, a ±0.5% modulation sweeps the clock frequency between 99.5MHz and 100.5MHz. If the sweep is symmetrical around the center frequency, the technique is known as center-spread modulation. However, a circuit that is designed for a 100MHz reference may not have enough timing margin to support a clock greater then 100MHz. The clock frequency can instead be modulated between f_{nom}, and (1-δ) $f_{nom,}$; the technique is known as down-spread modulation. For a δ of –0.5%, the clock will sweep between 99.5MHz and 100MHz. A small degradation in circuit performance may be noticed, as the clock frequency now averages 99.75MHz.

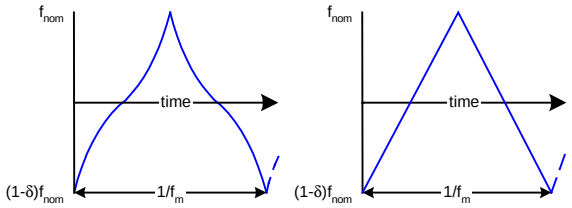
5.2 Modulation Frequency

The frequency of modulation, noted as f_m, describes how fast the center frequency sweeps between f_{nom}, and (1-δ) $f_{nom,}$. Typical modulation frequencies must be greater than 30kHz (above the audio band) but small enough to not upset system timing. Since a tracking PLL cannot instantaneously update the output clock to match a modulated input clock, any accumulation of the difference in phase between the modulated input clock and a tracking PLL output clock is called tracking skew. The resulting phase error will decrease the timing margins in any successive circuitry.

5.3 Modulation Profile

The modulation profile determines the shape of the spectral energy distribution by defining the time that the clock spends at a specific frequency. The longer a clock remains at a specific frequency, the larger the energy concentration at that frequency. A sinusoidal modulation spends a large portion of time between f_{nom}, and (1-δ) f_{nom}, resulting in large energy peaks at the edges of the spectral energy distribution. A linear modulation, such as a triangle profile, improves the spectral distribution but also exhibits energy peaking at the edges. A non-linear modulation profile, known as the “Hershey Kiss” profile offers the best distribution of spectral energy.

Figure 6: Modulation Profiles



The type of modulation profile used will also impact tracking skew. The maximum frequency change occurs at the profile limits where the modulation changes the slew rate polarity. To track the sudden reversal in clock frequency, the downstream PLL must have a large loop bandwidth.

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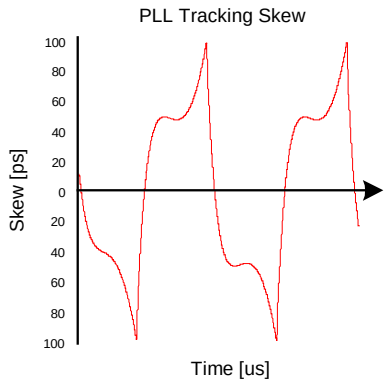
Compared to the profile limits the modulation slew rate is relatively slow between the limits, allowing the downstream PLL a chance to reduce the tracking skew. The ability of the downstream PLL to catch up is determined by the loop transfer function phase angle.

Spread spectrum clocking can be shown to have a negligible effect on cycle-to-cycle jitter performance. Any increase in jitter is less than 1ps when δ<1% and f_m<50kHz. Careful design of downstream PLLs can ensure that tracking skew is minimized. To have less than 100ps of tracking skew, a downstream PLL should have a loop bandwidth greater than 1MHz, and a phase angle less than 0.1°.

Figure 7 shows the tracking skew of a downstream PLL with a loop bandwidth of 1.5MHz and a phase angle of 0.26° following a non-linear profile-modulated 100MHz input clock with a δ=-0.5% and an f_m=31.2kHz.

Figure 7: PLL Tracking Skew

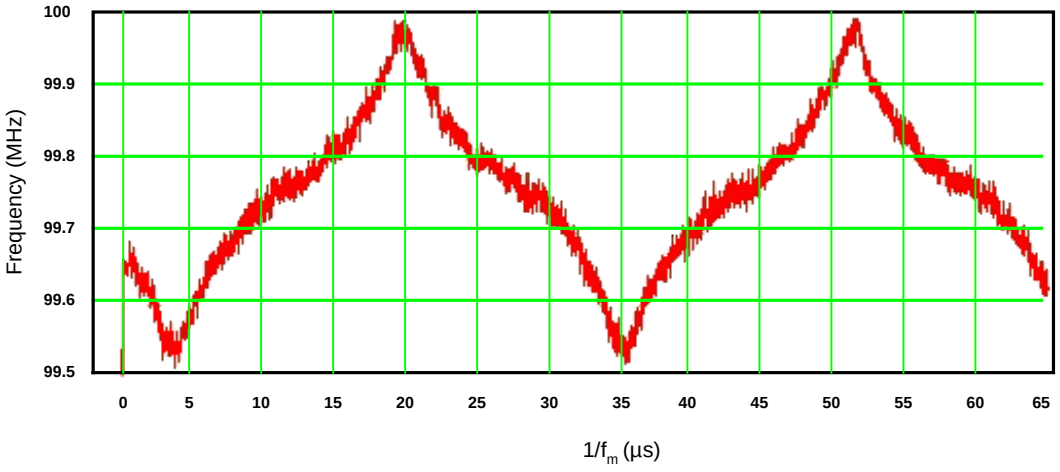


5.4 Spread Spectrum Enable

The active-low LVTTL SS_EN# input pin enables spread spectrum modulation of the CPU and PCI clocks. When SS_EN# is a logic-high, the spread spectrum modulation of these clocks is disabled. If SS_EN# is a logic-low, spread spectrum modulation is enabled.

A pull-up on this pin disables spread spectrum modulation by default.

Figure 8: Actual Modulation Profile



6.0 Electrical Specifications

Table 6: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 7: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	Core (VDD) @ 3.3V ± 5%	3.135	3.3	3.465	V
		Clock Buffers (VDD_P, VDD_R, VDD_66, VDD_48) @ 3.3V ± 5%	3.135	3.3	3.465	
		Clock Buffers (VDD_A, VDD_C, VDD_C2) @ 2.5V ± 5%	2.375	2.5	2.625	
Operating Temperature Range	T_A		0		70	°C
Crystal Resonator Frequency	f_{XTAL}		14.316	14.318	14.32	MHz
Crystal Resonator Load Capacitance	C_{XL}	XIN, XOUT pins	13.5	18	22.5	pF
Load Capacitance	C_L	APIC_0:2	10		20	pF
		CPU_0:3	10		20	
		CPU/2_0:3	10		20	
		PCI_F, PCI_1:7	10		30	
		CK48	10		20	
		CK66_0:3	10		30	
		REF_0:1	10		20	

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Table 8: DC Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{CPU} = 133MHz; SEL_0:1 = 11 VDD_A = VDD_C = VDD_C2 = 3.465V		120		mA
		f_{CPU} = 133MHz; SEL_0:1 = 11 VDD_A = VDD_C = VDD_C2 = 2.625V		88		
		f_{CPU} = 100MHz; SEL_0:1 = 11 VDD_A = VDD_C = VDD_C2 = 3.465V		120		
		f_{CPU} = 100MHz; SEL_0:1 = 11 VDD_A = VDD_C = VDD_C2 = 2.625V		86		
Supply Current, Static	I_{DDs}	PWR_DWN# low VDD_A = VDD_C = VDD_C2 = 3.465V		12		µA
		PWR_DWN# low VDD_A = VDD_C = VDD_C2 = 2.625V		8		
Digital Inputs (CPU_STOP#, PCI_STOP#, PWR_DWN#, SEL_0:1, SS_EN#)						
High-Level Input Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
High-Level Input Current	I_{IH}				5	µA
Low-Level Input Current (pull-up)	I_{IL}	V_{IL} = 0.4V	-2	-0.8		µA
Digital Inputs (SEL_133/100#)						
High-Level Input Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input Leakage Current	I_I		-5		+5	µA
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage	V_{TH}			1.5		V
High-Level Input Current	I_{IH}	V_{IH} = 3.3V		32		µA
Low-Level Input Current	I_{IL}	V_{IL} = 0V		-32		µA
Crystal Loading Capacitance *	$C_{L(xtal)}$	As seen by an external crystal connected to XIN and XOUT	13.5	18	22.5	pF
Input Loading Capacitance *	$C_{L(XIN)}$	As seen by an external clock driver on XOUT; XIN unconnected		36		pF
Crystal Oscillator Drive (XOUT)						
High Level Output Source Current	I_{OH}	V_I = 3.3V, V_O = 0V		-8.0		mA
Low Level Output Sink Current	I_{OL}	V_I = 0V, V_O = 3.3V		8.7		mA

Table 8: DC Electrical Specifications, continued

Unless otherwise stated, all power supplies = 3.3V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
CPU_0:3, CPU/2_0:1, APIC_0:2 Clock Outputs (2.5V Type 1 Clock Buffer)						
High Level Output Source Current	$I_{OH\ min}$	VDD_C, VDD_C2, VDD_A = 2.375V, V_O = 1.0V	-27			mA
	$I_{OH\ max}$	VDD_C, VDD_C2, VDD_A = 2.625V, V_O = 2.375V			-27	
Low Level Output Sink Current	$I_{OL\ min}$	VDD_C, VDD_C2, VDD_A = 2.375V, V_O = 1.2V	27			mA
	$I_{OL\ max}$	VDD_C, VDD_C2, VDD_A = 2.625V, V_O = 0.3V			30	
Output Impedance	z_{OL}	Measured at 1.25V, output driving low	13.5	23	45	Ω
	z_{OH}	Measured at 1.25V, output driving high	13.5	25	45	
Tristate Output Current	I_{OZ}		-10		10	µA
Short Circuit Output Source Current	I_{SCH}	V_O = 0V; shorted for 30s, max.		-56		mA
Short Circuit Output Sink Current	I_{SCL}	V_O = 2.5V; shorted for 30s, max.		58		mA
REF_0:1, CK48 Clock Outputs (3.3V Type 3 Clock Buffer)						
High-Level Output Source Current	$I_{OH\ min}$	VDD_R, VDD_48 = 3.135V, V_O = 1.0V	-29			mA
	$I_{OH\ max}$	VDD_R, VDD_48 = 3.465V, V_O = 3.135V			-23	
Low-Level Output Sink Current	$I_{OL\ min}$	VDD_R, VDD_48 = 3.135V, V_O = 1.95V	29			mA
	$I_{OL\ max}$	VDD_R, VDD_48 = 3.465V, V_O = 0.4V			27	
Output Impedance	z_{OL}	Measured at 1.65V, output driving low	20	45	60	Ω
	z_{OH}	Measured at 1.65V, output driving high	20	46	60	
Tristate Output Current	I_{OZ}		-10		10	µA
Short Circuit Output Source Current	I_{OSH}	V_O = 0V; shorted for 30s, max.		-41		mA
Short Circuit Output Sink Current	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		40		mA
PCI_1:7, PCI_F, CK66_0:1 Clock Outputs (3.3V Type 5 Clock Buffer)						
High Level Output Source Current	$I_{OH\ min}$	VDD_P, VDD_66 = 3.135V, V_O = 1.0V	-33			mA
	$I_{OH\ max}$	VDD_P, VDD_66 = 3.465V, V_O = 3.135V			-33	
Low Level Output Sink Current	$I_{OL\ min}$	VDD_P, VDD_66 = 3.135V, V_O = 1.95V	30			mA
	$I_{OL\ max}$	VDD_P, VDD_66 = 3.465V, V_O = 0.4V			38	
Output Impedance	z_{OL}	Measured at 1.65V, output driving low	12	29	55	Ω
	z_{OH}	Measured at 1.65V, output driving high	12	37	55	
Tristate Output Current	I_{OZ}		-10		10	µA
Short Circuit Output Source Current	I_{OSH}	V_O = 0V; shorted for 30s, max.		-51		mA
Short Circuit Output Sink Current	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		62		mA

Table 9: AC Timing Specifications

Unless otherwise stated, all power supplies = 3.3V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	133MHz			100MHz			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Overall									
Spread Spectrum Modulation Frequency *	f_m	SS_EN# low			31.5			31.5	kHz
Spread Spectrum Modulation Index*	δ_m	SS_EN# low			-0.5			-0.5	%
Clock Offset	t_{pd}	CPU @ 1.25V, C_L=20pF to CK66 @ 1.5V, C_L=30pF (rising edges)	0	0.3	1.5	0	0.4	1.5	ns
		CK66 @ 1.5V, C_L=30pF to PCI @ 1.5V, C_L=30pF (rising edges)	1.5	2.9	4.0	1.5	3.1	4.0	
		CPU @ 1.25V, C_L=20pF to APIC @ 1.25V, C_L=20pF (rising edges)	1.5	2.3	4.0	1.5	3.3	4.0	
Tristate Enable Delay *	t_{DZL}, t_{DZH}	SEL_0:1 and SEL_133/100#=0	1.0		10	1.0		10	ns
Tristate Disable Delay *	t_{DZL}, t_{DZH}	SEL_0:1 and SEL_133/100#=0	1.0		10	1.0		10	ns
Clock Stabilization (on power-up) *	t_{STB}	via PWR_DWN#			3.0			3.0	ms
APIC_0:2 Clock Output (2.5V Type 1 Clock Buffer)									
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45	50	55	45	50	55	%
Clock Skew *	t_{skw}	APIC to APIC @ 1.25V, C_L=20pF		-70			-70		
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.25V relative to an ideal clock, C_L=20pF, all PLLs active		204			122		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.25V, C_L=20pF, all PLLs active		82			88		ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.0V; C_L=10pF		1.2			1.2		ns
	$t_{r\ max}$	Measured @ 0.4V – 2.0V; C_L=20pF		1.5			1.5		
Fall Time *	$t_{f\ min}$	Measured @ 2.0V – 0.4V; C_L=10pF		1.8			1.5		ns
	$t_{f\ max}$	Measured @ 2.0V – 0.4V; C_L=20pF		2.1			1.8		
CPU/2_0:1 Clock Outputs (2.5V Type 1 Clock Buffer)									
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45	52	55	45	52	55	%
Clock Skew *	t_{skw}	CPU/2 to CPU/2 @ 1.25V, C_L=20pF		+10			+10		
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.25V relative to an ideal clock, C_L=20pF, all PLLs active		136			122		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.25V, C_L=20pF, all PLLs active		108			112		ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.0V; C_L=10pF		0.9			0.8		ns
	$t_{r\ max}$	Measured @ 0.4V – 2.0V; C_L=20pF		1.1			1.1		
Fall Time *	$t_{f\ min}$	Measured @ 2.0V – 0.4V; C_L=10pF		1.0			1.0		ns
	$t_{f\ max}$	Measured @ 2.0V – 0.4V; C_L=20pF		1.2			1.2		

Table 9: AC Timing Specifications, continued

Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

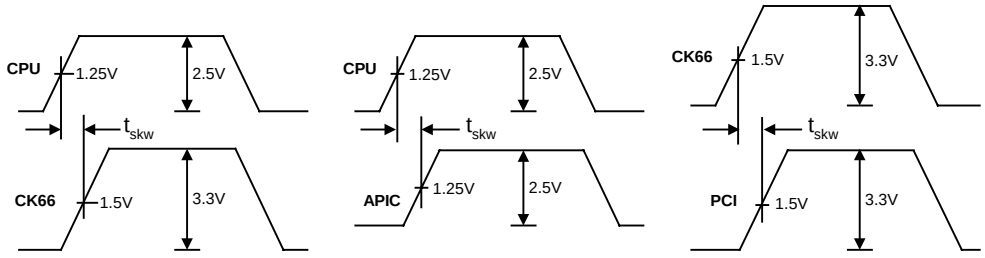
PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	133MHz			100MHz			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
CPU_0:3 Clock Outputs (2.5V Type 1 Clock Buffer)									
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45	49	55	45	49	55	%
Clock Skew *	t_{skw}	CPU to CPU @ 1.25V, C_L=20pF		+60			+60		
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.25V relative to an ideal clock, C_L=20pF, all PLLs active		136			134		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.25V, C_L=20pF, all PLLs active		123			97		ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.0V; C_L=10pF		1.1			0.9		ns
	$t_{r\ max}$	Measured @ 0.4V – 2.0V; C_L=20pF		1.4			1.4		
Fall Time *	$t_{f\ min}$	Measured @ 2.0V – 0.4V; C_L=10pF		1.0			0.9		ns
	$t_{f\ max}$	Measured @ 2.0V – 0.4V; C_L=20pF		1.1			1.2		
Enable Delay *	t_{DLH}	via CPU_STOP#	1.0		8.0	1.0		8.0	ns
Disable Delay *	t_{DHL}	via CPU_STOP#	1.0		8.0	1.0		8.0	ns
REF_0:1 Clock Outputs (3.3V Type 3 Clock Buffer)									
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45	50	55	45	50	55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.5V relative to an ideal clock, C_L=20pF, all PLLs active		27			23		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, C_L=20pF, all PLLs active		177			111		ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.4V; C_L=10pF		0.9			0.9		ns
	$t_{r\ max}$	Measured @ 0.4V – 2.4V; C_L=20pF		1.4			1.4		
Fall Time *	$t_{f\ min}$	Measured @ 2.4V – 0.4V; C_L=10pF		1.0			1.0		ns
	$t_{f\ max}$	Measured @ 2.4V – 0.4V; C_L=20pF		1.6			1.6		
CK48 Clock Output (3.3V Type 3 Clock Buffer)									
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45	51	55	45	51	55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.5V relative to an ideal clock, C_L=20pF, all PLLs active		244			246		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, C_L=20pF, all PLLs active		143			202		ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.4V; C_L=10pF		0.8			0.8		ns
	$t_{r\ max}$	Measured @ 0.4V – 2.4V; C_L=20pF		1.3			1.3		
Fall Time *	$t_{f\ min}$	Measured @ 2.4V – 0.4V; C_L=10pF		0.9			0.9		ns
	$t_{f\ max}$	Measured @ 2.4V – 0.4V; C_L=20pF		1.4			1.4		

Table 9: AC Timing Specifications, continued

Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

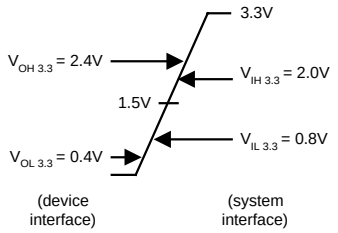
PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	133MHz			100MHz			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
PCI_1:7, PCI_F Clock Outputs (3.3V Type 5 Clock Buffer)									
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45	47	55	45	50	55	%
Clock Skew *	t_{skw}	PCI_F to PCI @ 1.5V, C_L=30pF		+660			+660		ps
		PCI to PCI @ 1.5V, C_L=30pF		+60			+60		
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.5V relative to an ideal clock, C_L=30pF, all PLLs active		220			131		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, C_L=30pF, all PLLs active		76			95		ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.4V; C_L=10pF		1.2			1.3		ns
	$t_{r\ max}$	Measured @ 0.4V – 2.4V; C_L=30pF		1.8			1.8		
Fall Time *	$t_{f\ min}$	Measured @ 2.4V – 0.4V; C_L=10pF		1.3			1.2		ns
	$t_{f\ max}$	Measured @ 2.4V – 0.4V; C_L=30pF		1.6			1.5		
Enable Delay *	t_{DLH}	via PCI_STOP#	1.0		8.0	1.0		8.0	ns
Disable Delay *	t_{DHL}	via PCI_STOP#	1.0		8.0	1.0		8.0	ns
CK66_0:3 Clock Outputs (3.3V Type 5 Clock Buffer)									
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45	52	55	45	51	55	%
Clock Skew *	t_{skw}	CK66 to CK66 @ 1.5V, C_L=30pF		120			120		ps
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 1.5V relative to an ideal clock, C_L=30pF, all PLLs on		137			123		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, C_L=30pF, all PLLs active		75			79		ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.4V; C_L=10pF		0.9			0.9		ns
	$t_{r\ max}$	Measured @ 0.4V – 2.4V; C_L=30pF		1.5			1.5		
Fall Time *	$t_{f\ min}$	Measured @ 2.4V – 0.4V; C_L=10pF		1.0			1.0		ns
	$t_{f\ max}$	Measured @ 2.4V – 0.4V; C_L=30pF		1.4			1.4		
Enable Delay *	t_{DLH}	via CPU_STOP#	1.0		8.0	1.0		8.0	ns
Disable Delay *	t_{DHL}	via CPU_STOP#	1.0		8.0	1.0		8.0	ns

Figure 9: Clock Skew Diagrams

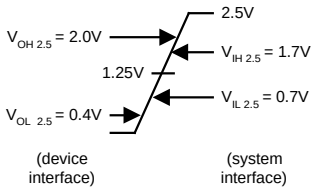


2.5V to 3.3V Clock Offset | 2.5V to 2.5V Clock Skew | 3.3V to 3.3V Clock Skew

Figure 10: DC Measurement Points

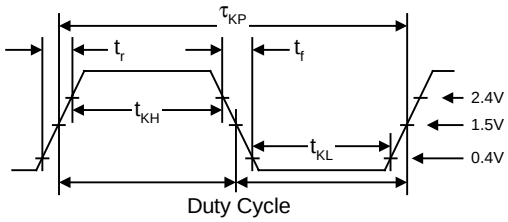


A. 3.3V Clock Interface

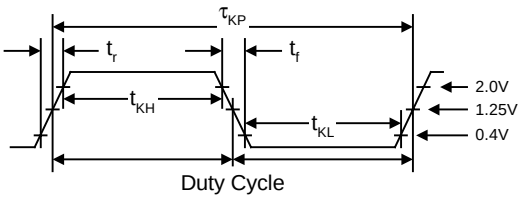


B. 2.5V Clock Interface

Figure 11: Timing Diagrams



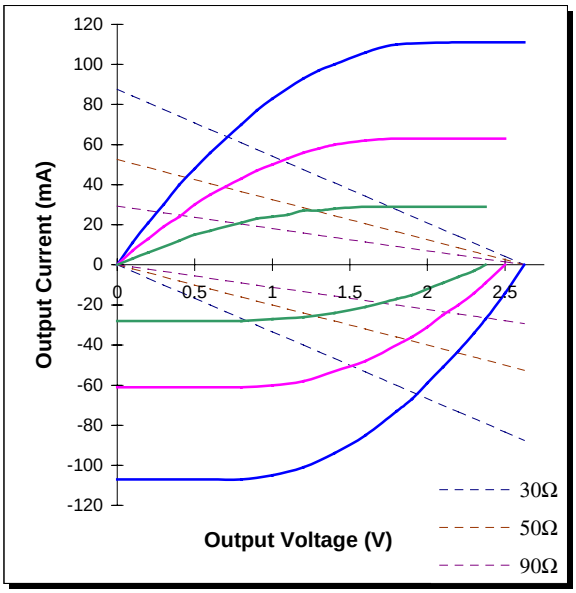
A. 3.3V Clock Interface



B. 2.5V Clock Interface

Table 10: CPU_0:3, CPU/2_0:1, APIC_0:2 Clock Outputs

Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-28	-61	-107
0.1	3	7	11	0.4	-28	-61	-107
0.2	6	13	21	0.6	-28	-61	-107
0.3	9	19	30	0.8	-28	-61	-107
0.4	12	24	40	1	-27	-60	-105
0.5	15	30	48	1.2	-26	-58	-101
0.6	17	35	56	1.4	-24	-53	-94
0.7	19	39	63	1.6	-21	-48	-85
0.8	21	43	70	1.8	-17	-40	-73
0.9	23	47	77	1.9	-15	-36	-67
1	24	50	83	2	-12	-31	-59
1.1	25	53	88	2.1	-9	-25	-51
1.2	27	56	93	2.2	-6	-20	-43
1.3	27	58	97	2.3	-3	-14	-34
1.4	28	60	100	2.375	0	-9	-27
1.6	29	62	106	2.5		0	-14
1.8	29	63	110	2.625			0
2.2	29	63	111				
2.375	29	63	111				
2.5		63	111				
2.625			111				



Data in this table represents nominal characterization data only

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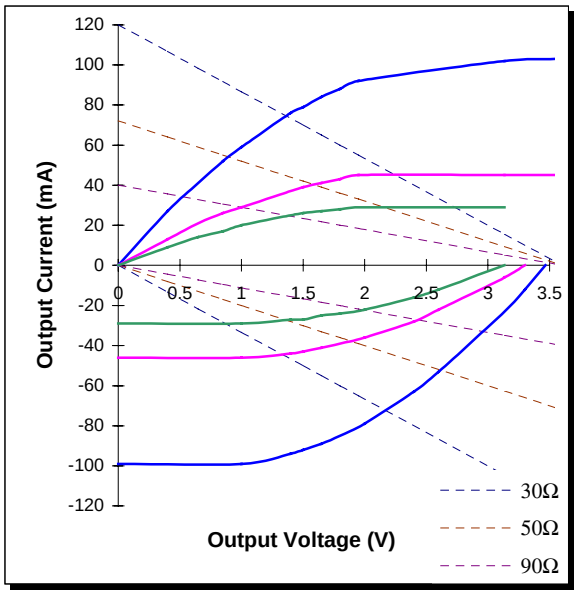
Table 11: REF_0:1, CK48 Clock Outputs

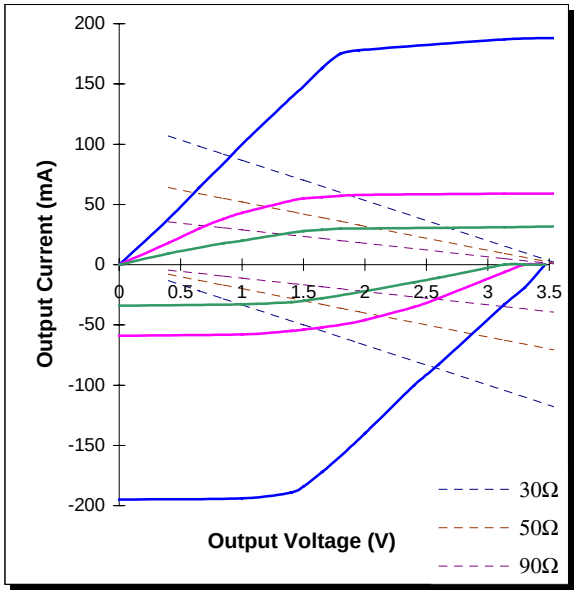
Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-29	-46	-99
0.4	9	13	27	1	-29	-46	-99
0.65	14	21	41	1.4	-27	-44	-94
0.85	17	26	52	1.5	-27	-43	-92
1	20	29	59	1.65	-25	-41	-89
1.4	25	37	76	1.8	-24	-39	-85
1.5	26	39	79	2	-22	-36	-79
1.65	27	41	84	2.4	-16	-28	-63
1.8	28	43	88	2.6	-12	-22	-53
1.95	29	45	92	3.135	0	-6	-23
3.135	29	45	102	3.3		0	-12
3.6		45	102	3.465			0



Data in this table represents nominal characterization data only

Table 12: PCI_1:7, PCI_F, CK66_0:3 Clock Outputs

Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-34	-59	-195
0.4	9.4	18	38	1	-33	-58	-194
0.65	14	30	64	1.4	-31	-55	-189
0.85	17.7	38	84	1.5	-30	-54	-184
1	20	43	100	1.65	-28	-52	-172
1.4	26.5	53	139	1.8	-25.5	-50	-159
1.5	28	55	148	2	-22	-46	-140
1.65	29	56	163	2.4	-14.5	-35	-100
1.8	30	57	175	2.6	-11	-28	-83
1.95	30	58	178	3.135	0	-6	-33
3.135	31	59	187	3.3		0	-19
3.6	32	59	188	3.465			0



Data in this table represents nominal characterization data only

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7.0 Package Information

Table 13: 56-pin SSOP (0.300") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.095	0.110	2.41	2.79
A_1	0.008	0.016	0.203	0.406
A_2	0.088	0.092	2.24	2.34
B	0.008	0.0135	0.203	0.343
C	0.005	0.010	0.127	0.254
D	0.720	0.730	18.29	18.54
E	0.292	0.299	7.42	7.59
e	0.025 BSC		0.64 BSC	
H	0.400	0.410	10.16	10.41
L	0.024	0.040	0.610	1.02
Θ	0°	8°	0°	8°

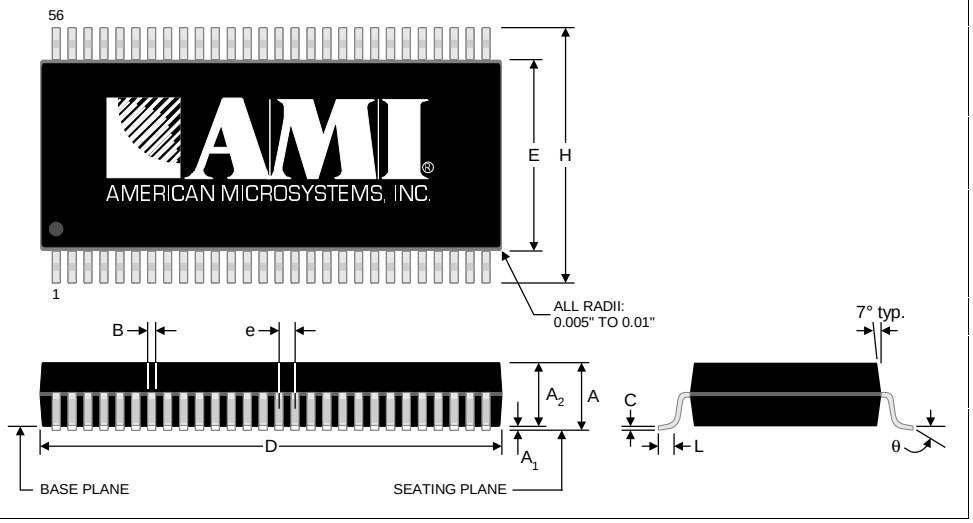

Table 14: 56-pin SSOP (0.300") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	81	°C/W
Lead Inductance, Self	L_{11}	Longest trace + wire	6.41	nH
		Shortest trace + wire	2.49	
Lead Inductance, Mutual	L_{12}	Longest trace + wire to first adjacent trace	3.65	nH
		Shortest trace + wire to first adjacent trace	1.35	
	L_{13}	Longest trace + wire to next adjacent trace	2.50	
		Shortest trace + wire to next adjacent trace	0.90	
Lead Capacitance, Bulk	C_{11}	Longest trace + wire to V_{SS}	0.94	pF
		Shortest trace + wire to V_{SS}	0.49	
Lead Capacitance, Mutual	C_{12}	Longest trace + wire to first adjacent trace	0.48	pF
		Shortest trace + wire to first adjacent trace	0.20	
	C_{13}	Longest trace + wire to next adjacent trace	0.04	
		Shortest trace + wire to next adjacent trace	0.01	

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8.0 Ordering Information

Table 15: Device Ordering Codes

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS6261-01	11565-801	48-pin (7.5mm/0.300") SSOP (Shrink Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
	11565-811	48-pin (7.5mm/0.300") SSOP (Shrink Small Outline Package)	0°C to 70°C (Commercial)	Tubes

9.0 Revision Information

DATE	PAGE	DESCRIPTION
1/31/00	11-13	Updated characterization data

American Microsystems, Inc., 2300 Buckskin Rd., Pocatello, ID 83201, (208) 233-4690, FAX (208) 234-6796, WWW Address: http://www.amis.com E-mail: tgp@amis.com