

Video Deinterlacer

DVD

Digital Camera

Digital TV

Imaging

IP Cores

Product Brief

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Benefits Overview

Zoran's Frame-It-1 Video Deinterlacer is a silicon-efficient, high-performance Intellectual Property Core for video IC designs requiring progressive video output. Frame-It-1 is based on Zoran's extensive experience delivering high quality, high volume video ICs to major consumer products manufacturers worldwide. Frame-It-1 employs a robust motion detection and an intelligent interpolation algorithm in a easily implemented, fully synchronous design. 3:2 pull-down, 2:2 pull-down, and bad edit detection enable superior deinterlacing of source material originally from film.

Proven in silicon, the Frame-It-1 Video Deinterlacer greatly reduces the risk and time involved when integrating the video deinterlacing

function into an IC. Expensive, discrete components can be eliminated from system designs. Frame-It-1 is designed into Zoran's Vaddis™ family of DVD decoders, which are in mass production and are used in brand name consumer products worldwide.

VIP-II Demonstration System

The VIP-II is an FPGA demonstration system for Zoran's IP Core products. The VIP-II accepts composite video, S-video and component video inputs and with its user friendly GUI, enables customers to thoroughly evaluate the performance of Zoran's IP Core products.

Features

- "I to P" converter
- Converts interlaced video to progressive output video
- Robust motion detection based algorithm
- Weaves still areas of the image
- Advanced interpolation for moving areas of the image
- 3:2 and 2:2 pull-down detection for film modes
- Bad edit detection
- Silicon efficient design
- Requires only a single clock input from 20 to 30 MHz
- Fully synchronous design
- Process technology independent "softcore"

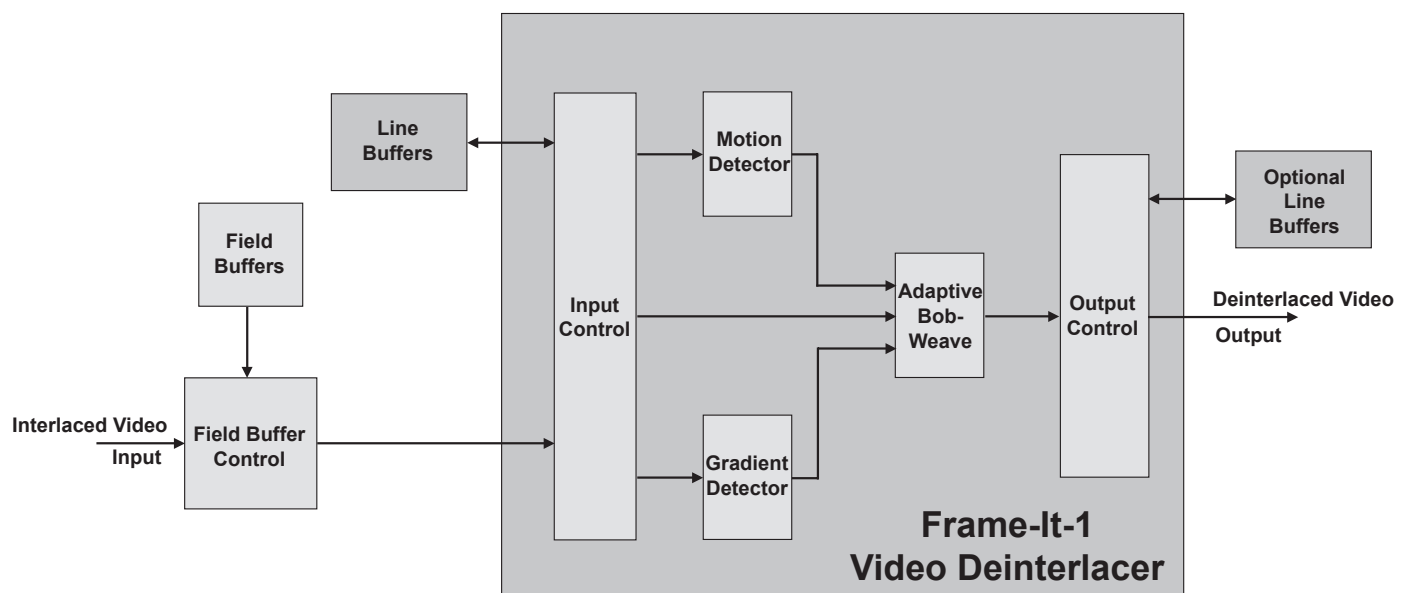
Integrated Circuit Applications

- LCD controllers
- LCD-TV
- PDP-TV
- Projector TV Systems
- Progressive output CRT-TV
- Any IC requiring progressive video output

Deliverables

- Compilable Verilog source code
- Bit-accurate, cycle-accurate C++ model
- Synopsis synthesis scripts
- Test input files
- Documentation
- VIP-II FPGA demonstration system available

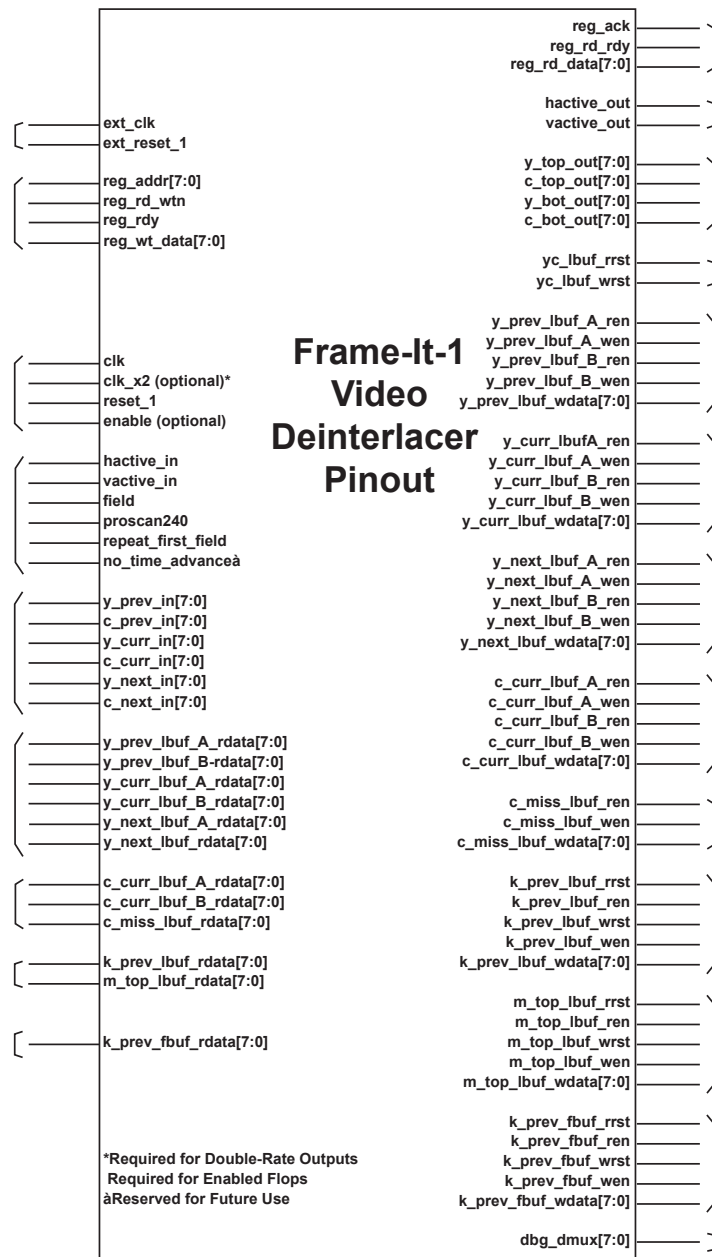
Frame-It-1 Video Deinterlacer Block Diagram



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Frame-It-1 Video Deinterlacer Logical Pinout



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