WESTERN DIGITAL
CORPORATION

FR1502 Series First-In/First-Out Buffer Register

FEBRUARY, 1981

FEATURES

- 40 CHARACTERS BY 9 BITS
- EXPANDABLE CHARACTER AND BIT SIZE (CASCADE CAPABILITY)
- DC TO 1 MHz ASYNCHRONOUS I/O ACCESS
- INPUT/OUTPUT READY STATUS FLAGS
- THREE STATE OUTPUTS
- SEPARATE INPUT AND OUTPUT ENABLES
- DIRECTLY TTL COMPATIBLE
- MASTER RESET
- NO EXTERNAL CLOCKS REQUIRED
- 28-PIN DIP PLASTIC OR CERAMIC PACKAGE

APPLICATIONS

POINT OF SALE TERMINALS

DATA TRANSMISSION BUFFER

LINE PRINTER INPUT BUFFER

KEY-TO-TAPE/KEY-TO-DISC EQUIPMENT

CARD/TAPE READERS

AUTO DIALERS

CRT BUFFER MEMORY

CONTROL STACK SILO ORIENTED MACHINES

COMPUTER/TERMINALS I/O INTERFACE BUFFER

TELEPRINTER BUFFER

GENERAL DESCRIPTION

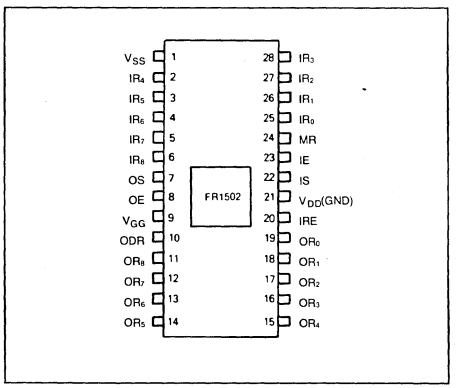
The FIFO (First-In/First-Out) Storage Chip is an asynchronous memory organized in a nine-bit by forty-character stack. Characters are loaded at the top of the stack and then "sink" to the bottom of the stack, or to the level of previously entered data, without external clocks being applied. As a character is taken from the bottom of the stack, all of the previously loaded characters will automatically propagate toward the output (bottom of stack).

Data can be entered whenever the INPUT REGISTER EMPTY line is high by strobing INPUT STROBE. The INPUT ENABLE line must also be high while strobing. The INPUT STROBE resets INPUT REGISTER EMPTY and latches the input data. As soon as this data is latched, INPUT REGISTER EMPTY will again go high and additional data can be loaded.

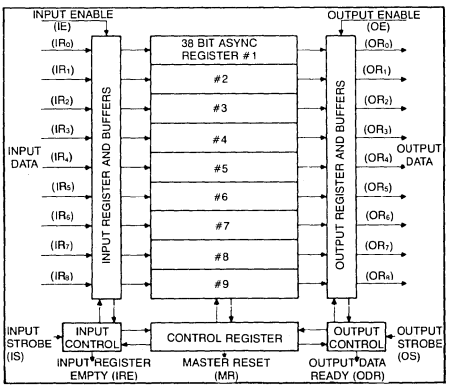
When data reaches the FIFO output, the OUTPUT DATA READY line will go high. The data is then valid at the outputs (providing the OUTPUT ENABLE line is high). The falling edge of the OUTPUT STROBE causes the OUTPUT DATA READY line to go low and to shift new data into the output register. When the new data is available, the OUTPUT DATA READY signal again goes high.

The FIFO output data lines are in high impedance state whenever the OUTPUT ENABLE line is low.

The logic conventions and internal delays designed into the FIFO allow direct expansion of the memory without external hardware (Cascade Mode).



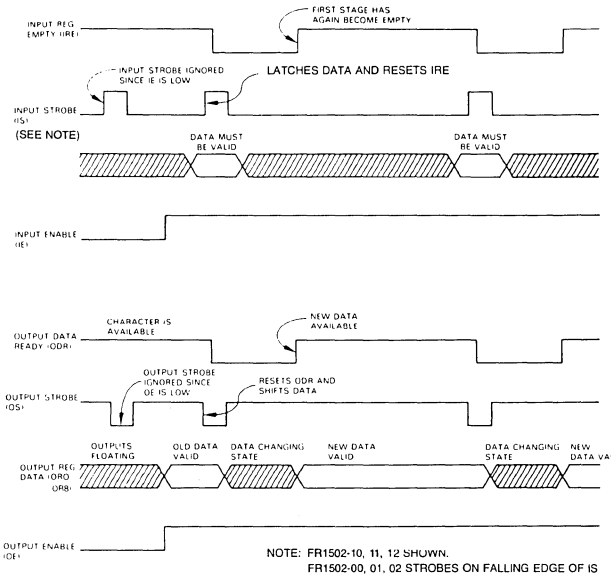
PIN CONNECTIONS



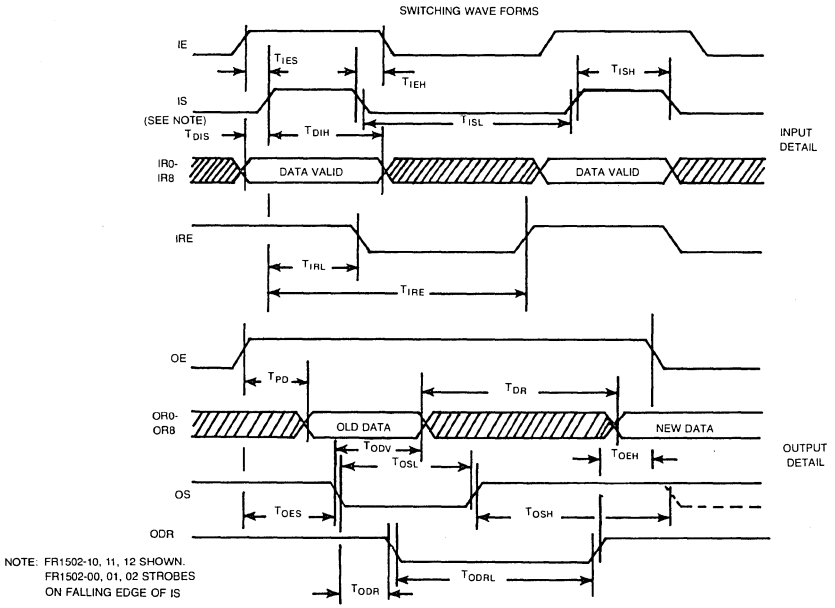
BLOCK DIAGRAM

INTERFACE SIGNALS DESCRIPTIONS

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
25-28, 2-6	INPUT REGISTER FR1502-00 -01 -02	IR0-IR8	Input data lines. These are input (but not latched) to the FIFO when the Input Enable and Input Strobe are active (high).
	FR1502-10 -11 -12	IR0-IR8	Input data lines. These are input (but not latched) to the FIFO independently of the Input Enable or Input Strobe.
20	INPUT REGISTER EMPTY FR1502-00 -01 -02	IRE	When high, indicates that data can be loaded into the FIFO. It is reset to a low by falling edge of the Input Strobe.
	FR1502-10 -11 -12	IRE	When high, indicates that data can be loaded into the FIFO. It is reset to a low by a rising edge of the Input Strobe.
22	INPUT STROBE FR1502-00 -01 -02	IS	Latches input data in the FIFO on a falling edge.
	FR1502-10 -11 -12	IS	Latches input data in the FIFO on a rising edge.
24	MASTER RESET	MR	When high, clears the FIFO control registers. This leaves the OUTPUT REGISTER DATA (OR0-OR8) in an undefined state, sets INPUT REGISTER EMPTY (IRE) to high and resets OUTPUT DATA READY (ODR) to low.
19-11	OUTPUT REGISTER DATA	ORO-OR8	Three state data outputs. When OE is low, the outputs are in the high impedance state. When OE is high, these lines present the previous latched data in a first-in/first-out manner.
10	OUTPUT DATA READY	ODR	ODR is high when data is latched and available at the data output lines. Is reset to low by the falling edge of OUTPUT STROBE (OS) if OUTPUT ENABLE (OE) is high.
7	OUTPUT STROBE	OS	A falling edge of this signal resets the OUTPUT DATA READY (ODR) line and then shifts the data one step towards the output if OUTPUT ENABLE (OE) is high.
23	INPUT ENABLE FR1502-00 -01 -02	IE	When high, enables the Input Register and Input Control logic. When INPUT STROBE (IS) is high, the input data will be transferred into the FIFO. IS can then be used to latch the data.
	FR1502-10 -11 -12	IE	When high, enables the Input Control Logic. At any state of IE or IS, the input data will be transferred into the FIFO, but can not be latched unless IE is high.
8	OUTPUT ENABLE	OE	When low, OE puts the output lines (OR0-OR8) in high impedance state. When high, the output lines present the output data.
1	V_{SS} POWER SUPPLY	V_{SS}	+5VDC
21	V_{DD} POWER SUPPLY	V_{DD}	0 Volt—GND
9	V_{GG} POWER SUPPLY	V_{GG}	−12VDC



SWITCHING CHARACTERISTICS



SWITCHING WAVE FORMS

ABSOLUTE MAXIMUM RATINGS

V_{GG} Supply Voltage	+0.3V to -20V
V_{DD} Supply Voltage	+0.3V to -20V
Clock Input Voltage*	+0.3V to -20V
Logic Input Voltage*	+0.3V to -20V
Logic Output Voltage*	+0.3V to -20V
Storage Temperature (Ceramic)	−65°C to +150°C
Storage Temperature (Plastic)	−55°C to +125°C

*V_{GG} = VDD = 0V

NOTE: These voltages are measured with respect to V_{SS} (Substrate)

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = 0V; V_{GG} =-12V ± 5%; TA = 0°C to +70°C unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
	INPUT LOGIC LEVELS			
V_{IL}	Low-level Input Voltage		0.8V	V_{SS} = 4.75V
V_{IH}	High-level Input Voltage	V_{SS}−1.5V		(NOTE 1)
	OUTPUT LOGIC LEVELS			(NOTE 2)
V_{OL}	Low-level Output Voltage		0.4V	V_{SS} = 5.25V I_{OL} = −1.6mA
V_{OH}	High-level Output Voltage	V_{SS}−1.0V		V_{SS} = 4.75V I_{OH} = +200 uA
	INPUT CURRENT			
I_{IL}	Low-level Input Current (each pin)		−1.6mA	V_{SS} = 5.25V V_{IN} = 0.4V
I_{SS}	SUBSTRATE SUPPLY CURRENT		65 mA	V_{SS} = 5.25V V_{GG} = −12.6V
I_{GG}	GATE SUPPLY CURRENT		−30mA	V_{IN} = 0.4V

NOTE 1: All inputs have pull-up resistors. This allows unloaded TTL outputs of 2.0V to be connected and operate properly. When connected, this voltage (2.0V) will become V_{SS} −1.5V.

NOTE 2: V_{OL} and V_{OH} when OE = V_{IH} (low impedance output). High impedance (OE = V_{IL}) ≈ 10 Mohm.

SWITCHING CHARACTERISTICS — See "Switching Waveforms"

(V_{SS} = +5V, V_{DD} = 0V, V_{GG} = −12V, T_A = 0°C to +70°C, C_{LOAD} = 10 pf)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
T_{IES}	Input Enable Setup Time	0 ns		
T_{IEH}	Input Enable Hold Time	0 ns		
T_{DIS}	Data Input Setup Time	0 ns		
T_{DIH}	Data Input Hold Time	250 ns		
T_{IRL}	Input Register Load Time		250 ns	
T_{IRE}	Input Register Empty Time		800 ns	
T_{ISL}	Input Strobe Low Time	450 ns		
T_{ISH}	Input Strobe High Time	150 ns		
T_{OES}	Output Enable Setup Time	50 ns		
T_{OEH}	Output Enable Hold Time	50 ns		(NOTE 1)
T_{OSL}	Output Strobe Low Time	150 ns		
T_{ODR}	Output Data Ready Time		200 ns	
T_{DR}	Data Reset Time		600 ns	
T_{PD}	Output Propagation Delay Time		250 ns	
T_{ODRL}	Output Data Ready Low		600 ns	
T_{OSH}	Output Strobe High Time	500 ns		
T_{ODV}	Output Data Valid Time		200 ns	
T_R	Maximum Ripple Time		10 μs	(NOTE 2)
T_B	Maximum Bubble Time		25 μS	(NOTE 3)
T_{MR}	Master Reset Pulse Time	500 ns		
f_D	Maximum Data Rate	250 kHz	1 MHz	(NOTE 4)

NOTE 1: $T_{rise} = T_{fall}$ = 10nS.

NOTE 2: Ripple Time—time required for a single data character to propagate from the input to the output of an empty FIFO (IS strobing edge to ODR rising edge).

NOTE 3: Bubble Time— time required for a "hole" to propagate from the output to the input of a full FIFO (falling edge of OS to rising edge of IRE).

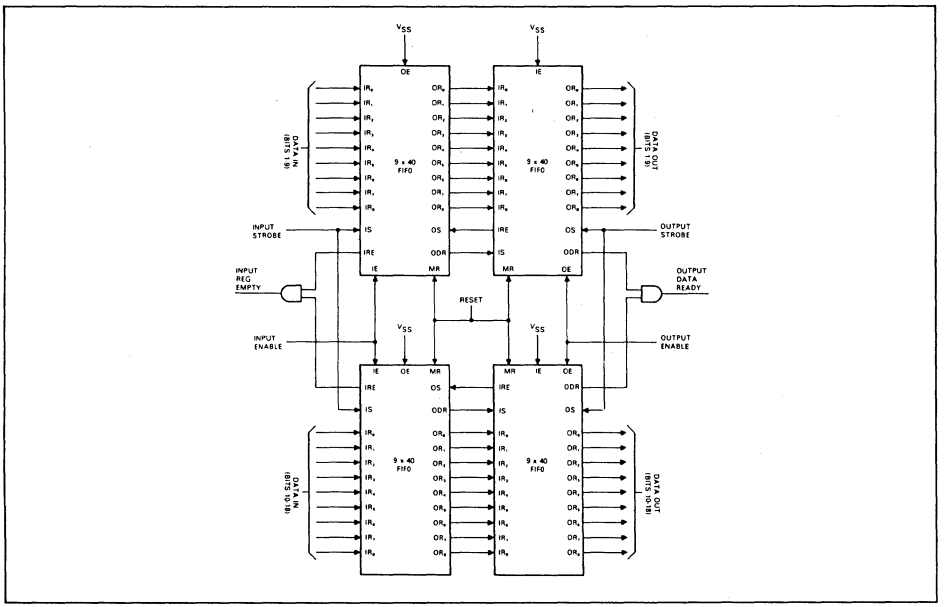
NOTE 4: The maximum data rates for a "single" FIFO (not cascaded) and for FIFO's cascaded together are the same.

GENERAL NOTE: All A.C. test points are at 0.8V or 2.0V.

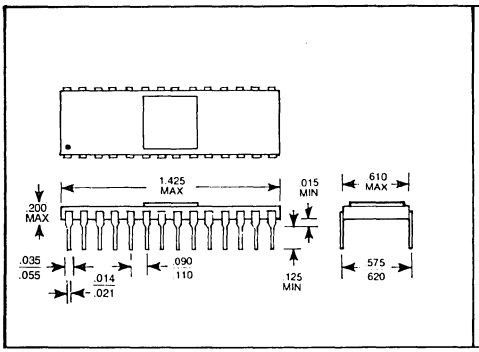
ORDERING INFORMATION

T_A = O°C to +70°C

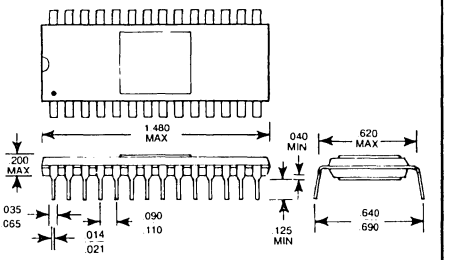
PART NO.	PACKAGE TYPE	CASCADABLE	INPUT STROBE EDGE	MAX. DATA RATE
FR1502E-00	CERAMIC	NO	FALLING	1.0 MHz
F-00	PLASTIC	NO	FALLING	1.0 MHz
E-01	CERAMIC	NO	FALLING	500 kHz
F-01	PLASTIC	NO	FALLING	500 kHz
E-02	CERAMIC	NO	FALLING	250 kHz
F-02	PLASTIC	NO	FALLING	250 kHz
E-10	CERAMIC	YES	RISING	1.0 MHz
F-10	PLASTIC	YES	RISING	1.0 MHz
E-11	CERAMIC	YES	RISING	500 kHz
F-11	PLASTIC	YES	RISING	500 kHz
E-12	CERAMIC	YES	RISING	250 kHz
F-12	PLASTIC	YES	RISING	250 kHz



EXPANSION EXAMPLE



FR1502E CERAMIC PACKAGE



FR1502F PLASTIC PACKAGE

WESTERN DIGITAL CORPORATION
3128 REDHILL AVENUE, BOX 2180
NEWPORT BEACH, CA 92663 (714) 557-3550, TWX 910-595-1139