FQD60N03

Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- Lead-Free

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	56	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	35	
I_{DM}	Pulsed Drain Current ①	200	
P_D @T_C = 25°C	Maximum Power Dissipation	50	W
P_D @T_C = 100°C	Maximum Power Dissipation	25	
	Linear Derating Factor	0.33	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount)	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.023	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.8	9.8	mΩ	V_{GS} = 10V, I_D = 15A
		—	11	13.5		V_{GS} = 4.5V, I_D = 12A
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.80	2.25	V	V_{DS} = V_{GS}, I_D = 25µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.0	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
		—	—	150		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	71	—	—	S	V_{DS} = 15V, I_D = 12A
Q_g	Total Gate Charge	—	9.6	14		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	2.6	—		V_{DS} = 15V
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	0.90	—	nC	V_{GS} = 4.5V
Q_{gd}	Gate-to-Drain Charge	—	3.5	—		I_D = 12A
Q_{godr}	Gate Charge Overdrive	—	2.6	—		See Fig. 16
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	4.4	—		
Q_{oss}	Output Charge	—	5.8	—	nC	V_{DS} = 15V, V_{GS} = 0V
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—		V_{DD} = 16V, V_{GS} = 4.5V
t_r	Rise Time	—	11	—		I_D = 12A
$t_{d(off)}$	Turn-Off Delay Time	—	12	—	ns	Clamped Inductive Load
t_f	Fall Time	—	3.3	—		
C_{iss}	Input Capacitance	—	1150	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	260	—	pF	V_{DS} = 15V
C_{rss}	Reverse Transfer Capacitance	—	120	—		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	40	mJ
I_{AR}	Avalanche Current ①	—	12	A
E_{AR}	Repetitive Avalanche Energy ①	—	5.0	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	56	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	—	—	200		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 10A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	25	38	ns	T_J = 25°C, I_F = 12A, V_{DD} = 15V
Q_{rr}	Reverse Recovery Charge	—	17	26	nC	di/dt = 100A/µs
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

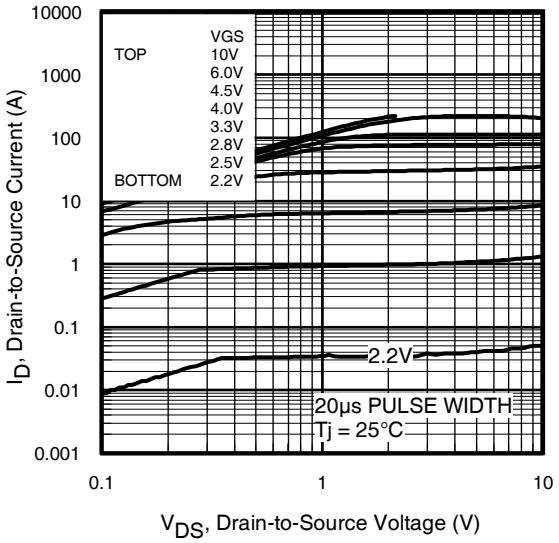

Fig 1. Typical Output Characteristics

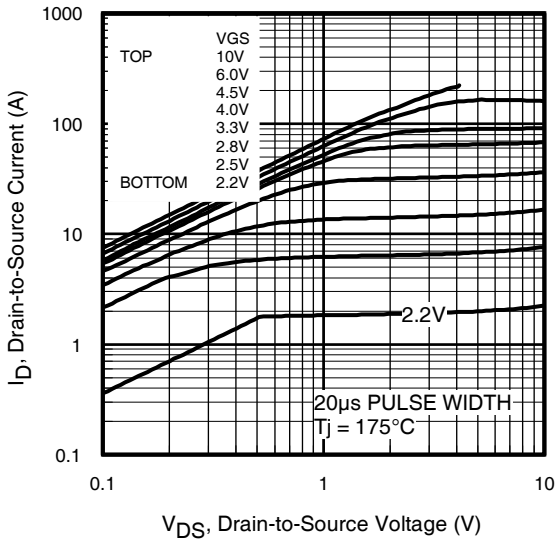

Fig 2. Typical Output Characteristics

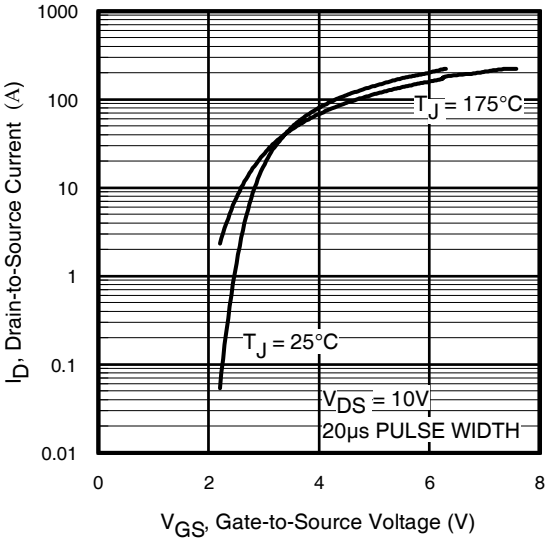

Fig 3. Typical Transfer Characteristics

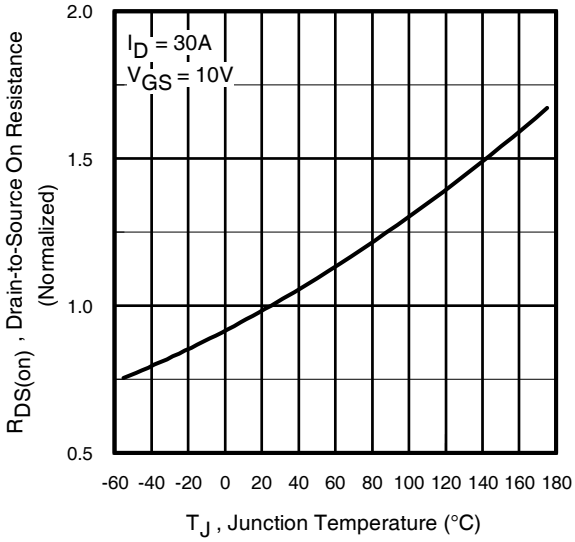

Fig 4. Normalized On-Resistance vs. Temperature

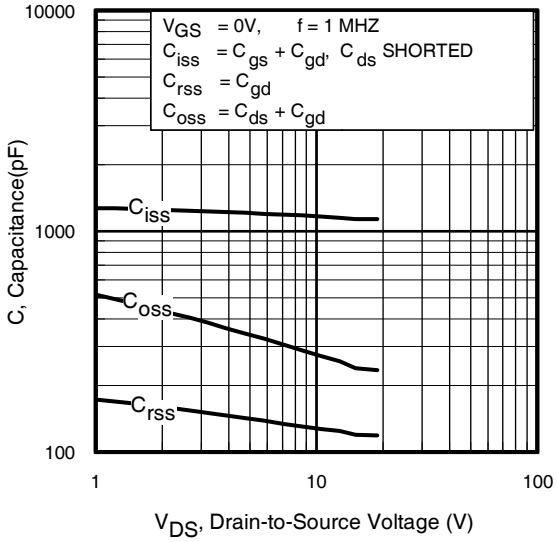

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

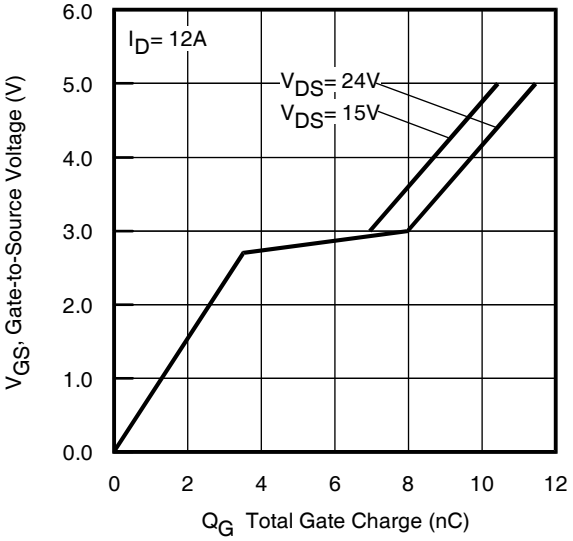

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

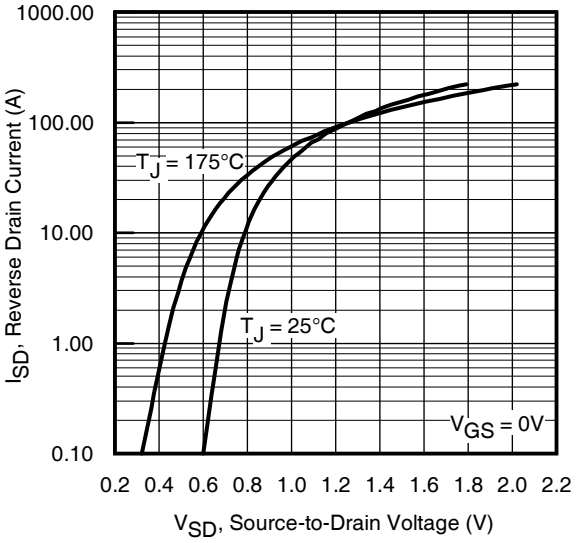

Fig 7. Typical Source-Drain Diode Forward Voltage

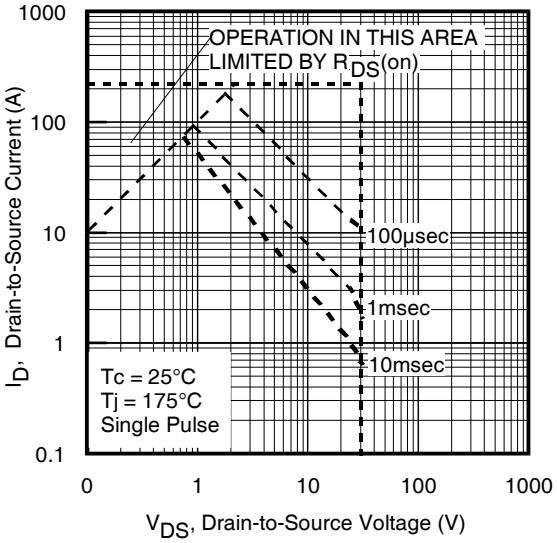

Fig 8. Maximum Safe Operating Area

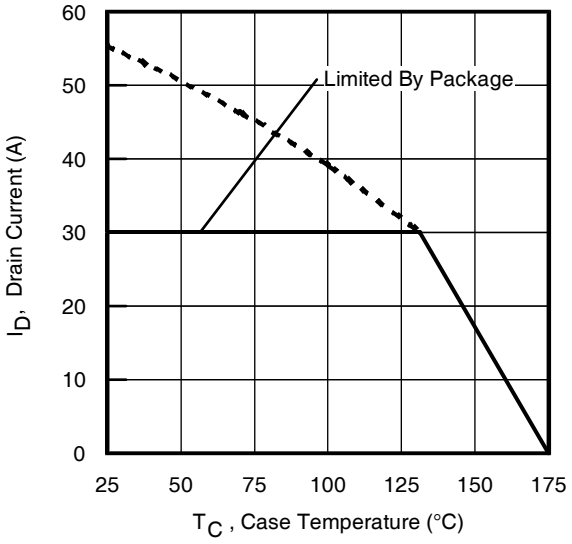

Fig 9. Maximum Drain Current vs. Case Temperature

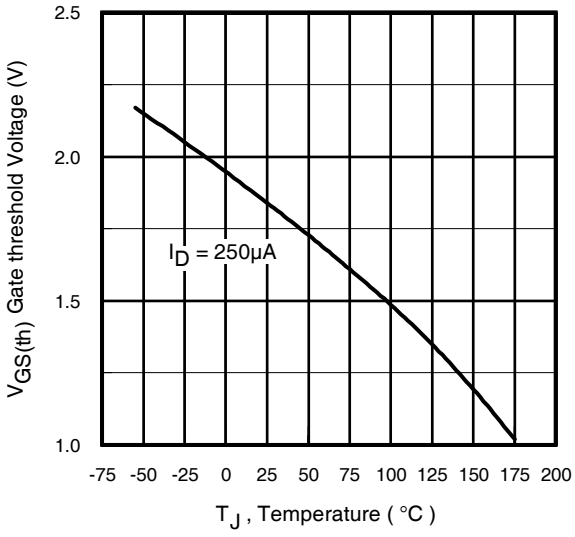

Fig 10. Threshold Voltage vs. Temperature

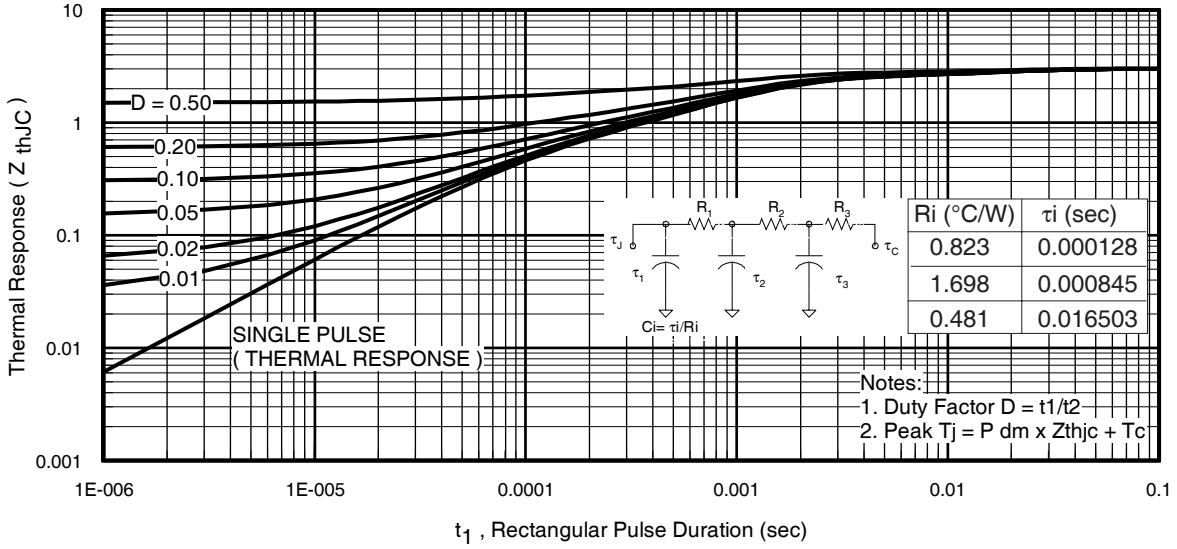

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

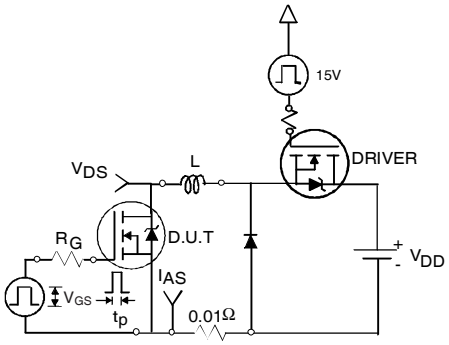

Fig 12a. Unclamped Inductive Test Circuit

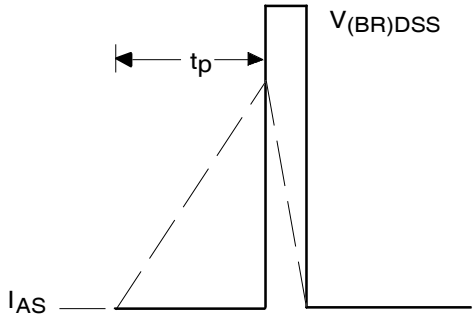

Fig 12b. Unclamped Inductive Waveforms

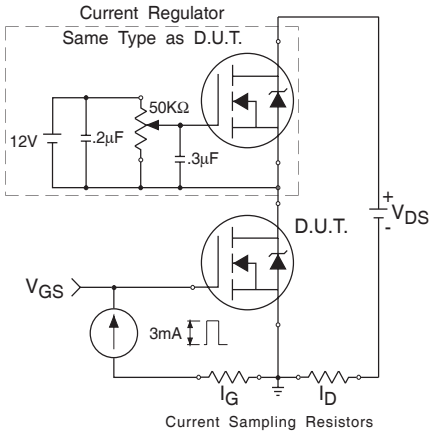

Fig 13. Gate Charge Test Circuit

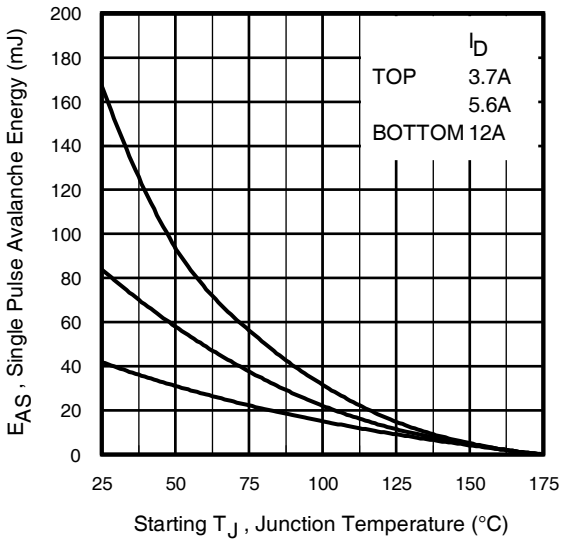

Fig 12c. Maximum Avalanche Energy vs. Drain Current

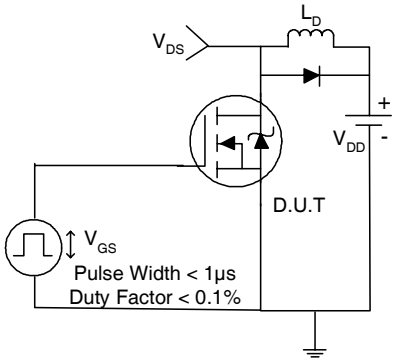

Fig 14a. Switching Time Test Circuit

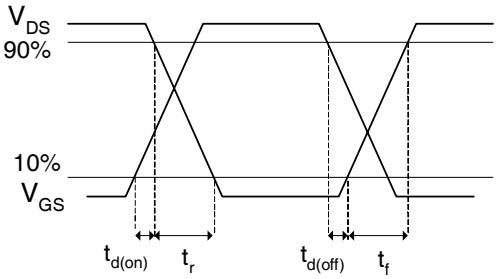

Fig 14b. Switching Time Waveforms

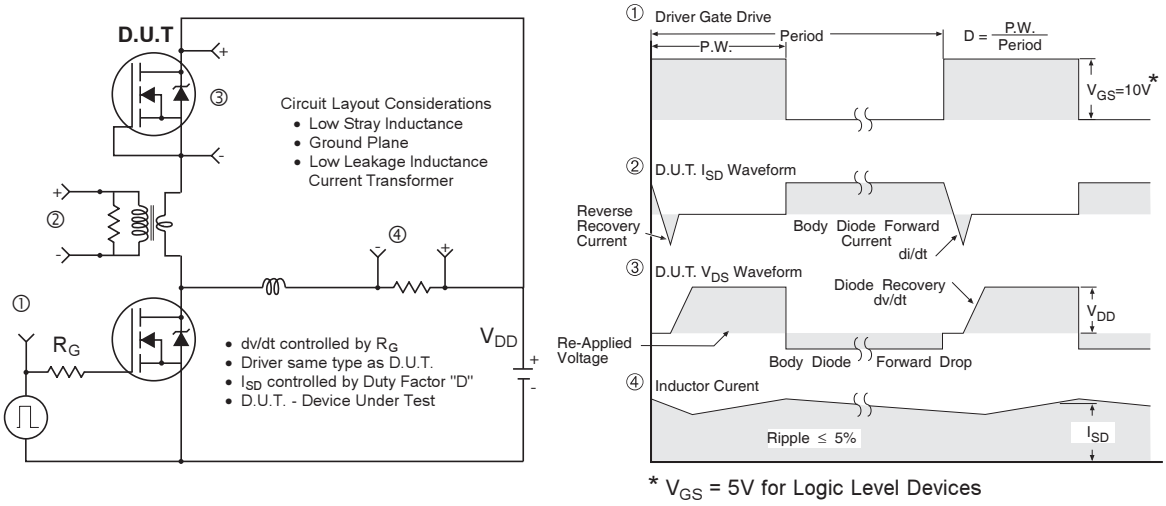

Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

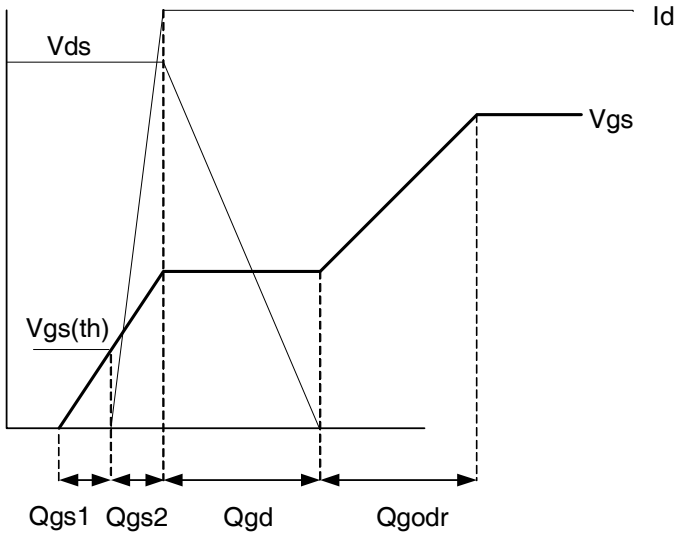

Fig 16. Gate Charge Waveform