Microprocessor Voltage Monitors with Manual Reset

Description

The FP6811 and FP6812 are cost-effective system supervisory circuits which are designed to monitor the power supply status in micro-processor (μP) and digital systems. In addition, they provide a de-bounced manual reset input pin to initiate a reset.

These circuits assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold.

The FP6811-N has an open-drain output stage, while FP6811-C and FP6812-C have push-pull outputs. The FP6811-N's open-drain output requires a pull-up resistor. The FP6811 has an active-low $\overline{\text{RESET}}$ output while the FP6812 has an active-high RESET output.

The FP6811 and FP6812 are optimized to reject fast transient glitches on the V_{CC} line. A low supply current makes these devices suitable for portable equipment. Each device is available in SOT-23-5, SC-82 and SOT-143 packages.

Features

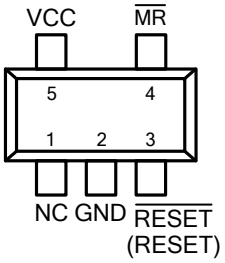
- Precision Monitoring of Power-Supply Voltage
- 140ms Guaranteed Minimum Reset Output Duration
- Low Supply Current
- V_{CC} Transient Immunity
- Small SOT-23-5, SC-82 and SOT-143 Packages
- No External Components
- Guaranteed Reset Valid to V_{CC}=1V
- Available in Three Output Configurations
  - Open-Drain $\overline{\text{RESET}}$ Output (FP6811-N)
  - Push-Pull $\overline{\text{RESET}}$ Output (FP6811-C)
  - Push-Pull RESET Output (FP6812-C)
- RoHS Compliant

Applications

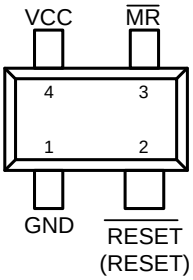
- Computer
- Battery Powered Equipment
- Microprocessor Power Supply Monitoring
- Embedded System
- Automotive

Pin Assignments

S5 Package (SOT-23-5)



C8 Package (SC-82)



Ordering Information

FP6811/12-□□□□□

- TR: Tape/Reel
- P: Green
  G: Green
- Package Type
  C8: SC-82
  SA: SOT-143
  S5: SOT-23-5
- N: Open-Drain (FP6811only)
  C: Push-Pull
- Reset Voltage
  23: 2.32V 40: 4.00V
  26: 2.63V 44: 4.38V
  29: 2.93V 46: 4.63V
  31: 3.08V
- FP6811: Active Low Reset
  FP6812: Active High Reset

Note1：Please consult Fitipower sales office or authorized distributors for availability of special reset voltages.

SA Package (SOT-143)

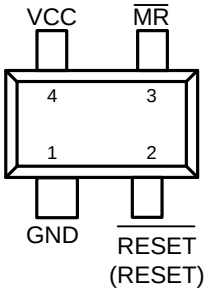


Figure 1. Pin Assignments of FP6811 / FP6812

SC-82 Marking (FP6811)

Part Number	Product Code	Part Number	Product Code
FP6811-23NC8P	**Ka**	FP6811-23CC8P	**Km**
FP6811-23NC8G	**Ka=**	FP6811-23CC8G	**Km=**
FP6811-26NC8P	**Kb**	FP6811-26CC8P	**Kn**
FP6811-26NC8G	**Kb=**	FP6811-26CC8G	**Kn=**
FP6811-29NC8P	**Kd**	FP6811-29CC8P	**Kr**
FP6811-29NC8G	**Kd=**	FP6811-29CC8G	**Kr=**
FP6811-31NC8P	**Ke**	FP6811-31CC8P	**Ks**
FP6811-31NC8G	**Ke=**	FP6811-31CC8G	**Ks=**
FP6811-40NC8P	**Kf**	FP6811-40CC8P	**Kt**
FP6811-40NC8G	**Kf=**	FP6811-40CC8G	**Kt=**
FP6811-44NC8P	**Kh**	FP6811-44CC8P	**Ku**
FP6811-44NC8G	**Kh=**	FP6811-44CC8G	**Ku=**
FP6811-46NC8P	**Ki**	FP6811-46CC8P	**Kv**
FP6811-46NC8G	**Ki=**	FP6811-46CC8G	**Kv=**

SC-82 Marking (FP6812)

Part Number	Product Code	Part Number	Product Code
FP6812-23CC8P	**Kw**	FP6812-31CC8G	**KA=**
FP6812-23CC8G	**Kw=**	FP6812-40CC8P	**KB**
FP6812-26CC8P	**Kx**	FP6812-40CC8G	**KB=**
FP6812-26CC8G	**Kx=**	FP6812-44CC8P	**KC**
FP6812-29CC8P	**Kz**	FP6812-44CC8G	**KC=**
FP6812-29CC8G	**Kz=**	FP6812-46CC8P	**KD**
FP6812-31CC8P	**KA**	FP6812-46CC8G	**KD=**

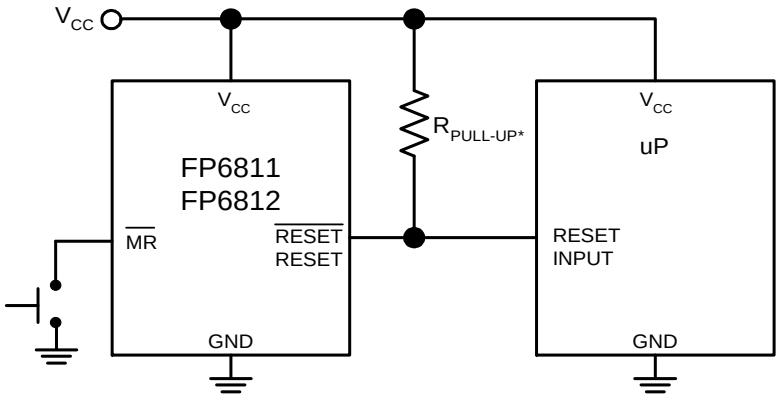
SOT-143 Marking (FP6811)

Part Number	Product Code	Part Number	Product Code
FP6811-23NSAG	**L4=**	FP6811-31CSAG	**M4=**
FP6811-23CSAG	**M1=**	FP6811-40NSAG	**L8=**
FP6811-26NSAG	**L5=**	FP6811-40CSAG	**M5=**
FP6811-26CSAG	**M2=**	FP6811-44NSAG	**L9=**
FP6811-29NSAG	**L6=**	FP6811-44CSAG	**M6=**
FP6811-29CSAG	**M3=**	FP6811-46NSAG	**L0=**
FP6811-31NSAG	**L7=**	FP6811-46CSAG	**M7=**

SOT-23-5 Marking (FP6811)

Part Number	Product Code
FP6811-29CS5G	**D3G**

Typical Application Circuit



*FP6811-N ONLY

Figure 2. Typical Application Circuit of FP6811/FP6812

Functional Pin Description

Pin Name	Pin Function
GND	Ground.
$\overline{\text{RESET}}$ (FP6811)	$\overline{\text{RESET}}$ Output remains low while V_{CC} is below the reset threshold or while $\overline{\text{MR}}$ is held low, and for at least 140ms after VCC rises above the reset threshold.
RESET (FP6812)	RESET Output remains high while V_{CC} is below the reset threshold or while $\overline{\text{MR}}$ is held low, and for at least 140ms after VCC rises above the reset threshold.
$\overline{\text{MR}}$	Manual Reset Input. Drive low to force a reset. Reset remains active as long as $\overline{\text{MR}}$ is low and for the reset timeout period after $\overline{\text{MR}}$ is released. $\overline{\text{MR}}$ has an internal 63kΩ pull up resistor to VCC.
V_{cc}	Supply Voltage.

Block Diagram

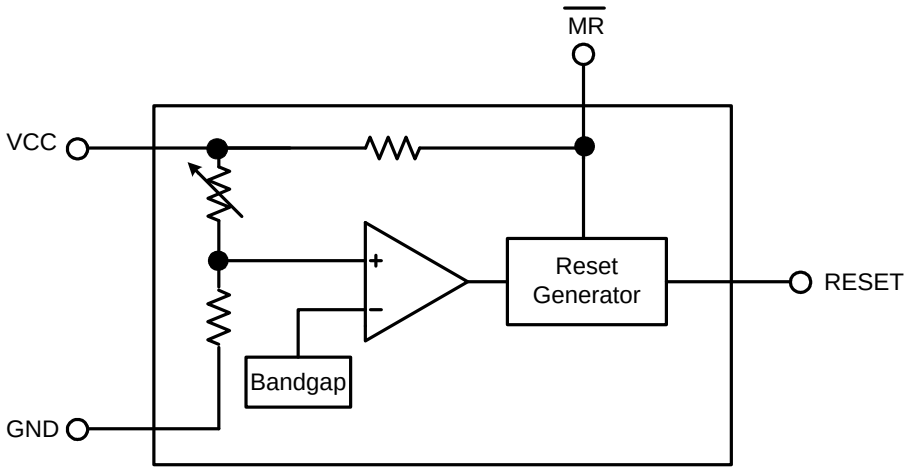


Figure 3. Block Diagram of FP6811/FP6812

Absolute Maximum Ratings

- Supply Voltage (VCC to GND) ---------- -0.3V to +6V
- RESET, $\overline{\text{RESET}}$ Voltage (Push-Pull) ---------- -0.3 to (Vcc+0.3V)
- $\overline{\text{RESET}}$ Voltage (Open Drain) ---------- -0.3V to (Vcc+0.3V)
- Input Current, V_{CC} ---------- 20mA
- Output Current, RESET, $\overline{\text{RESET}}$ ---------- 20mA
- Rate of Rise (V_{CC}) ---------- 100V/μs
- Power Dissipation @T_A=25°C, (P_D)
  - SOT-23-5 ---------- +0.4W
  - SC-82 ---------- +0.2W
  - SOT-143 ---------- +0.285W
- Package Thermal Resistance, (θ_{JA})
  - SOT-23-5 ---------- +250°C/W
  - SC-82 ---------- +500°C/W
  - SOT-143 ---------- +350°C/W
- Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec) ---------- +260°C

Note 2：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (V_{CC} to GND) ---------- +1.0V to +5.5V
- Operation Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(V_{CC}=full range, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
VCC Range	V_{CC}		1.0		5.5	V
Supply Current	I_{CC}	V_{CC}<5.5V, FP68__-46/44/40		3		µA
		V_{CC}<3.6V, FP68__-23/26/29/31		3		
Reset Threshold	V_{TH}	FP6811-46/ FP6812-46	4.54	4.63	4.72	V
		FP6811-44/ FP6812-44	4.29	4.38	4.47	
		FP6811-40/ FP6812-40	3.92	4.00	4.08	
		FP6811-31/ FP6812-31	3.02	3.08	3.14	
		FP6811-29/ FP6812-29	2.87	2.93	2.99	
		FP6811-26/ FP6812-26	2.58	2.63	2.68	
		FP6811-23/ FP6812-23	2.27	2.32	2.37	
Reset Threshold T.C. (Note3)				30		ppm/°C
$\overline{MR}$ Input Threshold	V_{IH}	V_{CC} > $V_{TH(MAX)}$, V_{CC}≧3V	2.3			V
	V_{IL}				0.8	
	V_{IH}	V_{CC} > $V_{TH(MAX)}$, V_{CC}<3V	0.7V_{CC}			
	V_{IL}				0.25V_{CC}	
$\overline{MR}$ Glitch Immunity (Note3)				100		ns
VCC to Reset Delay (Note3)		V_{CC}=V_{TH} to (Vth-100mV)		20		µs
Reset Active Timeout Period	T_{RP}		140	240	560	ms
$\overline{RESET}$ Output Voltage Low (Push-Pull active low and Open-Drain active low, FP6811)	V_{OL}	V_{CC}=V_{TH} min, I_{SINK}=1.2mA, FP6811-23/26/29/31			0.3	V
		V_{CC}=V_{TH} min, I_{SINK}=3.2mA, FP6811-44/46			0.4	
		V_{CC}>1.0V, I_{SINK}=50µA			0.3	
RESET Output Voltage Low (push-pull active high, FP6812)	V_{OL}	V_{CC}=V_{TH} max, I_{SINK}=1.2mA, FP6811-23/26/29/31			0.3	V
		V_{CC}=V_{TH} max, I_{SINK}=3.2mA, FP6811-44/46			0.4	V
$\overline{RESET}$ Output Voltage High (push-pull active low, FP6811)	V_{OH}	V_{CC}>V_{TH} max, I_{SOURCE}=500µA, FP6811-23/26/29/31	0.8Vcc			V
		V_{CC}>V_{TH} max, I_{SOURCE}=800µA, FP6811-44/46	Vcc-1.5			V
RESET Output Voltage High (push-pull active high, FP6812)	V_{OH}	1.8V<V_{CC}<V_{TH} min, I_{SOURCE}=150µA	0.8Vcc			V
$\overline{RESET}$ Open-Drain Output Leakage Current (FP6811-N)		V_{CC}>V_{TH}, RESET de-asserted			1	µA

Note 3：The specification is guaranteed by design, not production tested.

Typical Performance Curves

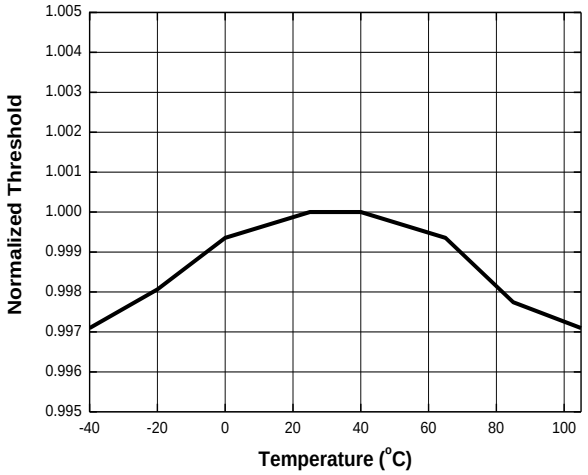


Figure 4. Normalized Reset Threshold vs. Temperature

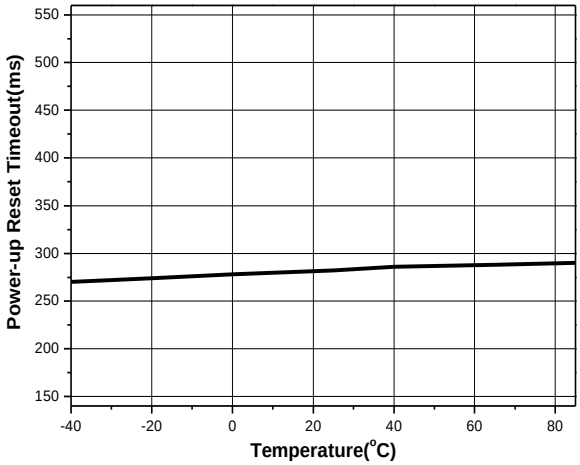


Figure 5. Power-up Timeout vs. Temperature

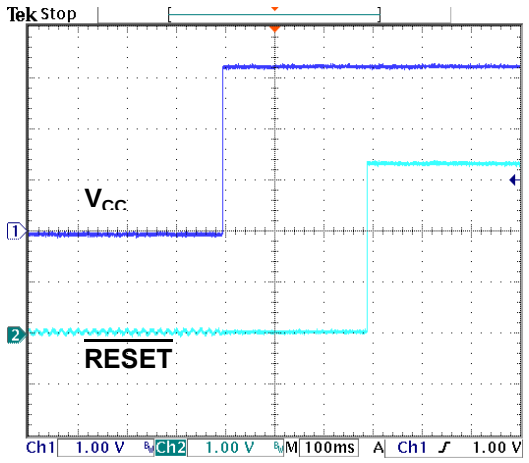


Figure 6. Power-Up $\overline{\text{RESET}}$ Timeout Waveforms;

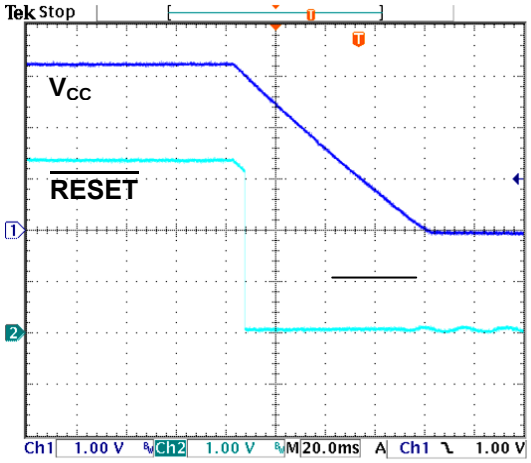


Figure 7. Power-Down $\overline{\text{RESET}}$ Delay Waveforms;

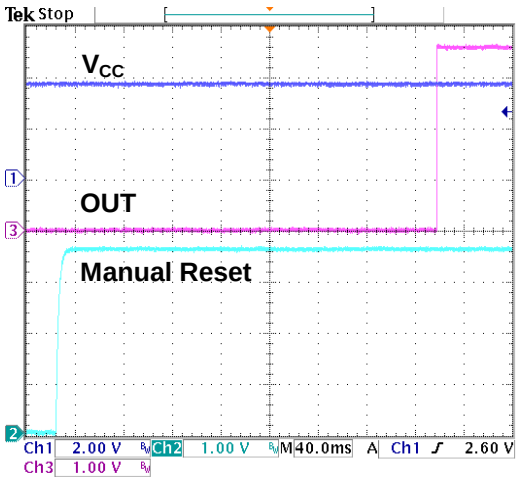


Figure 8. Manual Reset Voltage On Waveform for $-V_{TH}$=3.1V

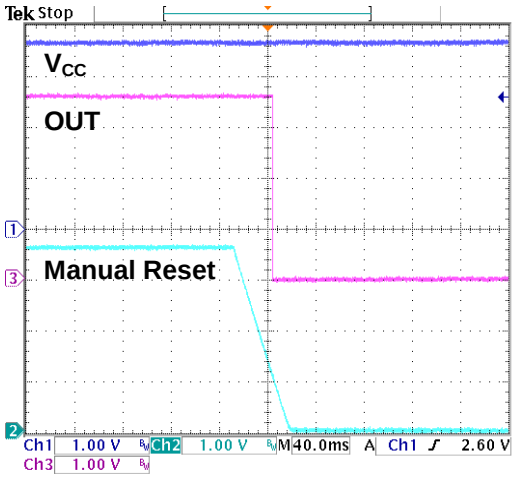


Figure 9. Manual Reset Voltage Off Waveform for $-V_{TH}$=3.1V

Typical Performance Curves (Continued)

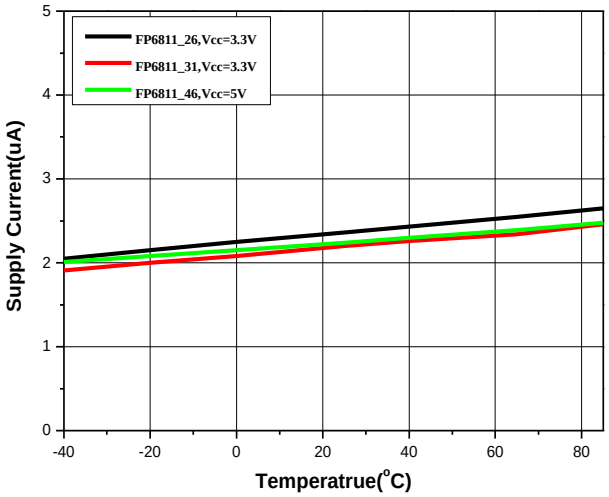


Figure 10. Supply Current vs. Temperature

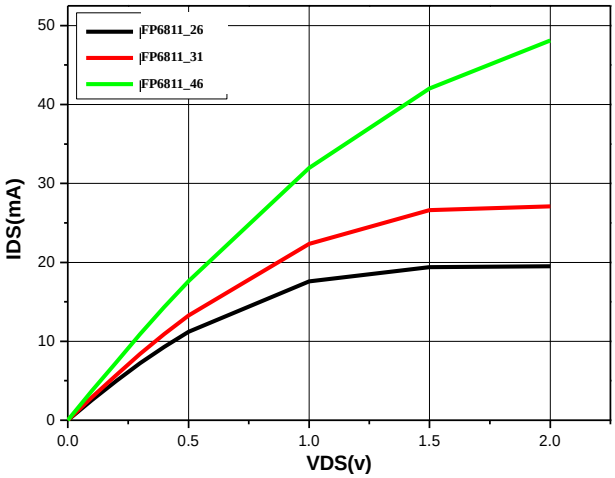


Figure 11. Output Sinking Capability

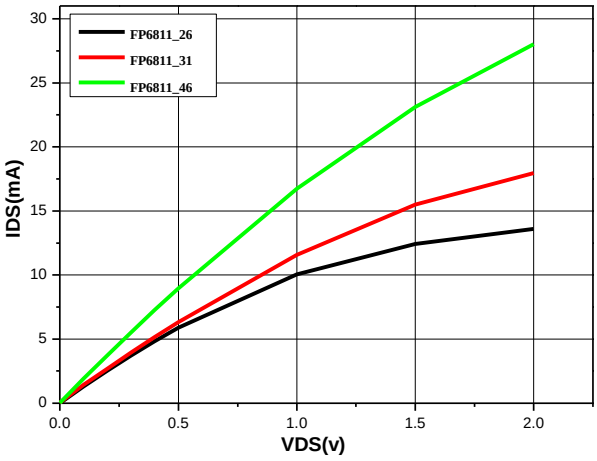


Figure 12. Output Sourcing Capability

Application Information

The FP6811/FP6812 are supervisory circuits, monitoring critical voltages and asserting reset signal to the subsequent devices. The reset signal can start the microprocessor in a known state, avoiding code-execution errors during power-up, power-down or brownout conditions. $\overline{\text{RESET}}$ (RESET) is guaranteed to be a logic low (high) for $V_{TH}>V_{CC}>0.9V$. Once V_{CC} exceeds the reset threshold, an internal timer will keep $\overline{\text{RESET}}$(RESET) low (high) for the reset timeout. After this period, $\overline{\text{RESET}}$(RESET) will go high (low). If V_{CC} falls below the reset threshold, $\overline{\text{RESET}}$(RESET) will go low (high) immediately.

Whenever V_{CC} drops below V_{TH}, the internal timer resets to zero and $\overline{\text{RESET}}$(RESET) goes low (high). The internal timer keeps activated only when $V_{CC}>V_{TH}$, and $\overline{\text{RESET}}$(RESET) remains low (high) for the reset timeout interval.

Benefits of Highly Accurate Reset Threshold

Most microprocessor supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when supply is 10% below nominal. In other words, the reset is guaranteed to assert after the power supply falls out of regulation, but keeps inactive even when power is at the minimum specified operating voltage of the system ICs.

Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator or external logic circuitry to initiate a reset. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low, and for the Reset Active Timeout Period (T_{RP}) after $\overline{\text{MR}}$ returns high. This input has an internal 63kΩ pull-up resistor, so it can be left open if it is not used. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from $\overline{\text{MR}}$ to ground provides additional noise immunity.

Negative-Going V_{CC} Transients

In addition to issuing a reset to microprocessor during power-up, power-down and brownout conditions, FP6811/FP6812 are relatively immune to short-duration negative-going V_{CC} transients (glitches). Figure 13 shows typical transient duration vs. reset comparator overdrive, for which the FP6811/ FP6812 do not generate a reset signal. The graph was generated by using a negative-going pulse applied to V_{CC}, as shown in Figure 14, starting 0.5V above the actual reset threshold and ending below it by the magnitude indication (reset comparator overdrive). As the reset comparator overdrive increases, the maximum allowable pulse width decreases. A typical 0.1µF bypass capacitor mounted as close as possible to the VCC pin provides additional transient immunity.

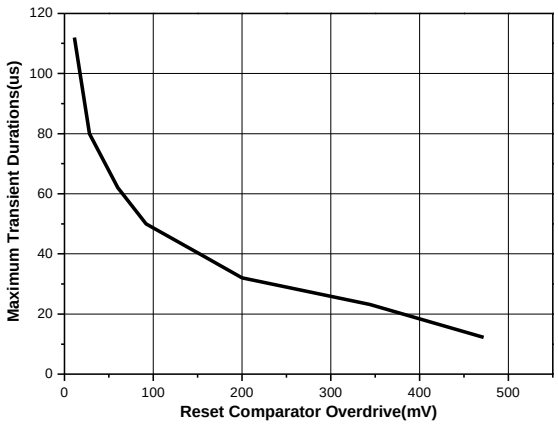


Figure 13. Maximum Transient Durations Without Causing a Reset Pulse vs. Reset Comparator Overdrive

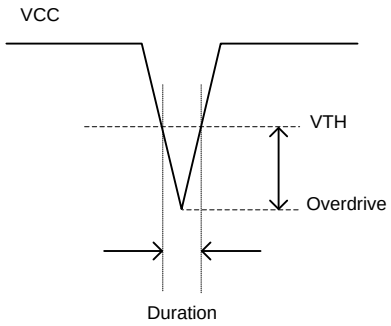


Figure 14. The VCC with Negative Going Transients

Application Information (Continued)

Ensuring a Valid Reset Output Down to V_{CC}=0

When V_{CC} falls below 1V and then the FP6811 no longer sinks current, it will become an open circuit. Therefore, high-impedance CMOS logic inputs connected to RESET can drift to undetermined voltages. This presents no problem in most applications for microprocessor's inoperative condition with V_{CC} below 1V. However, in applications where RESET must be valid down to 0V, adding a pull-down resistor to RESET causes stray leakage currents to flow to ground, providing some impedance between RESET and ground (Figure 15). R1 is recommended around 100kΩ.

A 100kΩ pull-up resistor to V_{CC} is also recommended for FP6811 if RESET is required to remain valid for V_{CC}<1V.

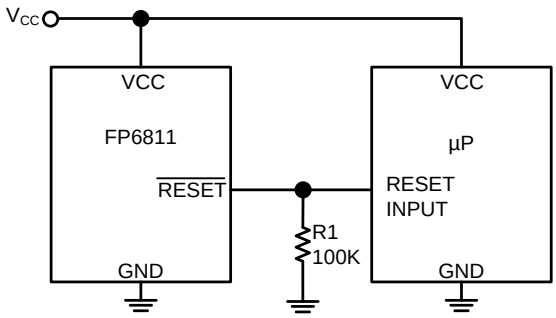


Figure 15. $\overline{\text{RESET}}$ Valid to V_{CC}=0V Circuit

Interfacing to µPs with Bidirectional Reset Pins

Since the RESET output of FP6811N is open drain, this device interfaces easily with µP which has bidirectional reset pins. Connecting the FP6809N's RESET output directly to the microcontroller's RESET pin with a single pull-up resistor allows either device to assert reset (Figure 16).

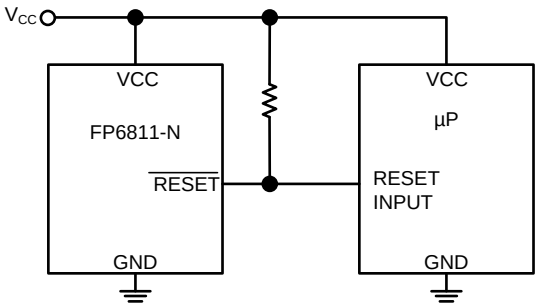
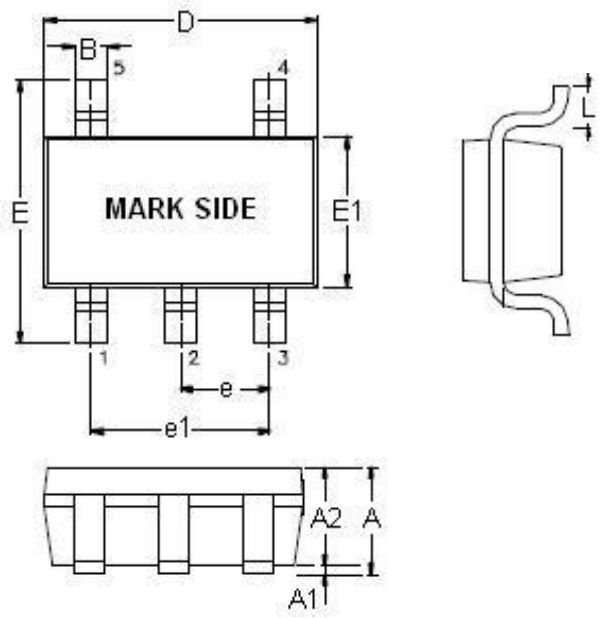


Figure 16. Interfacing to uPs with Bidirectional Reset I/O

Outline Information

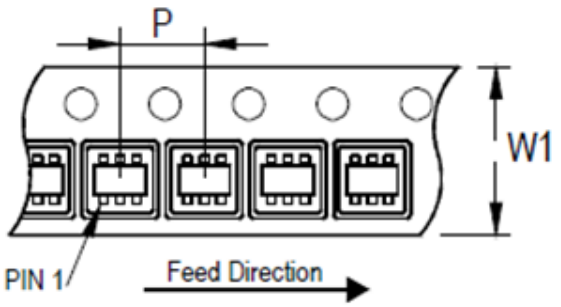
SOT-23-5 Package (Unit: mm)

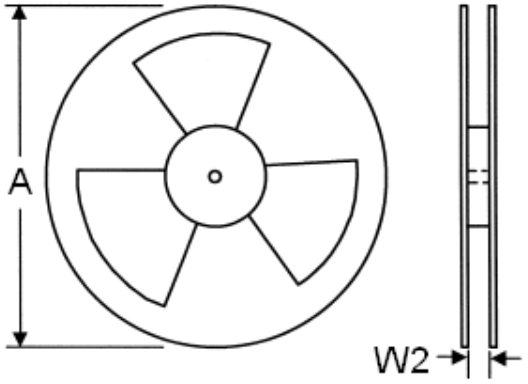


SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60

Note：Followed From JEDEC MO-178-C.

Carrier Dimensions

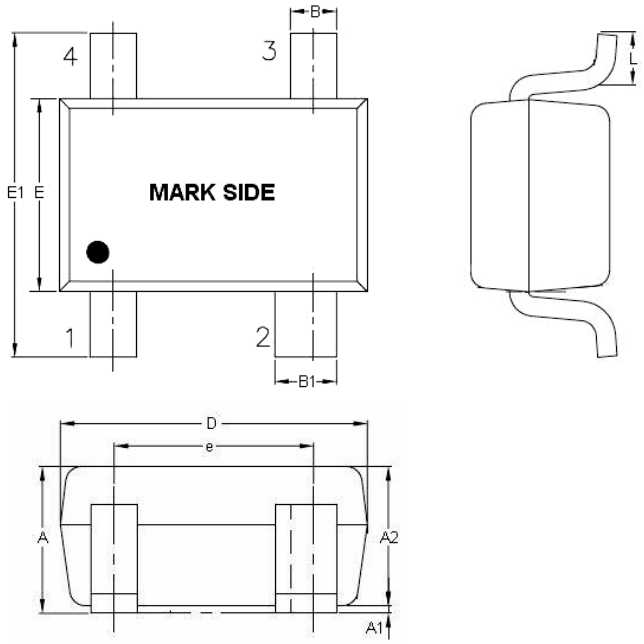




Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

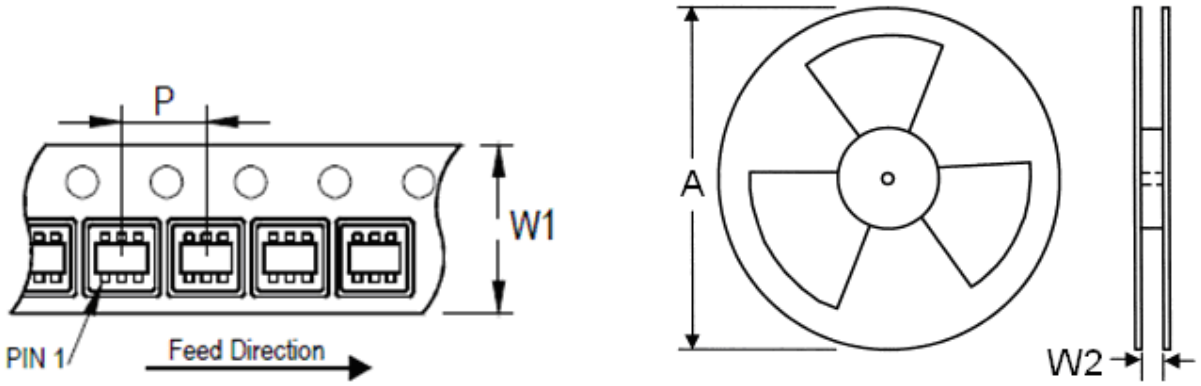
Outline Information (Continued)

SC-82 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.80	1.00
B	0.25	0.40
B1	0.35	0.50
D	1.80	2.20
E	1.15	1.35
E1	1.80	2.40
e	1.20	1.40
L	0.25	0.45

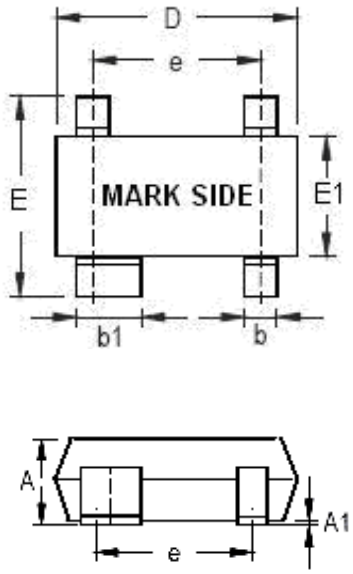
Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

Outline Information (Continued)

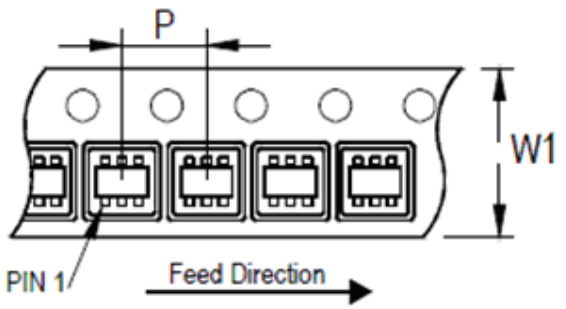
SOT-143 Package (Unit: mm)

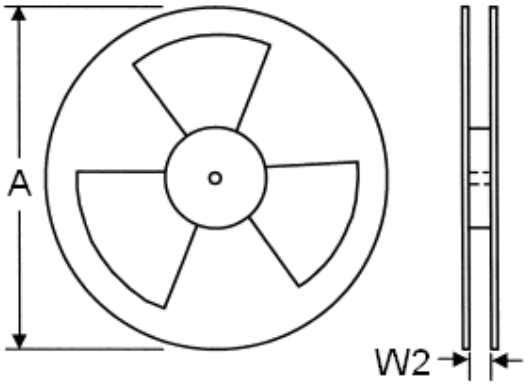


SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.80	1.20
A1	0.00	0.15
b	0.30	0.52
b1	0.76	0.92
C	0.08	0.20
D	2.80	3.04
E	2.10	2.64
E1	1.20	1.40
e	1.85	1.95
L	0.40	0.60

Note：Followed From JEDEC TO-261-C

Carrier Dimensions





Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

Life Support Policy
Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.