

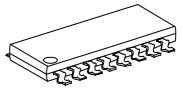
PHASE SHIFT DUAL PWM IC WITH SCP/OVP FUNCTION

GENERAL DESCRIPTION

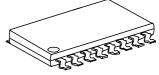
The **FP5352**, an 1-chip composed of dual channel phase shift 180° totem-pole output stage pulse-width-modulation control circuits with two independent error amplifiers for step-down converter application, the inverting input of amplifier connects to a 1.0V precision reference regulator, power down under-voltage lockout circuit (UVLO), short circuit and over voltage shutdown and auto-restart protection circuit (SCP/OVP) and dead-time control circuit (DTC), applied to offer the space and low cost in many applications of PC peripherals .

FEATURES

- Internal EA Bias Reference Voltage: 1.0V
- Reference Voltage Precision: 2%
- Totem-pole Output for MOS Driving
- Dual PWM Output Phase Shift 180°
- Wide operating voltage range: 3.6~25V
- · Variable Dead-time Control (DTC)
- · Power Down Under-voltage Lock-out (UVLO)
- SC/OV Protection (SCP/OVP)
- Protection Shutdown and Auto-restart
- Shutdown Mode (ON/OFF)
- Programming Oscillation Frequency
- Package: SOP16/SSOP16



SOP16



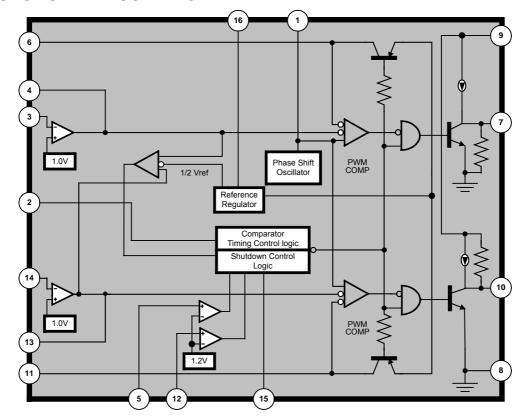
SSOP 16

TYPICAL APPLICATION

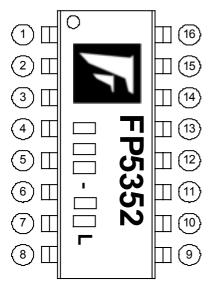
- PC Peripherals
- Networking products
- Royer CCFL Inverter
- Portable products



FUNCTIONAL BLOCK DIAGRAM



MARK VIEW



Website: http://www.feeling-tech.com.tw

PIN DESCRIPTION

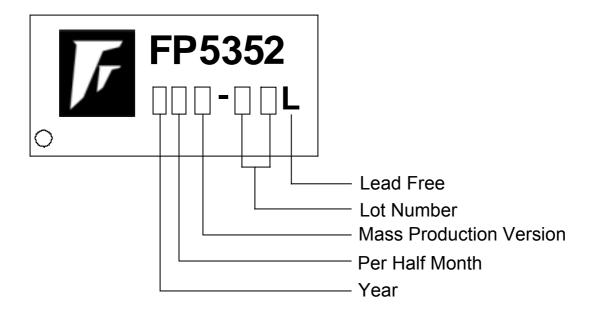
NAME	NO.	STATUS	DESCRIPTION
RT	1	I	Connect a Resistor for Oscillator
CP	2	- 1	Shutdown re-start control timer
FB1	3	- 1	Error Amplifier 1 Non-inverting Input
COMP1	4	0	Error Amplifier 1 Feedback Output
OVP1	5	- 1	CH1 Over-voltage Detection Input
DTC1	6	I	CH1 Dead-Time Control Input
OUT1	7	0	CH1 Totem-pole Output
GND	8	Р	IC Ground/Power Ground
PVCC	9	Р	IC Totem-pole Power Supply
OUT2	10	0	CH2 Totem-pole Output
DTC2	11	- 1	CH2 Dead-Time Control Input
OVP2	12	- 1	CH2 Over-voltage Detection Input
COMP2	13	0	Error Amplifier 2 Feedback Output
FB2	14	I	Error Amplifier 2 Non-inverting Input
ENB	15	I	ON/OFF Control Input
VCC	16	Р	IC Power Supply



ORDER INFORMATION

Part Number	Operating Temperature	Package	Description
FP5352D-LF	-20°C ~ +85°C	SOP16	Tube
FP5352DR-LF	-20°C ~ +85°C	SOP16	Tape & Reel
FP5352R-LF	-20°C ~ +85°C	SSOP16	Tube
FP5352RR-LF	-20°C ~ +85°C	SSOP16	Tape & Reel

IC DATE CODE DISTINGUISH



FOR EXAMPLE:

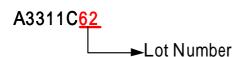
January A (Front Half Month), B (Last Half Month)

February C, D

March E, F -----And so on

Lot Number is the last two numbers

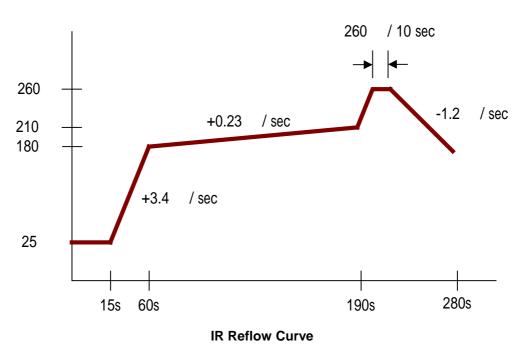
For Example:





ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Vcc)	+20	V
Output Current (Io)	+15	0mA
Maximum Junction Temperature (T _j)	+15	0°C
Thermal Resistance Junction to Ambient SOP16 package	150	°C /W
SSOP16 package	220	°C /W
Power Dissipation		
SOP16 package Ta=25 Ta=70	830 530	
SSOP16 package Ta=25 Ta=70	570 360	
Operating Temperature Range	-20°C	85°C
Storage Temperature Range	-65°C	150°C
Lead Temperature (soldering, 10 sec)	+26	0°C





DC ELECTRICAL CHARACTERISTICS

Electrical characteristics over recommended operating free-air temperature range, V_{CC} =6V, f=200kHz (unless otherwise noted)

Reference section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	V_{REF}	COMP connected to FB	0.98	1.0	1.2	V
Input voltage regulation	V_{REF}/V_{REF}	Vcc=3.6V 20V		2	12.5	mV
Output voltage change with		T _A =-20 to 25		-0.1	±1	%
Temperature		T _A =25 to 85		-0.2	±1	/0

Under voltage lockout section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Upper threshold voltage(Vcc)	V_{UPPER}			3.2		V
Lower threshold voltage(Vcc)	V_{LOW}	T _A =25		3.0		V
Hysteresis (Vcc)	V_{HYS}		100	200		mV

Short-circuit protection control section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCP standby voltage	V_{SB}	Vcomp <1.5V		0.5		V
SCP threshold voltage	V_{TH}	Vcomp >1.5V		1.0		V
SCP re-start charge current	I _{RSC}	Vcomp >1.5V		25		μА
SCP re-start / hold time	T _{RS} /T _{HOLD}	Vcomp >1.5V		1/35		-
SCP comparator 1 threshold voltage	V _{COMP(TH)}			1.5		V

Note1:Function Diagram figure 25

Oscillator section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	f	R _T =100K		150		KHz
Frequency change with voltage	f/ V	V _{CC} =3.6V to 20V		0.2		%
Frequency change with Temperature	f/ T	T _A =-20 to 25		-0.4	±2	%
Voltage at RT	V_{RT}			1		V

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DC ELECTRICAL CHARACTERISTICS (Cont.)

Dead-time control section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current (DTC)	I _{BIAS}				1	μΑ
Input threshold voltage	V	Zero duty cycle		2.0	2.20	W
Imput tilleshold voltage	V _{TH}	Maximum duty cycle	1.2	1.35		v

Error –amplifier section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage	V_{IN}	$V_{CC} = 3.6V \text{ to } 20V$	0		1.5	V
Input bias current	I _{BIAS}			160	500	nA
Open-loop voltage amplification	A _{VO}		70	80		dB
Unity-gain bandwidth	BW			1.5		MH_Z
Positive output voltage swing	V_{POS}		Vref-0.3			V
Negative output voltage swing	V_{NEG}				1	V
Output (sink) current	I_{SINK}	V_{ID} =-0.1V, V_{O} =1.25V	2	3		mA
Output (source) current	I _{SOURCE}	V_{ID} =0.1V, V_{O} =1.25V	-100	-140		μA

Output section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vout Low Voltage	V _{OL}	I _{SINK} =20mA		0.15	0.2	V
	VOL	I _{SINK} =130mA Vcc=15V		1.7	2.0	V
Vout High Voltage	V _{OH}	I _{SOURCE} =20mA	4.0	4.5		V
Vout High Voltage	VOH	I _{SOURCE} =130mA Vcc=15V	12.8	13.4		V
Output Pull High Resistance						K
Rise Time	t _R	$T_J=25$, $C_L=1nF$		50	100	nS
Fall Time	t_{F}	$T_J=25$, $C_L=1nF$		50	100	nS

PWM comparator section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input threshold voltage		Zero duty cycle		2.0	2.20	\/
Input threshold voltage	V _{TH}	Maximum duty cycle	1.2	1.35		V

Over Voltage Protect section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT

Total device

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standby supply current	I _{STANDBY}	Off-state				mA
Average supply current	I _{AVE}	R _T =100K				mA

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DETAILED DESCRIPTION

Voltage reference

A 2.5V reference regulator supplies FP5352 internal circuits and uses the resistive dividers to provide a 1.0V precision reference voltage on the non-inverting terminal of error amplifier and SCP comparator 1.0V threshold voltage.

Error amplifier

The error amplifier compares the feedback voltage from dc-dc converter output to the 1.0V reference and generates the error signal for the PWM comparator. The relation between VI(FB) and FP5352 error amplifier pins are shown below (see Figure 19).

The converter output voltage explains such as below expression:

$$VI(FB) = \left(1 + \frac{R1}{R2}\right) * V_{REF}$$

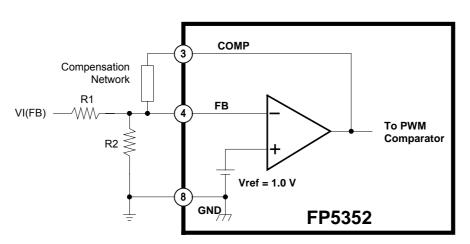


Figure 19. Error Amplifier with Converter Feedback Resistors

Note:

It is necessary to check the converter total open loop gain and phase shift from Bode plot before compensation network adjustment. Finally, let the system works stability.



Oscillator/PWM Comparator

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The oscillator frequency (fosc) can be decided from 20KHz to 1.5MHz by the resistor connected to R_T pin. The oscillator frequency can be determined by the follow formula or graph shown in Figure 5.

$$f = \frac{30000}{R_T}$$
 (KHz), and ${\rm R_T}$ value cannot be used below 20K Ω

The internal oscillator output is a triangular waveform and its minimum voltage level is approximately 0.7 V and maximum level approximately 1.3V (see Fig 20). The PWM comparator compares the triangular waveform with the signals from output voltage of error-amplifier and the DTC voltage, then PWM comparator output controls the output stage of totem-pole transistors pair off or on whenever the triangular wave is greater than the both input signals or less.

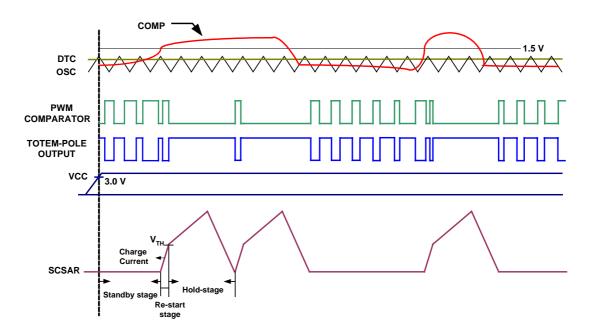


Figure 20. PWM Timing Diagram



Dead-time control (DTC)

DTC main function is a limitation of PWM duty cycle less than 100%. The source current of R_T is same as dead-time current I_{DT} at DTC pin. There is a resistor R_{DT} connecting between DTC and GND and generating a bias voltage V_{DT} that compares with the output waveform of oscillator in the PWM comparator. The PWM duty cycle begins 0% when V_{DT} sets at 0.7 V or less, and then V_{DT} sets at 1.3 V or greater and PWM duty cycle reaches 100%. Engineer can choose a resistor R_{DT} for a specific limitation of PWM duty cycle D.

According to the following formula, we can choose a RDT for a maximum duty cycle.

$$R_{DT} = (R_T + 1250) * (0.6 * D + 0.7)$$

For example:

R_T is 33K for oscillator frequency, and we assume the maximum duty cycle is 75%.

$$R_{DT} = (33K+1250)*(0.6*0.75+0.7) = 39.38K$$

When using a resistor R_{DT} is 39.38K , the limitation of PWM duty cycle is 75%.

A capacitor (C_{DT}), connecting with the resistor R_{DT} as shown in Figure 21, is a soft-start function when power on. The soft-start time formula is shown as below:

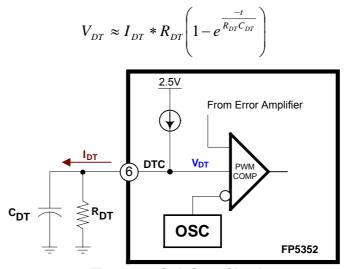


Figure 21. Soft-Start Circuit

Note:

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 C_{DT} is discharged by internal circuit every time when UVLO or SCP becomes active.



Under voltage lock-out (UVLO) protection

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When the power supply turns off, the output of **FP5352** also turns off and resets the SCP latch whenever the supply voltage drops under the UVLO off threshold voltage. It is a simple protection function when the supply voltage can not maintain at a stable operating condition. The UVLO hysteresis voltage avoids an internal false trigger whenever power noise or spike.

Short-circuit shutdown and auto re-start protection (SCSAR)

FP5352 includes short-circuit shutdown and auto re-start protection function (see Figure 22), which turns the Power MOS off to prevent damage when the converter output is over loading or short circuit.

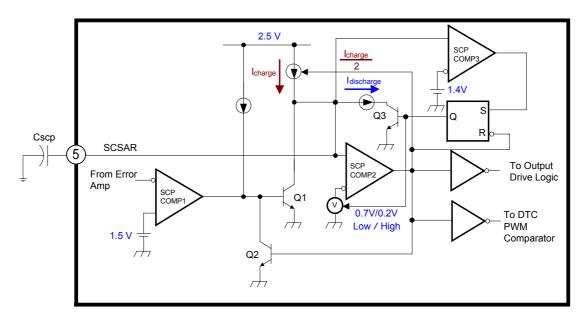


Figure 22. SCSAR Protection Circuit

Generally, error amplifier output voltage is lower than 1.5V, and SCP comparator 1 output keeps a high state and Q1 is turn-on, C_{SCP} cannot be charged. When short circuit occurs, the COMP pin of error-amplifier would rise more than 1.5V, SCP comparator 1 output changes to low state and C_{SCP} is charged by I_{CHARGE} current. The SC function of **FP5352** is release because short circuit is removed before Q2 active and SCP comparator 2 is latch. When C_{SCP} is charged until a 0.7V threshold voltage and SCP comparator 2 output changes to high state and Q2 is turn-on to keep Q1 off in latch mode. Meanwhile, the source current of C_{SCP} would change half of original current for the first shutdown phase, **FP5352** output is turn-off and DTC pin is pull-low. When C_{SCP} voltage is greater than 1.4V of SCP comparator 3, the output of S-R Latch would turn on Q3 and change SCP comparator 2 from 0.7V to 0.2V, when SCP comparator 3 is active, C_{SCP} is discharged until SCP comparator 2 is release the latch state,



output of FP5352 is active and DTC pin is working in soft-start state or limitation of duty cycle.

 C_{SCP} discharging time from 1.4V to 0.2V is the second shutdown phase which finishes and **FP5352** would be release shutdown state and re-start the normal operation. Figure 23 is a relation description about SCSAR pin and the other pins of **FP5352**.

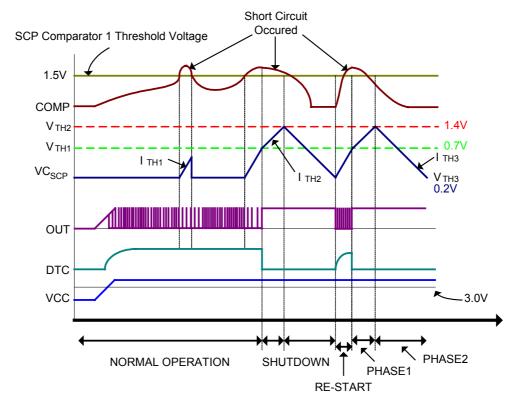


Figure 23. Shutdown and Re-start waveform

The formulas are shown below for shutdown and re-start time calculation:

AUTO RE-START time equation:

$$t_{\mathit{RE-START}} = \frac{V_{\mathit{TH1}} * C_{\mathit{SCP}}}{I_{\mathit{TH1}}}$$

SHUTDOWN time equation:

$$t_{\textit{SHUTDOWN}} = t_{\textit{PHASE1}} + t_{\textit{PHASE2}} = \frac{\left(V_{\textit{TH2}} - V_{\textit{TH1}}\right) * C_{\textit{SCP}}}{I_{\textit{TH2}}} + \frac{\left(V_{\textit{TH2}} - V_{\textit{TH3}}\right) * C_{\textit{SCP}}}{I_{\textit{TH3}}}$$



Output transistors

The output of the FP5352 is a totem-pole transistor pair, which supplies source and sink current capacity for driving the external MOSFET directly, a basic drive method is shown as figure 24.

When PWM operation frequency is different, the both of on and off time of MOSFET also are different.

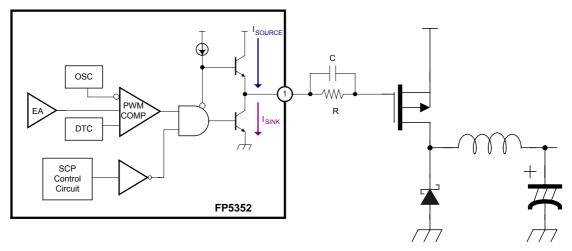


Figure 24. MOSFET Output Driving Cricuit

Note:

It is very important to choose a suitable MOSFET for high frequency operation. The larger capacitor between gate and source of MOSFET has more switching loss under the same condition as high frequency operation, supply voltage and driving current.



APPLICATION NOTE

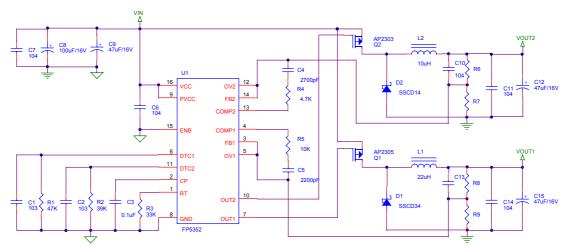


Figure 1 FP5352 2-channel Buck Regulators Application Circuits

Note

The R1-C1 and R2-C2 are dead-time limit and soft-start timing control.

The C3 is OC/OV/SC shutdown and re-start timing capacitor.

The R3 is adjustable for oscillation frequency.

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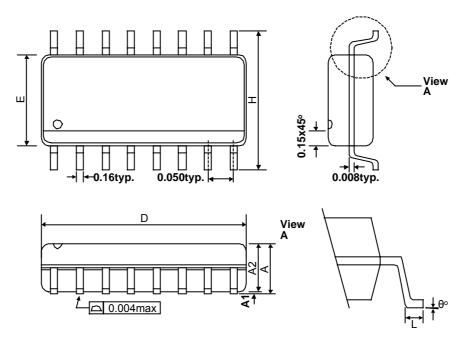
The R4-C4 and R5-C5 are type 3 compensation circuits for error amplifier 1/2.

The R6-R7 and R8-R9 with 1.0V reference are used for VOUT1/2 voltage.

The OV set point is higher than R6-R7/R8-R9 resistor ratio with 1.2V.



PACKAGE OUTLINE SOP-16L



SYMBOLS	MIN	MAX
Α	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
Н	0.228	0.244
L	0.016	0.050
0	0	8

UNIT:INCH

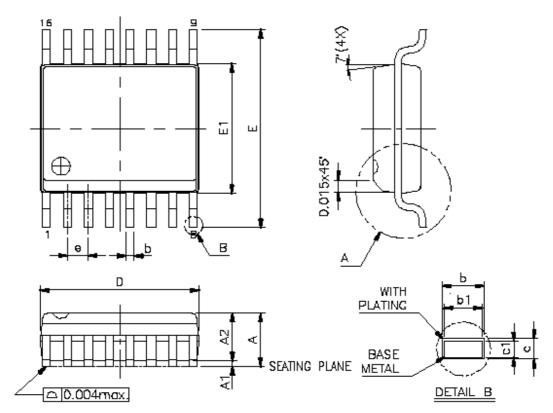
NOTE:

1.JEDEC OUTLINE:MS-012 AC

- 2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH,PROTRUSIONS OR GATE BURRS.MOLD FLASH,PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.0.06in) PER SIDE
- 3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH,OR PROTRUSIONS.
 4.INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.0.10in) PER SIDE.



SSOP-16L



SYMBOLS	MIN.	MAX.	
Α	0.053	0.069	
A1	0.004	0.010	
A2	-	0.059	
b	0.008	0.012	
b1	0.008	0.011	
С	0.007	0.010	
c1	0.007	0.009	
D	0.189	0.197	
E	0.228	0.244	
E1	0.150	0.157	
L	0.016	0.050	
е	0.025 Basic		
0	0	8	

UNIT:INCH

NOTES:

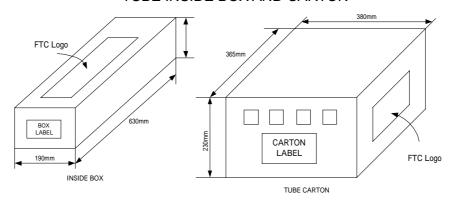
1.JEDEC OUTLINE: MO-137 AB

- 2."D",DIMENSIONS DO NOT INCLUDE MOLD FALSH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm(006in).
- 3."E",DIMENSIONS DO NOT INCLUDE MOLD FALSH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25mm(010in) PER SIDE.
- 4.DATUM PLANE CONCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

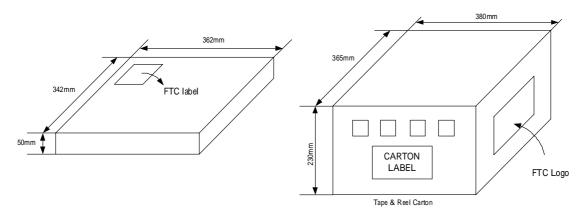


PACKING SPECIFICATIONS BOX DIMENSION

TUBE INSIDE BOX AND CARTON



TAPE AND REEL INSIDE BOX AND CARTON



PACKING QUANTITY SPECIFICATIONS

50 EA/TUBE	2500 EA / REEL
50 TUBES / INSIDE BOX	4 INSIDE BOXES / CARTON
4 INSIDE BOXES / CARTON	

LABEL SPECIFICATIONS

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TAPPING & REEL





CARTON

Feeling Technology Corp.

Product Type: FP5352DR-LF

Lot No: A3311C62

Date Code: 4Xx-XXL

Package Type:SOP-16L

Marking Type: Laser

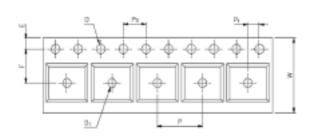
Total Q'ty: 10,000

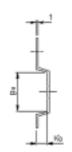
無鉛 Lead Free

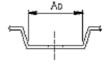
SOP16 CARRIER TAPE DIMENSIONS

APPLICATION	P ₀	P ₁	A_0	B ₀	K_0	t
SOP16	4.0±0.1	2.0±0.1	6.5±0.1	10.3±0.1	2.1±0.1	0.30±0.05

APPLICATION	W	Р	Е	F	D	D_1
SOP16	16.0±0.3	8.0±0.1	1.75±0.1	7.5±0.1	1.55 ^{+0.1}	1.5 ^{+0.25}

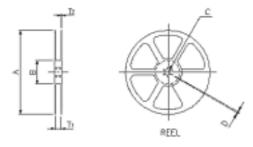






REEL DIMENISIONS

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APPLICATION	MATERIAL	Α	В	С	D	T1	T2
SOP16	PLASTIC REEL	330±3	100±2.0	13.0±0.5	2.0±0.5	16.4 +0.3 -0.2	2.5±0.5

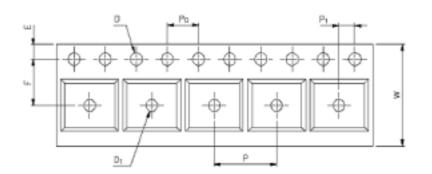
Rev0.1 July. 20, 2006 P17/FP5352



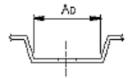
SSOP16 **CARRIER TAPE DIMENSIONS**

APPLICATION	W	Р	Е	F	D	D_1
SSOP16	12.0±0.3	8.0±0.1	1.75±0.1	5.5±0.05	1.5 ^{+0.1}	1.5 ^{+0.25}

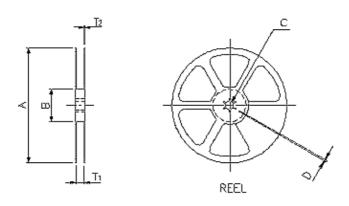
APPLICATION	P ₀	P ₁	A_0	B ₀	K ₀	t
SSOP16	4.0±0.1	2.0±0.05	6.5±0.1	10.3±0.1	2.1±0.1	0.30±0.05







REEL DIMENISIONS



APPLICATION	MATERIAL	А	В	С	D	T1	T2
SSOP16	PLASTIC REEL	330	62	12.75 ^{+0.15}	2.0±0.15	12.4	16.8

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