

Applications

- Mobile Infrastructure
- CATV / DBS
- W-LAN / ISM
- Defense / Homeland Security



SOT-89 Package

Product Features

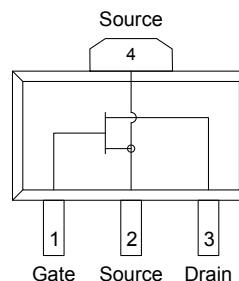
- 50 – 4000 MHz
- Low Noise Figure
- 18 dB Gain
- +36 dBm OIP3
- +18 dBm P1dB
- Single or Dual Supply Operation
- Lead-free/Green/RoHS-compliant SOT-89 Package
- MTTF > 100 years

General Description

The FH101-G is a high dynamic range FET- packaged in a low-cost surface-mount package. The combination of low noise figure and high output IP3 at the same bias point makes it ideal for receiver and transmitter applications. The device combines dependable performance with superb quality to maintain MTTF values exceeding 100 years at mounting temperatures of +85°C. The FH101-G is available the environmentally-friendly lead-free/green/RoHS-compliant SOT-89 package.

The device utilizes a high reliability GaAs MESFET technology and is targeted for applications where high linearity is required. It is well suited for various current and next generation wireless technologies such as GPRS, GSM, CDMA, and W-CDMA. In addition, the FH101-G will work for other applications within the 50 to 4000 MHz frequency range such as fixed wireless.

Product Features



Pin Configuration

Pin No.	Label
1	Gate
2, 4	Source
3	Drain

Ordering Information

Part No.	Description
FH101-G	High Dynamic Range FET

Standard T/R size = 1000 pieces on a 7" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150°C
Drain to Source Voltage	+7 V
Gate to Source Voltage	-6 V
Gate Current	4.5 mA
RF Input Power, CW, 50Ω, T=25°C	Input P1dB + 4dB

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
T _{CASE}	-40		+85	°C
T _j for >10 ⁶ hours MTTF			+160	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DS} = +5 V, V_{GS} = 0 V, Temp = +25°C, 50Ω System

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			800		MHz
Saturated Drain Current, I _{DSS}	V _{GS} =0 V		140	170	mA
Transconductance, G _m			120		mS
Pinch-off Voltage, V _P	I _{DS} =0.6 mA	-3	-1.5		V
Small-signal Gain, G _{SS}		17	18		dB
Max Stable Gain, G _{MSG}			23		dB
Output P1dB			+18		dBm
Output IP3	P _{out} = +5 dBm/tone, Δf = 10 MHz	+32	+36		dBm
Noise Figure	Γ _S = Γ _L = Γ _{OPT}		0.77		dB
Thermal Resistance, θ _{jc}	Module (junction to case)		59		°C/W

Typical Performance ⁽¹⁾

Test conditions unless otherwise noted: V_{DS} = +5V, I_{DS} = 140 mA, Temp = +25°C

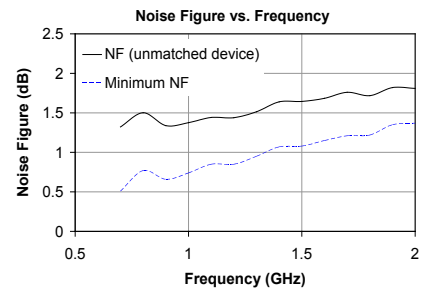
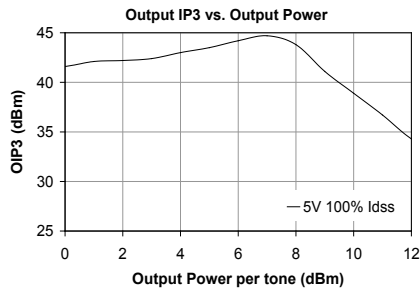
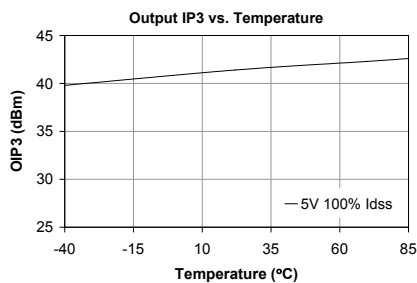
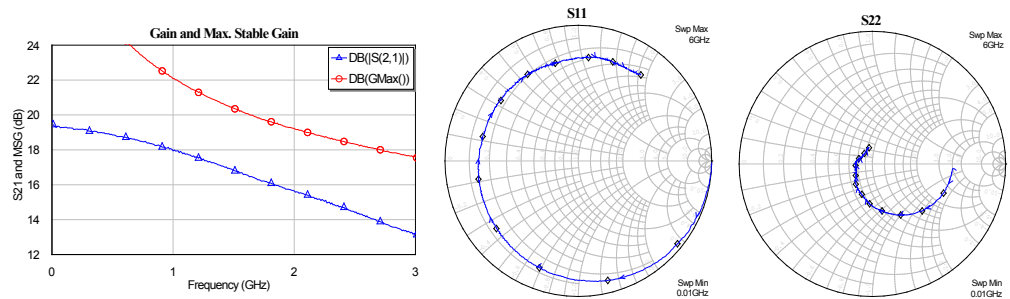
Parameter	Conditions	Typical Value			Units
Frequency		900	1960	2140	MHz
Gain		19	16.5	16.5	dB
Input Return Loss		11	20	22	dB
Output Return Loss		10	9	9	dB
Output P1dB		+18.8	+18.1	+19.1	dBm
OIP3	P _{out} = +5 dBm/tone, Δf = 10 MHz	+36	+36	+36	dBm
Noise figure		2.7	3.1	3.0	dB

Notes:

1. The device requires appropriate matching to become unconditionally stable. Parameters reflect performance in an appropriate application circuit.

Device Characterization Data

The gain for the unmatched device in 50 ohm system is shown as the trace in black color, [gain (S(2,1))]. The maximum stable gain is shown as the blue trace [Gmax]. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The impedance plots are shown from 0.05 – 6 GHz.



S-Parameters

Test Conditions: $V_D=+5$ V, $I_D=140$ mA, $T=+25^\circ\text{C}$, 50 ohm system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	0.00	-4.08	19.36	176.06	-51.05	87.96	-4.38	-3.34
250	-0.13	-19.64	19.19	164.65	-37.15	78.37	-4.52	-11.51
500	-0.34	-39.41	18.85	150.19	-31.34	66.75	-4.77	-22.43
750	-0.55	-58.33	18.47	136.21	-28.24	55.74	-5.19	-33.05
1000	-0.83	-75.93	17.95	123.24	-26.22	45.25	-5.77	-43.46
1250	-1.16	-93.29	17.47	110.92	-24.88	35.22	-6.44	-53.09
1500	-1.50	-110.36	16.82	99.18	-23.95	26.69	-7.14	-61.08
1750	-1.80	-125.64	16.21	88.19	-23.27	18.17	-7.94	-69.92
2000	-2.03	-140.92	15.65	77.53	-22.81	9.87	-8.84	-78.43
2250	-2.25	-155.64	15.05	67.15	-22.39	2.11	-9.57	-86.41
2500	-2.37	-169.80	14.42	57.62	-22.25	-4.68	-10.43	-93.92
2750	-2.55	177.26	13.74	48.11	-22.08	-11.35	-11.43	-101.88
3000	-2.62	165.93	13.18	39.86	-22.01	-17.16	-12.30	-108.95

Noise Parameters

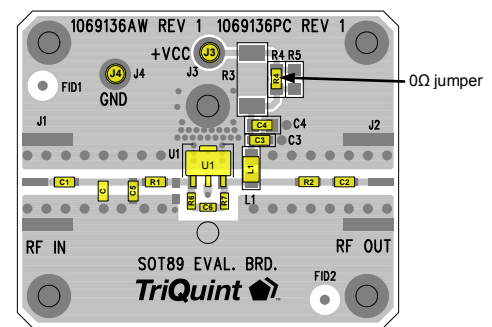
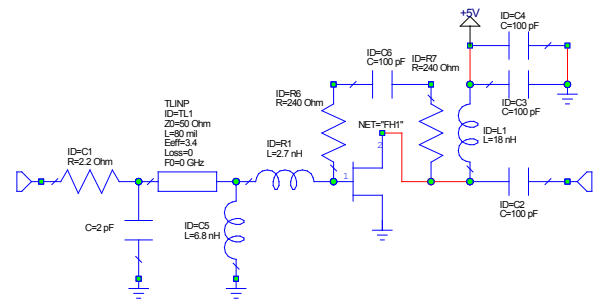
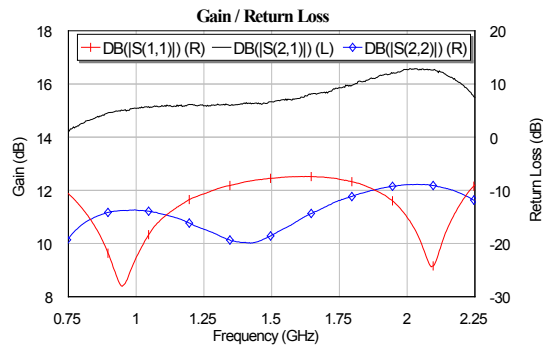
Test Conditions: $V_D=+5$ V, $I_D=140$ mA, $T=+25^\circ\text{C}$, 50 ohm system, calibrated to device leads

Freq (GHz)	NF _{min} (dB)	MagOpt (mag)	AngOpt (deg)	Rn (Ω)
700	0.51	0.574	32.8	0.403
800	0.77	0.535	37.4	0.409
900	0.66	0.508	44.1	0.379
1000	0.74	0.488	50.4	0.365
1100	0.85	0.463	56.4	0.357
1200	0.85	0.458	62.0	0.345
1300	0.95	0.446	67.3	0.335
1400	1.07	0.450	73.3	0.323

Reference Design – 800-2200 MHz, 15 dB Gain

Test Conditions: $V_{DS}=+5\text{ V}$, $I_{DS}=140\text{ mA}$, $T=+25^{\circ}\text{C}$

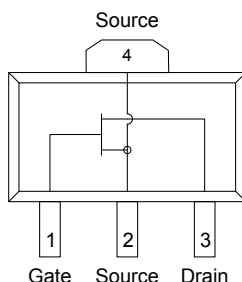
Parameter	Typical Value			Units
Frequency	900	1900	2140	MHz
Gain	14.9	16.3	16.4	dB
Input Return Loss	22	10	18	dB
Output Return Loss	14	9.7	9.6	dB
Output P1dB	+19.1	+19.4	+19.1	dBm
OIP3	+35.7	+37.0	+36.0	dBm
Noise figure	2.4	2.6	2.8	dB



Notes:

1. Gain for the circuit can be adjusted slightly with the modification of the feedback resistance.
2. A DC blocking capacitor needs to be placed to the left of C1 if DC is present at the input of the circuit.

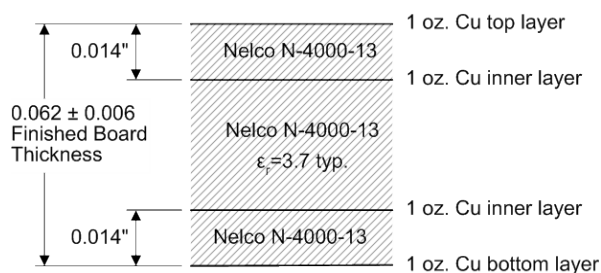
Pin Configuration and Description



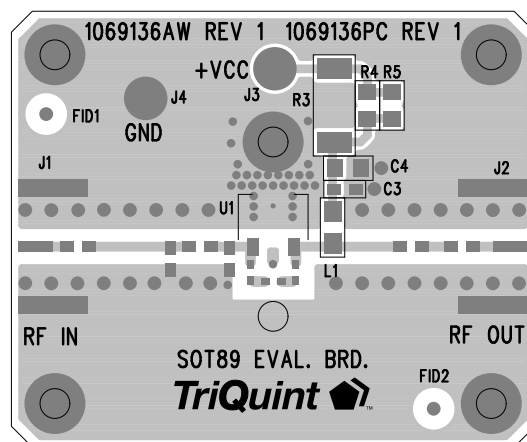
Pin No.	Label	Description
1	Gate	RF Input. Requires DC blocking capacitor.
3	Drain	RF Output/Bias. Supply DC bias via an inductor of appropriate value for frequency of operation.
2, 4	Source	RF/DC ground. Use recommended via pattern for optimum source inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

TriQuint PCB 1069136 Material and Stack-up



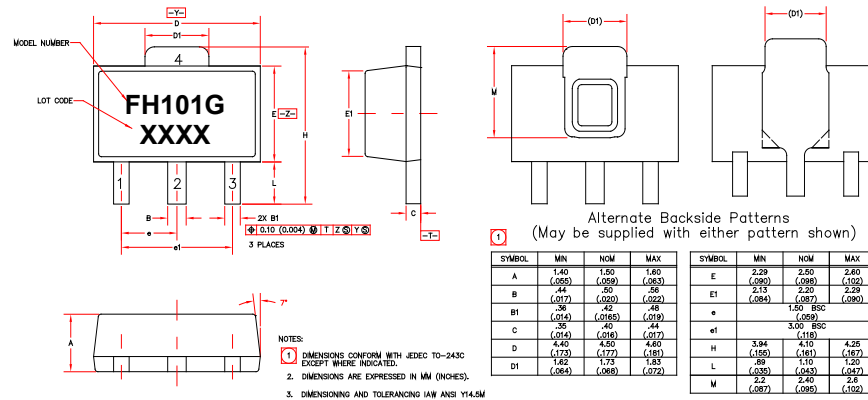
50 Ohm Line Width: 28 mils



Package Marking and Dimensions

Marking: Part number – FH101G

Lot code – AaXXXX



Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 1B
Value: Passes ≥ 500 V to < 1000 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000 V to < 2000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($\text{C}_{15}\text{H}_{12}\text{Br}_4\text{O}_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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