FAIRCHILD™

May 2014

FDMS7700S

Dual N-Channel PowerTrench® MOSFET
N-Channel: 30 V, 30 A, 7.5 mΩ N-Channel: 30 V, 40 A, 2.4 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 7.5 mΩ at V_{GS} = 10 V, I_D = 12 A
- Max $r_{DS(on)}$ = 12 mΩ at V_{GS} = 4.5 V, I_D = 10 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 2.4 mΩ at V_{GS} = 10 V, I_D = 20 A
- Max $r_{DS(on)}$ = 2.9 mΩ at V_{GS} = 4.5 V, I_D = 18 A
- RoHS Compliant

General Description

This device includes two specialized N-Channel MOSFETs in a dual MLP package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.
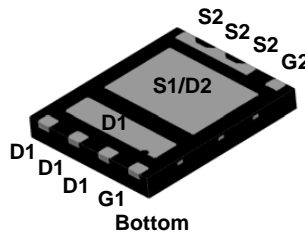
Applications

- Computing
- Communications
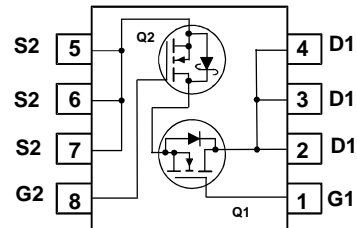- General Purpose Point of Load
- Notebook VCORE
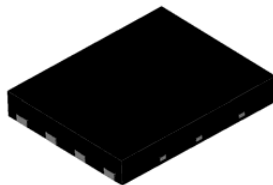
Top

Power 56

Bottom

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage (Note 3)		±20	±20	V
I_D	Drain Current -Continuous	T_C = 25 °C	30	40	A
	-Continuous	T_A = 25 °C	12[1a]	22[1b]	
	-Pulsed		40	60	
P_D	Power Dissipation for Single Operation	T_A = 25 °C	2.2[1a]	2.5[1b]	W
		T_A = 25 °C	1.0[1c]	1.0[1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57[1a]	50[1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125[1c]	120[1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	2	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7700S	FDMS7700S	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C I_D = 1 mA, referenced to 25 °C	Q1 Q2		15 14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 500	µA µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS}= 0 V	Q1 Q2			100 100	nA nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	1 1	1.8 1.5	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C I_D = 1 mA, referenced to 25 °C	Q1 Q2		-6 -4		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12 A V_{GS} = 4.5 V, I_D = 10 A V_{GS} = 10 V, I_D = 12 A , T_J = 125 °C	Q1		6.0 8.5 8.3	7.5 12 12	mΩ
		V_{GS} = 10 V, I_D = 20 A V_{GS} = 4.5 V, I_D = 18 A V_{GS} = 10 V, I_D = 20 A , T_J = 125 °C	Q2		1.9 2.2 2.1	2.4 2.9 3.4	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 12 A V_{DS} = 5 V, I_D = 20 A	Q1 Q2		63 160		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1315 7240	1750 9630	pF
C_{oss}	Output Capacitance	Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		445 2690	600 3580	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		45 185	70 280	pF
R_g	Gate Resistance		Q1 Q2		0.9 0.8		Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 15 V, I_D = 12 A, R_{GEN} = 6 Ω Q2: V_{DD} = 15 V, I_D = 20 A, R_{GEN} = 6 Ω	Q1 Q2		8.6 21	18 34	ns
t_r	Rise Time		Q1 Q2		2.5 9.2	10 18	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		20 58	32 93	ns
t_f	Fall Time		Q1 Q2		2.3 6.8	10 14	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	Q1 Q2		20 105	28 147	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V	Q1 Q2		9.3 48	13 67	nC
Q_{gs}	Gate to Source Gate Charge	Q1 V_{DD} = 15 V, I_D = 12 A	Q1 Q2		4.3 19		nC
Q_{gd}	Gate to Drain "Miller" Charge	Q2 V_{DD} = 15 V, I_D = 20 A	Q1 Q2		2.2 11		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 12 A (Note 2) V_{GS} = 0 V, I_S = 20 A (Note 2)	Q1 Q2		0.8 0.7	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 12 A, di/dt = 100 A/μs	Q1 Q2		27 53	43 85	ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 20 A, di/dt = 300 A/μs	Q1 Q2		10 100	18 160	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
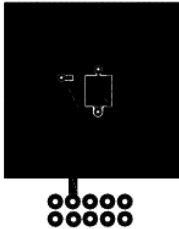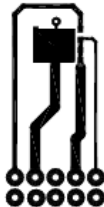

a. 57 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper

c. 125 °C/W when mounted on a minimum pad of 2 oz copper

d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3: As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted
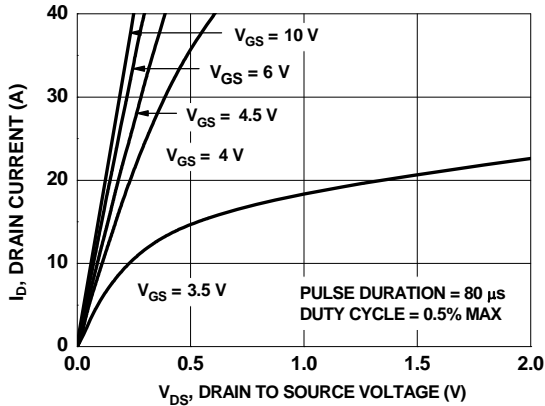

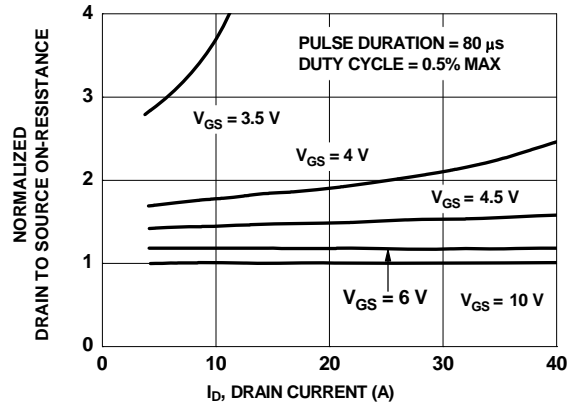**Figure 1. On Region Characteristics**

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage
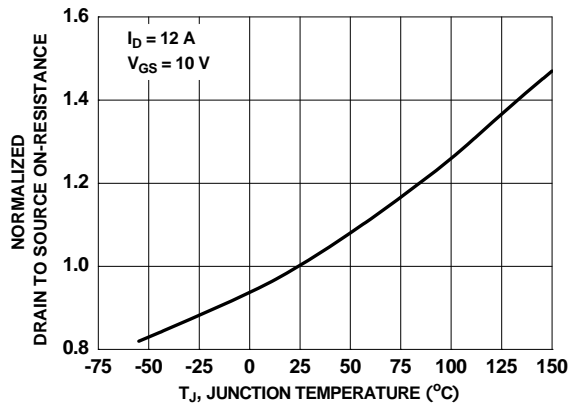

Figure 3. Normalized On Resistance vs Junction Temperature
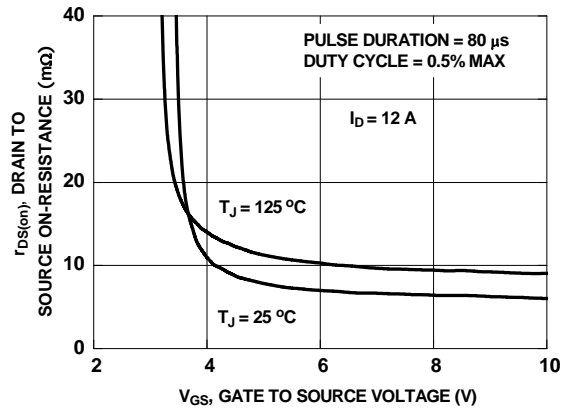
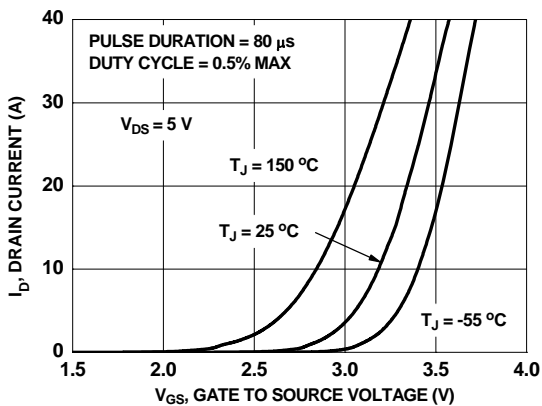

Figure 4. On-Resistance vs Gate to Source Voltage

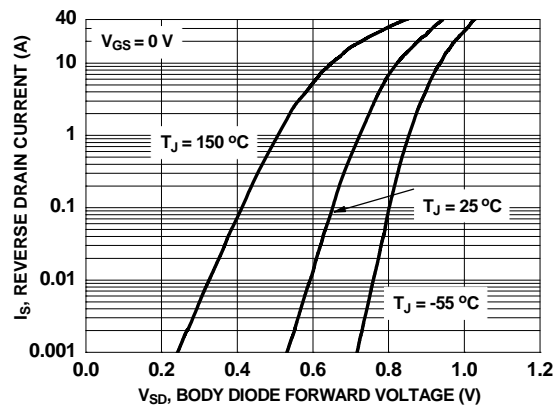

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

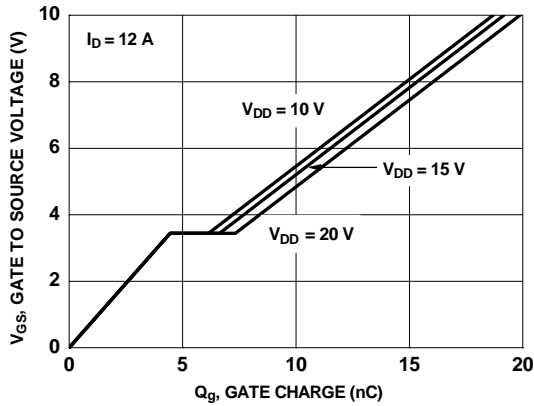## Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

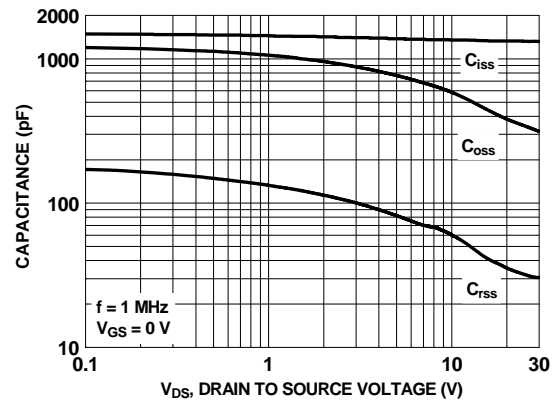**Figure 7. Gate Charge Characteristics**

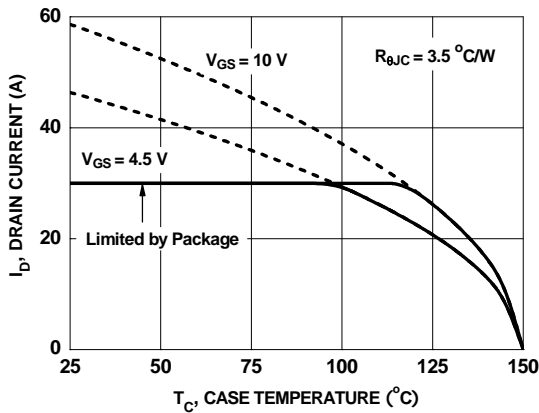**Figure 8. Capacitance vs Drain to Source Voltage**

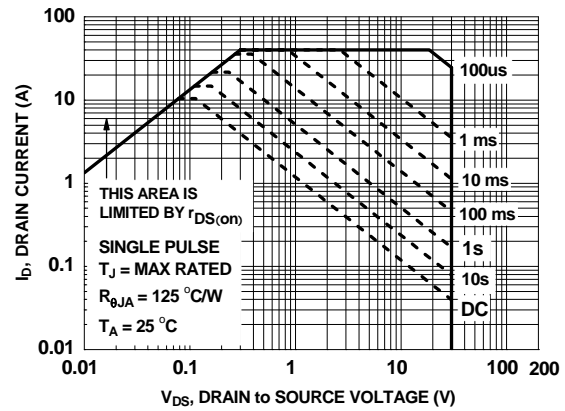**Figure 9. Maximum Continuous Drain Current vs Case Temperature**

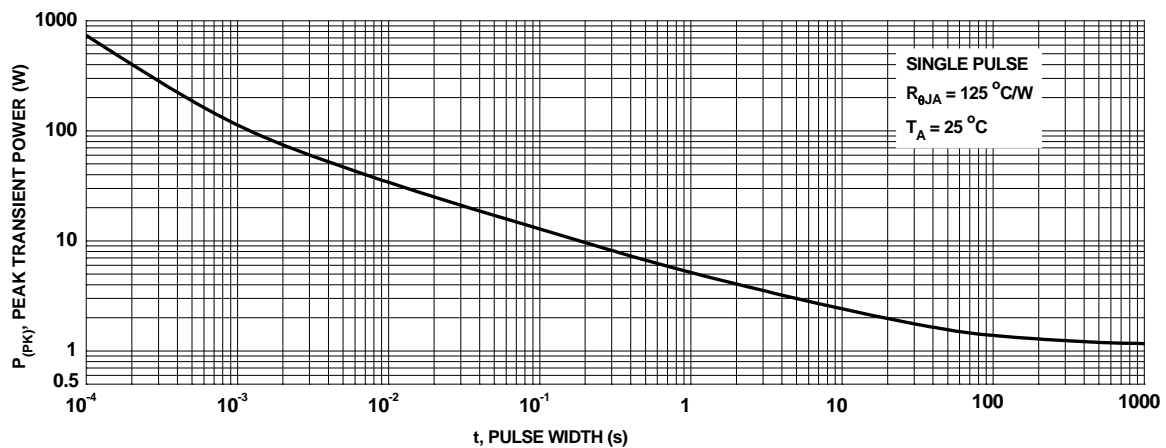**Figure 10. Forward Bias Safe Operating Area**

Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

DUTY CYCLE-DESCENDING ORDER

NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JA}$

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

$R_{\theta JA}$ = 125 °C/W

(Note 1c)

P_{DM}

t_1

t_2

NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JA} \times R_{\theta JA} + T_A$
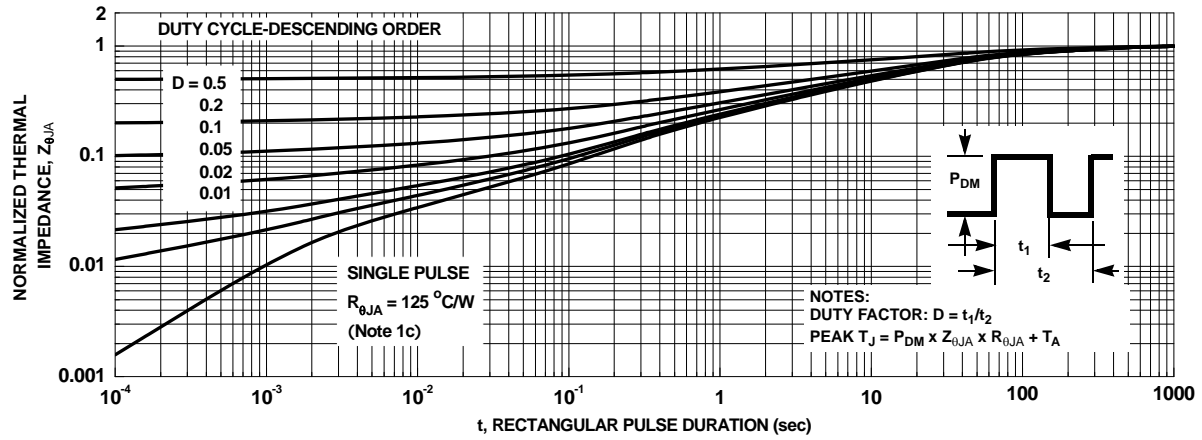
t, RECTANGULAR PULSE DURATION (sec)

Figure 12. Junction-to-Ambient Transient Thermal Response Curve
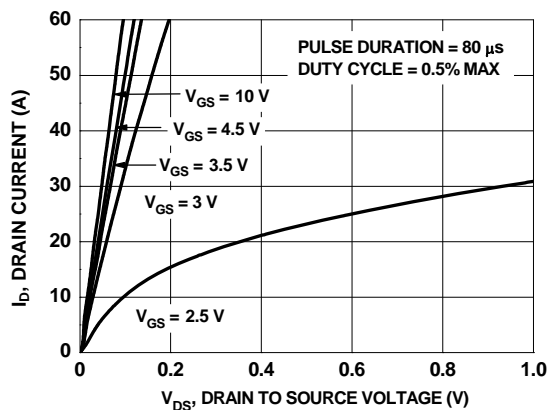
Typical Characteristics (Q2 SyncFET)

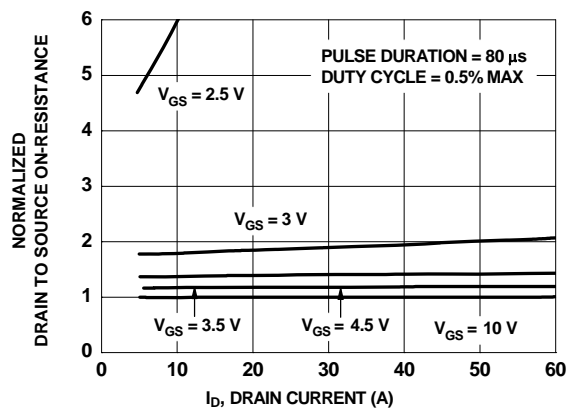**Figure 13. On-Region Characteristics**

Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage
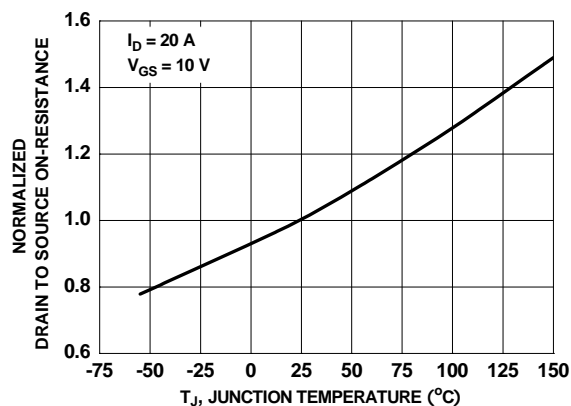
Figure 15. Normalized On-Resistance vs Junction Temperature
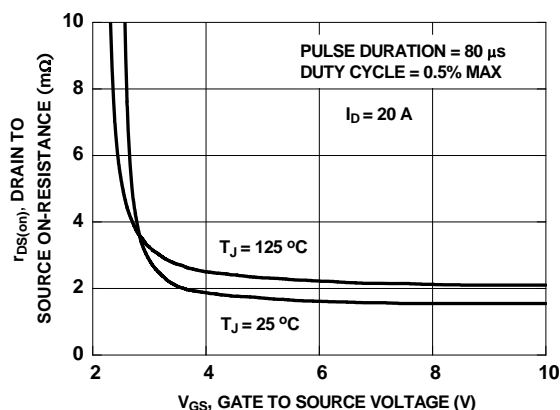
Figure 16. On-Resistance vs Gate to Source Voltage
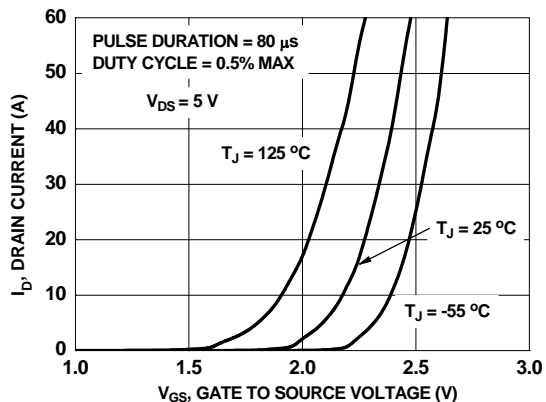
Figure 17. Transfer Characteristics
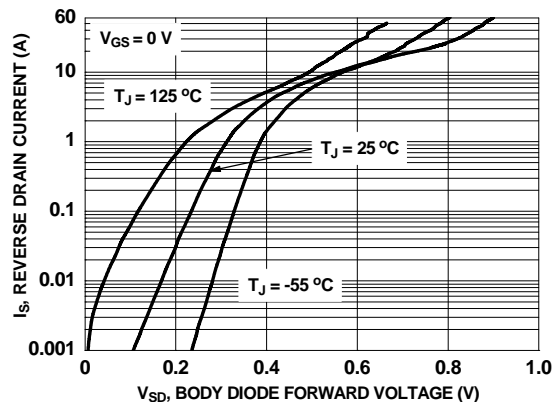
Figure 18. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 SyncFET)
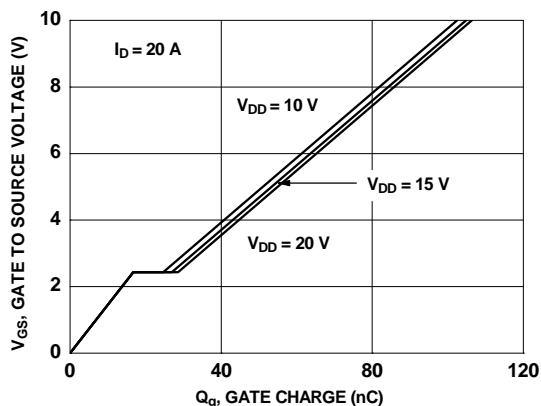
Figure 19. Gate Charge Characteristics
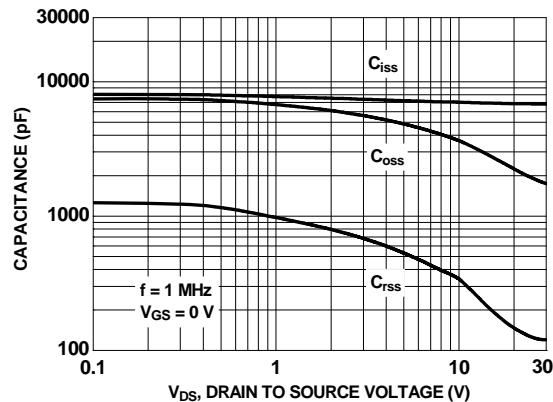
Figure 20. Capacitance vs Drain to Source Voltage
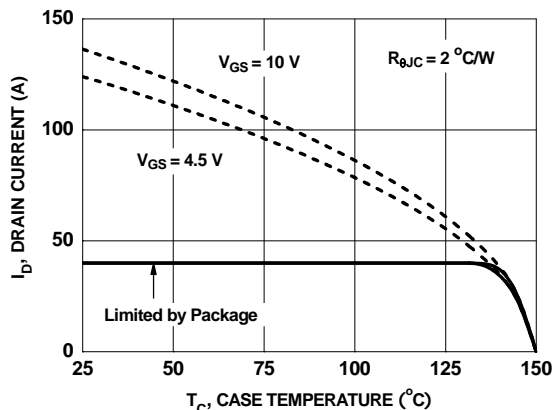
Figure 21. Maximum Continuous Drain Current vs Case Temperature
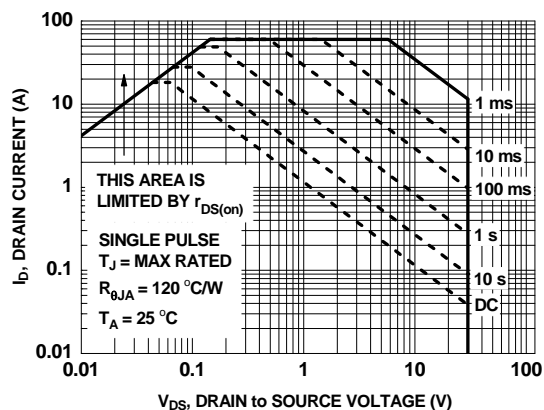
Figure 22. Forward Bias Safe Operating Area
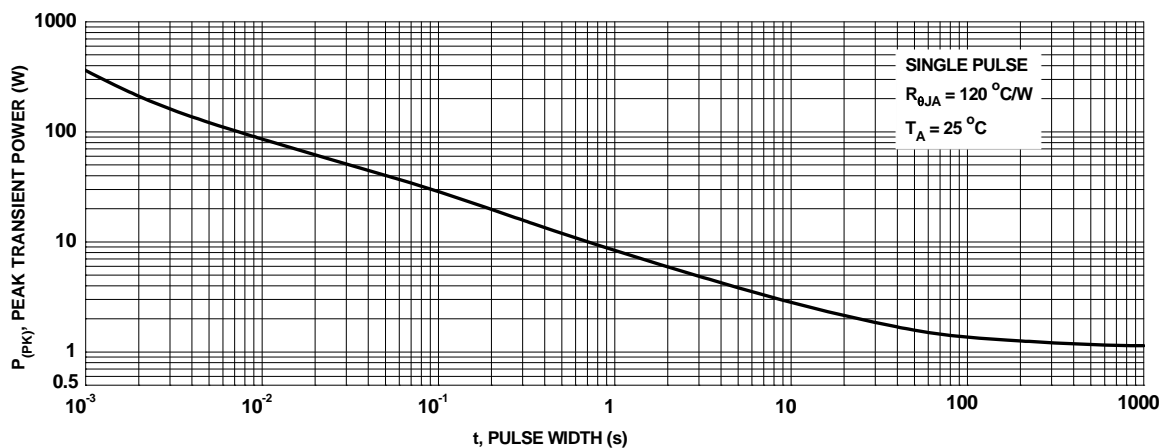
Figure 23. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 SyncFET)
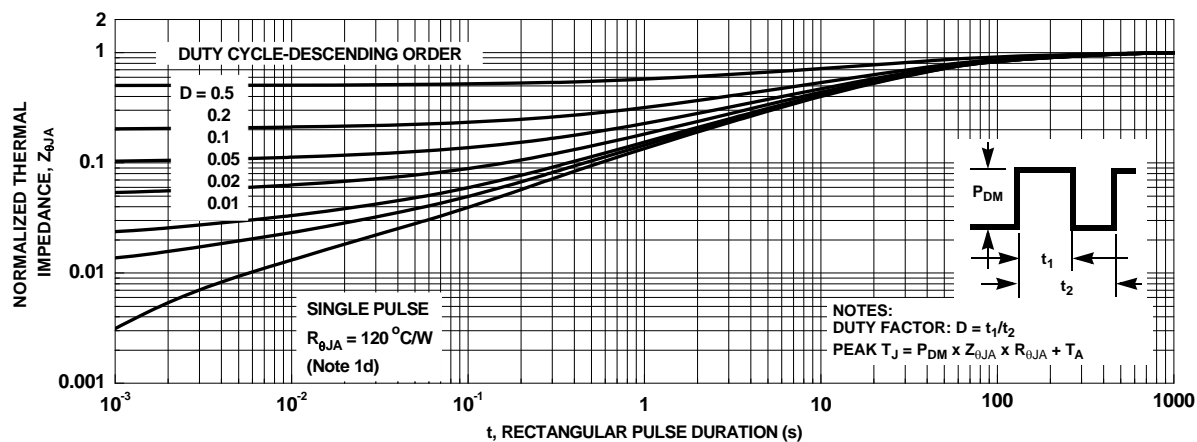
Figure 24. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky Body Diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench® MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 25 shows the reverse recovery characteristic of the FDMS7700S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.
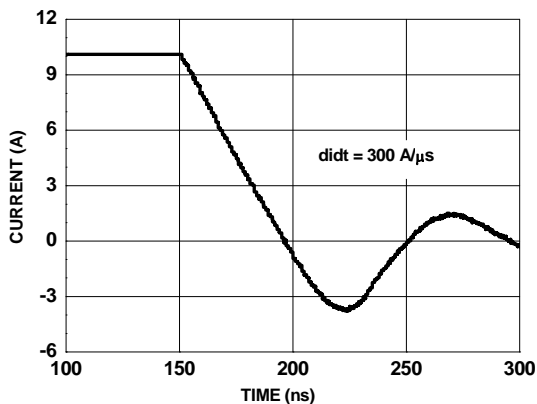
Figure 25. FDMS7700S SyncFET™ Body Diode Reverse Recovery Characteristic
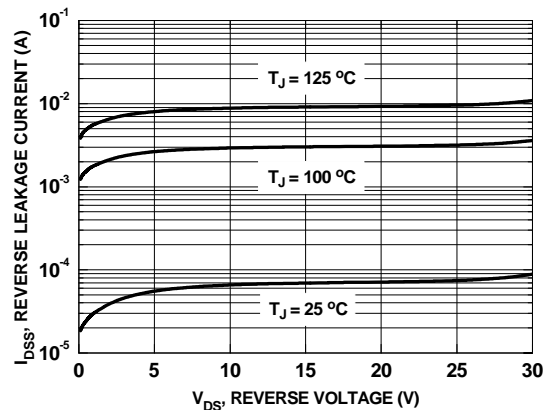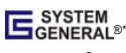
Figure 26. SyncFET™ Body Diode Reverse Leakage vs. Drain-Source Voltage

TOP VIEW

2X | 0.05 | C

5.00 → A | B

6.00

0.05 | C
2X

PIN#1 IDENT

SIDE VIEW

// | 0.10 | C
0.75±0.05

⌒ | 0.08 | C

0.025±0.025

0.20±0.05

C
SEATING
PLANE

BOTTOM VIEW

5.00±0.05

3.80±0.05

(0.34)4X

PIN#1 IDENT

0.43±0.05(5X)

1 2 3 4

0.92±0.05

(0.66)

0.55±0.05

6.00±0.05

2.67±0.05

0.45

8 7 6 5

0.51±0.05(5X)

1.27

3.81±0.05

⌖ | 0.10 | C | A | B
| 0.05 | C

RECOMMENDED LAND PATTERN
(OPTION 1 - FUSED LEADS 5,6,7)

4.46

1.27

0.65

8 7 6 5

0.63(5X)

0.25

0.40

2.67

6.30

0.54

0.66

0.92

1 2 3 4

0.65 (5X)

4.00

RECOMMENDED LAND PATTERN
(OPTION 2 - ISOLATED LEADS)

4.46

1.27

0.65(8X)

8 7 6 5

0.63(8X)

0.40

2.67

6.30

0.54

0.66

0.92

1 2 3 4

4.00

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP08Prev2.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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