

November 2015

FDMC4435BZ

P-Channel Power Trench[®] MOSFET -30 V, -18 A, 20 m Ω

Features

- Max $r_{DS(on)} = 20 \text{ m}\Omega$ at $V_{GS} = -10 \text{ V}$, $I_D = -8.5 \text{ A}$
- Max $r_{DS(on)}$ = 37 m Ω at V_{GS} = -4.5 V, I_D = -6.3 A
- Extended V_{GSS} range (-25 V) for battery applications
- High performance trench technology for extremely low r_{DS(on)}
- High power and current handling capability
- HBM ESD protection level >7 kV typical (Note 4)
- 100% UIL Tested
- Termination is Lead-free and RoHS Compliant

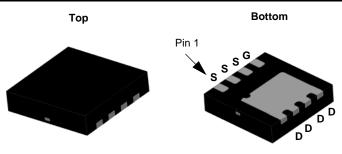
General Description

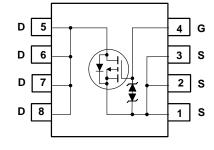
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Applications

- High side in DC DC Buck Converters
- Notebook battery power management
- Load switch in Notebook







MLP 3.3x3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V _{DS}	Drain to Source Voltage			-30	V
V_{GS}	Gate to Source Voltage			±25	V
	Drain Current -Continuous	T _C = 25 °C		-18	
I _D	-Continuous	T _A = 25 °C	(Note 1a)	-8.5	Α
	-Pulsed			-50	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	32	mJ
Б	Power Dissipation	T _C = 25 °C		31	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.3	VV
T _J , T _{STG}	Operating and Storage Junction Temperate	ure Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4	°C/\//
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1	a) 53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC4435BZ	FDMC4435BZ	MLP 3.3X3.3	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25 °C		21		mV/°C
l	Zero Gate Voltage Drain Current	V _{DS} = -24 V,			-1	μА
IDSS	Zero Gate Voltage Drain Current	$V_{GS} = 0 \text{ V},$ $T_J = 125 ^{\circ}\text{C}$			-100	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μΑ

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-1.0	-1.8	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		-5		mV/°C
		$V_{GS} = -10 \text{ V}, I_D = -8.5 \text{ A}$		14	20	
r	Static Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -6.3 \text{ A}$		21	37	mΩ
r _{DS(on)}	Static Brain to Cource On Nesistance	$V_{GS} = -10 \text{ V}, I_D = -8.5 \text{ A},$ $T_J = 125 ^{\circ}\text{C}$		20	29	11122
9 _{FS}	Forward Transconductance	$V_{DD} = -5 \text{ V}, \ I_{D} = -8.5 \text{ A}$		25		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 45.V.V 0.V	1535	2040	pF
C _{oss}	Output Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	310	410	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12	280	420	pF
R_g	Gate Resistance	f = 1 MHz	4		Ω

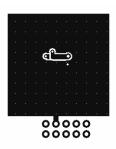
Switching Characteristics

t _{d(on)}	Turn-On Delay Time			10	20	ns
t _r	Rise Time	V _{DD} = -15 V, I _D = -8.5	5 A,	9	18	ns
t _{d(off)}	Turn-Off Delay Time	V _{GS} = -10 V, R _{GEN} =	: 6 Ω	35	56	ns
t _f	Fall Time			19	34	ns
Q_g	Total Gate Charge	V _{GS} =0V to -10V		38	53	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to -4.5 V}$	V _{DD} = -15 V,	20	28	nC
Q _{gs}	Gate to Source Charge		$I_D = -8.5 \text{ A}$	4.3		nC
Q_{gd}	Gate to Drain "Miller" Charge			11		nC

Drain-Source Diode Characteristics

V	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -8.5 \text{A}$	(Note 2)	0.86	1.5	\/
V _{SD}	Source to Drain blode Forward voltage	$V_{GS} = 0 \text{ V}, I_{S} = -1.9 \text{ A}$	(Note 2)	0.74	1.2	· ·
t _{rr}	Reverse Recovery Time	I _F = -8.5 A, di/dt = 100 A/μs		26	40	ns
Q _{rr}	Reverse Recovery Charge			12	20	nC

^{1.} R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

^{2.} Pulse Test: Pulse Width < 300 $\mu s,$ Duty cycle < 2.0 %.

^{3.} Starting T_J = 25°C; P-ch: L = 1mH, I_{AS} = -8A, V_{DD} = -27V, V_{GS} = -10V.

^{4.} The diode connected between the gate and source servers only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25°C unless otherwise noted

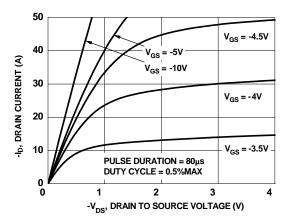


Figure 1. On-Region Characteristics

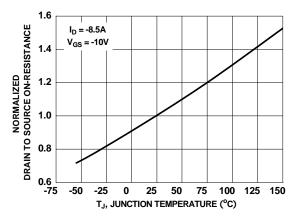


Figure 3. Normalized On-Resistance vs Junction Temperature

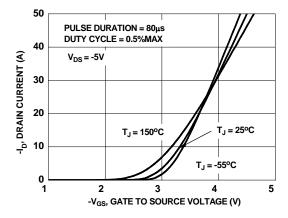


Figure 5. Transfer Characteristics

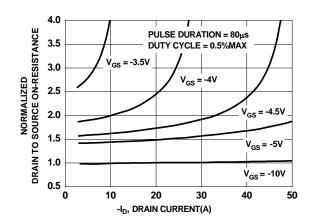


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

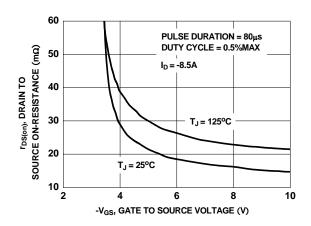


Figure 4. On-Resistance vs Gate to Source Voltage

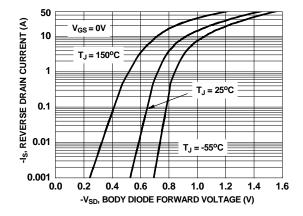


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

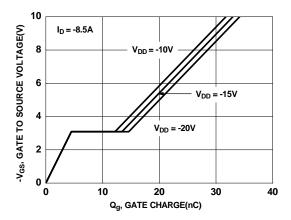


Figure 7. Gate Charge Characteristics

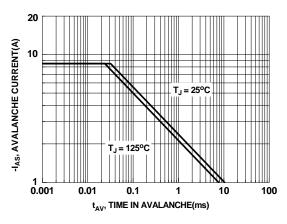


Figure 9. Unclamped Inductive Switching Capability

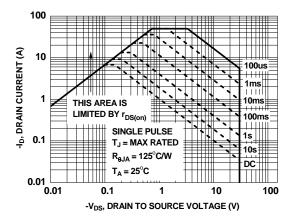


Figure 11. Forward Bias Safe Operating Area

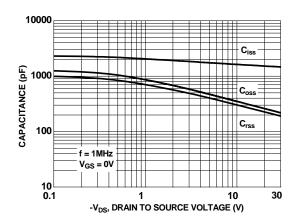


Figure 8. Capacitance vs Drain to Source Voltage

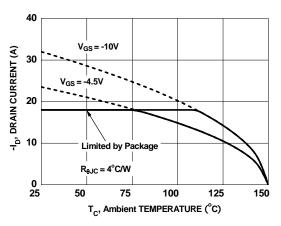


Figure 10. Maximum Continuous Drain Current vs Case Temperature

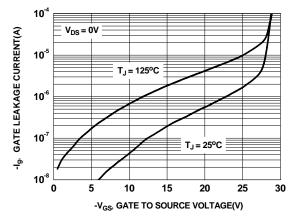


Figure 12. Igss vs Vgss

Typical Characteristics T_J = 25°C unless otherwise noted

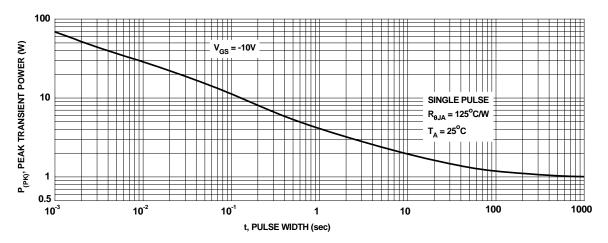


Figure 13. Single Pulse Maximum Power Dissipation

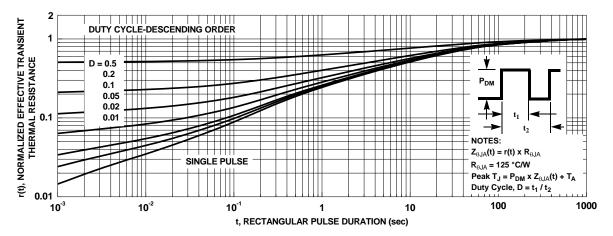
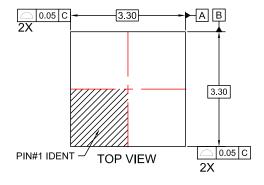
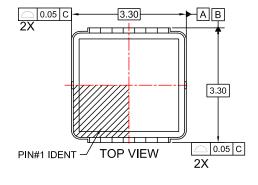
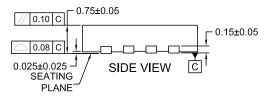


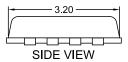
Figure 14. Transient Thermal Response Curve

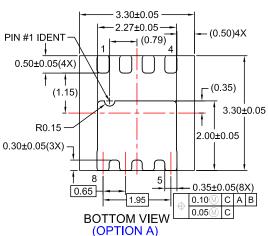
Dimensional Outline and Pad Layout

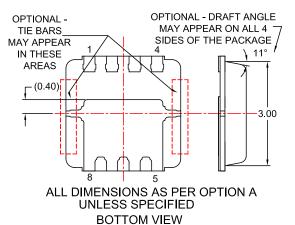




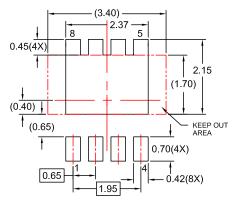








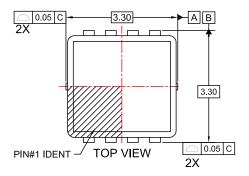
(OPTION B)

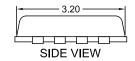


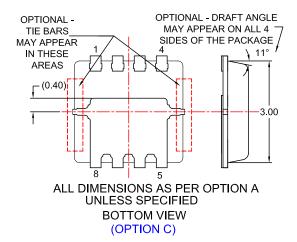


RECOMMENDED LAND PATTERN

Dimensional Outline and Pad Layout







NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.
- F. DRAWING FILENAME: MKT-MLP08Wrev3.
- G. OPTION A SAWN MLP, OPTIONS B & C PUNCH MLP.



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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information Formative / In Design		Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary First Production		Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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