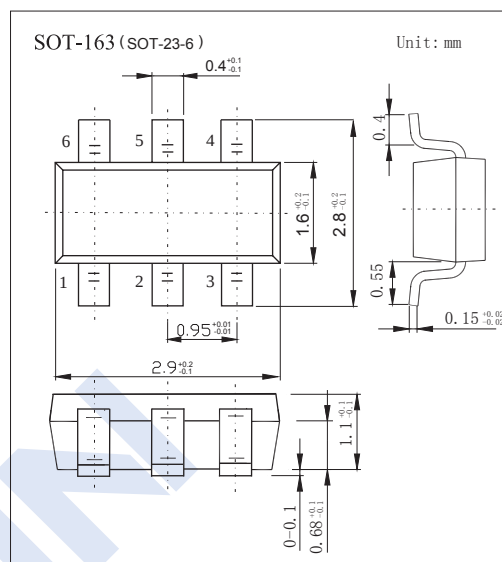
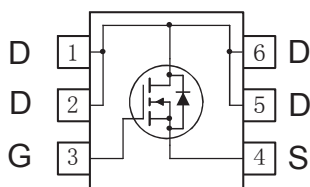


N-Channel Enhancement MOSFET

FDC2512 (KDC2512)

■ Features

- V_{DS} (V) = 150V
- I_D = 1.4A (V_{GS} = 10V)
- $R_{DS(ON)}$ < 425m Ω (V_{GS} = 10V)
- $R_{DS(ON)}$ < 475m Ω (V_{GS} = 6V)

■ Absolute Maximum Ratings T_a = 25°C

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	
Drain Current - Continuous *1a - Pulsed	I_D	1.4	A
		8	
Power Dissipation *1a *1b	P_D	1.6	W
		0.8	
Thermal Resistance.Junction- to-Ambient *1a	R_{thJA}	78	°C/W
Thermal Resistance.Junction- to-Case *1	R_{thJC}	30	
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-55 to 150	

*1. R_{thJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{thJC} is guaranteed by design while R_{thCA} is determined by the user's board design.

*1a. 78°C/W when mounted on a 1in2 pad of 2 oz copper

*1b. 156°C/W when mounted on a minimum pad of 2 oz copper

N-Channel Enhancement MOSFET

FDC2512 (KDC2512)

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D =250 μA, V _{GS} =0V	150			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =120V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSSF}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Gate Threshold Voltage *1	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250 μA	2	2.6	4	V
Static Drain-Source On-Resistance *1	R _{DS(on)}	V _{GS} =10V, I _D =1.4A		319	425	mΩ
		V _{GS} =10V, I _D =1.4A T _J =125℃		624	875	
		V _{GS} =6.0V, I _D =1.3A		332	475	
On State Drain Current *1	I _{D(ON)}	V _{GS} =10V, V _{DS} =5V	4			A
Forward Transconductance *1	g _{FS}	V _{DS} =10V, I _D =1.4A		4		S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =75V, f=1MHz		344		pF
Output Capacitance	C _{oss}			22		
Reverse Transfer Capacitance	C _{rss}			9		
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =75V, I _D =1.4A *1		8	11	nC
Gate Source Charge	Q _{gs}			1.5		
Gate Drain Charge	Q _{gd}			2.3		
Turn-On DelayTime	t _{d(on)}	V _{GS} =10V, V _{DS} =75V, I _D =1A, R _{GEN} =6 Ω *1		6.5	13	ns
Turn-On Rise Time	t _r			3.5	7	
Turn-Off DelayTime	t _{d(off)}			22	33	
Turn-Off Fall Time	t _f			4	8	
Body Diode Reverse Recovery Time	t _{rr}	I _F = 1.4A, di/dt= 300A/μs *1		45.8		nC
Body Diode Reverse Recovery Charge	Q _{rr}			119		
Maximum Body-Diode Continuous Current	I _S				1.3	A
Diode Forward Voltage *1	V _{SD}	I _S =1.3A, V _{GS} =0V		0.8	1.2	V

*1 Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

■ Marking

Marking	FDC2512
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N-Channel Enhancement MOSFET

FDC2512 (KDC2512)

■ Typical Characteristics

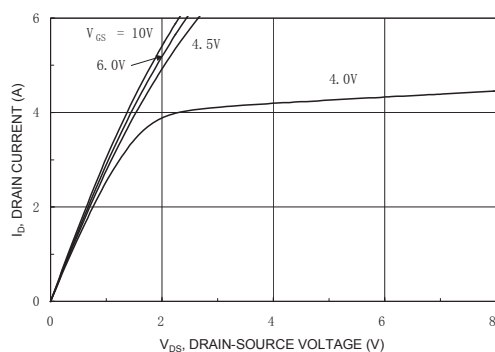


Figure 1. On-Region Characteristics.

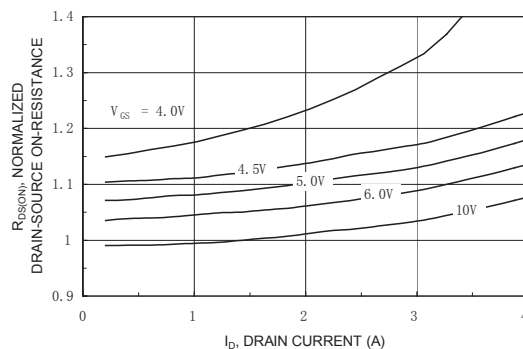


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

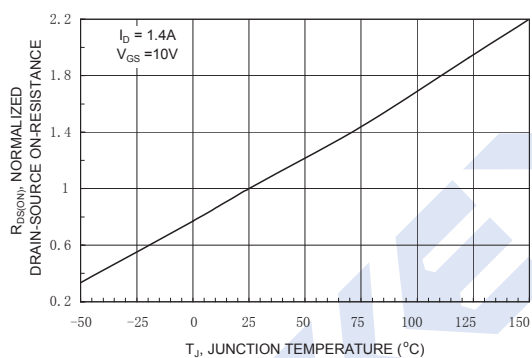


Figure 3. On-Resistance Variation with Temperature.

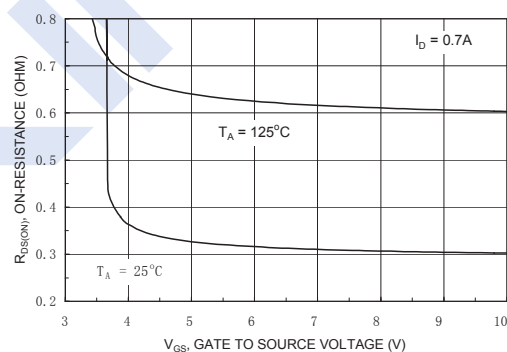


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

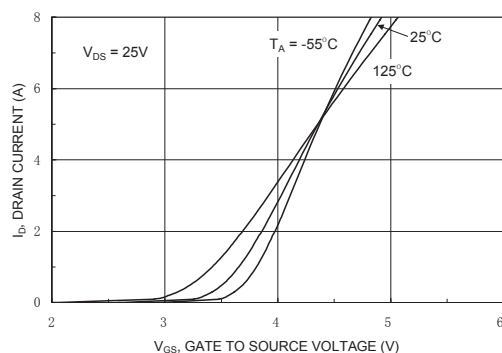


Figure 5. Transfer Characteristics.

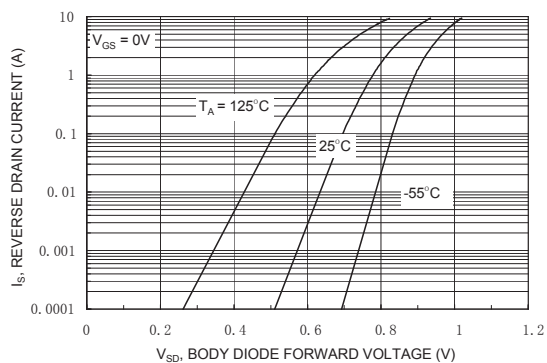


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

N-Channel Enhancement MOSFET

FDC2512 (KDC2512)

■ Typical Characteristics

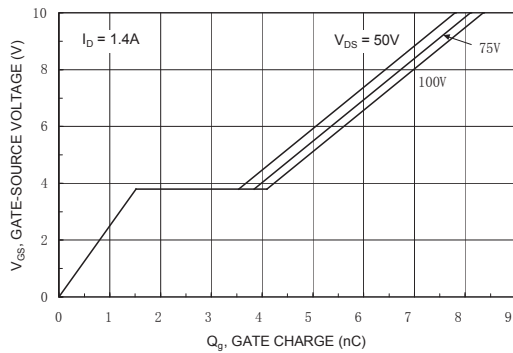


Figure 7. Gate Charge Characteristics.

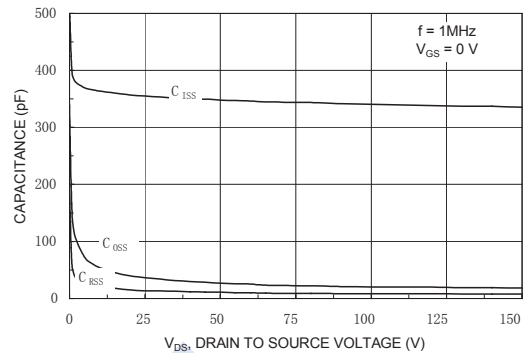


Figure 8. Capacitance Characteristics.

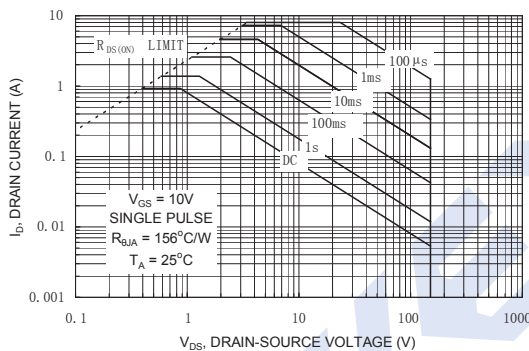


Figure 9. Maximum Safe Operating Area.

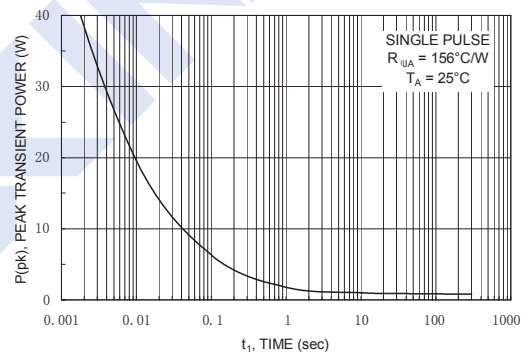


Figure 10. Single Pulse Maximum Power Dissipation.

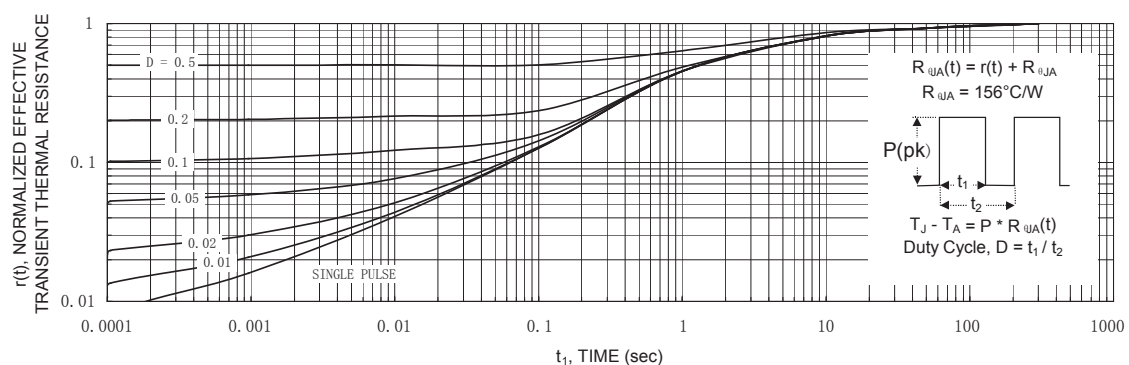


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.