FAIRCHILD SEMICONDUCTOR®

May 2024

# FAN7711
# Ballast Control Integrated Circuit



## Features

- Floating Channel for Bootstrap Operation to +600V
- Low Start-up and Operating Current: 120μA, 3.2mA
- Under-Voltage Lockout with 1.8V of Hysteresis
- Adjustable Run Frequency and Preheat Time
- Internal Active ZVS Control
- Internal Protection Function (Latch Mode)
- Internal Clamping Zener Diode
- High Accuracy Oscillator
- Soft-Start Functionality

## Description

The FAN7711, developed with Fairchild's unique high-voltage process, is a ballast control integrated circuit (IC) for a fluorescent lamp. FAN7711 incorporates a preheating / ignition function, controlled by an externally selected external capacitor, to increase lamp life. The FAN7711 detects switch operation from after ignition mode through an internal active Zero-Voltage Switching (ZVS) control circuit. This control scheme enables the FAN7711 to detect an open-lamp condition without the expense of external circuitry and prevents stress on MOSFETs. The high-side driver built into the FAN7711 has a common-mode noise cancellation circuit that provides robust operation against high-dv/dt noise intrusion.

## Applications

- Electronic Ballast

8-SOP 8-DIP

## Ordering Information

| Part Number | Package | Pb-Free | Operating Temperature Range | Packing Method |
|---|---|---|---|---|
| FAN7711N | 8-DIP | Yes | -25°C ~ 125°C | Tube |
| FAN7711M | 8-SOP | | | Tube |
| FAN7711MX | | | | Tape & Reel |

## Typical Application

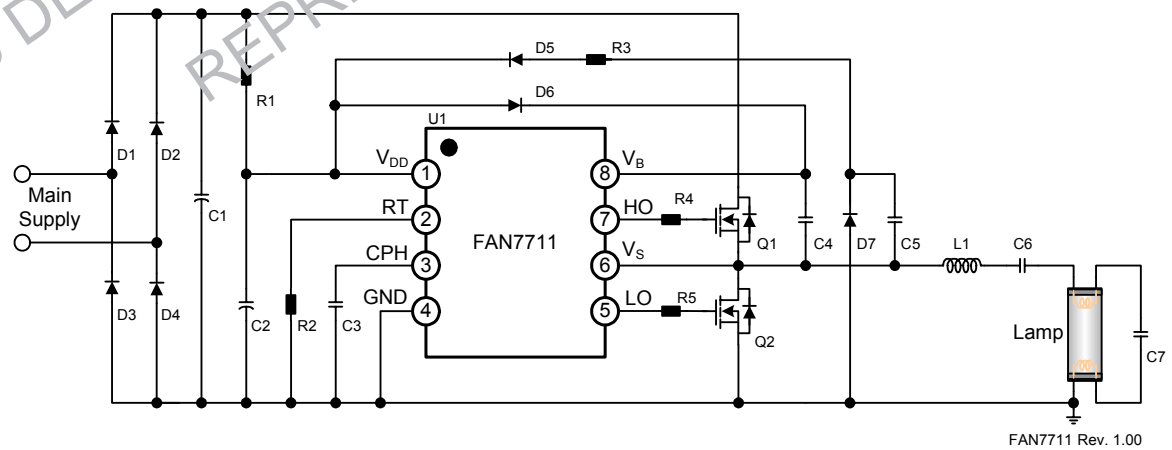


**Figure 1. Typical Application Circuit for Compact Fluorescent Lamp**

## Internal Block Diagram

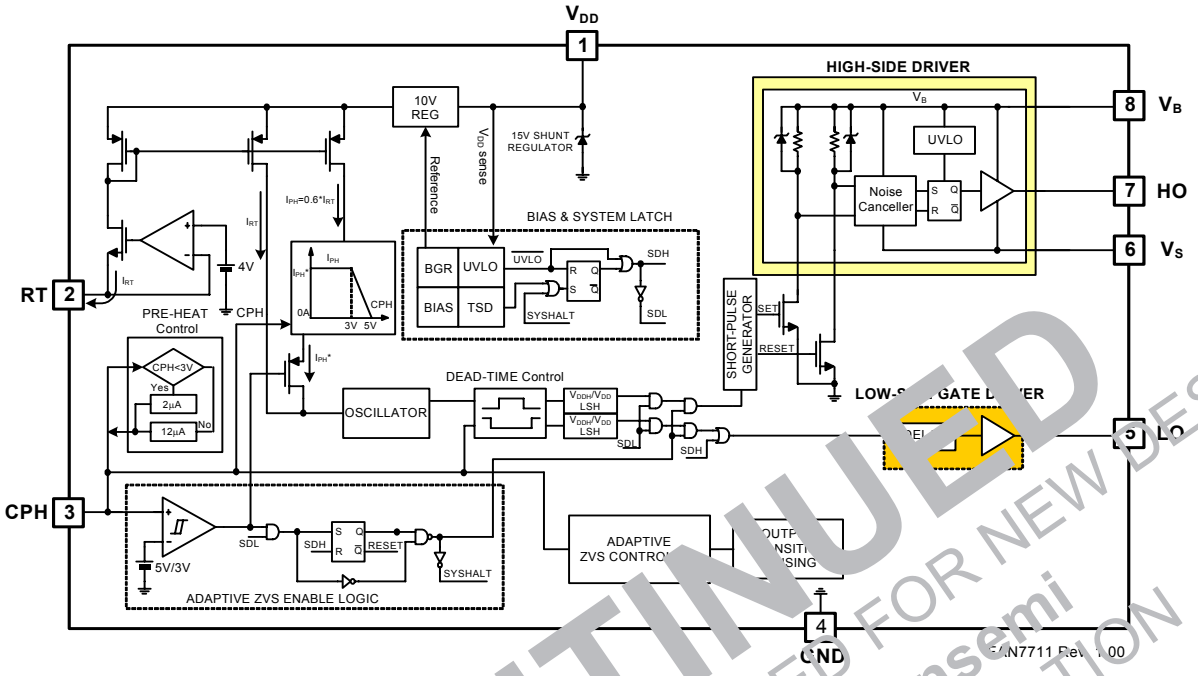


**Figure 2. Functional Block Diagram**

## Pin Configuration

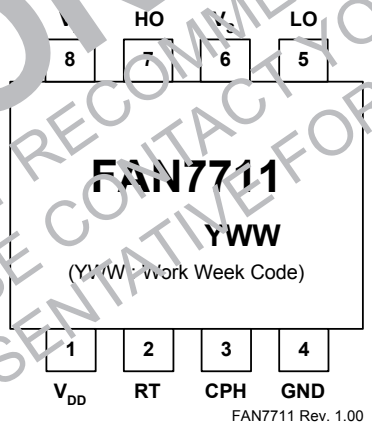


**Figure 3. Pin Configuration (Top View)**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | $V_{DD}$ | Supply voltage |
| 2 | RT | Oscillator frequency set resistor |
| 3 | CPH | Preheating time set capacitor |
| 4 | GND | Ground |
| 5 | LO | Low-side output |
| 6 | $V_S$ | High-side floating supply return |
| 7 | HO | High-side output |
| 8 | $V_B$ | High-side floating supply |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A$=25°C unless otherwise specified.

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_B$ | High-side floating supply | | -0.3 | | 625 | V |
| $V_S$ | High-side floating supply return | | -0.3 | | 600 | V |
| $V_{IN}$ | RT, CPH pins input voltage | | -0.3 | | 8 | V |
| $I_{CL}$ | Clamping current level | | | | 25 | mA |
| $dV_S/dt$ | Allowable offset voltage slew rate | | | 50 | | V/ns |
| $T_A$ | Operating temperature range | | -25 | | 125 | °C |
| $T_{STG}$ | Storage temperature range | | -55 | | 150 | °C |
| $P_D$ | Power dissipation | 8-SOP | | 0.625 | | W |
| | | 8-DIP | | 1.2 | | |
| $\theta_{JA}$ | Thermal resistance (junction-to-air) | 8-SOP | | 200 | | °C/W |
| | | 8-DIP | | 100 | | |

**Note:**

1. Do not supply a low-impedance voltage source to the internal clamping Zener diode between the GND and the $V_{DD}$ pin of this device.

## Electrical Characteristics

$V_{BIAS}$ ($V_{DD}$, $V_{BS}$) = 14.0V, $T_A$ = 25°C, unless otherwise specified.

| Symbol | Characteristics | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage Section** | | | | | | |
| $V_{DDTH(ST+)}$ | $V_{DD}$ UVLO positive going threshold | $V_{DD}$ increasing | 12.4 | 13.4 | 14.4 | V |
| $V_{DDTH(ST-)}$ | $V_{DD}$ UVLO negative going threshold | $V_{DD}$ decreasing | 10.8 | 11.6 | 12.4 | |
| $V_{DDHY(ST)}$ | $V_{DD}$-side UVLO hysteresis | | | 1.8 | | |
| $V_{CL}$ | Supply clamping voltage | $I_{DD}$ =10mA | 14.8 | 15.2 | | |
| $I_{ST}$ | Start-up supply current | $V_{DD}$ = 10V | | 120 | | µA |
| $I_{DD}$ | Dynamic operating supply current | 50kHz, $C_L$ = 1nF | | 2.2 | | mA |
| **High-Side Supply Section ($V_B$-$V_S$)** | | | | | | |
| $V_{HSTH(ST+)}$ | High-side UVLO positive going threshold | $V_{BS}$ increasing | 8.5 | 9.2 | 10.0 | V |
| $V_{HSTH(ST-)}$ | High-side UVLO negative going threshold | $V_{BS}$ decreasing | 8.9 | | 9.5 | |
| $V_{HSHY(ST)}$ | High-side UVLO hysteresis | | | 0.6 | | |
| $I_{HST}$ | High-side quiescent supply current | $V_{BS}$ = 14V | | 50 | | µA |
| $I_{HD}$ | High-side dynamic operating supply current | 50kHz, $C_L$ = 1nF | | 1 | | mA |
| $I_{LK}$ | Offset supply leakage current | $V_B$ = $V_S$ = 625V | | | 45 | µA |
| **Oscillator Section** | | | | | | |
| $V_{MPH}$ | CPH pin preheating voltage range | | 2.5 | 3.0 | 3.5 | V |
| $I_{PH}$ | CPH pin charging current during preheating | $V_{CPH}$ = 1V | 1.25 | 2.00 | 2.85 | µA |
| $I_{IG}$ | CPH pin charging current during ignition | $V_{CPH}$ = 4V | 8 | 12 | 16 | |
| $V_{MO}$ | CPH pin voltage level at run mode | | | 7.0 | | V |
| $f_{PRE}$ | Preheating frequency | $R_T$ = 80kΩ, $V_{CPH}$ = 2V | 72 | 85 | 98 | kHz |
| $f_{OSC}$ | Running frequency | $R_T$ = 80kΩ | 48.7 | 53.0 | 57.3 | kHz |
| $DT_{MAX}$ | Maximum dead time | $V_{CPH}$ = 1V, $V_S$ = GND during preheat mode | | 3.1 | | µs |
| $DT_{MIN}$ | Minimum dead time | $V_{CPH}$ = 6V, $V_S$ = GND during run mode | | 1.0 | | µs |
| **Output Section** | | | | | | |
| $I_{OH+}$ | High-side driver sourcing current | PW = 10µs | 250 | 350 | | mA |
| $I_{OH-}$ | High-side driver sinking current | PW = 10µs | 500 | 650 | | |
| $I_{OL+}$ | Low-side driver sourcing current | PW = 10µs | 250 | 350 | | |
| $I_{OL-}$ | Low-side driver sink current | PW = 10µs | 500 | 650 | | |
| $t_{HOR}$ | High-side driver turn-on rising time | $C_L$ = 1nF, $V_{BS}$ = 15V | | 45 | | ns |
| $t_{HOL}$ | High-side driver turn-off rising time | $C_L$ = 1nF, $V_{BS}$ = 15V | | 25 | | |
| $t_{LOR}$ | Low-side driver turn-on rising time | $C_L$ = 1nF, $V_{BS}$ = 15V | | 45 | | |
| $t_{LOL}$ | Low-side driver turn-off rising time | $C_L$ = 1nF, $V_{BS}$ = 15V | | 25 | | |
| $V_S$(2) | Maximum allowable negative $V_S$ swing range for signal propagation to high-side output | | | -9.8 | | V |
| **Protection Section** | | | | | | |
| $V_{CPHSD}$ | Shutdown voltage | $V_{RT}$ = 0 after run mode | 2.6 | | | V |
| $I_{SD}$ | Shutdown current | | | 250 | 450 | µA |
| TSD | Thermal shutdown(2) | | | 165 | | °C |

**Note:**
2. This parameter, although guaranteed, is not 100% tested in production.

## Typical Characteristics

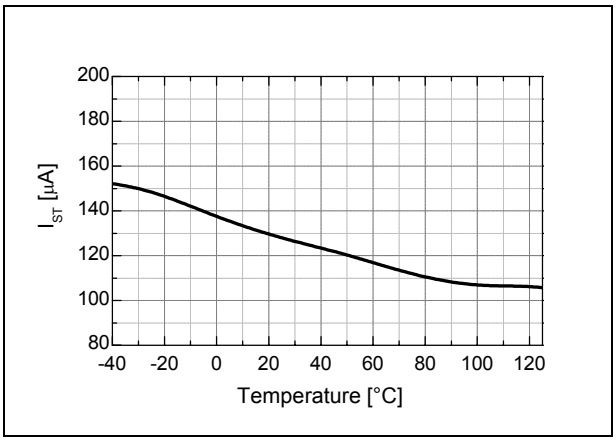


**Figure 4. Start-Up Current vs. Temp.**

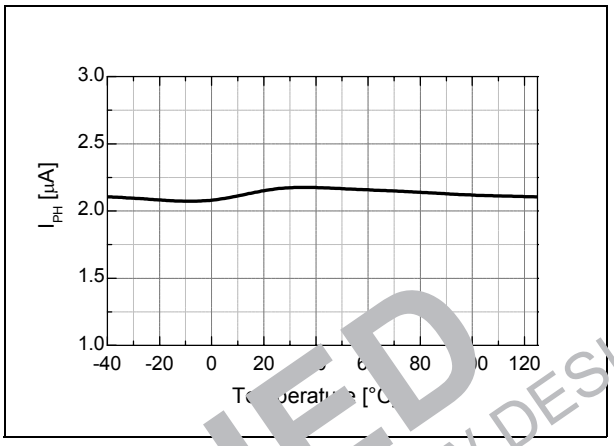


**Figure 5. Preheating Current vs. Temp.**

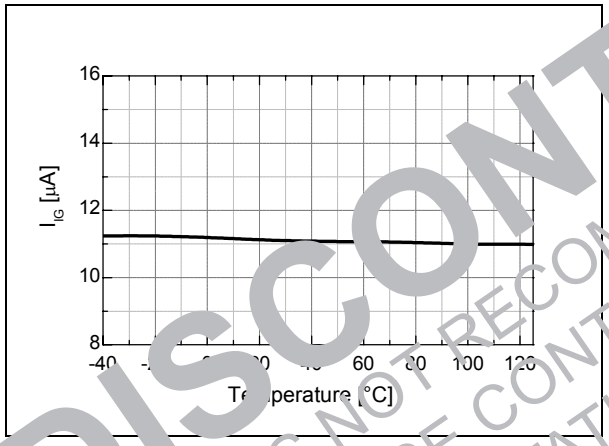


**Figure 6. Ignition Current vs. Temp**

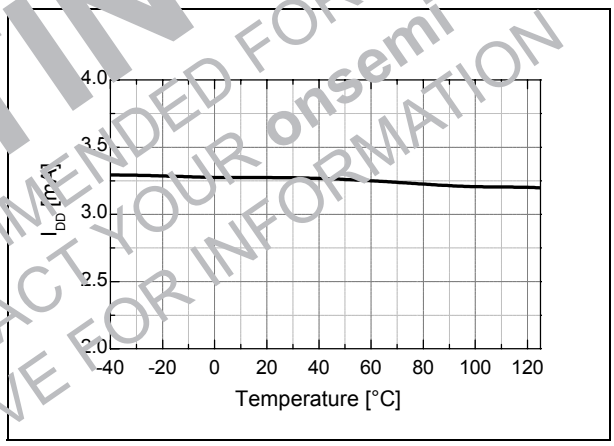


**Figure 7. Operating Current vs. Temp.**

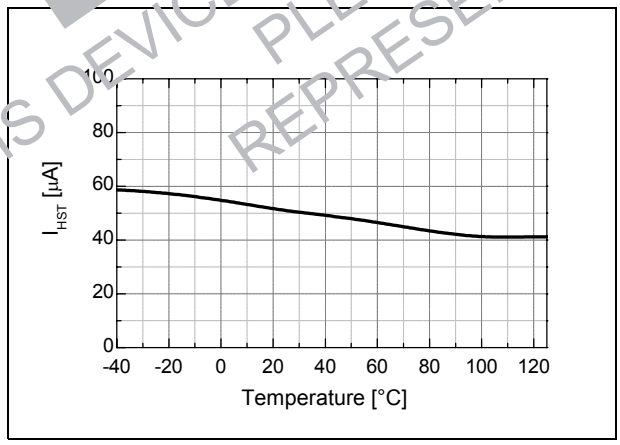


**Figure 8. Start-Up Current vs. Temp.**

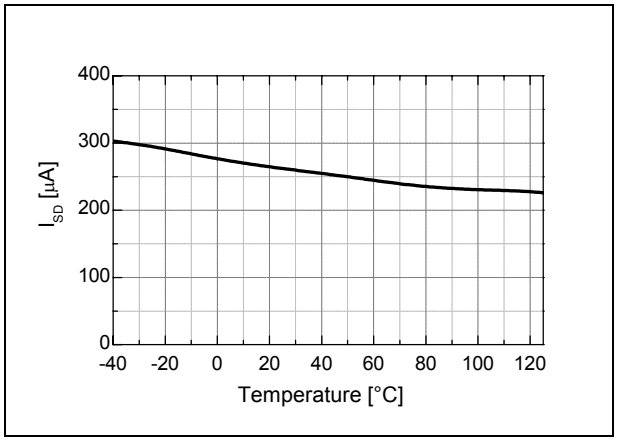


**Figure 9. Shutdown Current vs. Temp.**

## Typical Characteristics (Continued)

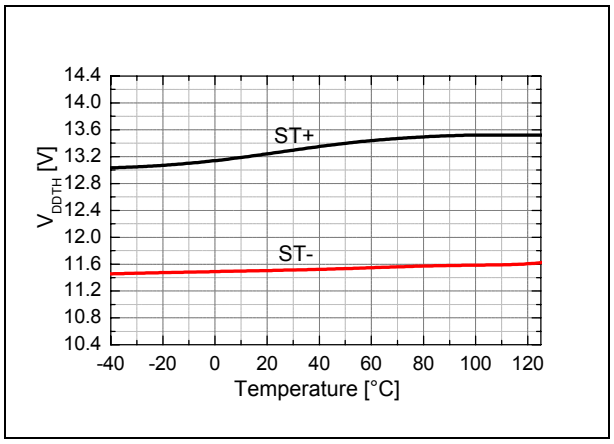


**Figure 10. $V_{DD}$ UVLO vs. Temp.**

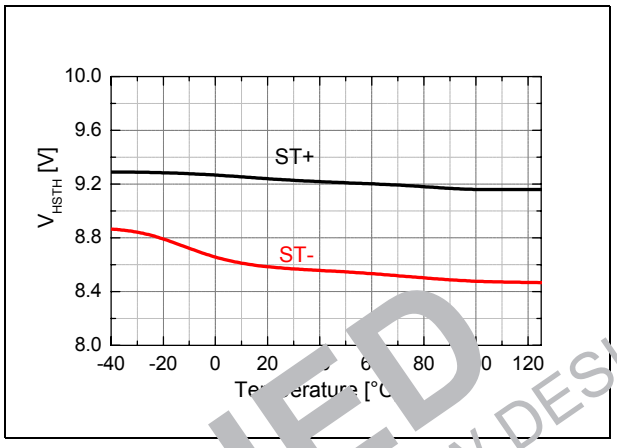


**Figure 11. $V_{BS}$ UVLO vs. Temp.**

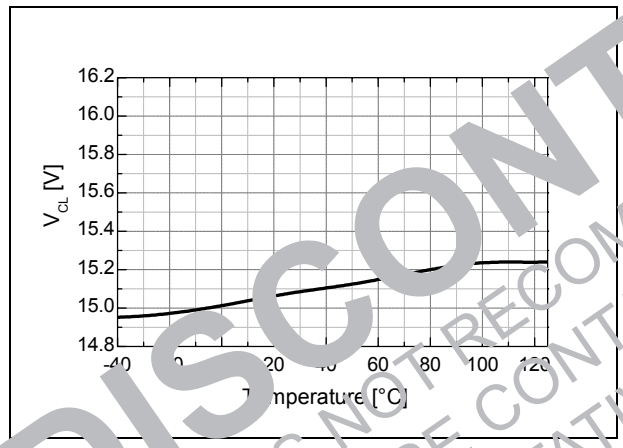


**Figure 12. $V_{DD}$ Clamp Voltage vs. Temp.**

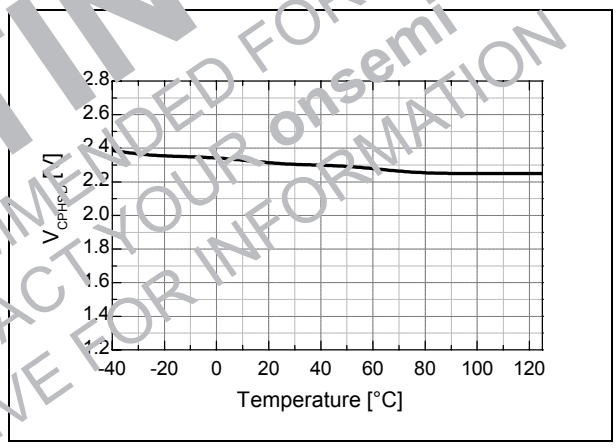


**Figure 13. Shutdown Voltage vs. Temp.**

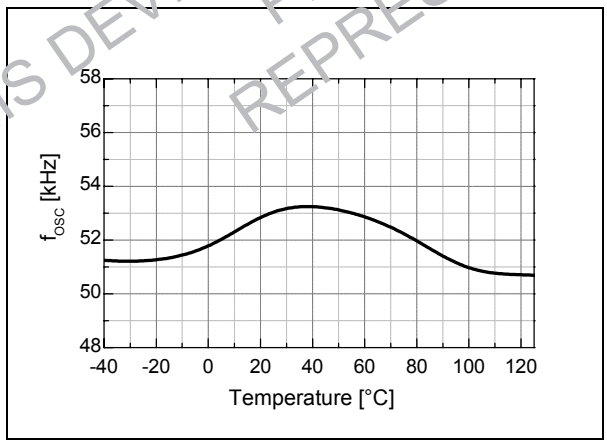


**Figure 14. Running Frequency vs. Temp.**

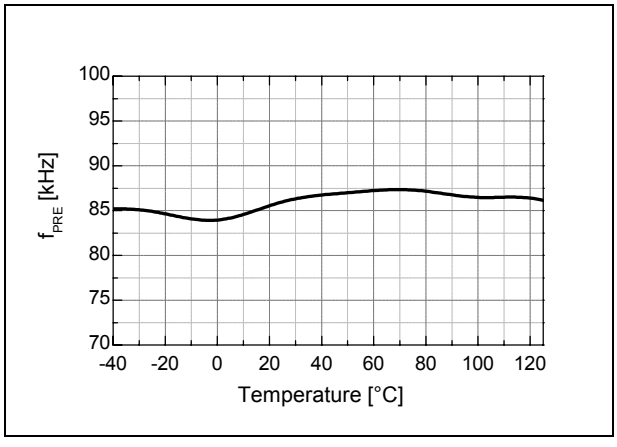


**Figure 15. Preheating Frequency vs. Temp.**

## Typical Characteristics (Continued)

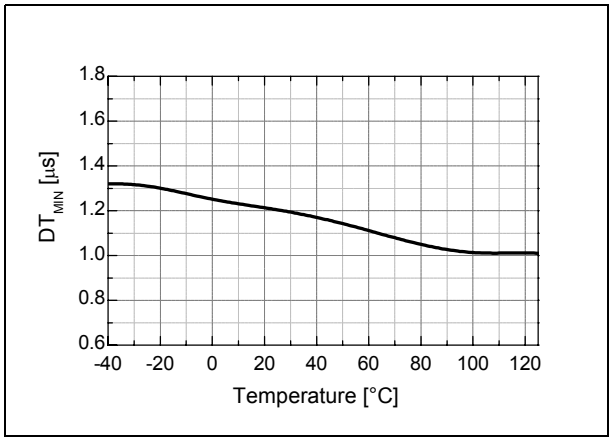


**Figure 16. Minimum Dead Time vs. Temp.**

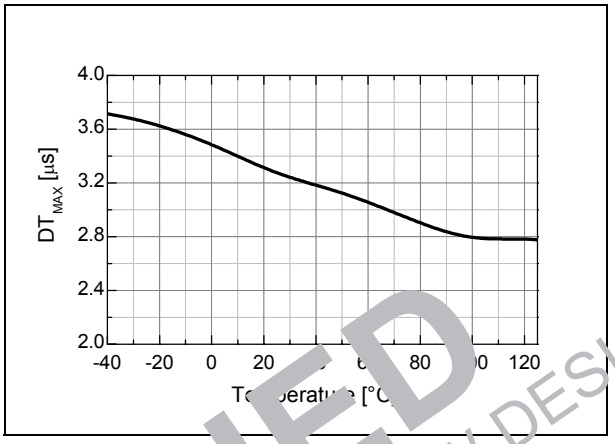


**Figure 17. Maximum Dead Time vs. Temp.**

## Typical Application Information

### 1. Under-Voltage Lockout (UVLO) Function

The FAN7711 has UVLO circuits for both high-side and low-side circuits. When $V_{DD}$ reaches $V_{DDTH(ST+)}$, UVLO is released and the FAN7711 operates normally. At UVLO condition, FAN7711 consumes little current, noted $I_{ST}$. Once UVLO is released, FAN7711 operates normally until $V_{DD}$ goes below $V_{DDTH(ST-)}$, the UVLO hysteresis. At UVLO condition, all latches that determine the status of the IC are reset. When the IC is in the shutdown mode, the IC can restart by lowering $V_{DD}$ below $V_{DDTH(ST-)}$.

FAN7711 has a high-side gate driver circuit. The supply for the high-side driver is applied between $V_B$ and $V_S$. To protect the malfunction of the driver at low supply voltage, between $V_B$ and $V_S$, FAN7711 provides an additional UVLO circuit between the supply rails. If $V_B$-$V_S$ is under $V_{HSTH(ST+)}$, the driver holds low-state to turn off the high-side switch, as shown in Figure 18. As long as $V_B$-$V_S$ is higher than $V_{HSTH(ST-)}$ after $V_B$-$V_S$ exceeds $V_{HSTH(ST+)}$, operation of the driver continues.

### 2. Oscillator

The ballast circuit for a fluorescent lamp is based on the LCC resonant tank and a half-bridge inverter circuit as shown in Figure 18. To accomplish Zero Voltage Switching (ZVS) of the half-bridge inverter circuit, the LCC is driven at a higher frequency than its resonant frequency, which is determined by $L_R$, $C_S$, $C_P$, and $R_L$, where $R_L$ is the equivalent lamp's impedance

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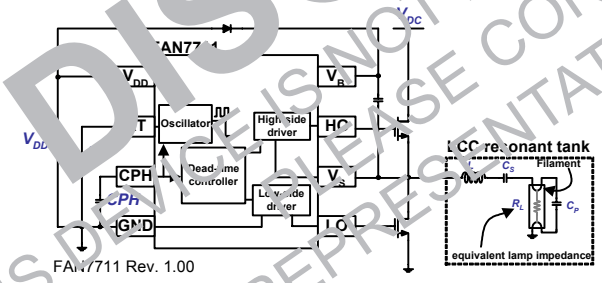



**Figure 18. Resonant Inverter Circuit Based on LCC Resonant Tank**

The transfer function of LCC resonant tank is heavily dependent on the lamp impedance, $R_L$, as illustrated in Figure 19. The oscillator in FAN7711 generates effective driving frequencies to assist lamp ignition and improve lamp life longevity. Accordingly, the oscillation frequency is changed in the following sequence:

*Preheating freq.->Ignition freq.-> Normal running freq*.

Before the lamp is ignited, the lamp impedance is very high. Once the lamp is turned on, the lamp impedance significantly decreases. Since the resonant peak is very high due to the high-resistance of the lamp at the instant of turning on the lamp, the lamp must be driven at higher frequency than the resonant frequency, shown as (A) in Figure 19. In this mode, the current supplied by the inverter mainly flows through $C_P$. $C_P$ connects both filaments and makes the current path to ground. As a result, the current warms up the filament for easy ignition. The amount of the current can be adjusted by controlling the oscillation frequency or changing the capacitance of $C_P$. The driving frequency, $f_{PRE}$, is called preheating frequency and is derived by:

$$f_{PRE} = 6 \times f_{OSC} \quad \text{(EQ 1)}$$

After start-up, the FAN7711 decreases the frequency, shown as (B) of Figure 19. This action increases the voltage of the lamp and helps the fluorescent lamp ignite. The ignition frequency is described as a function of CPH voltage, as follows:

$$f_G = \left[0.3 \times (5\text{-}V_{CPH}) + 1\right] \times f_{OSC} \quad \text{(EQ 2)}$$

where $V_{CPH}$ is the voltage of CPH capacitor.

Equation 2 is valid only when $V_{CPH}$ is between 3V to 5V before FAN7711 enters running mode. Once $V_{CPH}$ reaches 5V, the internal latch records the exit from ignition mode. Unless $V_{DD}$ is below $V_{DDTH(ST-)}$, the preheating and ignition modes appear only once during lamp start transition.

Finally, the lamp is driven at a fixed frequency by an external resistor, $R_T$, shown as (C) of Figure 19. If $V_{DD}$ is higher than $V_{DDTH(ST+)}$ and UVLO is released, the voltage of $R_T$ pin is regulated to 4V. This voltage adjusts the oscillator's control current according to the resistance of $R_T$. Because this current and an internal capacitor set the oscillation frequency, the FAN7711 does not need any external capacitors.

The proposed oscillation characteristic is given by:

$$f_{OSC} = \frac{4 \times 10^9}{RT} \quad \text{(EQ 3)}$$

Even in the active ZVS mode, shown as (D) in Figure 19, the oscillation frequency is not changed. The dead-time is varied according to the resonant tank characteristic.

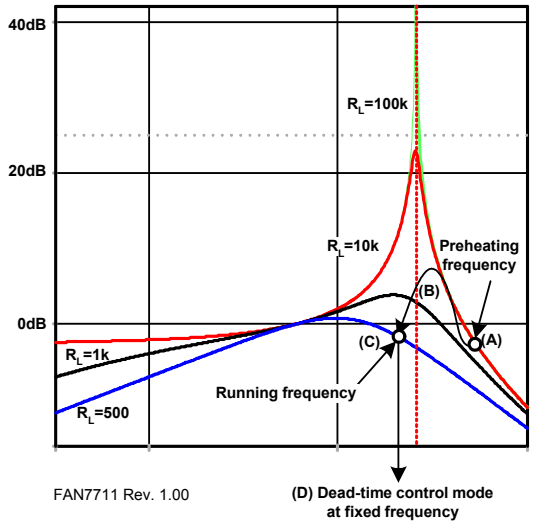



**Figure 19. LCC Transfer Function in Terms of Lamp Impedance**

## 3. Operation Modes

FAN7711 has four operation modes: (A) preheating mode, (B) ignition mode, (C) active ZVS mode, and (D) shutdown mode, depicted in Figure 20. The modes are automatically selected by the voltage on CPH capacitor, shown in Figure 20. In modes (A) and (B), the CPH acts as a timer to determine the preheating and ignition times. After the preheating and ignition modes, the role of the CPH is changed to stabilize the active ZVS control circuit. In this mode, the dead time of the inverter is selected by the voltage of CPH. Only when FAN7711 is in active ZVS mode is it possible to shut off the whole system using CPH pin. Pulling the CPH pin below 2V in active ZVS mode, causes the FAN7711 to enter shutdown mode. In shutdown mode, all active operation is stopped, except UVLO and some bias circuitry. The shutdown mode is triggered by the external CPH control or the active ZVS circuit. The active ZVS circuit automatically detects lamp removal (open-lamp condition) and decreases CPH voltage below 2V to protect the inverter switches from damage.

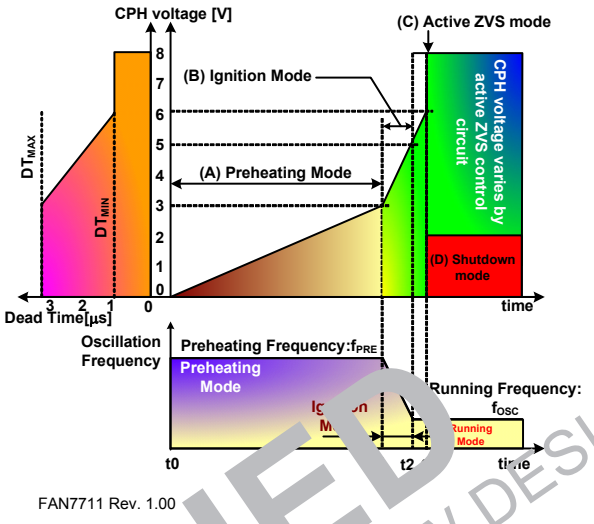



**Figure 20. Operation Modes**

### 3.1 Preheating Mode (t0~t1)

When $V_{DD}$ exceeds $V_{DDTH(ST+)}$, the FAN7711 starts operation. At this time, an internal current source ($I_{PH}$) charges CPH. CPH voltage increases from 0V to 3V in preheating mode. Accordingly, the oscillation frequency follows the Equation 4. In this mode, the lamp is not ignited but warmed up for easy ignition. The preheating time depends on the size of CPH:

$$t_{preheat} = \frac{3 \times CPH}{I_{PH}} \quad [Sec.] \qquad \text{(EQ 4)}$$

According to preheating process, the voltage across the lamp to ignite is reduced and the lifetime of the lamp is increased. In this mode, the dead time is fixed at its maximum value.

### 3.2 Ignition Mode (t1~t2)

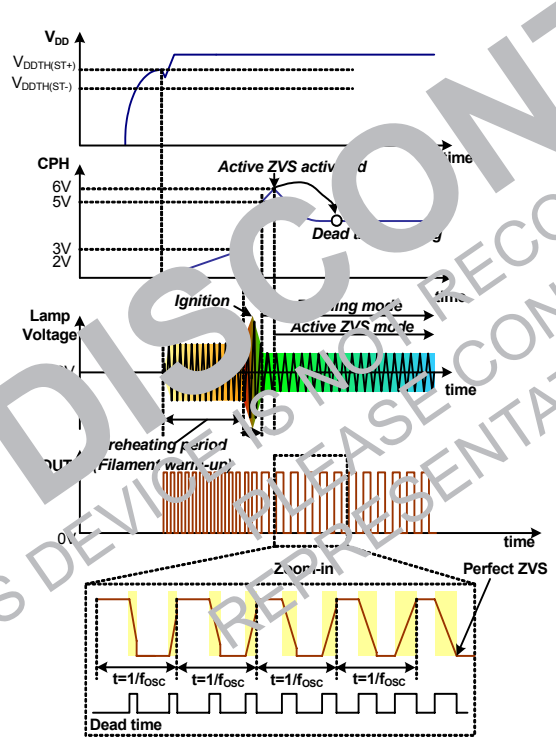
When the CPH voltage exceeds 3V, the internal current source to charge CPH is increased about six times larger than $I_{PH}$, noted as $I_{IG}$, causing rapid increase in CPH voltage. The internal oscillator decreases the oscillation frequency from $f_{PRE}$ to $f_{OSC}$ as CPH voltage increases. As depicted in Figure 20, lowering the frequency increases the voltage across the lamp. Finally, the lamp ignites. Ignition mode is defined when CPH voltage lies between 3V and 5V. Once CPH voltage reaches 5V, the FAN7711 does not return to ignition mode, even if the CPH voltage is in that range, until the FAN7711 restarts from below $V_{DDTH(ST-)}$. Since the ignition mode continues when CPH is from 3V to 5V, the ignition time is given by:

$$t_{ignition} = \frac{2 \times CPH}{I_{IG}} \quad [Sec.] \qquad \text{(EQ 5)}$$

In this mode, dead time varies according to the CPH voltage.

### 3.3 Running and Active Zero-Voltage Switching (AZVS) Modes (t2~)

When CPH voltage exceeds 5V, the operating frequency is fixed to $f_{OSC}$ by $R_T$. However, active ZVS operation is not activated until CPH reaches ~6V. The FAN7711 prepares for active ZVS operation from the instant CPH exceeds 5V during t2 to t3. When CPH becomes higher than ~6V at t3, the active ZVS operation is activated. To determine the switching condition, FAN7711 detects the transition time of the output ($V_S$ pin) of the inverter by using VB pin. From the output-transition information, FAN7711 controls the dead time to meet the ZVS condition. If ZVS is satisfied, the FAN7711 slightly increases the CPH voltage to reduce the dead time and to find optimal dead time, which increases the efficiency and decreases the thermal dissipation and EMI of the inverter switches. If ZVS fails, the FAN7711 decreases CPH voltage to increase the dead time. CPH voltage is adjusted to meet optimal ZVS operation. During the active ZVS mode, the amount of the charging/ discharging current is the same as $I_{PH}$. Figure 21 depicts normal operation waveforms.

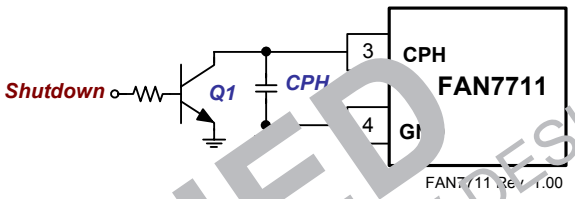



FAN7711 Rev. 1.00

**Figure 21. Typical Transient Waveform from Preheating to Active ZVS Mode**

### 3.4 Shutdown Mode

If the voltage of capacitor CPH is decreased below ~2.6V by an external application circuit or internal protection circuit, the IC enters shutdown mode. Once the IC enters shutdown mode, this status continues until an internal latch is reset by decreasing $V_{DD}$ below $V_{DDTH(ST-)}$. Figure 22 shows an example of external shutdown control circuit.




FAN7711 Rev. 1.00

**Figure 22. External Shutdown Circuit**

The amount of the CPH charging current is the same as $I_{PH}$, making it possible to shut off the IC using small signal transistor. FAN7711 provides active ZVS operation by controlling the dead time according to the voltage of CPH. If ZVS fails even at the maximum dead time, FAN7711 stops driving the inverter.

The FAN7711 thermal shutdown circuit senses the junction temperature of the IC. If the temperature exceeds ~160°C, the thermal shutdown circuit stops operation of the FAN7711.

The current usages of shutdown mode and under-voltage lockout status are different. In shutdown mode, some circuit blocks, such as bias circuits, are kept alive. Therefore, the current consumption is slightly higher than during under-voltage lockout.

### 4. Automatic Open-Lamp Detection

FAN7711 can automatically detect the open-lamp condition. When the lamp is opened, the resonant tank fails to make a closed-loop to the ground, as shown in Figure 23. The supplied current from the $V_S$ pin is used to charge and discharge the charge pump capacitor, $C_P$. Since the open-lamp condition means resonant tank absence, it is impossible to meet ZVS condition. In this condition, the power dissipation of the FAN7711, due to capacitive load drive, is estimated as:

$$P_{Dissipation} = \frac{1}{2} \times C_P \times V_{DC}{}^2 \times f \quad [W] \qquad \text{(EQ 6)}$$

where $f$ is driving frequency and $V_{DC}$ is DC-link voltage.

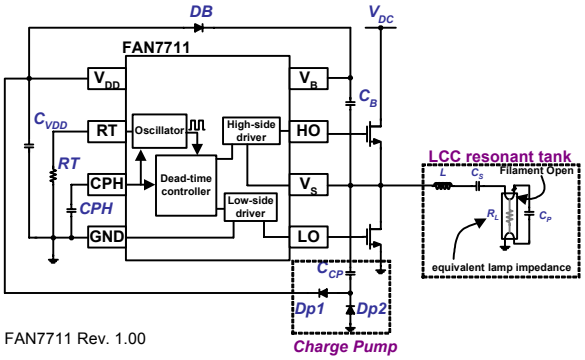



**Figure 23. Current Flow When the Lamp is Open**

Assuming that $C_P$, $V_{DC}$, and f are 1nF, 311V, and 50kHz, respectively; the power dissipation reaches about 2.4W and the temperature of FAN7711 is increased rapidly. If no protection is provided, the IC can be damaged by the thermal attack. Note that hard-switching condition during the capacitive-load drive causes lots of EMI.

Figure 24 illustrates the waveforms during the ope lamp condition. In this condition, the charging and discharging current of $C_P$ is directly determined by FAN7711 and considered hard-switching condition. The FAN7711 tries to meet ZVS condition by decreasing CPH voltage to increase dead time. If ZVS fails and CPH goes below 2V, even though the dead time reaches its maximum value, FAN7711 shuts off the IC to protect against damage. To restart FAN7711, $V_{DD}$ must be below $V_{DDTH(ST-)}$. There is an internal latch circuit, which remembers the status of the

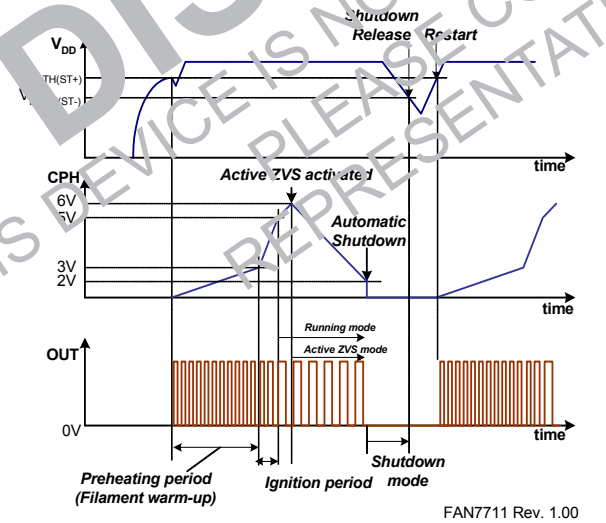



**Figure 24. CPH Voltage Variation in Open-Lamp Condition**

## 5. Power Supply

When $V_{DD}$ is lower than $V_{DDTH(ST+)}$, it consumes very little current, $I_{ST}$, making it possible to supply current to the $V_{DD}$ pin using a resistor with high resistance ($R_{start}$ in Figure 25). Once UVLO is released, the current consumption is increased and whole circuits are operated, which requires additional power supply for stable operation. The supply must deliver at least several mA. A charge pump circuit is a cost-effective method to create an additional power supply and allows $C_P$ to be used to reduce the EMI.

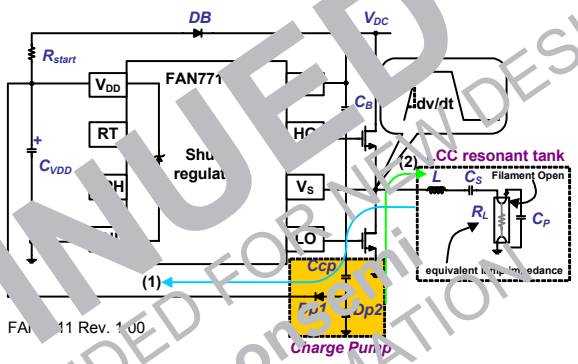



**Figure 25. Local Power Supply for $V_{DD}$ Using a Charge Pump Circuit**

As presented in Figure 25, when $V_S$ is high, the inductor current and $C_{CP}$ create an output transition with the slope of dv/dt. The rising edge of $V_S$ charges $C_{CP}$. At that time, the current that flows through $C_{CP}$ is:

$$I \cong C_{CP} \times \frac{dv}{dt} \qquad \text{(EQ 7)}$$

This current flows along the path (1). It charges $C_{VDD}$, which is a bypass capacitor to reduce the noise on the supply rail. If $C_{VDD}$ is charged over the threshold voltage of the internal shunt regulator, the shunt regulator is turned on and regulates $V_{DD}$ with the trigger voltage.

When $V_S$ is changing from high to low state, $C_{CP}$ is discharged through Dp2, shown as path (2) in Figure 26. These charging/discharging operations are continued until FAN7711 is halted by shutdown operation. The charging current, I, must be large enough to supply the operating current of FAN7711.

The supply for the high-side gate driver is provided by the boot-strap technique, as illustrated in Figure 26. When the low-side MOSFET connected between $V_S$ and GND pins is turned on, the charging current for $V_B$ flows through $D_B$. Every low $V_S$ gives the chance to charge the $C_B$. Therefore $C_B$ voltage builds up only when FAN7711 operates normally.

When $V_S$ goes high, the diode $D_B$ is reverse-biased and $C_B$ supplies the current to the high-side driver. At this time, since $C_B$ discharges, $V_B$-$V_S$ voltage decreases. If $V_B$-$V_S$ goes below $V_{HSTH(ST-)}$, the high-side driver cannot operate due to the high-side UVLO protection circuit. $C_B$ must be chosen to be large enough not to fall into UVLO range due to the discharge during a half of the oscillation period, especially when the high-side MOSFET is turned on.

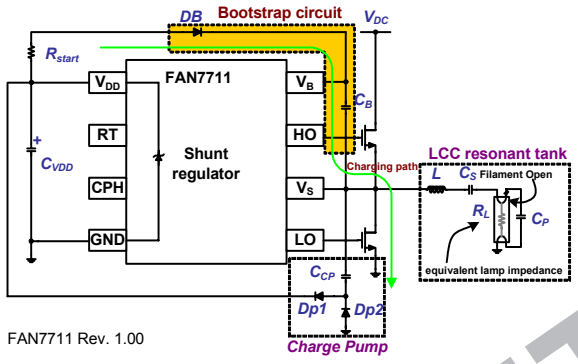



**Figure 26. Implementation of Floating Power Supply Using the Bootstrap Method**

## Design Guide

### 1. Start-up Circuit

The start-up current ($I_{ST}$) is supplied to the IC through the start-up resistor, $R_{start}$. Once operation starts, the power is supplied by the charge pump circuit. To reduce the power dissipation in $R_{start}$, select $R_{start}$ as high as possible, considering the current requirements at start-up. For $220V_{AC}$ power, the rectified voltage by the full-wave rectifier makes DC voltage, as shown in Equation 8. The voltage contains lots of AC component due to poor regulation characteristic of the simple full-wave rectifier:

$$V_{DC} = \sqrt{2} \times 220[V] \cong 311[V] \quad \text{(EQ 8)}$$

Considering the selected parameters, $R_{start}$ must satisfy the following equation:

$$\frac{V_{DC} - V_{DDTH(ST+)}}{R_{start}} > I_{ST} \quad \text{(EQ 9)}$$

From Equation 9, $R_{start}$ is selected as:

$$\frac{V_{DC} - V_{DDTH(ST+)}}{I_{ST}} > R_{start} \quad \text{(EQ 10)}$$

Note that if choosing the maximum $R_{start}$ takes long time for $V_{DD}$ to reach $V_{DDTH(st+)}$. Considering $V_{DD}$ g time, $R_{start}$ must be selected as shown in Figure 30.

Another important conce[illegible]r choosing $R_{start}$ is the available power rating of $R_{start}$. To [illegible] commercially available, low-co[illegible]1/4W resistor, $R_{start}$ must obey the following rule:

$$\frac{(V_{DC} - V_{CL})^2}{R_{start}} < \frac{1}{4}[W] \quad \text{(EQ 11)}$$

Assuming $V_{DC}$=311V and $V_{CL}$=15V, the minimum resistance of $R_{start}$ is about 350kΩ.

When the IC operates in shutdown mode due to thermal protection, open-lamp protection, or hard-switching protection, the IC consumes shutdown current, $I_{SD}$, which is larger than $I_{ST}$. To prevent restart during this mode, $R_{start}$ must be selected to cover $I_{SD}$ current consumption. The following equation must be satisfied:

$$\frac{V_{DC} - V_{DDTH(ST+)}}{I_{SD}} > R_{start} \quad \text{(EQ 12)}$$

From Equations 10 - 12; it is possible to select $R_{start}$:

*(1) For safe start-up without restart in shutdown mode:*

$$4(V_{DC} - V_{CL})^2 < R_{start} < \frac{V_{DC} - V_{DDTH(ST+)}}{I_{SD}} \quad \text{(EQ 13)}$$

*(2) For safe start-up with restart from shutdown mode:*

$$\frac{V_{DC} - V_{DDTH(ST+)}}{I_{SD}} < R_{start} < \frac{V_{DC} - V_{DDTH(ST+)}}{I_{ST}} \quad \text{(EQ 14)}$$

If $R_{start}$ meets Equation 14, restart operation is possible. However, it is not recommended to choose $R_{start}$ at that range because $V_{DD}$ rising time could be long and it increases the lamp's turn-on delay time, as depicted in Figure 27.

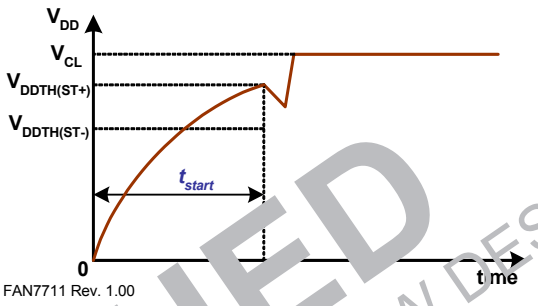



**Figure 27. $V_{DD}$ Build-up**

Figure 28 shows the equivalent circuit for estimating $t_{start}$ for circuit analysis. $V_{DD}$ variation versus time is given by:

$$V_{DD}(t) = (V_{DC} - R_{start} \cdot I_{ST})\left(1 - e^{-t/(R_{start} \cdot C_{VDD})}\right) \quad \text{(EQ 15)}$$

where $C_{VDD}$ is the total capacitance of the bypass capacitors connected between $V_{DD}$ and GND.

From Equation 15, it is possible to calculate $t_{start}$ by substituting $V_{DD(t)}$ with $V_{DDTH(ST+)}$:

$$t_{start} = -R_{start} \cdot C_{VDD} \cdot \ln\frac{V_{DC} - R_{start} \cdot I_{ST} - V_{DDTH(ST+)}}{V_{DD} - R_{start} \cdot I_{ST}} \quad \text{(EQ 16)}$$

In general, Equation 16 can be simplified as:

$$t_{start} \approx \frac{R_{start} \cdot C_{VDD} \cdot V_{DDTH(ST+)}}{V_{DC} - R_{start} \cdot I_{ST} - V_{DDTH(ST+)}} \quad \text{(EQ 17)}$$

Accordingly, $t_{start}$ can be controlled by adjusting the value of $R_{start}$ and $C_{VDD}$. For example, if $V_{DC}$=311V, $R_{start}$=560k, $C_{VDD}$=10μF, $I_{st}$=120μA, and $V_{DDTH(ST+)}$= 13.5V, $t_{start}$ is about 0.33s.

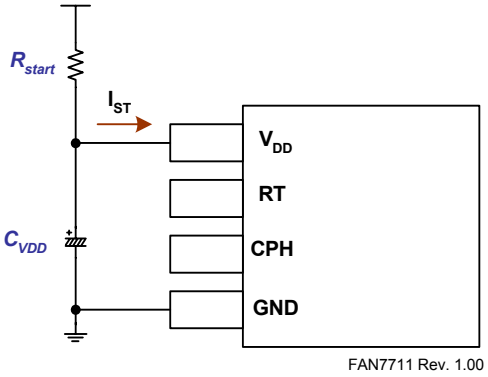



**Figure 28. Equivalent Circuit During Start**

## 2. Current Supplied by Charge Pump

For the IC supply, the charge pump method is used in Figure 29. Since $C_{CP}$ is connected to the half-bridge output, the supplied current by $C_{CP}$ to the IC is determined by the output voltage of the half-bridge.

When the half-bridge output shows rising slope, $C_{CP}$ is charged and the charging current is supplied to the IC. The current can be estimated as:

$$I = C_{CP}\frac{dV}{dt} \approx C_{CP}\frac{V_{DC}}{DT} \qquad \text{(EQ 18)}$$

where DT is the dead time and dV/dt is the voltage variation of the half-bridge output.

When the half-bridge shows falling slope, $C_{CP}$ is discharged through Dp2. Total supplied current, $I_{total}$, to the IC during switching period, t, is:

$$I_{total} = I \cdot DT = C_{CP} \cdot V_{DC} \qquad \text{(EQ 19)}$$

From Equation 19, the average current, $I_{avg}$, supplied to the IC is obtained by:

$$I_{avg} = \frac{I_{total}}{t} = \frac{C_{CP} \cdot V_{DC}}{t} = C_{CP} \cdot V_{DC} \cdot f \qquad \text{(EQ 20)}$$

For the stable operation, $I_{avg}$ must be higher than the required current. If $I_{avg}$ exceeds the required current, the residual current flows through the shunt regulator implemented on the chip, which can cause unwanted heat generation. Therefore, $C_{CP}$ must be selected considering stable operation and thermal generation.

For example, if $C_{CP}$=0.5nF, $V_{DC}$=311V, and f=50kHz, $I_{avg}$ is 7.8mA. It is enough current for stable operation.

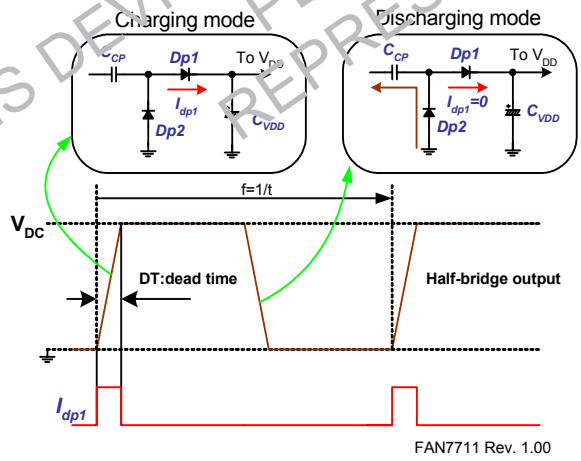



**Figure 29. Charge Pump Operation**

## 3. Lamp Turn-on Time

The turn-on time of the lamp is determined by supply build-up time $t_{start}$, preheating time, and ignition time; where $t_{start}$ has been obtained by Equation 17. When the IC's supply voltage exceeds $V_{DDTH(ST+)}$ after turn-on or restart, the IC operates in preheating mode. This operation continues until CPH pin's voltage reaches ~3V. In this mode, CPH capacitor is charged by $I_{PH}$ current, as depicted in Figure 30. The preheating time is achieved by calculating:

$$t_{preheat} = 3\frac{CPH}{I_{PH}} \qquad \text{(EQ 21)}$$

The preheating time is related to lamp life (especially filament); therefore, the characteristics of a given lamp should be considered when choosing the time.

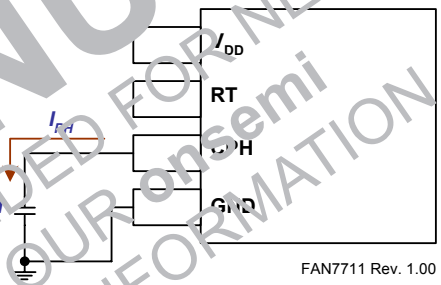



**Figure 30. Preheating Timer**

Compared to the preheating time, it is almost impossible to exactly predict the ignition time, whose definition is the time from the end of the preheating time to ignition. In general, the lamp ignites during the ignition mode. Therefore, assume that the maximum ignition time is the same as the duration of ignition mode, from 3V until CPH reaches 5V. Thus, ignition time can be defined as:

$$t_{ignition} = (5-3)\frac{CPH}{I_{IG}} = 2\frac{CPH}{I_{IG}} \qquad \text{(EQ 22)}$$

Note that, at ignition mode, CPH is charged by $I_{IG}$, which is six times larger than $I_{PH}$. Consequently, total turn-on time is approximately:

*VDD Build-Time + Preheating Time + Ignition Time =*

$$t_{ignition} = (5-3)\frac{CPH}{I_{IG}} = 2\frac{CPH}{I_{IG}}\ [Sec.] \qquad \text{(EQ 23)}$$

## 4. PCB Guideline

Component selection and placement on PCB is important when using power control ICs. Bypass the $V_{CC}$ to GND as close to the IC terminals as possible with a low-ESR/ESL capacitor, as shown in Figure 31. This bypassed capacitor ($C_{BP}$) can reduce the noise from the power supply parts, such as start-up resistor and charge pump.

The signal GND must be separated from the power GND. So, the signal GND should be directly connected to the rectify capacitor using an individual PCB trace.

In addition, the ground return path of the timing components ($C_{PH}$, $R_T$) and $V_{DD}$ decoupling capacitor should be connected directly to the IC GND lead and not via separate traces or jumpers to other ground traces on the board. These connection techniques prevent high-current ground loops from interfering with sensitive timing component operations and allow the control circuit to reduce common-mode noise due to output switching.

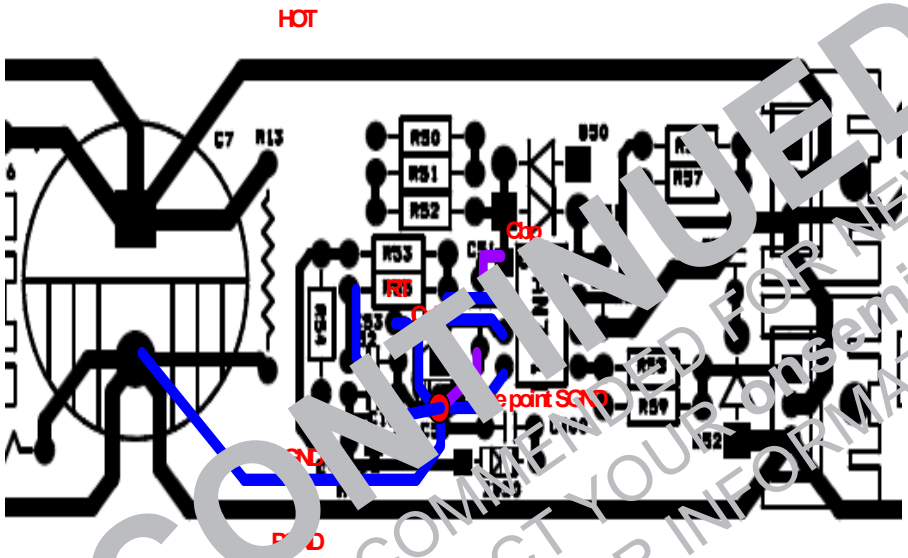
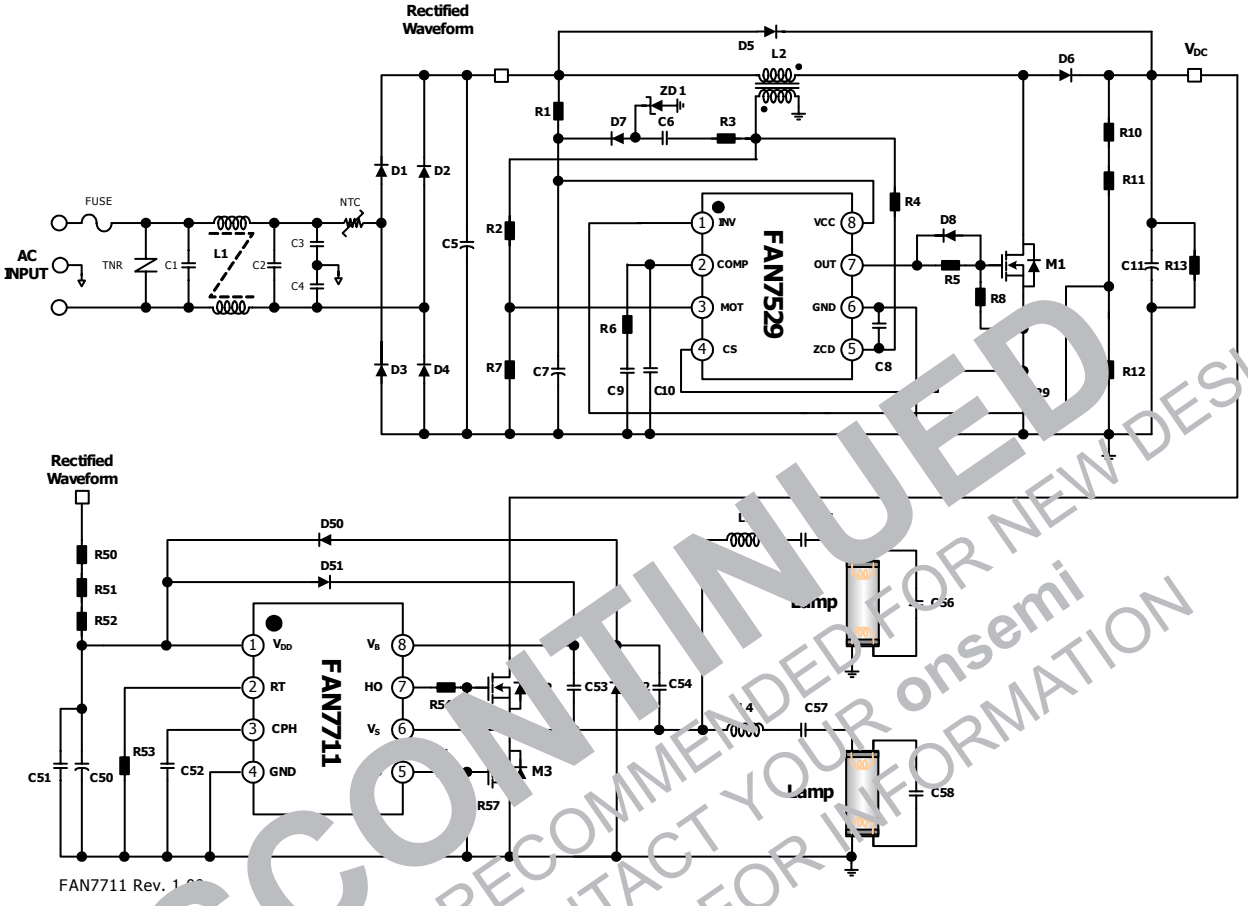



Figure 31. Preheating Timer

## Typical Application Diagram




FAN7711 Rev. 1.0.0

**Figure 32. Application Circuit of 32W Two Lamps**

## Component List for 32W Two Lamps

| Part | Value | Note |
|---|---|---|
| **Resistor** | | |
| R1 | 330kΩ | 1/2W |
| R2 | 750kΩ | 1/4W |
| R3 | 100Ω | 1/2W |
| R4 | 20kΩ | 1/4W |
| R5 | 47Ω | 1/4W |
| R6 | 10kΩ | 1/4W |
| R7 | 50kΩ | 1/4W |
| R8 | 47kΩ | 1/4W |
| R9 | 0.3Ω | 1W |
| R10 | 1MΩ | 1/4W |
| R11 | 1MΩ | 1/4W |
| R12 | 12.6kΩ | 1/4W,1% |
| R13 | 220kΩ | 2W |
| R50 | 150kΩ | 1/4W |
| R51 | 150kΩ | 1/4W |
| R52 | 150kΩ | 1/4W |
| R53 | 90kΩ | 1/4W,1% |
| R54 | 10Ω | 1/4W |
| R55 | 47Ω | 1/4W |
| R56 | 47kΩ | 1/4W |
| R57 | 47Ω | 1/4W |
| R58 | 47kΩ | 1/4W |
| **Capacitor** | | |
| C1 | 47nF/275V$_{AC}$ | Box Capacitor |
| C2 | 100nF/275V$_{AC}$ | Box Capacitor |
| C3 | 2200pF/3kV | Ceramic Capacitor |
| C4 | 2200pF/3kV | Ceramic Capacitor |
| C5 | 0.22μF/630V | Miller Capacitor |
| C6 | 12nF/50V | Ceramic Capacitor |
| C7 | 22μF/50V | Electrolytic Capacitor |
| C8 | 39pF/50V | Ceramic Capacitor |
| C9 | 1μF/50V | Ceramic Capacitor |
| C10 | 0.1μF/50V | Ceramic Capacitor |
| C11 | 47μF/450V | Electrolytic Capacitor |
| C50 | 10μF/50V | Electrolytic Capacitor |
| C51 | 1μF/50V | Ceramic Capacitor |
| C52 | 0.47μF/25V | Ceramic Capacitor,5% |
| C53 | 100nF/50V | Ceramic Capacitor |
| C54 | 470pF/1kV | Ceramic Capacitor |
| C55 | 15nF/630V | Miller Capacitor |
| C56 | 2.7nF/1kV | Miller Capacitor |
| C57 | 15nF/630V | Miller Capacitor |
| C58 | 2.7nF/1kV | Miller Capacitor |
| **Diode** | | |
| D1 | 1N4007 | 1kV,1A |
| D2 | 1N4007 | 1kV,1A |
| D3 | 1N4007 | 1kV,1A |
| D4 | 1N4007 | 1kV,1A |
| D5 | UF4007 | Ultra Fast,1kV,1A |
| D6 | UF4007 | Ultra Fast,1kV,1A |
| D7 | 1N4148 | 100V,1A |
| D8 | 1N4148 | 100V,1A |
| D50 | UF4007 | Ultra Fast,1kV,1A |
| D51 | UF4007 | Ultra Fast,1kV,1A |
| D52 | UF4007 | Ultra Fast,1kV,1A |
| ZD1 | 1N4746A | Zener 18V, 1W |
| **MOSFET** | | |
| M1 | FQPF5N60C | 500V,6A |
| M2 | FQPF5N50C | 500V,5A |
| M3 | FQPF5N50C | 500V,5A |
| **Fuse** | | |
| Fuse | 3A/250V | |
| **TNR** | | |
| TNR | 471 | |
| | | |
| **NTC** | | |
| NTC | 10D-09 | |
| **Line Filter** | | |
| LF1 | 40mH | |
| **Transformer** | | |
| L1 | 0.94mH(75T:10T) | EI2820 |
| **Inductor** | | |
| L2 | 3.2mH(130T) | EI2820 |
| L3 | 3.2mH(130T) | EI2820 |
| **IC** | | |
| U1 | FAN7711 | Fairchild Semiconductor |
| U2 | FAN7529 | Fairchild Semiconductor |
| | | |
| | | |

## Component List for 20W CFL

| Part | Value | Note |
|---|---|---|
| **Resistor** | | |
| R1 | 470kΩ | 1/4W |
| R2 | 90kΩ | 1/4W |
| R3 | 10Ω | 1/4W |
| R4 | 47Ω | 1/4W |
| R5 | 47Ω | 1/4W |
| | | |
| **Capacitor** | | |
| C1 | 22µF/250V | Electrolytic Capacitor |
| C2 | 10µF/50V | Electrolytic Capacitor |
| C3 | 470nF/25V | Miller Capacitor |
| C4 | 100nF/25V | Miller Capacitor |
| C5 | 470pF/630V | Miller Capacitor |
| C6 | 33nF/630V | Miller Capacitor |
| C7 | 3.3nF/1kV | Miller Capacitor |

| Part | Value | Note |
|---|---|---|
| **Diode** | | |
| D1 | 1N4007 | 1kV/1A |
| D2 | 1N4007 | 1kV/1A |
| D3 | 1N4007 | 1kV/1A |
| D4 | 1N4007 | 1kV/1A |
| D5 | UF4007 | 1kV/1A,Ultra Fast |
| D6 | UF4007 | 1kV/1A,Ultra Fast |
| D7 | UF4007 | 1kV/1A,Ultra Fast |
| **Inductor** | | |
| L1 | 2.5mH (28T) | EE16.6S |
| **MOSFET** | | |
| Q1 | FQPF1N50C | 500V,1A |
| Q2 | FQPF1N50C | 500V,1A |
| **IC** | | |
| U1 | FAN7711 | Fairchild Semiconductor |

**Note:**
3. Refer to the typical application circuit provided in figure 1.

## Package Dimensions

### 8-SOP

Dimensions are in millimeters unless otherwise noted.

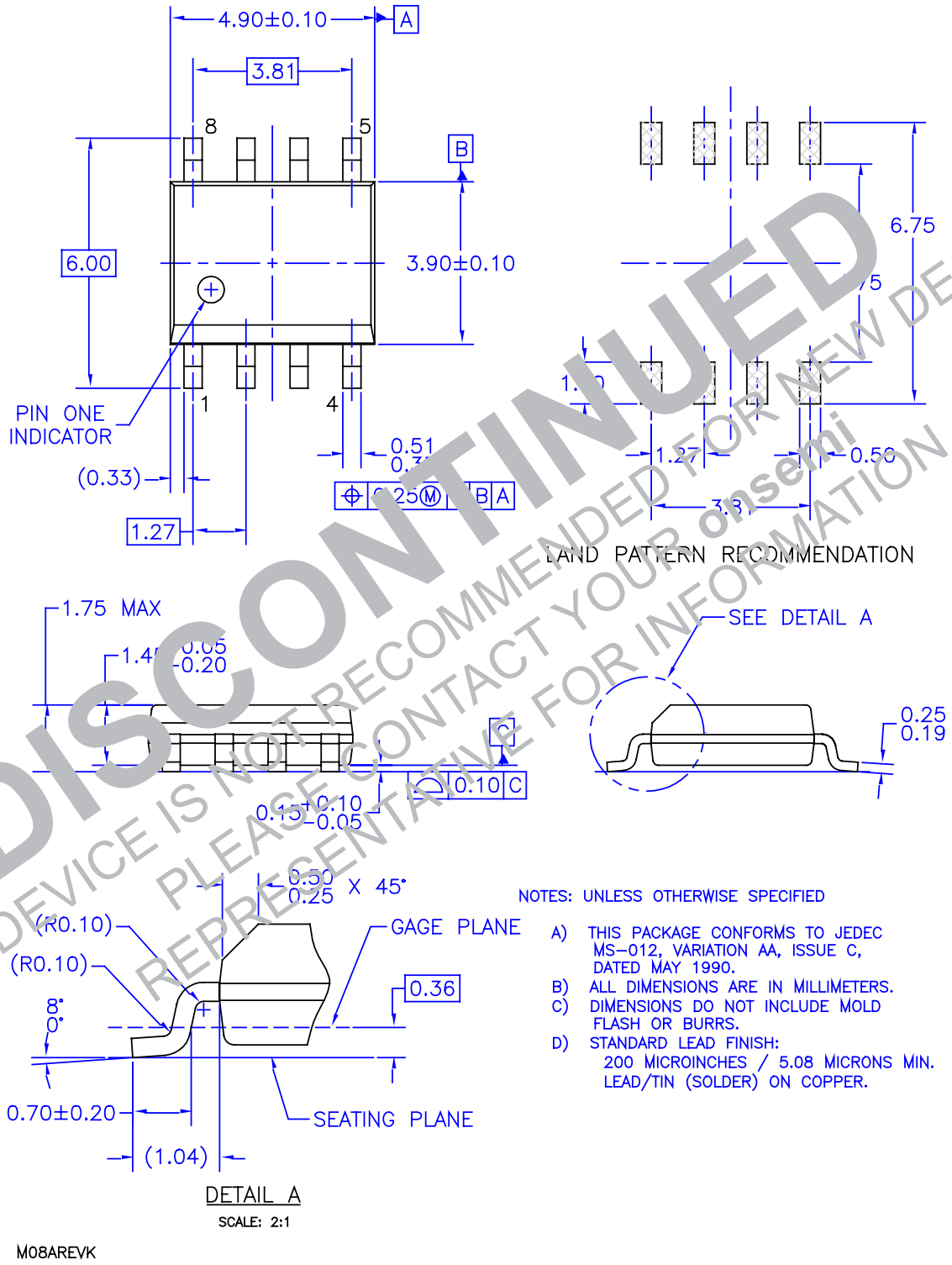


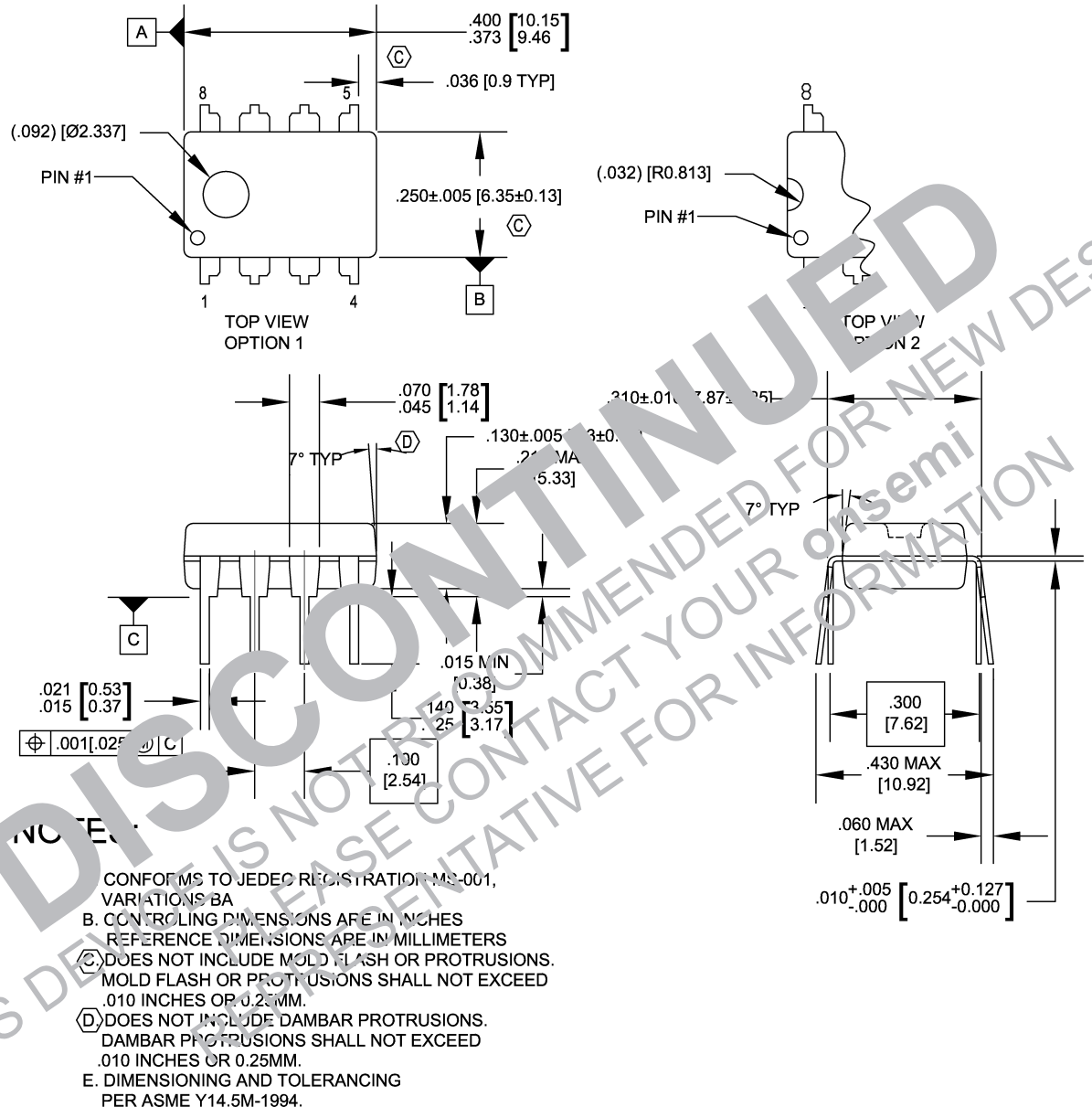



**Figure 33. 8-Lead Small Outline Package (SOP)**

## Package Dimensions

### 8-DIP

Dimensions are in inches and [millimeters] unless otherwise noted.




NOTES:

CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS BA

B. CONTROLING DIMENSIONS ARE IN INCHES REFERENCE DIMENSIONS ARE IN MILLIMETERS

C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.

D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.

E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

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**Figure 34. 8-Lead Dual In-Line Package (DIP)**

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Power-SPM™
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QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
ScalarPump™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
Sup[illegible]T™-[illegible]
[illegible]ync[illegible]™
[illegible]™
The Pow[illegible] Franchise®
[illegible]™
TinyBoost™
TinyBuck™
TinyLogic®
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UH[illegible]
U[illegible]FET™
VC[illegible]™
[illegible]Wire

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