FAIRCHILD SEMICONDUCTOR®

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FAN5365
1A / 0.8A, 6MHz Digitally Programmable Regulator

Features

- High Efficiency (>88%) at 6MHz
- 800mA or 1A Output Current
- Regulation Maintained with V_{IN} from 2.3V to 5.5V
- 6-Bit V_{OUT} Programmable from 0.75 to 1.975V
- 6MHz Fixed-Frequency Operation (PWM Mode)
- Excellent Load and Line Transient Response
- Small Size, 470nH Inductor Solution
- ±2% DC Voltage Accuracy in PWM Mode
- 25ns Minimum On-Time
- High-Efficiency, Low-Ripple, Light-Load PFM
- Smooth Transition between PWM and PFM
- 40µA Operating PFM Quiescent Current
- I²C™-Compatible Interface up to 3.4Mbps
- Pin-Selectable or I²C™ Programmable Output Voltage
- 9-Bump, 1.27 x 1.29mm, 0.4mm Pitch WLCSP Package

Applications

- 3G, WiFi®, WiMAX™, and WiBro® Data Cards
- Netbooks®, Ultra-Mobile PCs
- SmartReflex™-Compliant Power Supply
- Split Supply DSPs and µP Solutions OMAP™, XSCALE™
- Handset Graphic Processors (NVIDIA®, ATI)

Description

The FAN5365 is a high-frequency, ultra-fast transient response, synchronous step-down, DC-DC converter optimized for low-power applications using small, low-cost inductors and capacitors. The FAN5365 supports up to 800mA or 1A load current.

The FAN5365 is ideal for mobile phones and similar portable applications powered by a single-cell Lithium-Ion battery. With an output voltage range adjustable via I²C™ interface from 0.75V to 1.975V, it supports low-voltage DSPs and processors, core power supplies, and memory modules in smart phones, data cards, and hand-held computers.

The FAN5365 operates at 6MHz (nominal) fixed switching frequency in PWM mode.

During light-load conditions, the regulator includes a PFM mode to enhance light-load efficiency. The regulator transitions smoothly between PWM and PFM modes with no glitches on V_{OUT}. In hardware shutdown, the current consumption is reduced to less than 200nA.

The serial interface is compatible with fast / standard mode, fast mode plus, and high-speed mode I²C specifications, allowing transfers up to 3.4Mbps. This interface is used for dynamic voltage scaling with 12.5mV voltage steps, for reprogramming the mode of operation (PFM or forced PWM), or to disable/enable the output voltage.

The chip's advanced protection features include short-circuit protection and current and temperature limits. During a sustained over-current event, the IC shuts down and restarts after a delay to reduce average power dissipation into a fault.

During startup, the IC controls the output slew rate to minimize input current and output overshoot at the end of soft-start. The IC maintains a consistent soft-start ramp, regardless of output load during startup.

The FAN5365 is available in a 1.27 x 1.29mm, 9-bump WLCSP package.

Ordering Information

Part Number[1]	Option	Slave Address LSB			Output Current	V_{OUT} Programming		Power-up Defaults		Package
		A2	A1	A0	mA	Min.	Max.	VSEL0	VSEL1	
FAN5365UC00X	00	0	1	0	800	0.7500	1.4375[3]	1.05	1.20	WLCSP-09
FAN5365UC02X	02	1	1	0	800	0.7500	1.4375[3]	0.95	1.10	WLCSP-09
FAN5365UC03X[2]	03	0	0	0	1000	0.7500	1.5375	1.00	1.20	WLCSP-09
FAN5355UC06X[2]	06	0	0	0	1000	1.1875	1.9750	1.80	1.80	WLCSP-09

Notes:
1. The “X” designator on the part number indicates tape and reel packaging.
2. Preliminary; not full production release at this time. Contact a Fairchild representative for information.
3. V_{OUT} is limited to the maximum voltage for all VSEL codes greater than the maximum V_{OUT} listed.

Typical Application

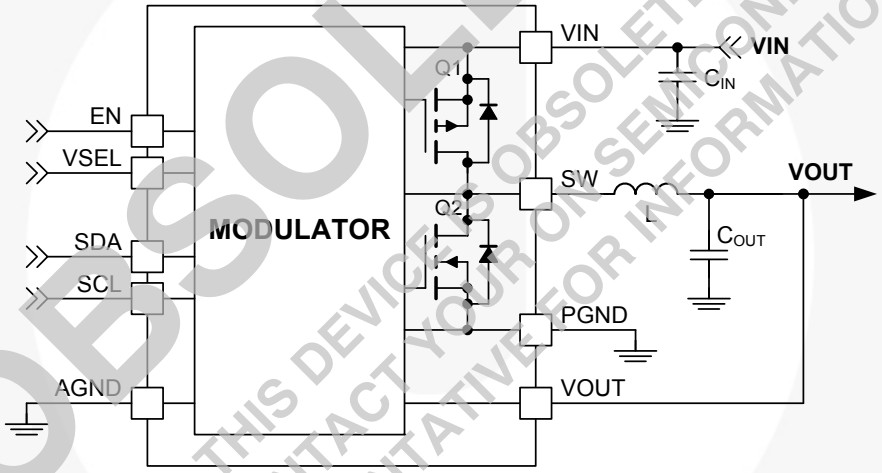

Figure 1. Typical Application

Table 1. Recommended External Components

Component	Description	Vendor	Parameter	Min.	Typ.	Max.	Units
L (L_{OUT})	470nH Nominal	Murata, TDK, FDK	L[4]	390	470	600	nH
			DCR (Series R)		80		mΩ
C_{OUT}[5]	0603 (1.6x0.8x0.8), 10µF X5R	Various	C[6]	2.2	10.0	15.0	µF
C_{IN}	0402 (1x0.5x0.25), 4.7µF X5R	Taiyo-Yuden		1.6	4.7		µF

Notes:
4. Minimum L incorporates tolerance, temperature, and partial saturation effects (L decreases when increasing current).
5. A capacitor similar to C_{IN} can be used for C_{OUT}. With 1.4V of bias, a 4.7µF 0402 capacitor minimum value is 2.5µF. The regulator is stable, but transient response degraded due to large signal effects.
6. Minimum C is a function of initial tolerance, maximum temperature, and the effective capacitance being reduced due to frequency, dielectric, and voltage bias effects. C_{IN} is biased with a higher voltage which reduces its effective capacitance by a larger amount.

Pin Configuration

Bumps Facing Down **Bumps Facing Up**

Figure 2. WLCSP-09, 0.4mm Pitch

Pin Definitions

Pin #	Name	Description
A1	VSEL	**Voltage Select**. When HIGH, V_{OUT} is set by VSEL1. When LOW, V_{OUT} is set by VSEL0. This behavior can be overridden through I^2C register settings. This pin should not be left floating.
A2	VIN	**Input Voltage**. Connect to input power source. The connection from this pin to C_{IN} should be as short as possible.
A3	SDA	**SDA**. I^2C interface serial data. This pin should not be left floating.
B1	SW	**Switching Node**. Connect to output inductor.
B2	SCL	**SCL**. I^2C interface serial clock. This pin should not be left floating.
B3	EN	**Enable**. When this pin is HIGH, the circuit is enabled. When LOW, part enters shutdown mode and input current is minimized. This pin should not be left floating.
C1	VOUT	**Output Voltage Monitor**. Tie this pin to the output voltage at C_{OUT}. This is a signal input pin to the control circuit and does not carry DC current.
C2	PGND	**Power GND**. Power return for gate drive and power transistors. Connect to AGND on PCB. The connection from this pin to the bottom of C_{IN} should be as short as possible.
C3	AGND	**Analog GND**. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin. AGND should be connected to PGND at a single point.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V_{CC}	VIN, SW Pins		–0.3	6.5	V
	V_{OUT}		–0.3	2.5	
	Other Pins		–0.3	V_{IN} + 0.3[7]	
ESD	Electrostatic Discharge Protection	Human Body Model, JESD22-A114	3		KV
		Charged Device Model, JESD22-C101	1		
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:

7. Lesser of 6.5V or V_{CC}+0.3V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{IN}	Supply Voltage	2.3	5.5	V
V_{CCIO}	SDA and SCL Voltage Swing[8]	1.2	2.0	V
T_A	Ambient Temperature	–40	+85	°C
T_J	Junction Temperature	–40	+125	°C

Note:

8. The I^2C interface operates with $t_{HD;DAT}$ = 0 as long as the pull-up voltage for SDA and SCL is less than 2.5V. If voltage swings greater than 2.5V are required (for example, if the I^2C bus is pulled up to V_{IN}), the minimum $t_{HD;DAT}$ must be increased to 80ns. Most I^2C masters change SDA near the midpoint between the falling and rising edges of SCL, which provides ample $t_{HD;DAT}$.

Dissipation Ratings[9]

Package	$R_{\theta JA}$[10]	Power Rating at $T_A \le 25°C$	Derating Factor > T_A = 25ºC
Wafer-Level Chip-Scale Package (WLCSP)	110ºC/W	900mW	9mW/ºC

Notes:

9. Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_{J(max)} - T_A] / \theta_{JA}$.
10. This thermal data is measured with a high-K board (four-layer board, according to the JESD51-7 JEDEC standard).

Electrical Specifications

Unless otherwise noted, over the recommended operating range for V_{IN} and T_A, EN = VSEL = SCL = SDA = 1.8V, and register VSEL0[6] bit = 1. Typical values are at V_{IN} = 3.6V, T_A = 25°C. Circuit and components according to Figure 1.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies						
I_Q	Quiescent Current	I_O = 0mA, PFM Mode, 2.3V<=V_{IN}<=4.5V		40	55	µA
		I_O = 0mA, PFM Mode, 2.3V<=V_{IN}<=5.5V		40	65	
		I_O = 0mA, 6MHz PWM Mode		6.3		mA
I_{SD}	Shutdown Supply Current	EN = GND		0.1	1.0	µA
		EN = V_{IN}, EN_DCDC bit = 0, SDA = SCL = 1.8V (Software Shutdown)		N/A	N/A	
V_{UVLO}	Under-Voltage Lockout Threshold	V_{IN} Rising		2.18	2.25	V
		V_{IN} Falling	1.95	2.02		V
V_{UVHYST}	Under-Voltage Lockout Hysteresis			160		mV
ENABLE, VSEL, SDA, SCL						
V_{IH}	HIGH-Level Input Voltage		1.05			V
V_{IL}	LOW-Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{IN}		0.01	1.00	µA
Power Switch and Protection						
$R_{DS(ON)P}$	P-Channel MOSFET On Resistance	V_{IN} = 3.6V		300		mΩ
I_{LKGP}	P-Channel Leakage Current	V_{DS} = 5.5V		0.2	1.0	µA
$R_{DS(ON)N}$	N-Channel MOSFET On Resistance	V_{IN} = 3.6V		200		mΩ
I_{LKGN}	N-Channel Leakage Current	V_{DS} = 5.5V		0.3	1.0	µA
I_{LIMPK}	P-MOS Current Limit	Options 00, 02	1150	1350	1600	mA
		Options 03, 06	1300	1550	1840	
T_{LIMIT}	Thermal Shutdown			150		°C
T_{HYST}	Thermal Shutdown Hysteresis			20		°C
Frequency Control						
f_{SW}	Switching Frequency(11)	PWM Operation	5.4	6.0	6.6	MHz
Output Regulation						
V_{OUT}	V_{OUT} Accuracy	$I_{OUT(DC)}$ = 0, Forced PWM, V_{OUT} = VSEL1 Default Value	–1.5		1.5	%
		2.3V ≤ V_{IN} ≤ 5.5V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 1A, Forced PWM	–2.0		2.0	%
		2.3V ≤ V_{IN} ≤ 5.5V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 1A, Auto PWM/PFM	–2.0		3.5	%
$\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$	Load Regulation	$I_{OUT(DC)}$ = 0 to 1A, Forced PWM		–0.2		%/A
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	2.3V ≤ V_{IN} ≤ 5.5V, $I_{OUT(DC)}$ = 300mA, Forced PWM		0		%/V
V_{RIPPLE}	Output Ripple Voltage	PWM Mode, V_{OUT} = 1.2V		4		mV_{P-P}
		PFM Mode, $I_{OUT(DC)}$ = 10mA		16		mV_{P-P}

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Electrical Specifications (Continued)

Unless otherwise noted, over the recommended operating range for V_{IN} and T_A, EN = VSEL = SCL = SDA = 1.8V, and register VSEL0[6] bit = 1. Typical values are at V_{IN} = 3.6V, T_A = 25°C. Circuit and components according to Figure 1.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
DAC						
	Resolution			6		Bits
	Differential Nonlinearity	Monotonicity Assured by Design			0.8	LSB
Timing						
I^2C_{EN}	EN HIGH to I^2C Start		250			µs
$t_{V(L-H)}$	V_{OUT} LOW to HIGH Settling	Transition from 0.75V to 1.438V V_{OUT} Settled to within 2% of Setpoint		7		µs
Soft-Start						
t_{SS}	Regulator Enable to Regulated V_{OUT}	$R_{LOAD} \geq 5\Omega$, to V_{OUT} = Power-up Default		140	180	µs

Notes:
11. Limited by the effect of t_{OFF} minimum *(see Figure 14 in Typical Performance Characteristics)*.

Block Diagram

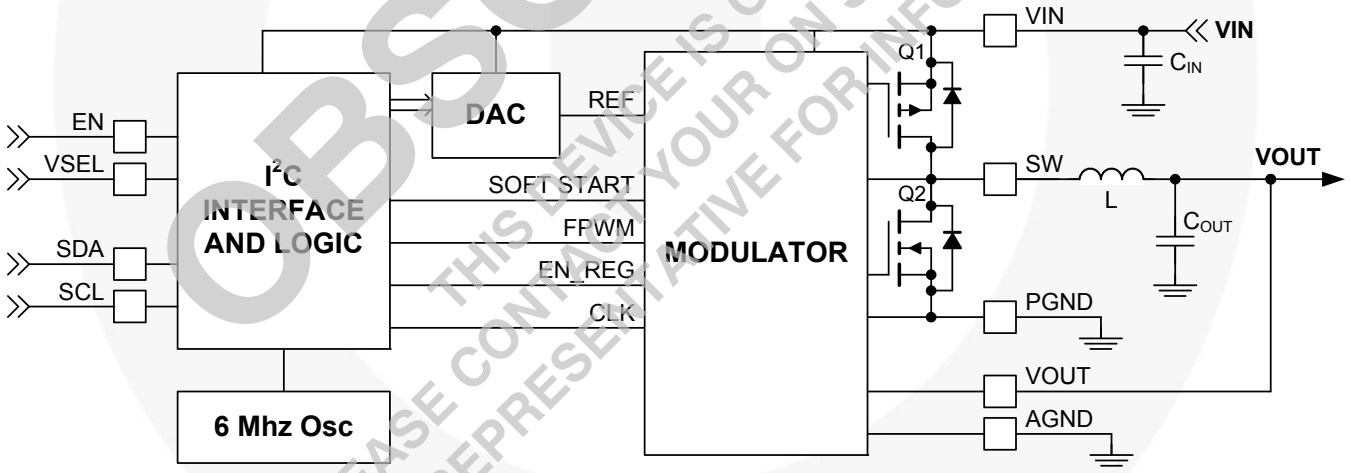

Figure 3 Block Diagram

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		Fast Mode Plus			1000	
		High-Speed Mode, $C_B \leq 100pF$			3400	
		High-Speed Mode, $C_B \leq 400pF$			1700	
t_{BUF}	Bus-free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
		Fast Mode Plus		0.5		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		Fast Mode Plus		0.5		µs
		High-Speed Mode, $C_B \leq 100pF$		160.0		ns
		High-Speed Mode, $C_B \leq 400pF$		320.0		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High-Speed Mode, $C_B \leq 100pF$		60		ns
		High-Speed Mode, $C_B \leq 400pF$		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600.0		ns
		Fast Mode Plus		260.0		ns
		High-Speed Mode		160.0		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		Fast Mode Plus		50		
		High-Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time[8]	Standard Mode	0		3.45	µs
		Fast Mode	0		900.00	ns
		Fast Mode Plus	0		450.00	ns
		High-Speed Mode, $C_B \leq 100pF$	0		70.00	ns
		High-Speed Mode, $C_B \leq 400pF$	0		150.00	ns
t_{RCL}	SCL Rise Time	Standard Mode		$20+0.1C_B$	1000	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High-Speed Mode, $C_B \leq 100pF$		10	80	
		High-Speed Mode, $C_B \leq 400pF$		20	160	

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I^2C Timing Specifications (Continued)

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High-Speed Mode, $C_B \leq 100pF$		10	40	
		High-Speed Mode, $C_B \leq 400pF$		20	80	
t_{RCL1}	Rise Time of SCL after a Repeated START Condition and after ACK Bit	High-Speed Mode, $C_B \leq 100pF$		10	80	ns
		High-Speed Mode, $C_B \leq 400pF$		20	160	
t_{RDA}	SDA Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High-Speed Mode, $C_B \leq 100pF$		10	80	
		High-Speed Mode, $C_B \leq 400pF$		20	160	
t_{FDA}	SDA Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High-Speed Mode, $C_B \leq 100pF$		10	80	
		High-Speed Mode, $C_B \leq 400pF$		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		120		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

Timing Diagrams

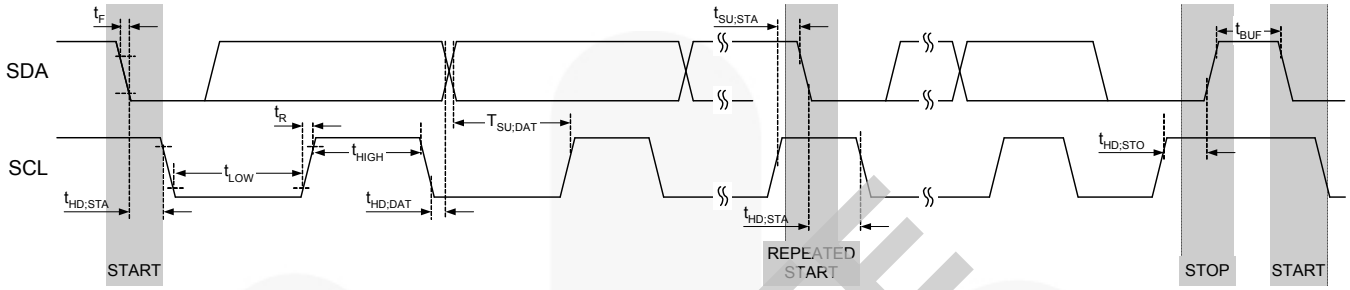
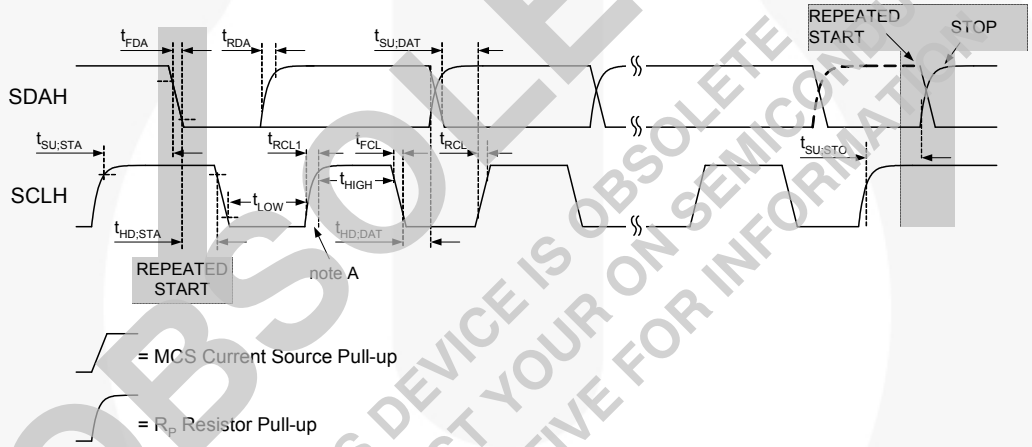


Figure 4. I²C Interface Timing for Fast Plus, Fast, and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 5. I²C Interface Timing for High-Speed Mode

Typical Characteristics

Unless otherwise specified, Auto PWM/PFM, V_{IN} = 3.6V, SCL = SCA = VSEL = EN = 1.8V, T_A = 25°C; circuit and components according to Figure 1.

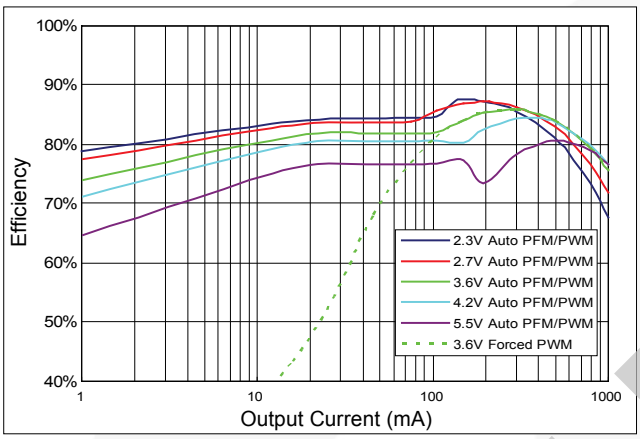


Figure 6. Efficiency vs. Load and Input Supply at V_{OUT} = 1.1V

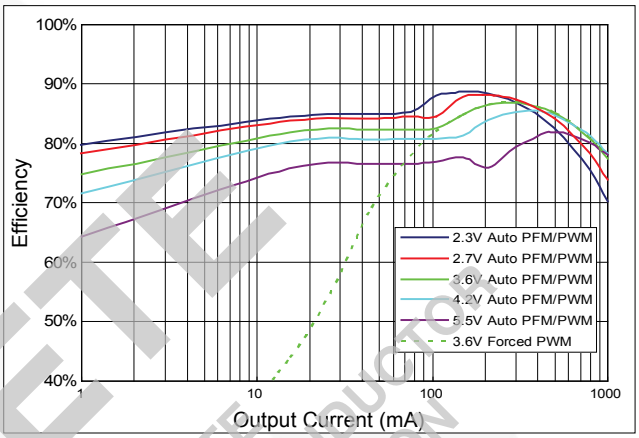


Figure 7. Efficiency vs. Load and Input Supply at V_{OUT} = 1.2V

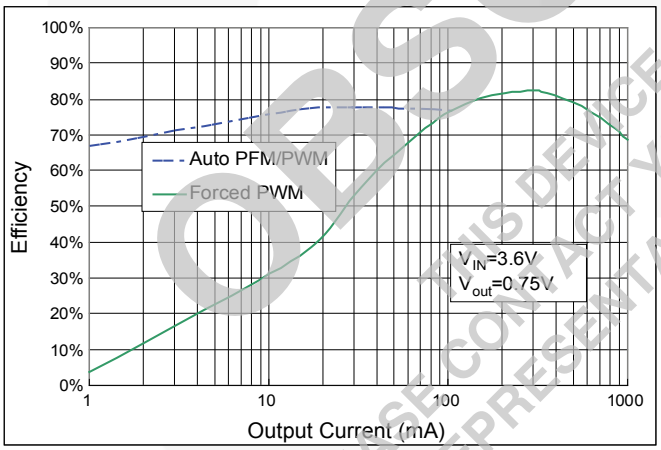


Figure 8. Efficiency, Auto PWM/PFM vs. Forced PWM at V_{OUT} = 0.75V

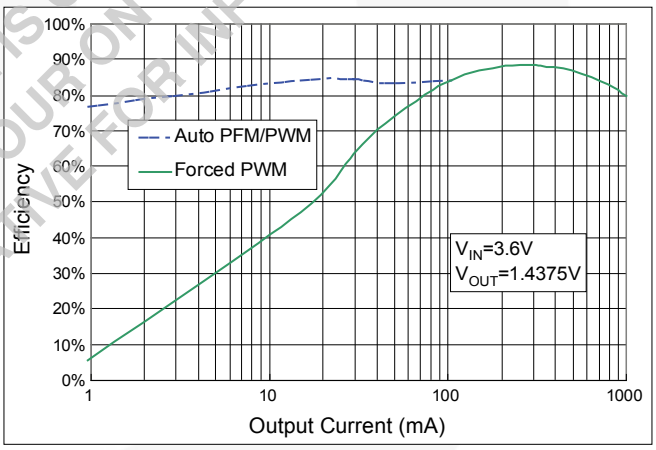


Figure 9. Efficiency, Auto PWM/PFM vs. Forced PWM at V_{OUT} = 1.4375V

Typical Characteristics

Unless otherwise specified, Auto PWM/PFM, V_{IN} = 3.6V, SCL = SCA = VSEL = EN = 1.8V, T_A = 25°C; circuit and components according to Figure 1.

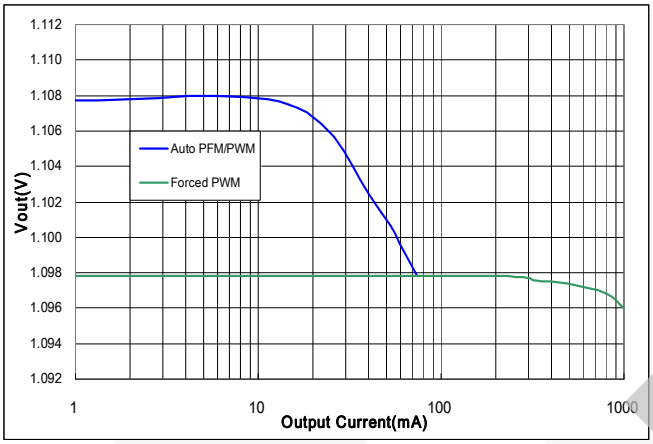


Figure 10. Load Regulation, Auto PFM / PWM and Forced PWM at V_{OUT} = 1.1V

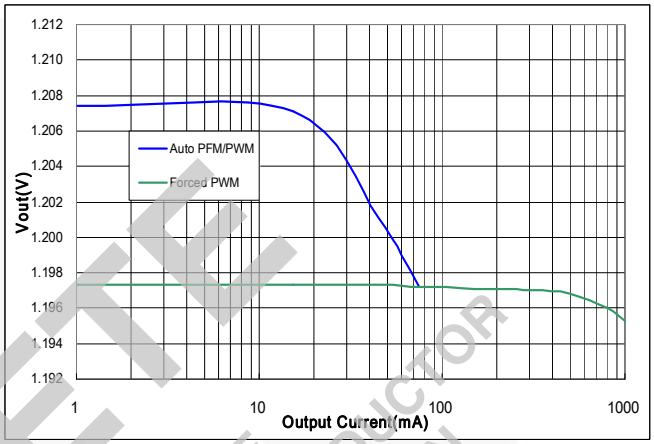


Figure 11. Load Regulation, Auto PFM / PWM and Forced PWM at V_{OUT} = 1.2V

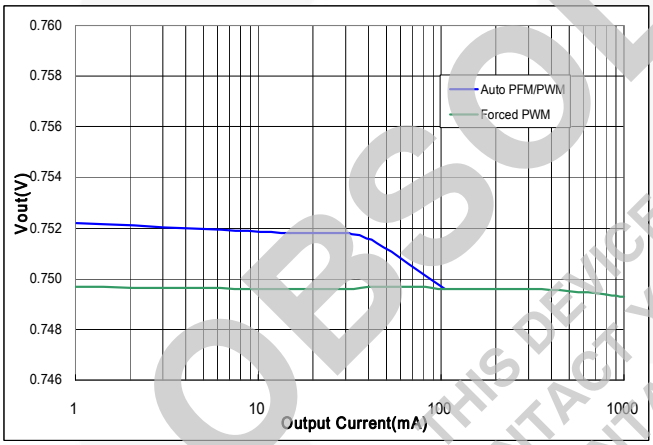


Figure 12. Load Regulation, Auto PFM / PWM and Forced PWM at V_{OUT} = 0.75V

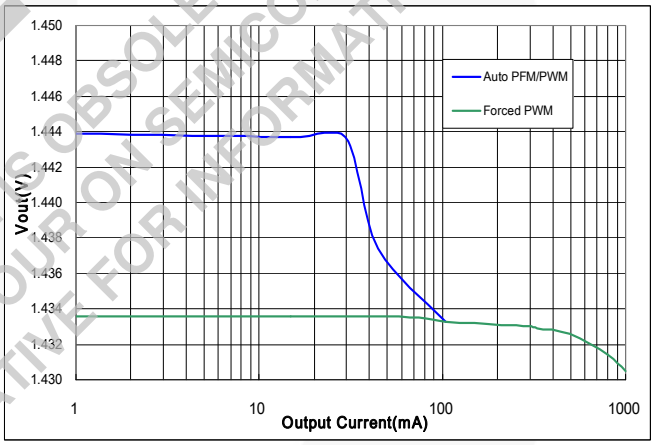


Figure 13. Load Regulation, Auto PFM / PWM and Forced PWM at V_{OUT} = 1.4375V

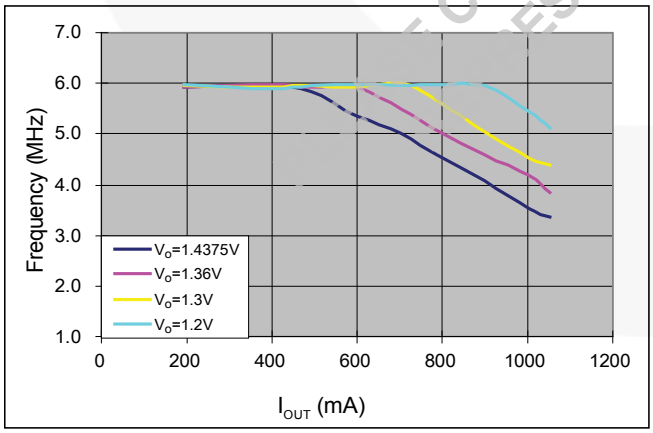


Figure 14. Effect of $t_{OFF(MIN)}$ on Reducing the PWM Switching Frequency, V_{IN}=2.3V

Typical Characteristics

Unless otherwise specified, Auto PWM/PFM, V_{IN} = 3.6V, SCL = SCA = VSEL = EN = 1.8V, T_A = 25°C; circuit and components according to Figure 1.

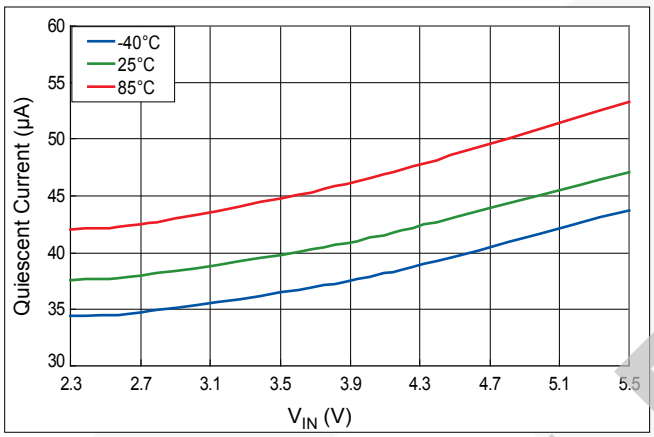


Figure 15. Quiescent Current in PFM Mode vs. Input Voltage and Temperature

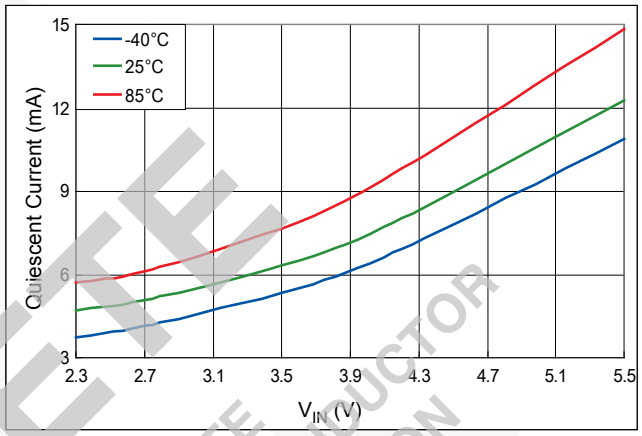


Figure 16. Quiescent Current in PWM Mode vs. Input Voltage and Temperature

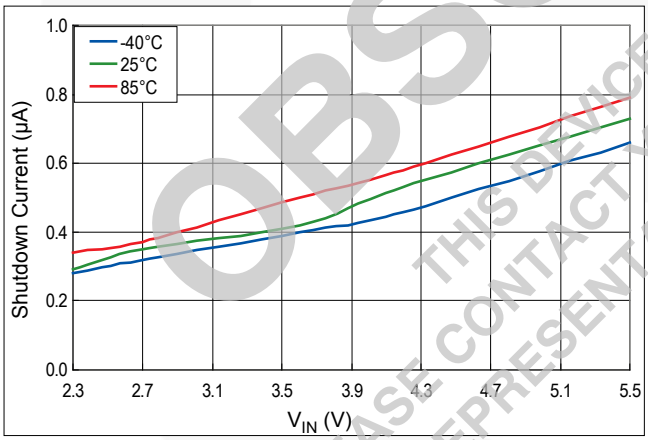


Figure 17. Shutdown Current (EN = 0) vs. Input Voltage and Temperature

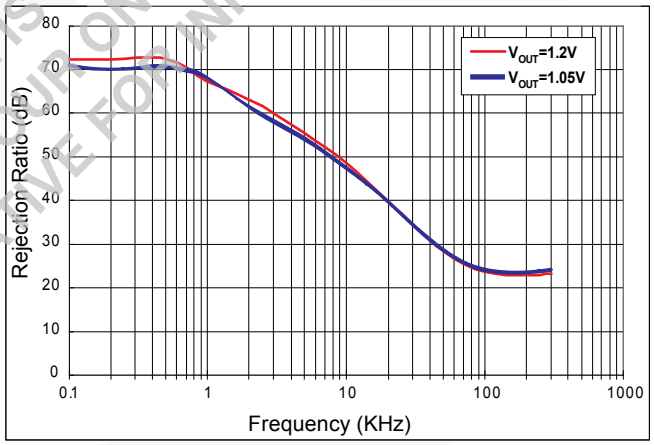


Figure 18. V_{IN} Ripple Rejection (PSRR) in Forced PWM at 200mA

Typical Characteristics

Unless otherwise specified, Auto PWM/PFM, V_{IN} = 3.6V, SCL = SCA = VSEL = EN = 1.8V, T_A = 25°C; circuit and components according to Figure 1.

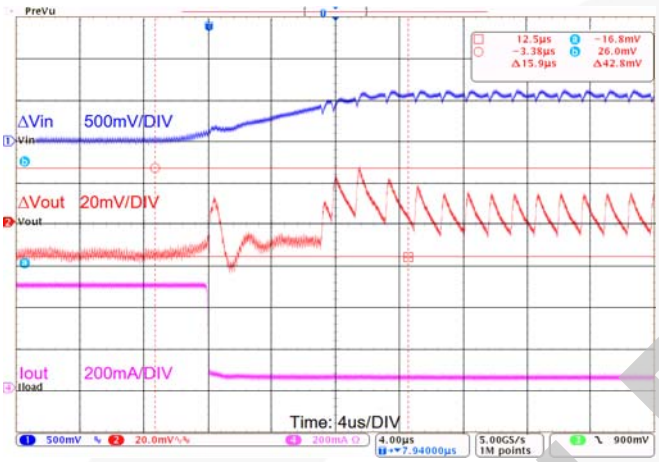


Figure 19. Combined Line/Load Transient 3.0 to 3.6V_{IN} Combined with 500 to 50mA Load Transient

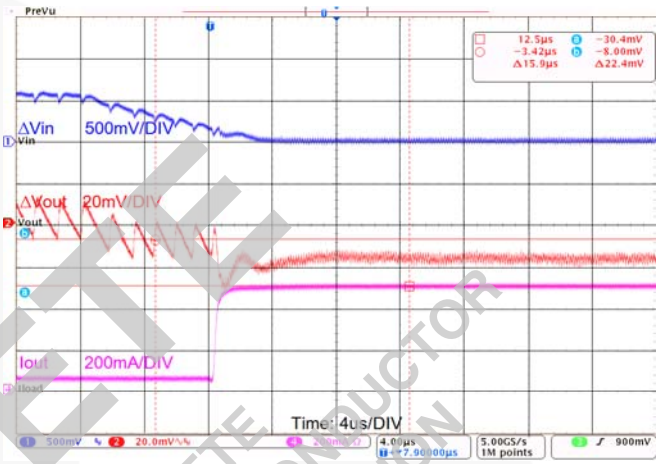


Figure 20. Combined Line/Load Transient 3.6 to 3.0V_{IN} Combined with 50 to 500mA Load Transient

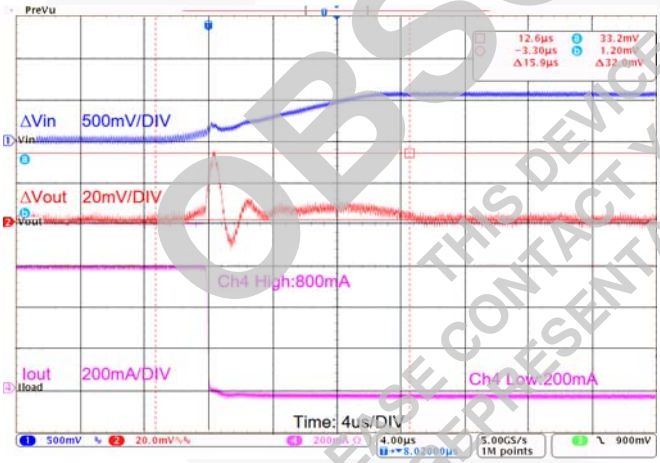


Figure 21. Combined Line/Load Transient 3.0 to 3.6V_{IN} Combined with 800 to 200mA Load Transient

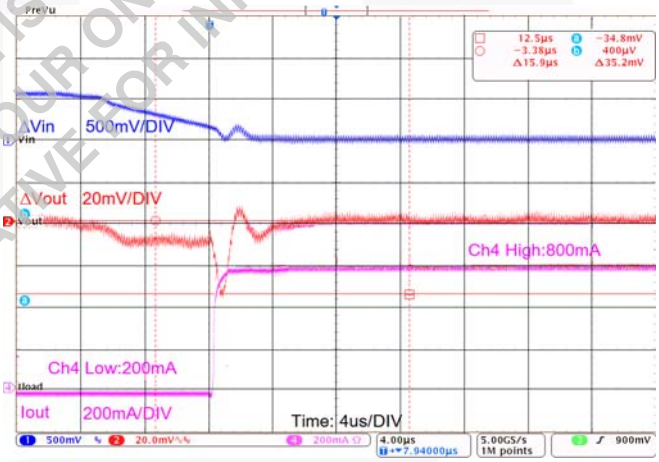


Figure 22. Combined Line/Load Transient 3.6 to 3.0V_{IN} Combined with 200 to 800mA Load Transient

Typical Characteristics

Unless otherwise specified, Auto PWM/PFM, V_{IN} = 3.6V, SCL = SCA = VSEL = EN = 1.8V, T_A = 25°C; circuit and components according to Figure 1.

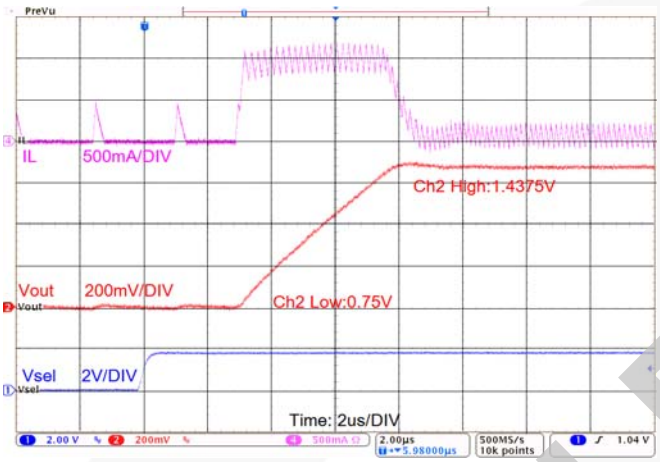


Figure 23. VSEL Transition, Single Step (DefSlew = 7), R_{LOAD} = 24Ω

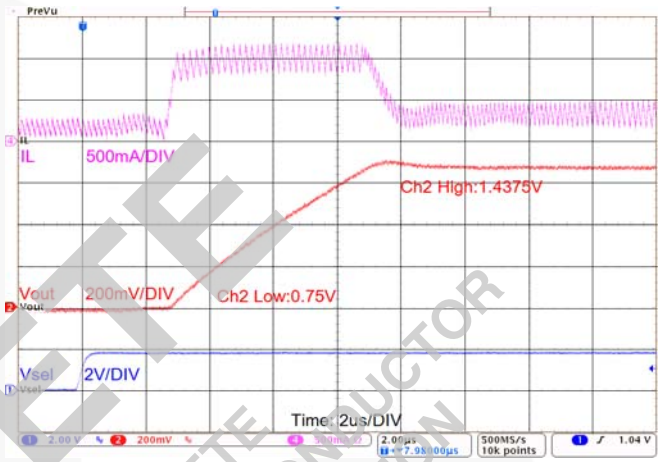


Figure 24. VSEL Transition, Single Step (DefSlew = 7), R_{LOAD} = 4Ω

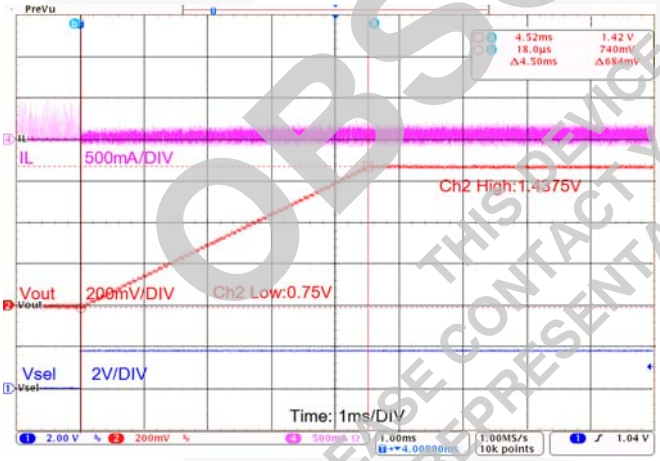


Figure 25. VSEL Transition, DefSlew = 0, R_{LOAD} = 24Ω

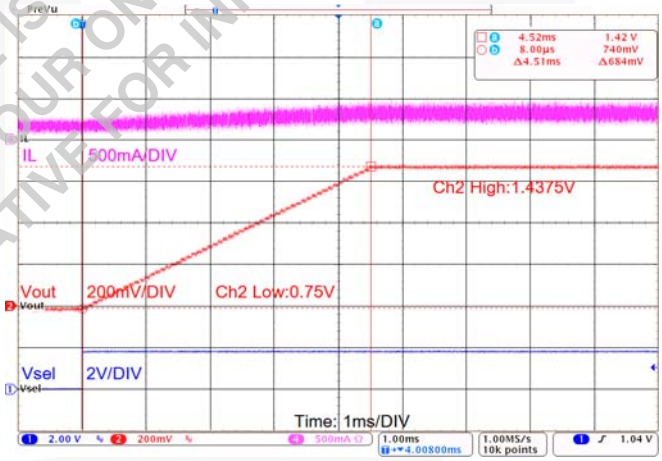


Figure 26. VSEL Transition, DefSlew = 0, R_{LOAD} = 4Ω

Typical Characteristics

Unless otherwise specified, Auto PWM/PFM, V_{IN} = 3.6V, SCL = SCA = VSEL = EN = 1.8V, T_A = 25°C; circuit and components according to Figure 1.

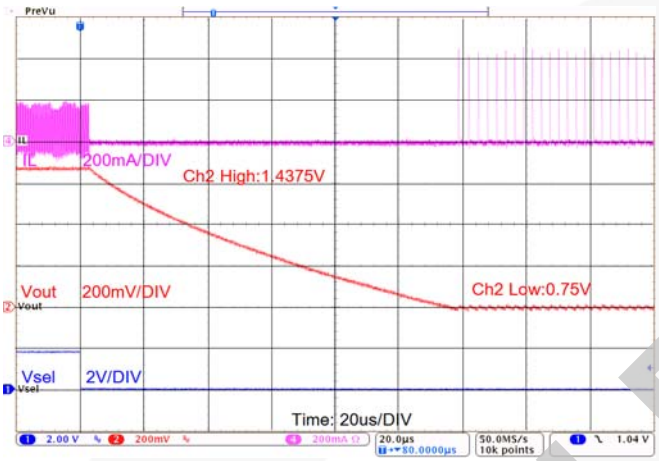


Figure 27. VSEL Transition, VSEL 1 to 0, R_{LOAD} = 24Ω

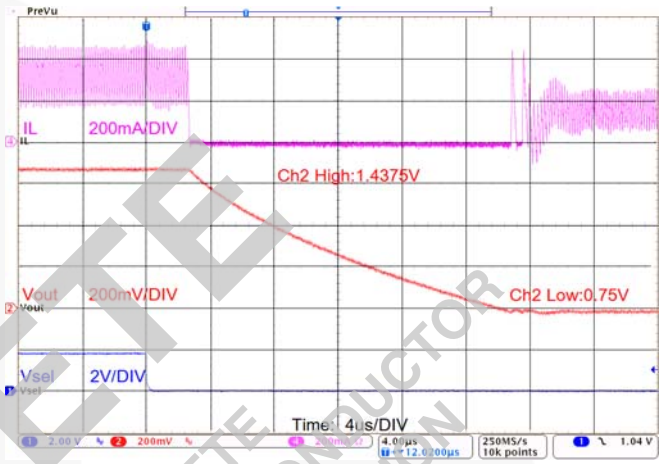


Figure 28. VSEL Transition, VSEL 1 to 0, R_{LOAD} = 4Ω

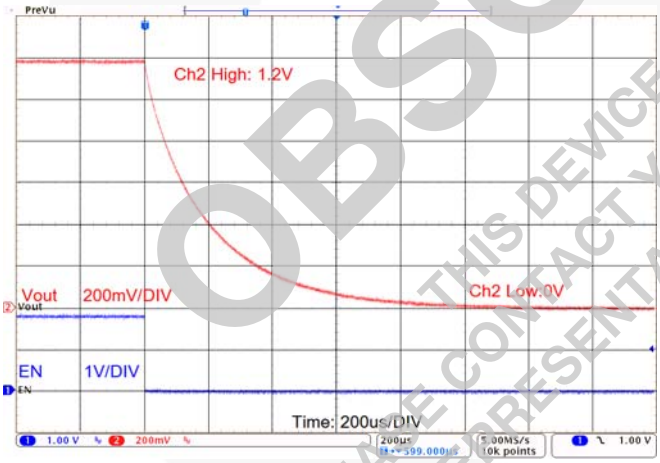


Figure 29. Shutdown, Output Discharge On

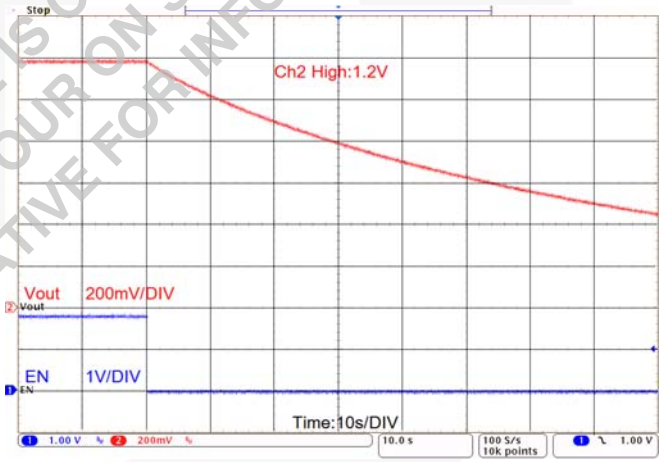


Figure 30. Shutdown, Output Discharge Off

Typical Characteristics

Unless otherwise specified, Auto PWM/PFM, V_{IN} = 3.6V, SCL = SCA = VSEL = EN = 1.8V, T_A = 25°C; circuit and components according to Figure 1.

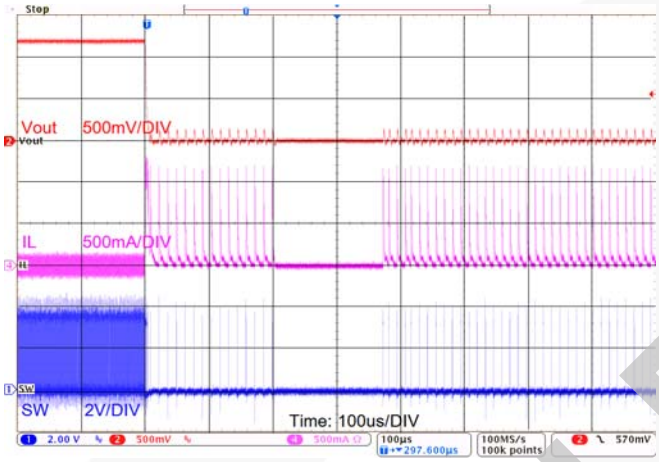


Figure 31. Metallic Short Applied at V_{OUT}

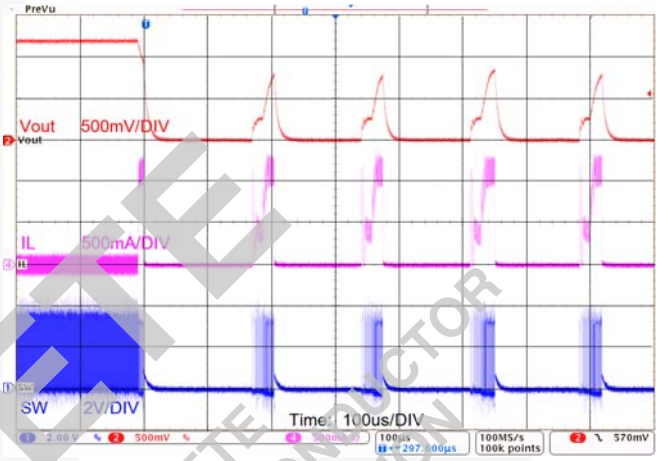


Figure 32. Over-Current Fault Response, R_{LOAD} = 500mΩ

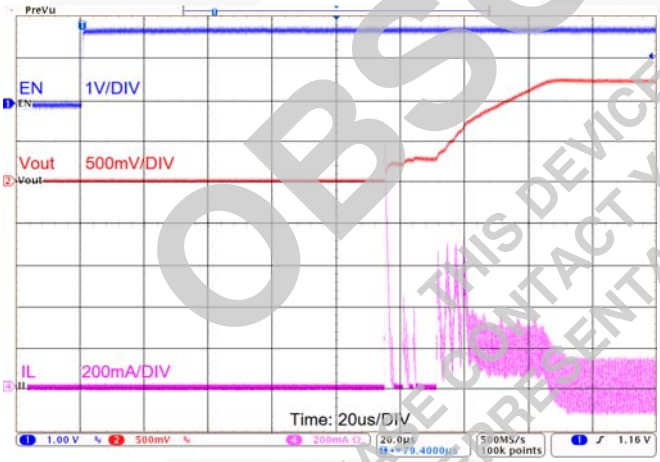


Figure 33. Soft Start, No Load

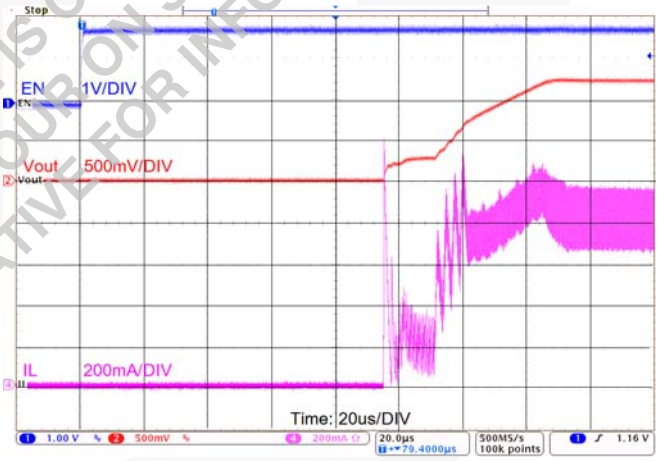


Figure 34. Soft Start, R_{LOAD} = 1.5Ω

Circuit Description

The FAN5365 is a synchronous buck regulator that typically operates at 6MHz with moderate to heavy load currents. At light load currents, the converter operates in power-saving PFM mode. The regulator automatically transitions between fixed-frequency PWM mode and variable-frequency PFM mode to maintain the highest possible efficiency over the full range of load current.

The FAN5365 uses a very fast, non-linear control architecture to achieve excellent transient response with minimum-sized external components.

The FAN5365 integrates an I^2C-compatible interface, allowing transfers up to 3.4Mbps. This communication interface can be used to:

- Dynamically re-program the output voltage in 12.5mV increments
- Reprogram the mode of operation to enable or disable PFM mode
- Control voltage transition slew rate
- Enable / disable the regulator.

For more details, refer to the I^2C Interface and Register Description sections.

Output Voltage Programming

V_{OUT} is programmed according to the following equations:

Option[12]	V_{OUT} Equation	
00, 02, 03	$V_{OUT} = 0.75 + N_{VSEL} \bullet 12.5mV$	(1)
06	$V_{OUT} = 1.1875 + N_{VSEL} \bullet 12.5mV$	(2)

Note:
12. For option 00 and 02, the maximum voltage is 1.4375V.

Table 2. V_{SEL} vs. V_{OUT}

VSEL Value			VOUT		
Dec (NVSEL)	Binary	Hex	00, 02	03	06
0	000000	00	0.7500	0.7500	1.1875
1	000001	01	0.7625	0.7625	1.2000
2	000010	02	0.7750	0.7750	1.2125
3	000011	03	0.7875	0.7875	1.2250
4	000100	04	0.8000	0.8000	1.2375
5	000101	05	0.8125	0.8125	1.2500
6	000110	06	0.8250	0.8250	1.2625
7	000111	07	0.8375	0.8375	1.2750
8	001000	08	0.8500	0.8500	1.2875
9	001001	09	0.8625	0.8625	1.3000
10	001010	0A	0.8750	0.8750	1.3125
11	001011	0B	0.8875	0.8875	1.3250
12	001100	0C	0.9000	0.9000	1.3375
13	001101	0D	0.9125	0.9125	1.3500
14	001110	0E	0.9250	0.9250	1.3625
15	001111	0F	0.9375	0.9375	1.3750
16	010000	10	0.9500	0.9500	1.3875
17	010001	11	0.9625	0.9625	1.4000
18	010010	12	0.9750	0.9750	1.4125
19	010011	13	0.9875	0.9875	1.4250
20	010100	14	1.0000	1.0000	1.4375
21	010101	15	1.0125	1.0125	1.4500
22	010110	16	1.0250	1.0250	1.4625
23	010111	17	1.0375	1.0375	1.4750
24	011000	18	1.0500	1.0500	1.4875
25	011001	19	1.0625	1.0625	1.5000
26	011010	1A	1.0750	1.0750	1.5125
27	011011	1B	1.0875	1.0875	1.5250
28	011100	1C	1.1000	1.1000	1.5375
29	011101	1D	1.1125	1.1125	1.5500
30	011110	1E	1.1250	1.1250	1.5625
31	011111	1F	1.1375	1.1375	1.5750
32	100000	20	1.1500	1.1500	1.5875
33	100001	21	1.1625	1.1625	1.6000
34	100010	22	1.1750	1.1750	1.6125
35	100011	23	1.1875	1.1875	1.6250
36	100100	24	1.2000	1.2000	1.6375
37	100101	25	1.2125	1.2125	1.6500
38	100110	26	1.2250	1.2250	1.6625
39	100111	27	1.2375	1.2375	1.6750
40	101000	28	1.2500	1.2500	1.6875
41	101001	29	1.2625	1.2625	1.7000
42	101010	2A	1.2750	1.2750	1.7125
43	101011	2B	1.2875	1.2875	1.7250
44	101100	2C	1.3000	1.3000	1.7375
45	101101	2D	1.3125	1.3125	1.7500
46	101110	2E	1.3250	1.3250	1.7625
47	101111	2F	1.3375	1.3375	1.7750
48	110000	30	1.3500	1.3500	1.7875
49	110001	31	1.3625	1.3625	1.8000
50	110010	32	1.3750	1.3750	1.8125
51	110011	33	1.3875	1.3875	1.8250
52	110100	34	1.4000	1.4000	1.8375
53	110101	35	1.4125	1.4125	1.8500
54	110110	36	1.4250	1.4250	1.8625
55	110111	37	1.4375	1.4375	1.8750
56	111000	38	1.4375	1.4500	1.8875
57	111001	39	1.4375	1.4625	1.9000
58	111010	3A	1.4375	1.4750	1.9125
59	111011	3B	1.4375	1.4875	1.9250
60	111100	3C	1.4375	1.5000	1.9375
61	111101	3D	1.4375	1.5125	1.9500
62	111110	3E	1.4375	1.5250	1.9625
63	111111	3F	1.4375	1.5375	1.9750

Power-Up, EN, and Soft-Start

All internal circuits remain de-biased and the IC is in a very low quiescent current state until the following are true:

- V_{IN} is above its rising UVLO threshold, and
- EN is HIGH.

At that point, the IC begins a soft-start cycle, its I^2C interface is enabled, and its registers are loaded with their default values.

During the initial soft-start, V_{OUT} ramps linearly to the setpoint programmed in the VSEL register selected by the VSEL pin. The soft-start features a fixed output voltage slew rate of 20V/ms and achieves regulation approximately 90µs after EN rises. PFM mode is enabled during soft-start until the output is in regulation, regardless of the MODE bit settings. This allows the regulator to start into a partially charged output without discharging it; in other words, the regulator does not allow current to flow from the load back to the battery.

As soon as the output has reached its setpoint, the control forces PWM mode for about 85µs to allow all internal control circuits to calibrate.

Table 3. Soft-Start Timing

Symbol	Description	Value (µs)
t_{SSDLY}	Time from EN to start of soft-start ramp	100
t_{REG}	V_{OUT} ramp start to regulation	(VSEL–0.1) X 53
t_{POK}	PWROK (CONTROL2[5]) rising from t_{REG}	11
t_{CAL}	Regulator stays in PWM mode during this time	10

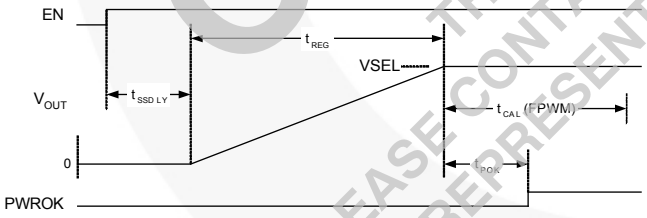


Figure 35. Soft-Start Timing

Table 4. EN_DCDC Behavior

EN_DCDC Bit	EN Pin	I^2C	REGULATOR
0	0	OFF	OFF
1	1	ON	ON
1	0	OFF	OFF
0	1	ON	OFF

Software Enable

The EN_DCDC bit, VSELx[7], can be used to enable the regulator in conjunction with the EN pin. Setting EN_DCDC with EN HIGH begins the soft-start sequence described above.

Light-Load (PFM) Operation

The FAN5365 provides a low ripple, single-pulse, PFM mode that ensures:

- Smooth transitions between PFM and PWM modes
- Single-pulse operation for low ripple
- Predictable PFM entry and exit currents.

PFM begins after the inductor current has become discontinuous, crossing zero during the PWM cycle for 32 consecutive cycles. PFM exit occurs when discontinuous current mode (DCM) operation cannot supply sufficient current to maintain regulation. During PFM mode, the inductor current ripple is about 40% higher than in PWM mode. The load current required to exit PFM mode is thereby about 20% higher than the load current required to enter PFM mode, providing sufficient hysteresis to prevent "mode chatter."

While PWM ripple voltage is typically less than $4mV_{P-P}$, PFM ripple voltage can be up to $30mV_{P-P}$ during very light load. To prevent significant undershoot when a load transient occurs, the initial DC setpoint for the regulator in PFM mode is set 10mV higher than in PWM mode. This offset decays to about 5mV after the regulator has been in PFM mode for ~100µs. The maximum instantaneous voltage in PFM is 30mV above the setpoint.

PFM mode can be disabled by writing to the mode control bits: CONTROL1[3:0] (*see Table 5*)

Output Voltage Transitions

The IC regulates V_{OUT} to one of two setpoint voltages, as determined by the VSEL pin and the HW_nSW bit.

Table 5. V_{OUT} Setpoint and Mode Control MODE_CTRL, CONTROL1[3:2] = 00

VSEL Pin	HW_nSW Bit	V_{OUT} Setpoint	PFM
0	1	VSEL0	Allowed
1	1	VSEL1	Per MODE1
x	0	VSEL1	Per MODE1

If HW_nSW = 0, V_{OUT} transitions are initiated through the following sequence:

1. Write the new setpoint in VSEL1.
2. Write desired transition rate in DEFSLEW, CONTROL2[2:0], and set the GO bit in CONTROL2[7].

If HW_nSW = 1, V_{OUT} transitions are initiated either by changing the state of the VSEL pin or by writing to the VSEL register selected by the VSEL pin.

Positive Transitions

When transitioning to a higher V_{OUT}, the regulator can perform the transition using multi-step or single-step mode.

Multi-Step Mode:
The internal DAC is stepped at a rate defined by DEFSLEW, CONTROL2[2:0], ranging from 000 to 110. This mode minimizes the current required to charge C_{OUT} and thereby minimizes the current drain from the battery when transitioning. The PWROK bit, CONTROL2[5], remains LOW until about 1.5µs after the DAC completes its ramp.

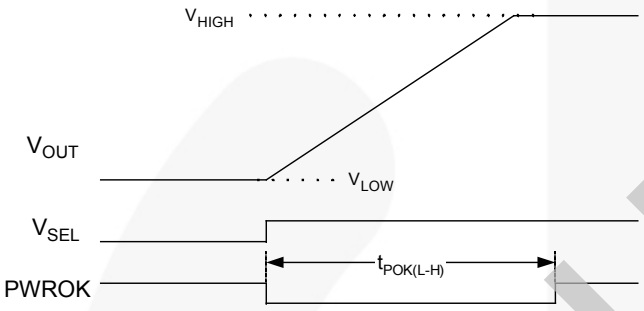


Figure 36. Multi-Step V_{OUT} Transition

Single-Step Mode:
Used if DEFSLEW, CONTROL2[2:0] = 111. The internal DAC is immediately set to the higher voltage and the regulator performs the transition as quickly as its current limit circuit allows, while avoiding excessive overshoot.

Figure 37 shows single-step transition timing. $t_{V(L-H)}$ is the time it takes the regulator to settle to within 2% of the new setpoint, typically 7µs for a full-range transition. The PWROK bit, CONTROL2[5], goes LOW until the transition is complete and V_{OUT} settled. This typically occurs ~2µs after $t_{V(L-H)}$.

It is good practice to reduce the load current before making positive V_{SEL} transitions. This reduces the time required to make positive load transitions and avoids current-limit-induced overshoot.

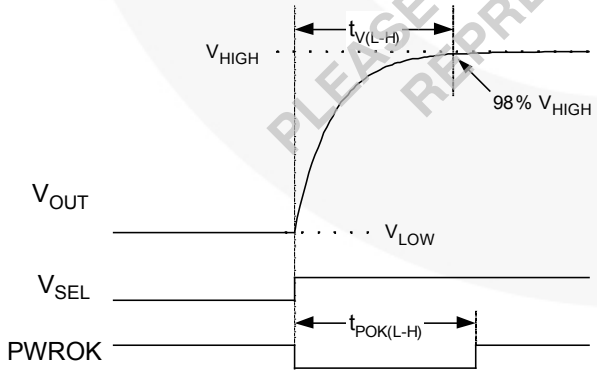


Figure 37. Single-Step V_{OUT} Transition

All positive V_{OUT} transitions inhibit PFM until the transition is complete, which occurs at the end of $t_{POK(L-H)}$.

Negative Transitions
When moving from V_{SEL} = 1 to V_{SEL} = 0, the regulator enters PFM mode, regardless of the condition of the MODE bits, and remains in PFM until the transition is complete. Reverse current through the inductor is blocked, and the PFM minimum frequency control inhibited, until the new setpoint is reached; at which time, the regulator resumes control using the mode established by MODE_CTRL. The transition time from V_{HIGH} to V_{LOW} is controlled by load current and output capacitance as:

$$t_{V(H-L)} = C_{OUT} \bullet \frac{V_{HIGH} - V_{LOW}}{I_{LOAD}} \quad (3)$$

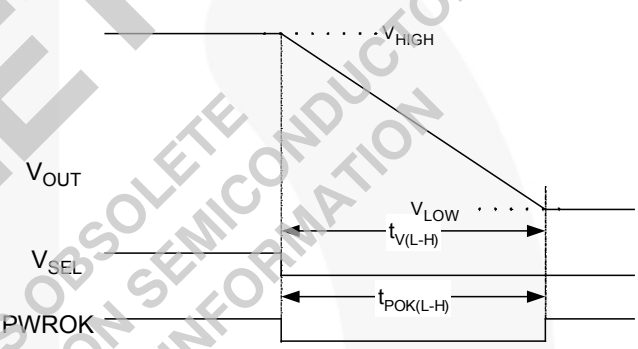


Figure 38. Negative V_{OUT} Transition

Protection Features

Current Limit / Auto-Restart
The regulator includes cycle-by-cycle current limiting, which prevents the instantaneous inductor current from exceeding the "PMOS Current Limit" threshold.

The IC enters "fault" mode after sustained over-current. If current limit is asserted for more than 32 consecutive cycles (about 20µs), the IC returns to shutdown state and remains in that condition for ~80µs. After that time, the regulator attempts to restart with a normal soft-start cycle. If the fault has not cleared, it shuts down ~20µs later.

If the fault is a short circuit, the initial current limit is ~30% of the normal current limit, which produces a very small drain on the system power source.

Thermal Protection
When the junction temperature of the IC exceeds 150°C, the device turns off all output MOSFETs and remains in a low quiescent current state until the die cools to 130°C before starting a normal soft-start cycle.

Under-Voltage Lockout (UVLO)
The IC turns off all MOSFETs and remains in a low quiescent current state until V_{IN} rises above the UVLO threshold.

I²C Interface

The FAN5365's serial interface is compatible with standard, fast, fast plus, and high-speed mode I²C bus specifications. The FAN5365's SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

In Table 6, A1 and A0 are according to the Ordering Information table on page 2.

Table 6. I²C Slave Address

7	6	5	4	3	2	1	0
1	0	0	1	A2	A1	A0	R/$\overline{W}$

In Hex notation, the slave address assumes a 0 LSB. For example, the hex slave address of option 00 is 94H.

Register Addressing

FAN5365 has four user-accessible registers:

Table 7. I²C Register Address

	Address							
	7	6	5	4	3	2	1	0
VSEL0	0	0	0	0	0	0	0	0
VSEL1	0	0	0	0	0	0	0	1
CONTROL1	0	0	0	0	0	0	1	0
CONTROL2	0	0	0	0	0	0	1	1

Bus Timing

As shown in Figure 39, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

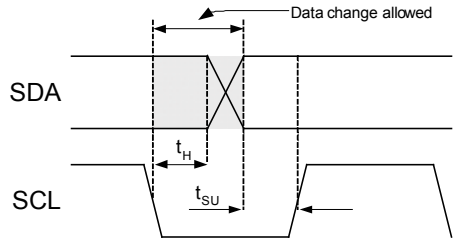


Figure 39. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a "START" condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 40.

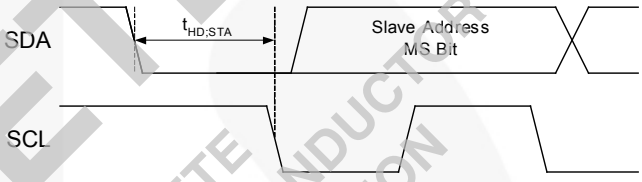


Figure 40. Start Bit

A transaction ends with a "STOP" condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, shown in Figure 41.

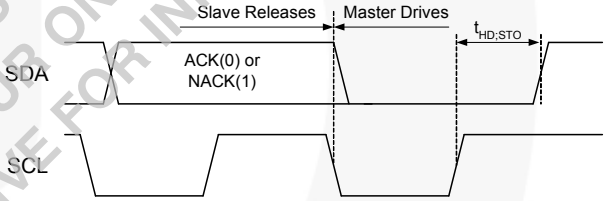


Figure 41. Stop Bit

During a read from the FAN5365 (Figure 44), the master issues a "Repeated Start" command after sending the register address and before resending the slave address. The "Repeated Start" is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 42.

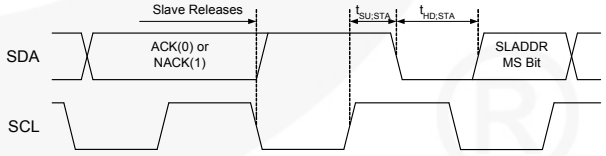


Figure 42. Repeated Start Timing

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) modes are identical, except the bus speed for HS mode is 3.4MHz. HS mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in Fast or Fast Plus mode (less than 1MHz clock) and slaves do not acknowledge (ACK) this transmission.

The master then generates a repeated start condition (Figure 42) that causes all slaves on the bus to switch to HS mode. The master then sends I²C packets, as described above, using the HS mode clock rate and timing.

The bus remains in HS mode until a stop bit (Figure 41) is sent by the master. While in HS mode, packets are separated by repeated start conditions.

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 8. I²C Bit Definitions for Figure 43 and Figure 44

Symbol	Definition
S	START, *Figure 40.*
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, *see Figure 42.*
P	STOP, *see Figure 41.*

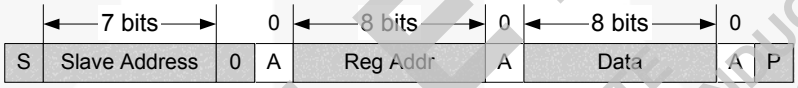


Figure 43. Write Transaction

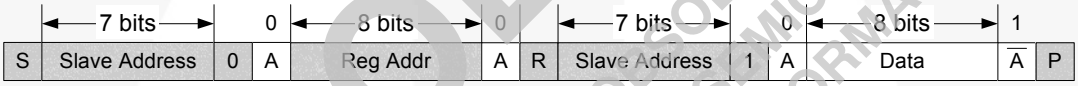


Figure 44. Read Transaction

Register Descriptions

Default Values

Each option of the FAN5365 *(see Table 9)* has different default values for the some of the register bits. Table 9 defines both the default values and the bit's type (as defined in Table 10) for each available option.

Table 9. Default Values and Bit Types for V_{SEL} and CONTROL Registers

VSEL0

Option	7	6	5	4	3	2	1	0	V_{OUT}
00	1	1	0	1	1	0	0	0	1.05
02	1	1	0	1	0	0	0	0	0.95
03	1	1	0	1	0	1	0	0	1.00
06	1	1	1	1	0	0	0	1	1.80

VSEL1

Option	7	6	5	4	3	2	1	0	V_{OUT}
00	1	1	1	0	0	1	0	0	1.20
02	1	1	0	1	1	1	0	0	1.10
03	1	1	1	0	0	1	0	0	1.20
06	1	1	1	1	0	0	0	1	1.80

CONTROL1

Option	7	6	5	4	3	2	1	0
00, 02	1	0	0	1	0	0	0	0
03, 06	1	0	0	1	0	0	0	0

CONTROL2

Option	7	6	5	4	3	2	1	0
00, 02	0	1	0	0	0	1	1	1
03, 06	0	0	0	0	0	1	1	1

Table 10. Bit Type Definitions for Table 9

#	**Active Bit**	Changing this bit changes the behavior of the converter, as described below.
#	**Disabled**	Converter logic ignores changes made to this bit. Bit can be written and read-back.
#	**Read-Only**	Writing to this bit through I²C does not change the read-back value, nor does it change converter behavior.

Bit Definitions

Table 11 defines the operation of each register bit. Superscript characters define the default state for each option. Superscripts [0,2,3,6] signify the default values for options 00, 02, 03, and 06, respectively. [A] signifies the default for all options.

Table 11. Bit Definitions

Bit	Name	Value	Description
VSEL0			**Register Address: 00**
7	EN_DCDC	0	Device in shutdown regardless of the state of the EN pin. This bit is mirrored in VSEL1. A write to bit 7 in either register establishes the EN_DCDC value.
		1[A]	Device enabled when EN pin is HIGH, disabled when EN is LOW.
6	Reserved	1[A]	
5:0	DAC[5:0]	Table 9[A]	6-bit DAC value to set V_{OUT}.
VSEL1			**Register Address: 01**
7	EN_DCDC	0	Device in shutdown regardless of the state of the EN pin. This bit is mirrored in VSEL1. A write to bit 7 in either register establishes the EN_DCDC value.
		1[A]	Device enabled when EN pin is HIGH, disabled when EN is LOW.
6	Reserved	1[A]	
5:0	DAC[5:0]	Table 9[A]	6-bit DAC value to set V_{OUT}.
CONTROL1			**Register Address: 02**
7:6	Reserved	10[A]	Vendor ID bits. Writing to these bits has no effect on regulator operation. These bits can be used to distinguish between vendors via I^2C.
5	Reserved	1[A]	
4	HW_nSW	0	V_{OUT} is controlled by VSEL1. Voltage transitions occur by writing to the VSEL1, then setting the GO bit.
		1[A]	V_{OUT} is programmed by the VSEL pin. V_{OUT} = VSEL1 when VSEL is HIGH and V_{OUT} = VSEL0 when VSEL is LOW.
3:2	MODE_CTRL	00[A]	Operation follows MODE0, MODE1.
		01	PFM with automatic transitions to PWM, regardless of VSEL.
		10	PFM disabled (forced PWM), regardless of VSEL.
		11	PFM with automatic transitions to PWM, regardless of VSEL.
1	MODE1	0[A]	PFM disabled (forced PWM) when regulator output is controlled by VSEL1.
		1	PFM with automatic transitions to PWM when regulator output is controlled by VSEL1.
0	MODE0	0[A]	PFM with automatic transitions to PWM when VSEL is LOW. Changing this bit has no effect on the operation of the regulator.
		1	
CONTROL2			**Register Address: 03**
7	GO	0[A]	This bit has no effect when HW_nSW = 1. At the end of a V_{OUT} transition, this bit is reset to 0.
		1	Starts a V_{OUT} transition if HW_nSW = 0.
6	OUTPUT_ DISCHARGE	0 [3,6]	When the regulator is disabled, V_{OUT} is not discharged.
		1 [0,2]	When the regulator is disabled, V_{OUT} discharges through an internal pull-down.
5	PWROK (read only)	0	V_{OUT} is not in regulation or is in current limit.
		1	V_{OUT} is in regulation.
4:3	Reserved	00[A]	
2:0	DEFSLEW	000	V_{OUT} slews at 0.15mV/µs during positive V_{OUT} transitions.
		001	V_{OUT} slews at 0.30mV/µs during positive V_{OUT} transitions.
		010	V_{OUT} slews at 0.60mV/µs during positive V_{OUT} transitions.
		011	V_{OUT} slews at 1.20mV/µs during positive V_{OUT} transitions.
		100	V_{OUT} slews at 2.40mV/µs during positive V_{OUT} transitions.
		101	V_{OUT} slews at 4.80mV/µs during positive V_{OUT} transitions.
		110	V_{OUT} slews at 9.60mV/µs during positive V_{OUT} transitions.
		111[A]	Positive V_{OUT} transitions use single-step mode *(see Figure 37)*.

Layout Recommendations

FAN5365 switches at a relatively high frequency of 6MHz; thus the recommended layout should be followed carefully as additional parasitic effects caused by moving components further away or routing through internal layers can cause issues. In addition, possible detrimental effects to regulator performance EMI issues can be generated by introducing unintentional coupling paths in the layout.

To minimize VIN and SW spikes and thereby reduce voltage stress on the IC power switches; it is critical to minimize the loop length for the VIN bypass capacitor. C_{IN} must be placed next to the IC with routing on the top layer, as shown in Figure 45 and Figure 46.

Switching current paths through C_{IN} and C_{OUT} should be returned directly to the GND bumps of the IC on the top layer of the printed circuit board (PCB).

The SW node should be treated as a noisy signal and separated by the ground plane or “keepout region” from any sensitive signals in the system. Routing sensitive high-impedance voltage reference signals should be avoided on the layer directly beneath the SW node.

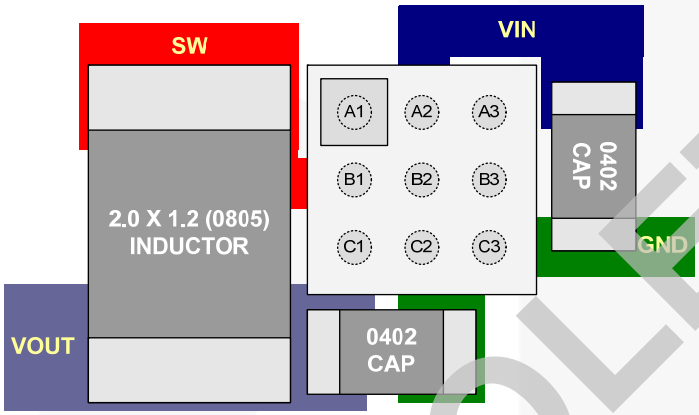


Figure 45. Simplified Layout Drawing

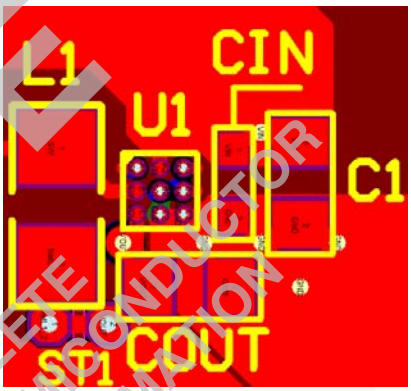
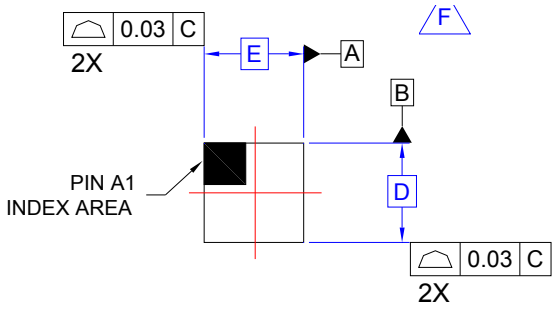
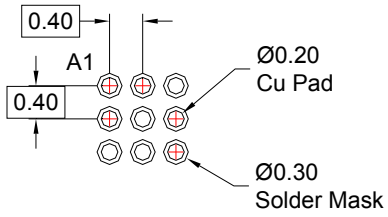


Figure 46. Fairchild Reference Board Layout

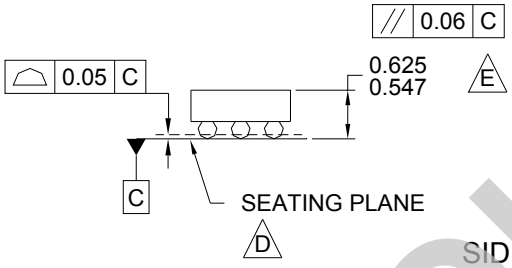
Physical Dimensions

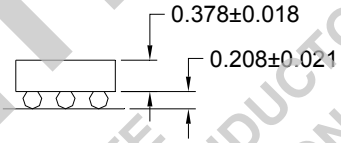


TOP VIEW

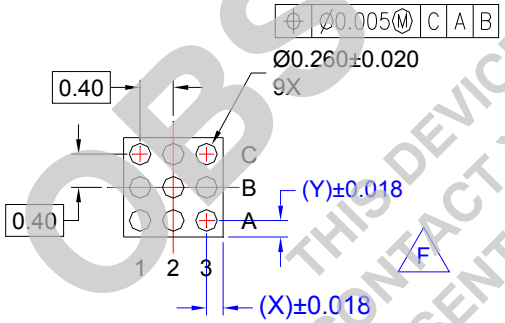


LAND PATTERN RECOMMENDATION
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC009ABrev2

Figure 47. 9-Ball WLCSP, 3X3 Array, 0.4mm Pitch, 250µm Ball

Product-Specific Dimensions

Product	D	E	X	Y
FAN5365UC	1.290 +/-0.030	1.270 +/-0.030	0.250	0.250

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