FAIRCHILD SEMICONDUCTOR®

October 2013

FAN2012
1.5 A Low-Voltage, Current-Mode Synchronous PWM Buck Regulator

Features

- 95% Efficiency, Synchronous Operation
- Adjustable Output Voltage from 0.8 V to 3.5 V
- 4.5 V to 5.5 V Input Voltage Range
- Up to 1.5 A Output Current
- Fixed-Frequency 1.3 MHz PWM Operation
- Soft Start
- Excellent Load Transient Response
- 3 x 3 mm, 6-Lead, MLP

Applications

- Hard Disk Drive
- Set-Top Box
- Point-of-Load Power
- Notebook Computer
- Communications Equipment

Description

The FAN2012 is a high-efficiency, low-noise, synchronous Pulse Width Modulated (PWM) current-mode DC-DC converter designed for low-voltage applications. It provides up to 1.5 A continuous-load current from the 4.5 V to 5.5 V input. The output voltage is adjustable over a wide range of 0.8 V to 3.5 V by means of an external voltage divider.

The FAN2012 has an “Enable Input” and the device can be put in shutdown mode, in which the ground current falls below 1 µA.

A current-mode control loop with a fast transient response ensures excellent line and load regulation. The fixed 1.3 MHz switching frequency enables designers to choose a small, inexpensive external inductor and capacitor. Filtering is easily accomplished with very small components.

Protection features include input under-voltage lockout, short-circuit protection, and thermal shutdown. Soft-start limits inrush current during start-up conditions.

The device is available in a 3x3 mm 6-lead molded leadless package (MLP), making it possible to build a 1.5 A complete DC-DC converter in limited space on the printed circuit board (PCB).

Ordering Information

Part Number	Output Voltage	Operating Temperature Range	Package
FAN2012MPX	Adjustable	0°C to 85°C	3x3 mm 6-Lead MLP
FAN2012EMPX	Adjustable	-40°C to 85°C	3x3 mm 6-Lead MLP

Typical Application

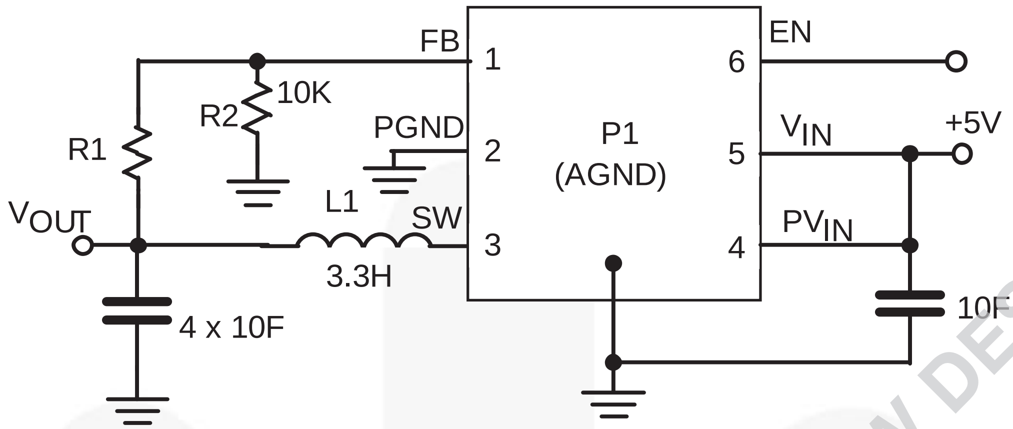


Figure 1. Typical Application

Pin Configuration

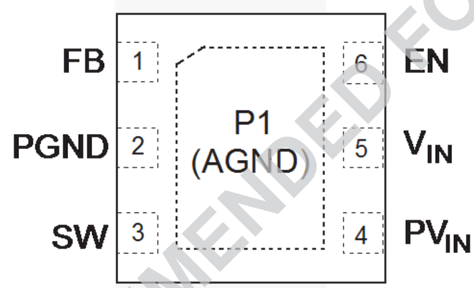


Figure 2. Pin Assignments

Pin Definitions

Pin #	Name	Description
P1	AGND	**Analog Ground**. P1 must be soldered to the PCB ground.
1	FB	**Feedback Input**. Adjustable voltage option; connect this pin to the resistor divider.
2	PGND	**Power Ground**. This pin is connected to the internal MOSFET switches. This pin must be externally connected to AGND.
3	SW	**Switching Node**. This pin is connected to the internal MOSFET switches.
4	PVIN	**Supply Voltage Input**. This pin is connected to the internal MOSFET switches.
5	VIN	**Supply Voltage Input**.
6	EN	**Enable Input**. Logic HIGH enables the chip and logic LOW disables the chip, reducing the supply current to less than 1 µA. Do not float this pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Input Voltage		-0.3	6.5	V
V_{IN}	Input Voltage on PVIN and Any Other Pin		-0.3	V_{IN}	V
θ_{JC}	Thermal Resistance-Junction to Tab[(1)]			8	°C/W
T_L	Lead Soldering Temperature (10 Seconds)			260	°C
T_{STG}	Storage Temperature		-65	150	°C
T_J	Junction Temperature		-40	150	°C
ESD	Electrostatic Discharge Protection Level[(2)]	HBM	4		kV
		CDM	2		

Notes:
1. Junction-to-ambient thermal resistance, θ_{JA}, is a strong function of PCB material, board thickness, thickness and number of copper planes, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics.
2. Using Mil Std. 883E, method 3015.7 (Human Body Model) and EIA/JESD22C101-A (Charged Device Model).

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbols	Parameter		Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage Range		4.5		5.5	V
V_{OUT}	Output Voltage Range, Adjustable Version		0.8		3.5	V
I_{OUT}	Output Current				1.5	A
L	Inductor[(3)]			3.3		µH
C_{IN}	Input Capacitor[(3)]			10		µF
C_{OUT}	Output Capacitor[(3)]			4 x 10		µF
T_A	Operating Ambient Temperature Range	FAN2012MPX	0		+85	°C
		FAN2012EMPX	-40		+85	°C

Notes:
3. Refer to the *Applications* section for details.

Electrical Characteristics

V_{IN} = 4.5 V to 5.5 V, V_{OUT} = 1.2 V, I_{OUT} = 200 mA, C_{IN} = 10 µF, C_{OUT} = 4 x 10 µF, L = 3.3 µH, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Input Voltage		4.5		5.5	V
I_Q	Quiescent Current	I_{OUT} = 0 mA		7	10	mA
V_{UVLO}	UVLO Threshold	V_{IN} Rising	3.4	3.7	4.0	V
		Hysteresis		150		mV
R_{ON_PMOS}	PMOS On Resistance	V_{IN} = V_{GS} = 5 V		150	290	M□
R_{ON_NMOS}	NMOS On Resistance	V_{IN} = V_{GS} = 5 V		150	290	m□
I_{LIMIT}	P-Channel Current Limit	4.5 V < V_{IN} < 5.5 V	2.2	2.6	3.5	A
T_{OVP}	Over-Temperature Protection	Rising Temperature		150		°C
		Hysteresis		20		°C
f_{SW}	Switching Frequency		1000	1300	1600	kHz
R_{LINE}	Line Regulation	V_{IN} = 4.5 to 5.5 V, I_{OUT} = 100 mA		0.16		%/V
R_{LOAD}	Load Regulation	0 mA ≤ I_{OUT} ≤ 1500 mA		0.2	0.5	%
V_{OUT}	Output Voltage During Load Transition(4)	I_{OUT} from 700 mA to 100 mA			5	%
		I_{OUT} from 100 mA to 700 mA	-5			%
I_{LEAK}	Reverse Leakage Current into Pin SW	V_{IN} = Open, EN = GND, V_{SW} = 5.5 V		0.1	1.0	µA
V_{REF}	Reference Voltage			0.8		V
V_{OUT}	Output Voltage Accuracy	V_{IN} = 4.5 to 5.5 V, 0 mA ≤ I_{OUT} ≤ 1500 mA; FAN2012MPX	-2		2	%
		FAN2012EMPX	-3		3	%
I_{SD}	Shutdown Mode Supply Current	V_{EN} = 0 V		0.1	1.0	µA
I_{BIAS}	EN Bias Current				0.1	µA
V_{ENH}	EN HIGH Voltage		1.3			V
V_{ENL}	EN LOW Voltage				0.4	V

Notes:

4. Please refer to the load transient response test waveform shown in Figure 3.

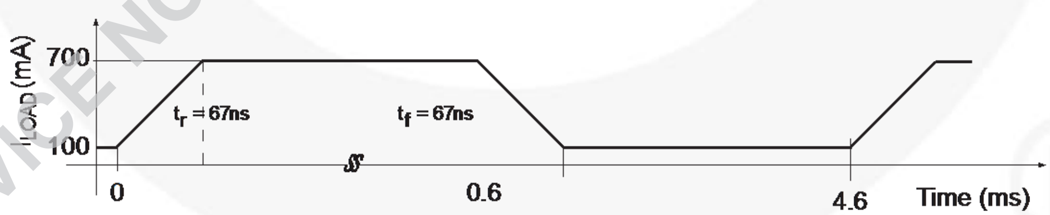


Figure 3. Load Transient Response Test Waveform

Typical Performance Characteristics

T_A = 25°C, C_{IN} = 10 µF, C_{OUT} = 40 µF, L = 3.3 µH, V_{IN} = 5 V; unless otherwise noted.

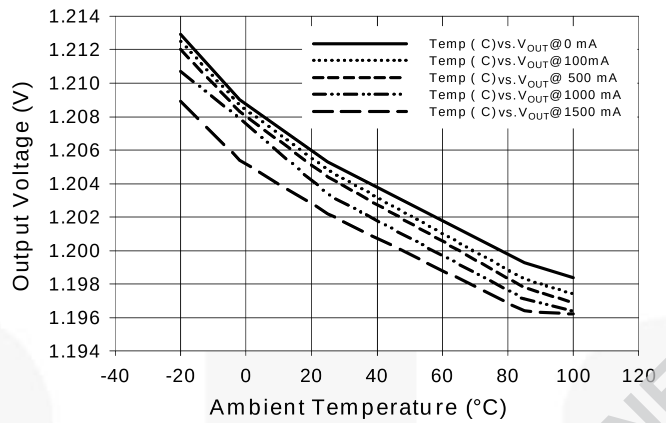


Figure 4. Output Voltage vs. Ambient Temperature

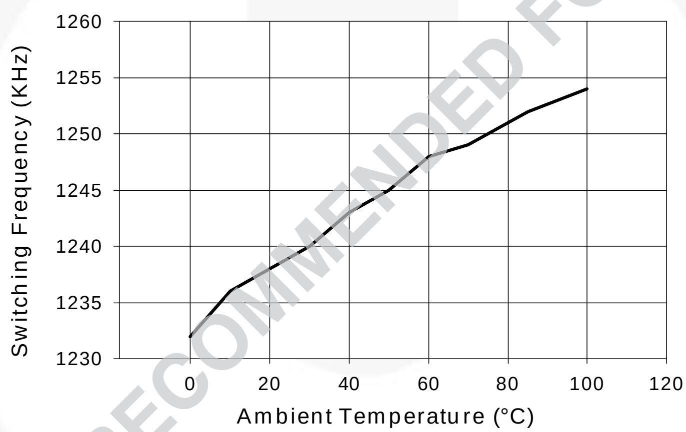


Figure 5. Switching Frequency vs. Ambient Temperature

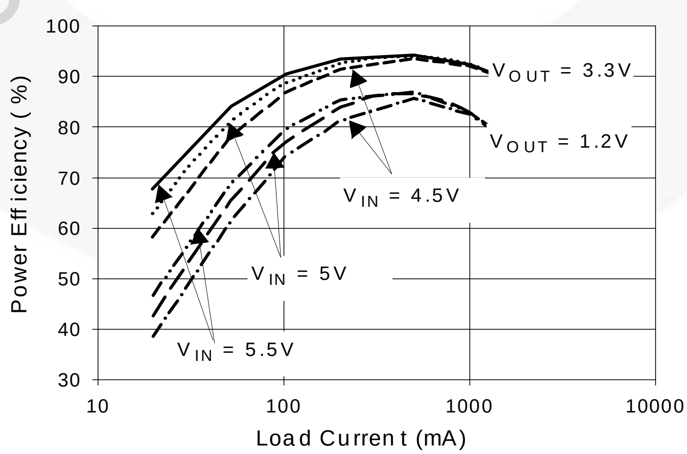


Figure 6. Efficiency vs. Load Current

Typical Performance Characteristics (Continued)

T_A = 25°C, C_{IN} = 10 µF, C_{OUT} = 40 µF, L = 3.3 µH, V_{IN} = 5 V; unless otherwise noted.

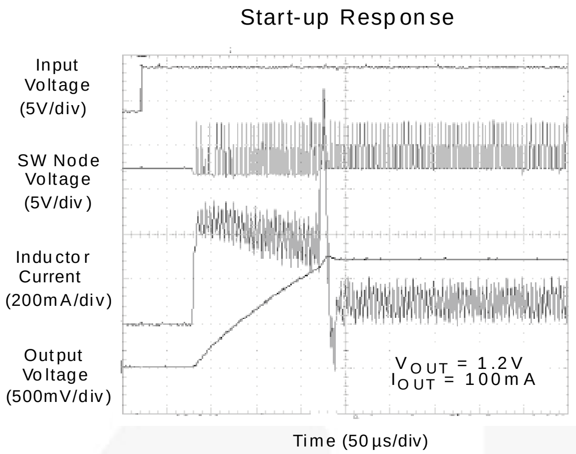


Figure 7. Startup Response

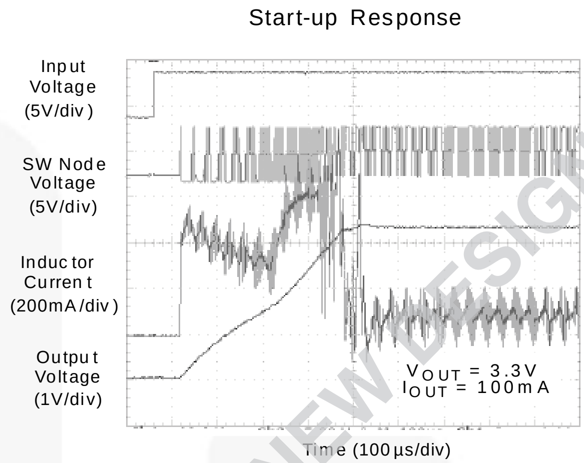


Figure 8. Startup Response

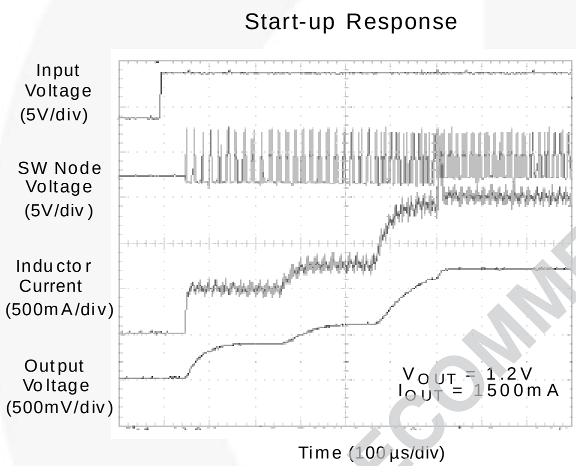


Figure 9. Startup Response

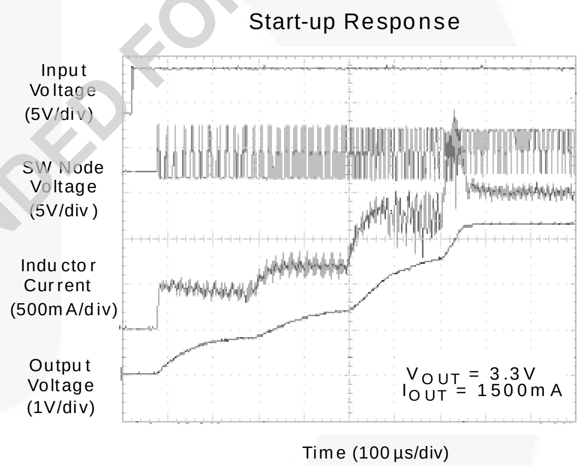


Figure 10. Startup Response

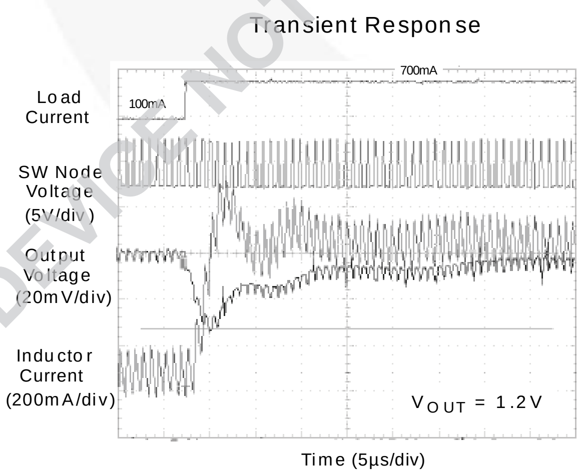


Figure 11. Transient Response

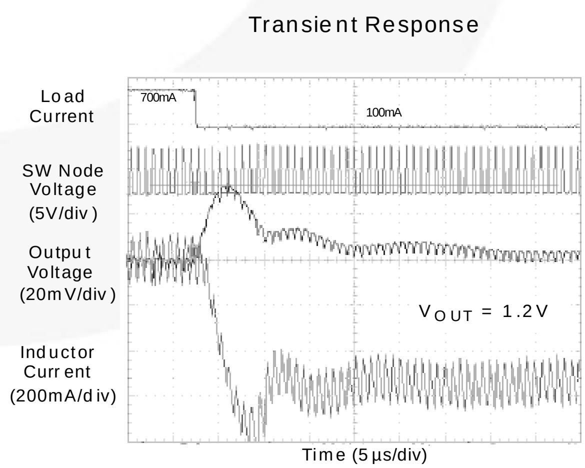


Figure 12. Transient Response

Block Diagram

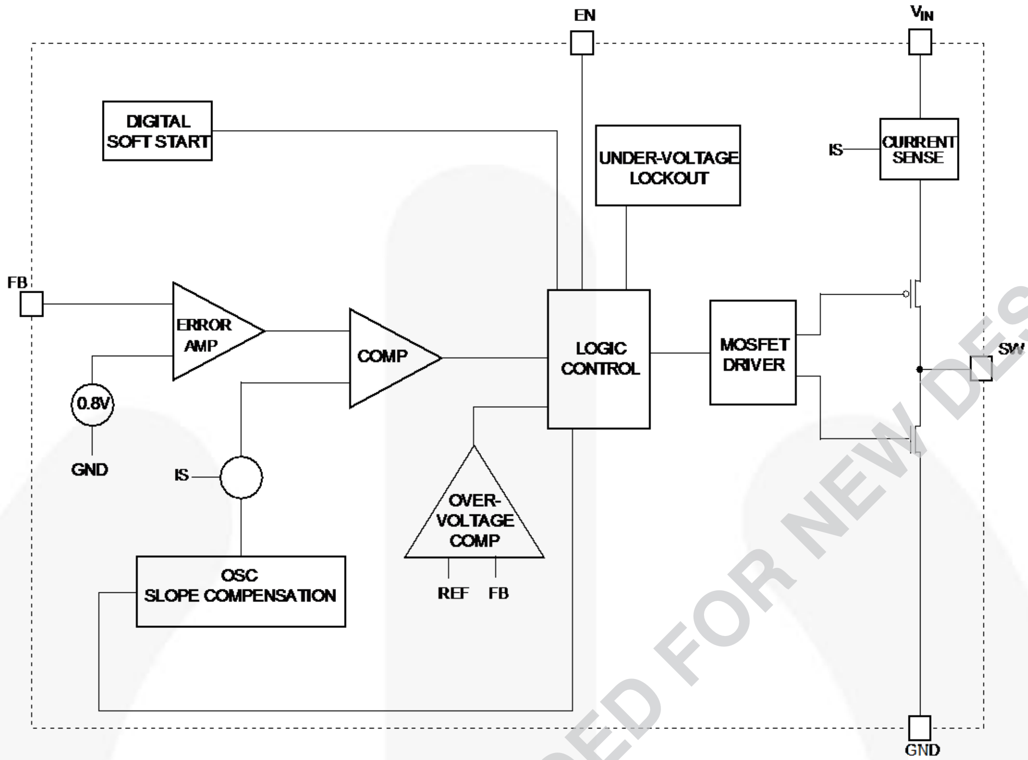


Figure 13. Block Diagram

Detailed Operation Description

The FAN2012 is a step-down pulse width modulated (PWM) current mode converter with a typical switching frequency of 1.3 MHz. At the beginning of each clock cycle, the P-channel transistor is turned on. The inductor current ramps up and is monitored via an internal circuit. The P-channel switch is turned off when the sensed current causes the PWM comparator to trip when the output voltage is in regulation or when the inductor current reaches the current limit (set internally, typically 2600 mA). After a minimum dead time, the N-channel transistor is turned on and the inductor current ramps down. As the clock cycle is completed, the N-channel switch is turned off and the next clock cycle starts. The duty cycle is solely given by the ratio of output voltage and input voltage. Therefore, the converter runs with a minimum duty cycle when output voltage is at minimum and input voltage is at maximum.

UVLO and Soft Start

The reference and the circuit remain reset until the V_{IN} crosses its UVLO threshold.

The FAN2012 has an internal soft-start circuit that limits the in-rush current during start-up. This prevents possible voltage drops of the input voltage and eliminates the output voltage overshoot. The soft-start is implemented as a digital circuit, increasing the switch current in four steps to the P-channel current limit (2600 mA). Typical start-up time for a 40 µF output capacitor and a load current of 1500 mA is 800 µs.

Short-Circuit Protection

The switch peak current is limited cycle by cycle to a typical value of 2600 mA. In the event of an output voltage short circuit, the device operates with a frequency of 400 kHz and minimum-duty cycle, therefore the average input current is typically 350 mA.

Thermal Shutdown

When the die temperature exceeds 150°C, a reset occurs and remains in effect until the die cools to 130°C, at which point, the circuit restarts.

Applications Information

Setting the Output Voltage

The internal voltage reference is 0.8 V. The output is divided down by a voltage divider, R1 and R2 to the FB pin. The output voltage is:

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right) \qquad \text{EQ. 2}$$

According to this equation, and assuming desired output voltage of 1.5096 V, and given R2 = 10 kΩ, the calculated value of R1 is 8.87 kΩ.

Inductor Selection

The inductor parameters directly related to device performance are saturation current and DC resistance. The FAN2012 operates with a typical inductor value of 3.3 µH. The lower the DC resistance, the higher the efficiency. For saturation current, the inductor should be rated higher than the maximum load current, plus half of the inductor ripple current calculated as follows:

$$\Delta I_L = V_{OUT} \times \frac{1-(V_{OUT}/V_{IN})}{L \times f} \qquad \text{EQ. 3}$$

where:

ΔI_L = Inductor Ripple Current
f = Switching Frequency
L = Inductor Value

Some recommended inductors are suggested in the table below:

Table 1. Recommended Inductors

Inductor Value	Vendor	Part Number
3.3 µH	Panasonic	ELL6PM3R3N
3.3 µH	Murata	LQS66C3R3M04
3.3 µH	Coiltronics	SD-3R3-R

Capacitors Selection

For best performances, a low-ESR input capacitor is required. A ceramic capacitor of at least 10 µF, placed as close to the VIN and AGND pins of the device is recommended. The output capacitor determines the output ripple and the transient response.

Table 2. Recommended Capacitors

Capacitor Value	Vendor	Part Number
10 µF	Taiyo Yuden	JMK212BJ106MG
		JMK316BJ106KL
	TDK	C2012X5ROJ106K
		C3216X5ROJ106M
	Murata	GRM32ER61C106K

PCB Layout Recommendations

The inherently high peak currents and switching frequency of power supplies require a careful PCB layout design. For best results, use wide traces for high-current paths and place the input capacitor, the inductor, and the output capacitor as close as possible to the integrated circuit terminals. To minimize voltage stress to the device resulting from ever-present switching spikes, use an input bypass capacitor with low ESR. Use of an external Schottky diode, with its anode connected to SW node and cathode connected to PVIN, further reduces switching spikes. Note that the peak amplitude of the switching spikes depends upon the load current; the higher the load current, the higher the switching spikes.

The resistor divider that sets the output voltage should be routed away from the inductor to avoid RF coupling. The ground plane at the bottom side of the PCB acts as an electromagnetic shield to reduce EMI. The recommended PCB layout is shown below in Figure 14.

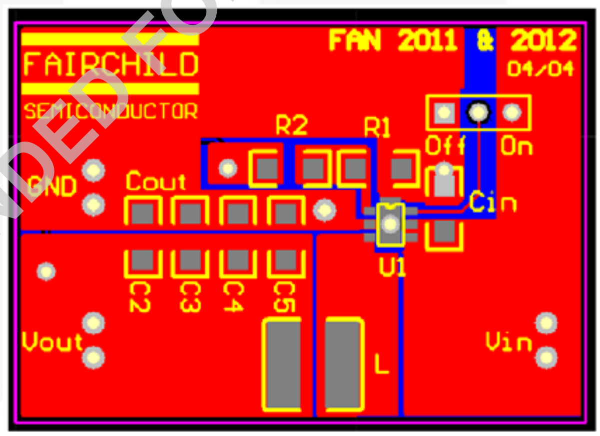
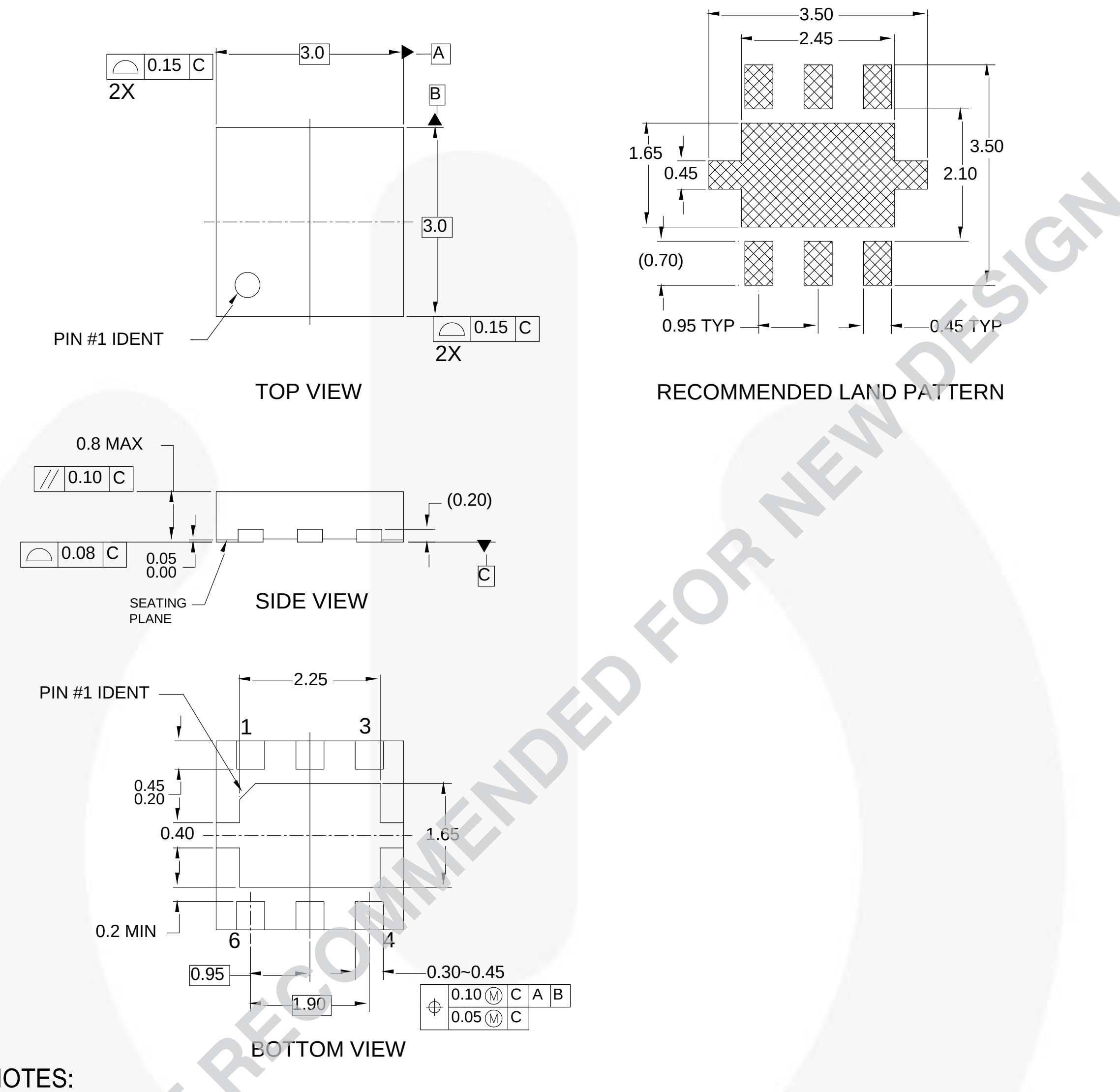


Figure 14. Recommended PCB Layout

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION WEEA, DATED 11/2001 EXCEPT FOR DAP EXTENSION TABS

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP06FrevA

Figure 15. 3x3 mm, 6-Lead, Molded Leadless Package (MLP)

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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