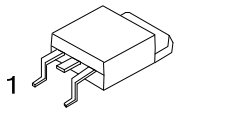
F5N50K-TC

Power MOSFET

5.0A, 500V N-CHANNEL POWER MOSFET



TO-252

■ DESCRIPTION

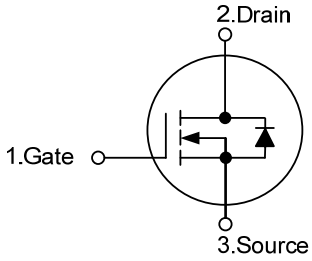
The UTC **F5N50K-TC** is a N-channel power MOSFET adopting UTC's advanced technology to provide customers with DMOS, planar stripe technology. This technology is designed to meet the requirements of the minimum on-state resistance and perfect switching performance. It also can withstand high energy pulse in the avalanche and communication mode.

The UTC **F5N50K-TC** can be used in applications, such as active power factor correction, high efficiency switched mode power supplies, electronic lamp ballasts based on half bridge topology.

■ FEATURES

* $R_{DS(ON)} \leq 1.8\Omega$ @ V_{GS}=10V, I_D=2.5A
* 100% avalanche tested
* High switching speed

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
F5N50KL-TN3-R	F5N50KG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

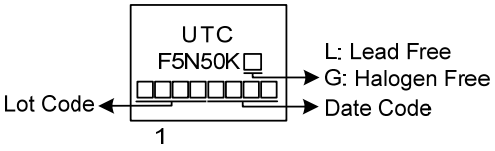
F5N50KG-TN3-R

(1)Packing Type — (1) R: Tape Reel

(2)Package Type — (2) TN3: TO-252

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous	I_D	5	A
	Pulsed (Note 2)	I_{DM}	20	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	104	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	6.3	V/ns
Power Dissipation		P_D	54	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. L = 16mH, I_{AS} = 3.6A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. I_{SD} ≤5.0A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

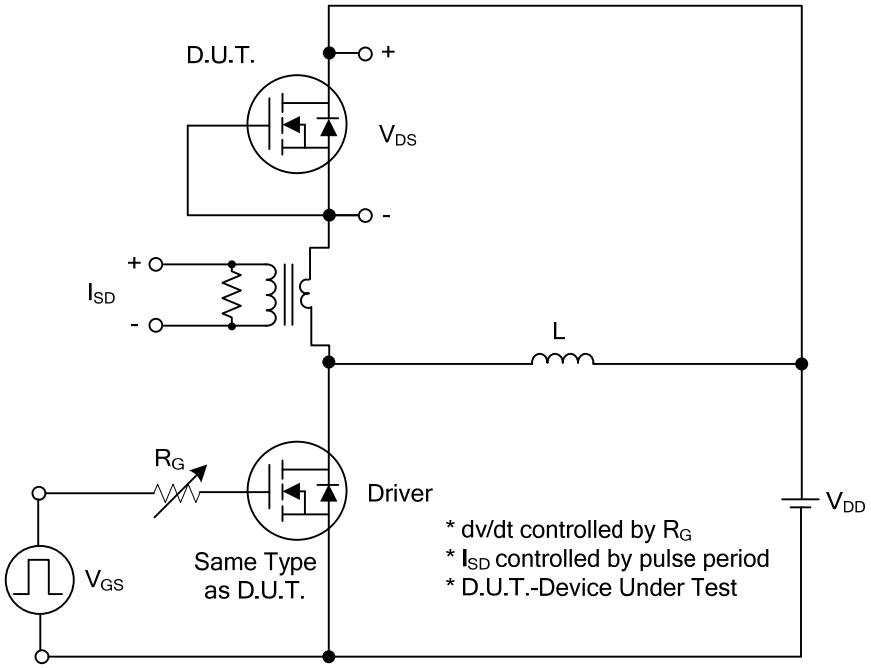
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	°C/W
Junction to Case	θ_{JC}	2.3	°C/W

■ ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

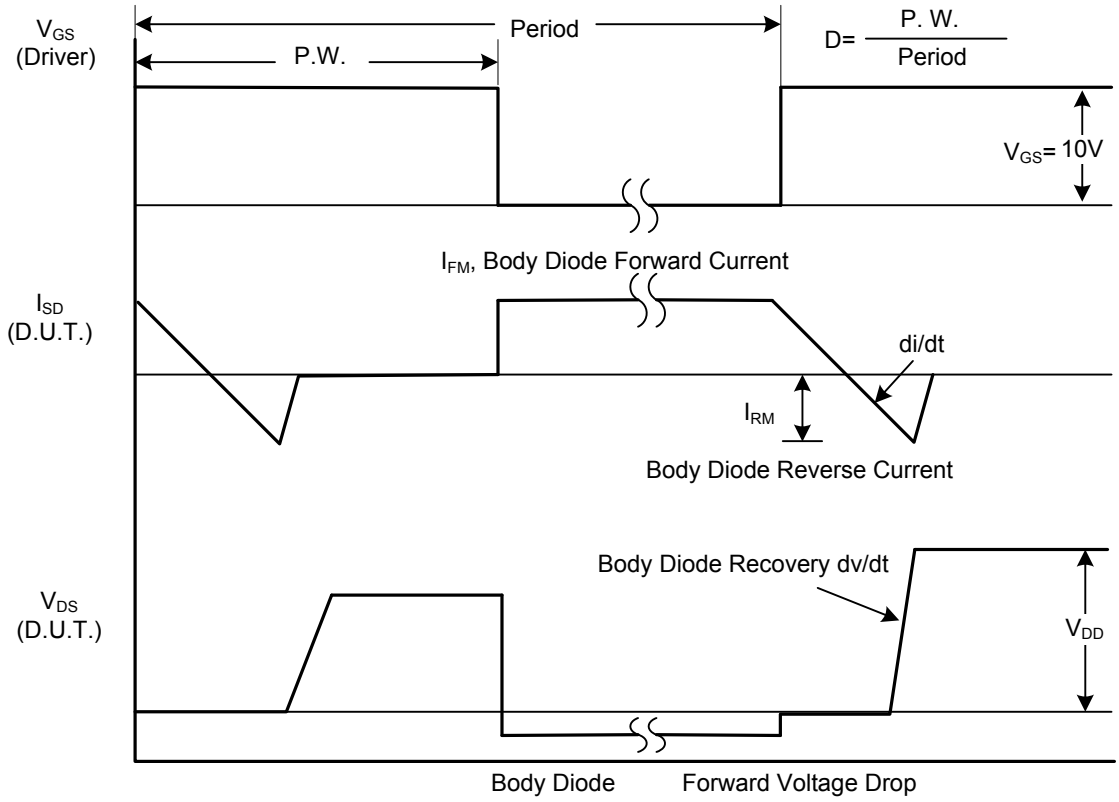
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	500			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=500V, V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V, V_{DS}=0V			100	nA
	Reverse		V_{GS}=-30V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=2.5A			1.8	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V V_{GS}=0V,V_{DS}=25V, f=1.0MHz		585		pF
Output Capacitance		C_{OSS}			58		pF
Reverse Transfer Capacitance		C_{RSS}			7.0		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	V_{DS}=200V, V_{GS}=10V, I_D=5.0A I_G=1mA (Note 1, 2)		5.2		nC
Gate to Source Charge		Q_{GS}			2.8		nC
Gate to Drain Charge		Q_{GD}			1.1		nC
Turn-ON Delay Time (Note 1)		$t_{D(ON)}$	V_{DD}=30V, V_{GS}=10V, $_D$=0.75A, R_G =25Ω (Note 1, 2)		7.6		ns
Rise Time		t_R			18.6		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			36		ns
Fall-Time		t_F			18		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				5	A
Maximum Body-Diode Pulsed Current		I_{SM}				20	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	I_S=5.0A, V_{GS}=0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)		t_{rr}	I_S=5.0A, V_{GS}=0V, dI_F/dt=100A/μs		102		ns
Body Diode Reverse Recovery Charge		Q_{rr}			0.33		μC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

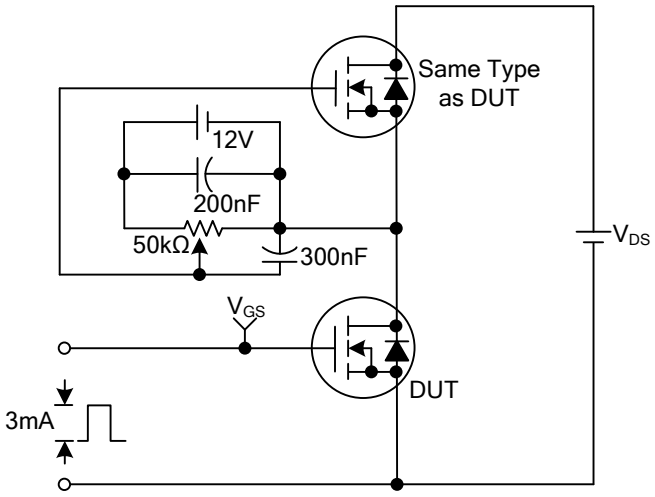


Peak Diode Recovery dv/dt Test Circuit

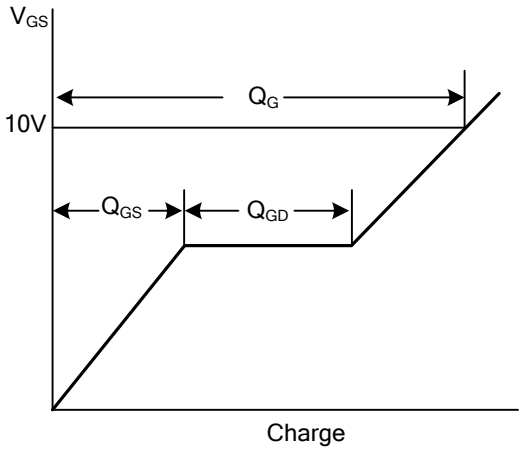


Peak Diode Recovery dv/dt Waveforms

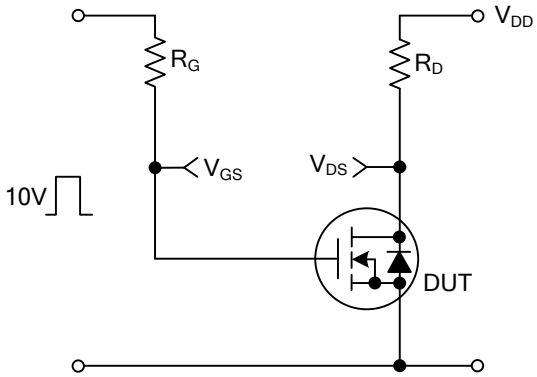
■ TEST CIRCUITS AND WAVEFORMS



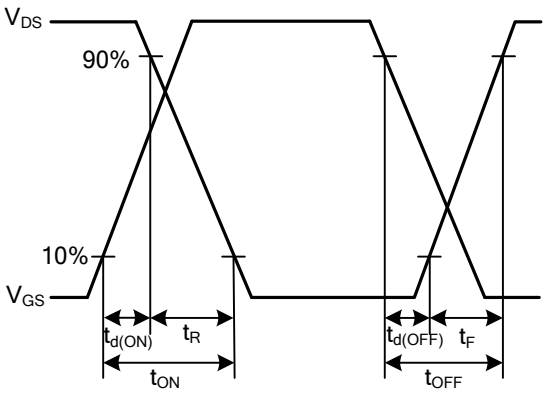
Gate Charge Test Circuit



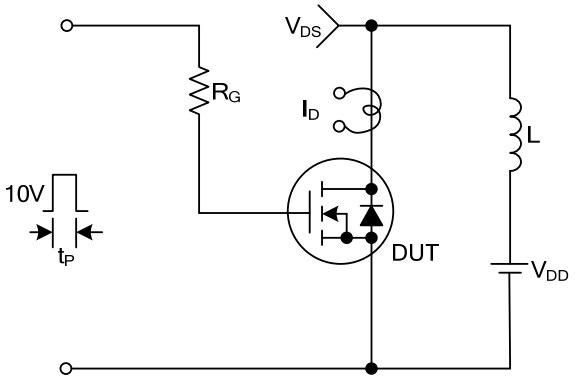
Gate Charge Waveforms



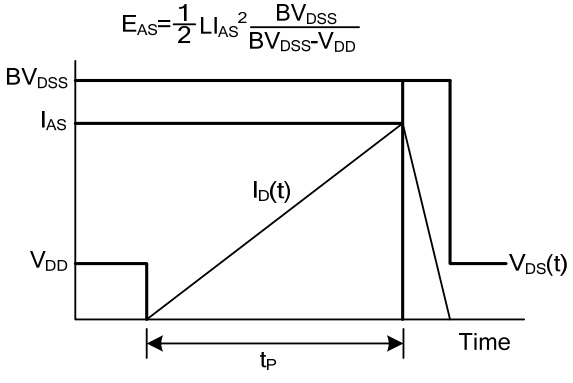
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms