



600V Depletion-Mode Power MOSFET

Pb Lead Free Package and Finish

General Features

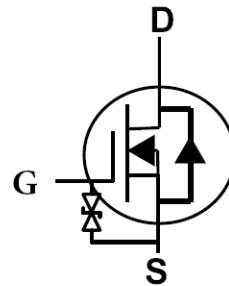
- Proprietary Advanced Planar Technology
- Depletion Mode (Normally On)
- ESD improved Capability
- Rugged Polysilicon Gate Cell Structure
- Fast Switching Speed
- RoHS Compliant
- Halogen-free available

Applications

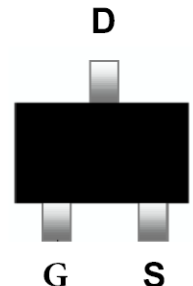
- Synchronous Rectification
- Normally-on Switches
- Linear Amplifier, Converters
- Constant Current Source
- Telecom

BV_{DSX}	$R_{DS(ON),typ.}$	I_{DSS}
600V	350Ω	12mA

Symbol



Package:SOT-23



Ordering Information

Part Number	Marking	Package	Brand
F501D	F501D	SOT-23	

Absolute Maximum Ratings

$T_C=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	F501D	Unit
V_{DSX}	Drain-to-Source Voltage _[1]	600	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D	Continuous Drain Current	0.030	A
	Continuous Drain Current @ $T_C=70^{\circ}\text{C}$	0.025	
I_{DM}	Pulsed Drain Current _[2]	0.120	
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5k Ω)	300	V
P_D	Power Dissipation	0.5	W
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300	$^{\circ}\text{C}$
$T_J \& T_{STG}$	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	F501D	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	250	K / W



Electrical Characteristics

OFF Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSX}	Drain-to-Source Breakdown Voltage	600	--	--	V	$V_{GS} = -15\text{V}$, $I_D = 250\mu\text{A}$
$I_{D(OFF)}$	Drain-to-Source Leakage Current	--	--	0.1	μA	$V_{DS} = 600\text{V}$, $V_{GS} = -5\text{V}$
		--	--	10		$V_{DS} = 480\text{V}$, $V_{GS} = -5\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	$V_{GS} = +10\text{V}$, $V_{DS} = 0\text{V}$
		--	--	-100		$V_{GS} = -10\text{V}$, $V_{DS} = 0\text{V}$

ON Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{DSS}	Saturated Drain-to-Source Current	12	--	--	mA	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	350	700	Ω	$V_{GS} = 0\text{V}$, $I_D = 3.0\text{mA}_{[3]}$
$V_{GS(OFF)}$	Gate-to-Source Cut-off Voltage	-2.7	-1.8	-1.0	V	$V_{DS} = 3\text{V}$, $I_D = 8.0\mu\text{A}$
g_{fs}	Forward Transconductance	0.008	0.017	--	S	$V_{DS} = 50\text{V}$, $I_D = 0.01\text{A}$

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	50	--	pF	$V_{GS} = -5\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$
C_{rss}	Reverse Transfer Capacitance	--	1.1	--		
C_{oss}	Output Capacitance	--	4.5	--		
Q_g	Total Gate Charge	--	1.1	--	nC	$V_{GS} = -5\text{V} \sim +5\text{V}$, $I_D = 10\text{mA}$, $V_{DS} = 400\text{V}$
Q_{gs}	Gate-to-Source Charge	--	0.5	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	0.35	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	9.9	--	nS	$V_{DD} = 300\text{V}$, $I_D = 10\text{mA}$, $V_{GS} = -5\text{V} \sim +5\text{V}$ $R_G = 6.1\Omega$
t_{rise}	Rise Time	--	50	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	55	--		
t_{fall}	Fall Time	--	130	--		

**Source-Drain Body Diode Characteristics** $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	0.025	A	$T_a=25^{\circ}\text{C}$
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	0.100		
V_{SD}	Diode Forward Voltage	--	--	1.2	V	$I_S=15\text{mA}$, $V_{GS}=-5\text{V}$
t_{rr}	Reverse Recovery Time	--	240	--	ns	$I_F=10\text{mA}$, $T_J=25^{\circ}\text{C}$, $dI_F/dt=100\text{A}/\mu\text{s}$, $V_R=300\text{V}$
Q_{rr}	Reverse Recovery Charge	--	625	--	nC	

Note: $V_{GSO@IGS}=\pm 1\text{mA}(\text{Open Drain})>20$

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.



Typical Characteristics

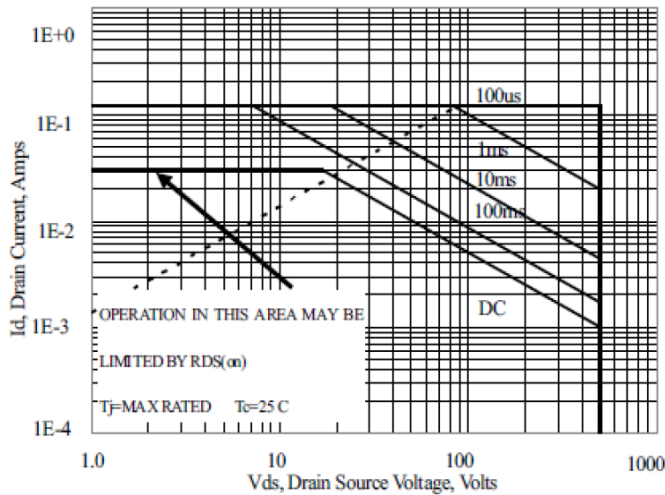


Figure 1 Maximum Forward Bias Safe Operating Area

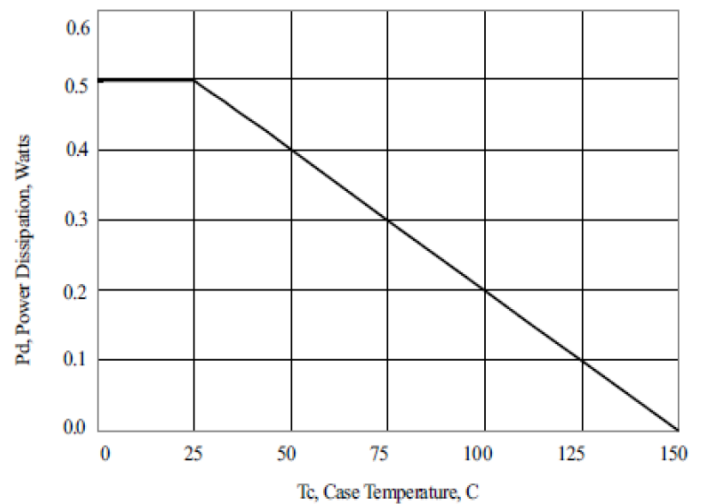


Figure 2 Maximum Power Dissipation vs Case Temperature

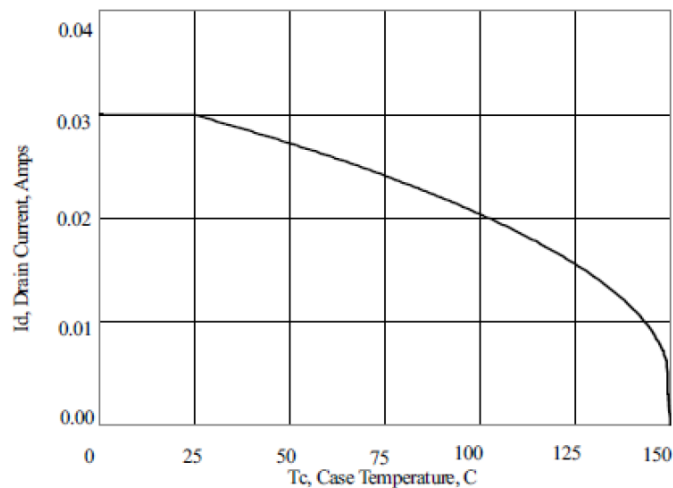


Figure 3 Maximum Continuous Drain Current vs Case Temperature

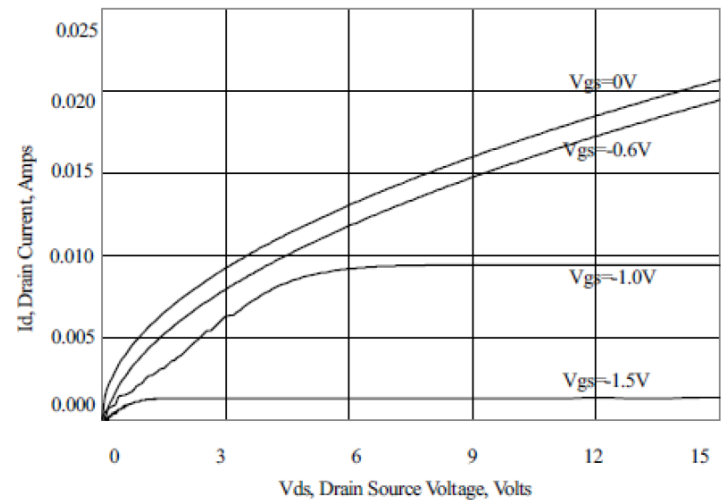


Figure 4 Typical Output Characteristics

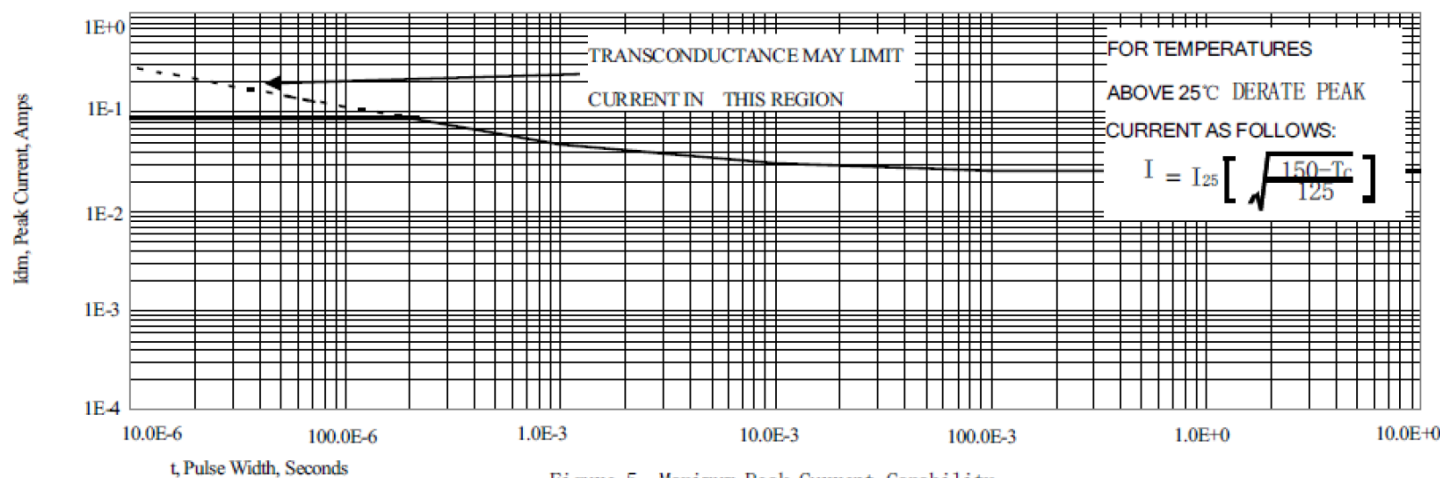


Figure 5 Maximum Peak Current Capability

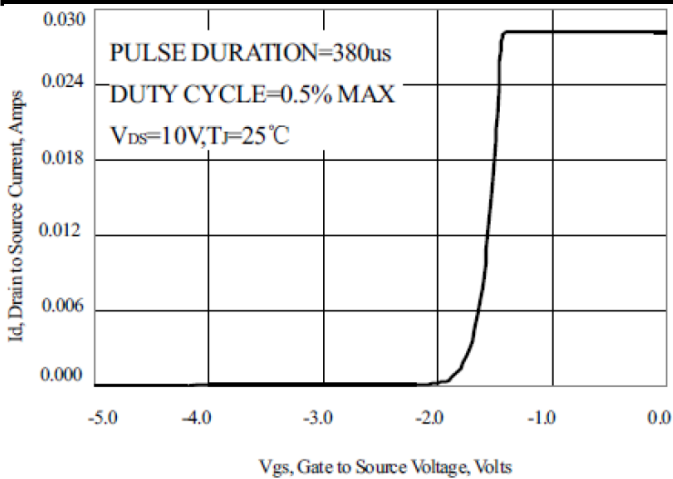


Figure 6 Typical Transfer Characteristics

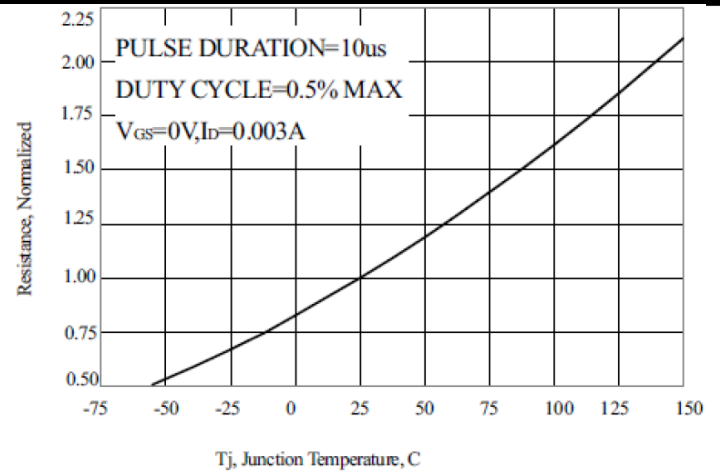


Figure 7 Typical Drain to Source ON Resistance vs Junction Temperature

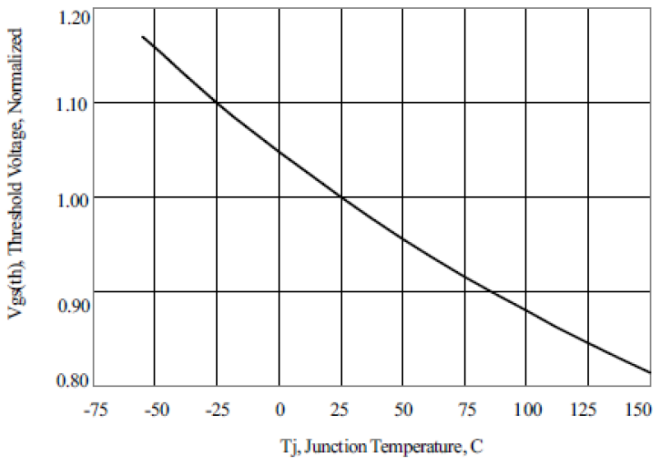


Figure 8 Typical Threshold Voltage vs Junction Temperature

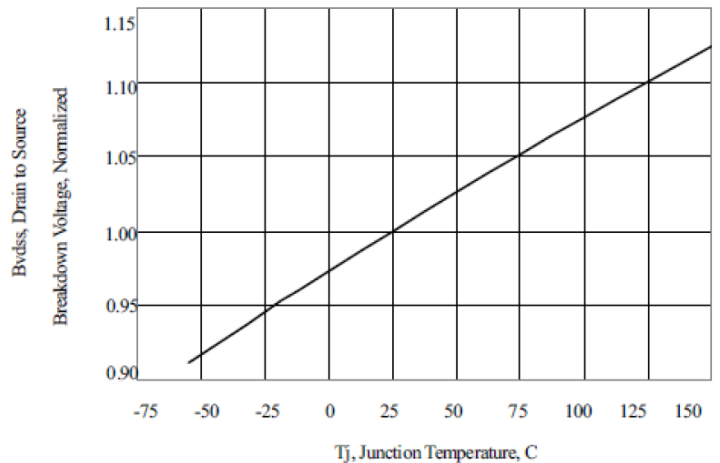


Figure 9 Typical Breakdown Voltage vs Junction Temperature

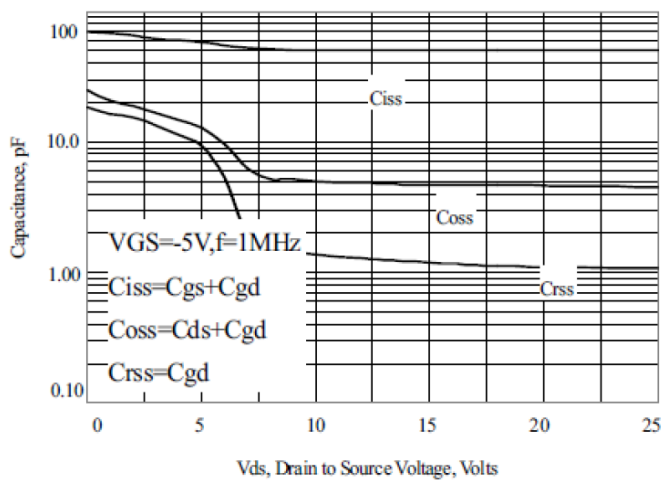


Figure 10 Typical Capacitance vs Drain to Source Voltage

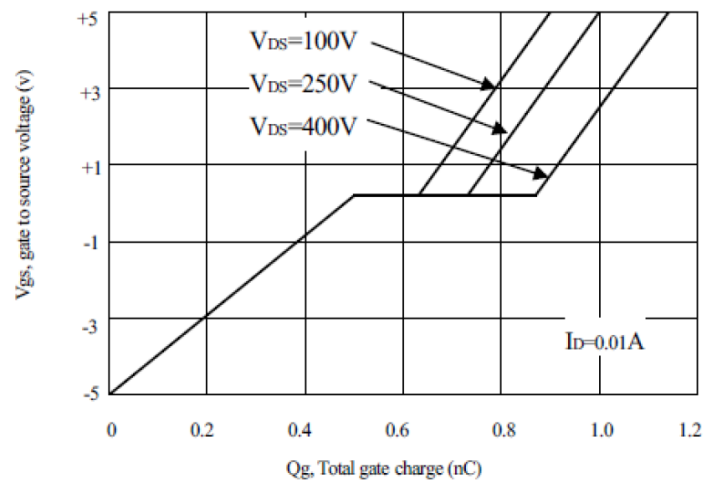


Figure 11 Typical Gate Charge vs Gate to Source Voltage



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