Description

The F2911 is a high reliability, low insertion loss, 75Ω SPST RF switch designed for a multitude of wireless and RF applications. This device covers a broad frequency range from 1MHz to 3500MHz. In addition to providing low insertion loss, the F2911 also delivers excellent linearity and isolation performance while providing a 75Ω termination on one port in the isolation mode.

The F2911 uses a single positive supply voltage supporting either 3.3V or 1.8V control logic.

Competitive Advantage

The F2911 provides broadband RF performance to support the CATV market along with high power handling, and high isolation.

- Low insertion loss
- High isolation
- Excellent linearity
- Extended temperature range

Typical Applications

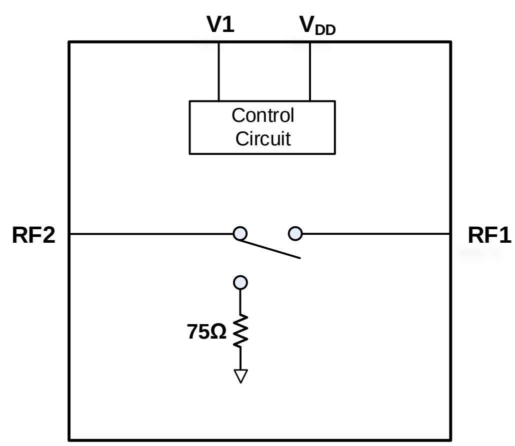
- CATV Infrastructure
- CATV Set-Top Boxes
- CATV Satellite Modems
- Data Network Equipment
- Fiber Networks

Features

- Low insertion loss: 0.33dB at 1200MHz
- High isolation: 53dB at 1200MHz
- Supply voltage: +2.7V to +5.5V
- 1.8V and 3.3V compatible control logic
- -40°C to +105°C operating temperature range
- 2mm x 2mm, 8-pin DFN package

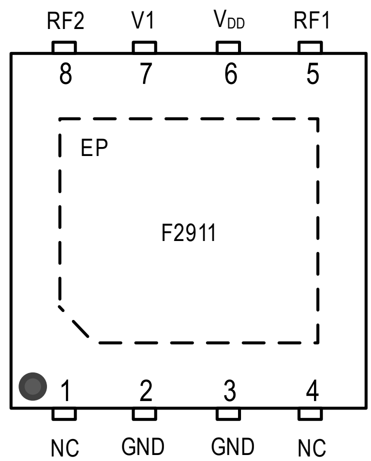
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 2mm x 2mm x 0.9mm 8-DFN – Top View



Pin Descriptions

Table 1. Pin Descriptions

Pin	Name	Function
1, 4	NC	No internal connection. This pin may be connected to the exposed paddle and can be grounded.
2, 3	GND	Ground. This pin is internally connected to the ground paddle. Ground this pin as close to the device as possible.
5	RF1	RF1 port. This pin is matched to 75Ω in the insertion loss state only. If this pin is not 0V DC, then an external coupling capacitor must be used.
6	V_{DD}	Power supply. Bypass to GND with capacitors as shown in the Figure 16 as close as possible to pin.
7	V1	Logic control pin. See Table 7 for proper logic setting.
8	RF2	RF2 port. Matched to 75Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
	EP	Exposed pad. This pad is internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device and into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
V_{DD} to GND		V_{DD}	-0.3	+6.0	V
V1 to GND		V_{LOGIC}	-0.3	Lower of (V_{DD} + 0.3V, 3.6V)	V
RF1, RF2 to GND		V_{RF}	-0.3	+0.3	V
RF Input Power, CW $Z_S = Z_L = 75\Omega$ T_{EP} = 25°C [a] V_{DD} = +3.3V	RF1 or RF2 as input (Insertion loss state)	P_{RFCW12}		31	dBm
	RF1 as input (Isolation state)	P_{RF1CW_ISO}		21	
	RF2 as input (Isolation state)	P_{RF2CW_ISO}		28	
RF Input Power, Peak $Z_S = Z_L = 75\Omega$ T_{EP} = 25°C [a], [b] V_{DD} = +3.3V	RF1 or RF2 as input (Insertion loss state)	P_{RFPK12}		34	dBm
	RF1 as input (Isolation state)	P_{RF1PK_ISO}		24	
	RF2 as input (Isolation state)	P_{RF2PK_ISO}		31	
Maximum Junction Temperature		T_{JMAX}		+140	°C
Storage Temperature Range		T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)		T_{LEAD}		+260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)		V_{ESDHBM}		2000 (Class 2)	V
ElectroStatic Discharge – CDM (JEDEC 22-C101F)		V_{ESDCDM}		1000 (Class C3)	V

a. T_{EP} = Temperature at the exposed paddle (see Table 3).
b. 5% duty cycle of a 4.6ms period.

Recommended Operating Conditions

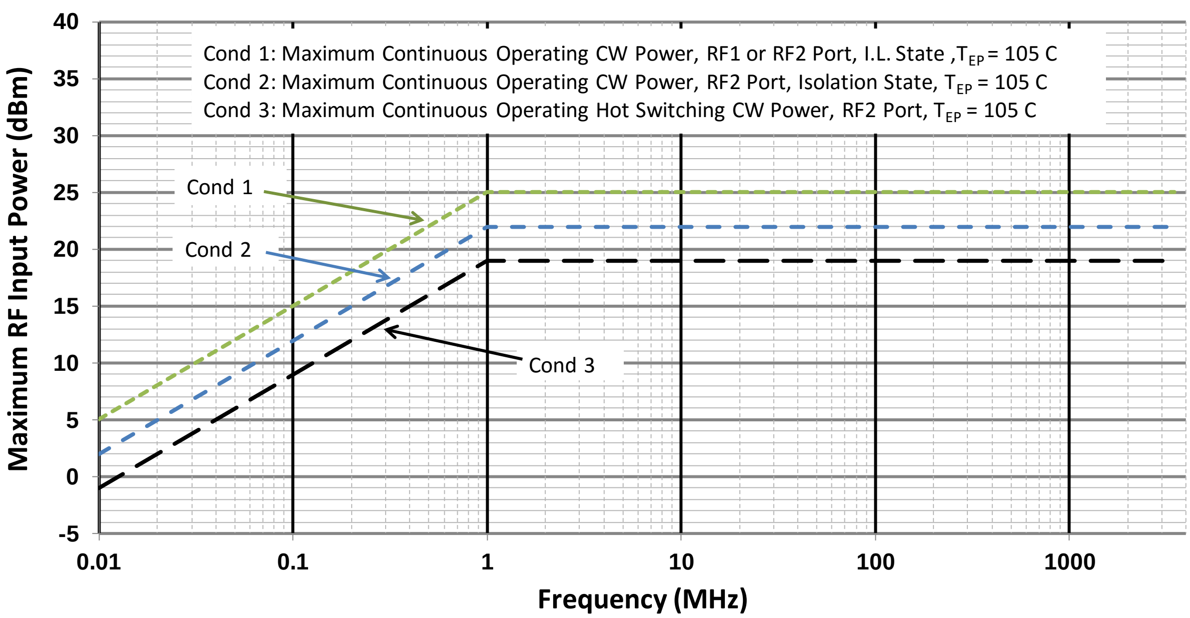
Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition		Min	Typical	Max	Units
Power Supply Voltage	V_{DD}			2.7		5.5	V
Operating Temperature Range	T_{EP}	Exposed paddle temperature		-40		+105	°C
RF Frequency Range	f_{RF}			1		3500	MHz
RF Input CW Power (Non-Switched) [a]	P_{RFCW}	RF1 or RF2 as the input (Insertion loss state)	T_{EP} = 85°C			28	dBm
			T_{EP} = 105°C			25	
		RF1 as the input (Isolation state)	T_{EP} = 85°C			18	
			T_{EP} = 105°C			15	
		RF2 as the input (Isolation state)	T_{EP} = 85°C			25	
			T_{EP} = 105°C			22	
RF Input Peak Power (Non-Switched) [a], [b]	P_{RFPK}	RF1 or RF2 as the input (Insertion loss state)	T_{EP} = 85°C			31	dBm
			T_{EP} = 105°C			28	
		RF1 as the input (Isolation state)	T_{EP} = 85°C			21	
			T_{EP} = 105°C			18	
		RF2 as the input (Isolation state)	T_{EP} = 85°C			28	
			T_{EP} = 105°C			25	
RF Continuous Input Power (RF Hot Switching CW) [a]	P_{RFSW}	Applied to RF2 and switching between insertion loss to isolation state	T_{EP} = 85°C			22	dBm
			T_{EP} = 105°C			19	
RF1/2 Port Impedance	Z_{RFx}	Insertion loss state			75		Ω
RF2 Port Impedance	Z_{RFx}	Isolation state			75		Ω

a. Levels based on: V_{DD} = +2.7V to +5.5V, 1MHz ≤ f_{RF} ≤ 3500MHz, Z_S = Z_L = 75Ω. See Figure 3 for power handling derating vs. RF frequency.

b. 5% duty cycle of a 4.6ms period.

Figure 3. Maximum RF Input Operating Power vs. RF Frequency (Z_S = Z_L = 75Ω)



Electrical Characteristics

Table 4. Electrical Characteristics

See the F2911 Typical Application Circuit. Specifications apply when operated with V_{DD} = +3.3V, T_{EP} = +25°C, f_{RF} = 1000MHz, driven port = RF2, P_{IN} = 0dBm, Z_S = Z_L = 75Ω. PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Min	Typical	Max	Units
Logic Input High	V_{IH}	+2.7V ≤ V_{DD} ≤ +5.5V	***1.1*** [a]		Lower of (V_{DD}, 3.6)	V
Logic Input Low	V_{IL}		-0.3 [b]		***0.6***	V
Logic Current	I_{IH}, I_{IL}		***-1***		***+1***	µA
DC Current	I_{DD}	V_{DD} = 3.3V		190	***304***	µA
		V_{DD} = 5.0V		230		
Insertion Loss	IL	1MHz ≤ f_{RF} ≤ 50MHz [c]		0.24	***0.44***	dB
		50MHz < f_{RF} ≤ 250MHz		0.26		
		250MHz < f_{RF} ≤ 750MHz		0.29		
		750MHz < f_{RF} ≤ 1000MHz		0.31		
		1000MHz < f_{RF} ≤ 1200MHz		0.33		
		1200MHz < f_{RF} ≤ 1800MHz [c]		0.39	***0.55***	
		1800MHz < f_{RF} ≤ 2000MHz		0.39		
		2000MHz < f_{RF} ≤ 3500MHz		0.89		
Isolation	ISO	1MHz ≤ f_{RF} ≤ 50MHz	75	84		dB
		50MHz < f_{RF} ≤ 250MHz		70		
		250MHz < f_{RF} ≤ 750MHz		59		
		750MHz < f_{RF} ≤ 1000MHz		55		
		1000MHz < f_{RF} ≤ 1200MHz		53		
		1200MHz < f_{RF} ≤ 1800MHz		46		
		1800MHz < f_{RF} ≤ 2000MHz		45		
		2000MHz < f_{RF} ≤ 3500MHz		35		
RF1, RF2 Return Loss [d] (Insertion Loss State)	RF_{RL}	1MHz ≤ f_{RF} ≤ 50MHz		33		dB
		50MHz < f_{RF} ≤ 250MHz		32		
		250MHz < f_{RF} ≤ 750MHz		27		
		750MHz < f_{RF} ≤ 1000MHz		25		
		1000MHz < f_{RF} ≤ 1200MHz		23		
		1200MHz < f_{RF} ≤ 1800MHz		20		
		1800MHz < f_{RF} ≤ 2000MHz		20		
		2000MHz < f_{RF} ≤ 3500MHz		10		
RF2 Return Loss [d] (Isolation State)	RF_{RLISO}	1MHz ≤ f_{RF} ≤ 50MHz		27		dB
		50MHz < f_{RF} ≤ 250MHz		27		
		250MHz < f_{RF} ≤ 750MHz		25		
		750MHz < f_{RF} ≤ 1000MHz		23		
		1000MHz < f_{RF} ≤ 1200MHz		22		
		1200MHz < f_{RF} ≤ 1800MHz		20		
		1800MHz < f_{RF} ≤ 2000MHz		20		
		2000MHz < f_{RF} ≤ 3500MHz		11		

a. Items in min/max columns in ***bold italics*** are guaranteed by test (GBT).
b. Items in min/max columns that are not bold italics are guaranteed by design characterization (GBDC).
c. Maximum specification limit is GBT at 50MHz and 1.8GHz, and it is GBDC over the whole frequency range.
d. Return loss includes mismatch effects of the Evaluation Kit PCB and RF connectors.

Electrical Characteristics

Table 5. Electrical Characteristics

See the F2911 Typical Application Circuit. Specifications apply when operated with V_{DD} = +3.3V, T_{EP} = +25°C, f_{RF} = 1000MHz, driven port = RF2, P_{IN} = 0dBm, Z_S = Z_L = 75Ω. PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Input 1dB Compression [c]	ICP_{1dB}	f_{RF} =1MHz			33		dBm
		f_{RF} = 10MHz			34		
		f_{RF} = 2000MHz			34		
		f_{RF} = 3500MHz			34		
Input 0.1dB Compression [c]	$ICP_{0.1dB}$	f_{RF} = 1MHz			30		dBm
		f_{RF} = 10MHz			33		
		f_{RF} = 2000MHz			33		
		f_{RF} = 3500MHz			33		
Input IP2 [d]	IIP2	P_{IN} = 13dBm/tone f_1+ f_2 frequency	f_1 = 5MHz f_2 = 6MHz		86		dBm
			f_1 = 185MHz f_2 = 190MHz		120		
			f_1 = 895MHz f_2 = 900MHz		121		
			f_1 = 1745MHz f_2 = 1750MHz		117		
Input IP3 [d]	IIP3	P_{IN} = 13dBm/tone	f_1 = 5MHz f_2 = 6MHz		52		dBm
			f_1 = 185MHz f_2 = 190MHz		64		
			f_1 = 1790MHz f_2 = 1795MHz		66		
			f_1 = 3490MHz f_2 = 3495MHz		64		
CTB / CSO		77 and 110 channels, P_{OUT} = 44dBmV			-95		dBc
Non-RF Driven Spurious [e]	$Spur_{MAX}$	Out any RF port when externally terminated into 75Ω			-100		dBm
Switching Time [f]	T_{SW}	50% control to 90% RF			1.0		μs
		50% control to 10% RF			1.0		
		50% control to RF settled to within +/- 0.1dB of I.L. value			1.1		
Maximum Switching Rate	SW_{RATE}				25		kHz
Maximum Video Feed-Through on RF Ports	VID_{FT}	Peak transients during switching Measured with 20ns rise time 0 to +3.3V control pulse			10		mV_{pp}

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns not in bold italics are guaranteed by design characterization.
c. The input 0.1dB and 1dB compression points are linearity figures of merit. Refer to the “Recommended Operating Conditions” section and Figure 3 for the maximum operating power levels.
d. RF1 or RF2 driven IIP2 and IIP3 results when in the insertion loss state.
e. Spurious due to on-chip negative voltage generator. Spurious fundamental = approximately 5.7MHz.
f. f_{RF} = 1GHz.

Thermal Characteristics

Table 6. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	160	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	θ_{JC_BOT}	15.1	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL1	

Typical Operating Conditions (TOCs)

Unless otherwise noted:

- V_{DD} = +3.3V
- T_{EP} = 25°C
- Z_S = Z_L = 75Ω
- f_{RF} = 1GHz
- Small signal tests done at 0dBm input power.
- RF2 is the driven port.
- All temperatures are referenced to the exposed paddle.
- Evaluation Kit (EVKit) traces and connector losses are de-embedded for the insertion loss and isolation plots. All other plots include the loss and effects of the PCB.

Typical Performance Characteristics [1]

Figure 4. RF2 to RF1 Insertion Loss vs. Frequency over Temp. and Voltage

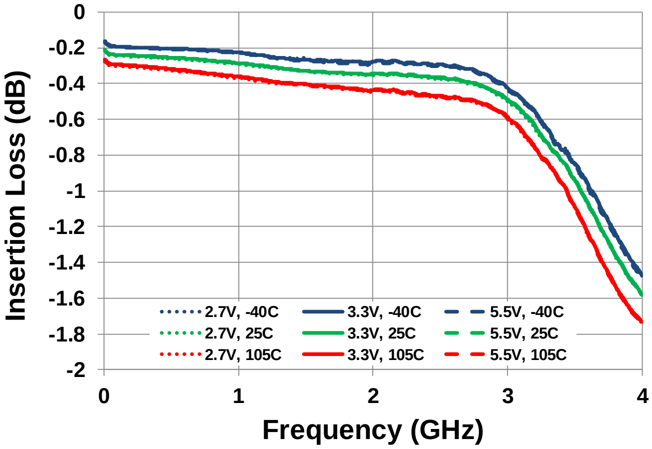


Figure 5. RF2 to RF1 Isolation vs. Frequency over Temperature and Voltage

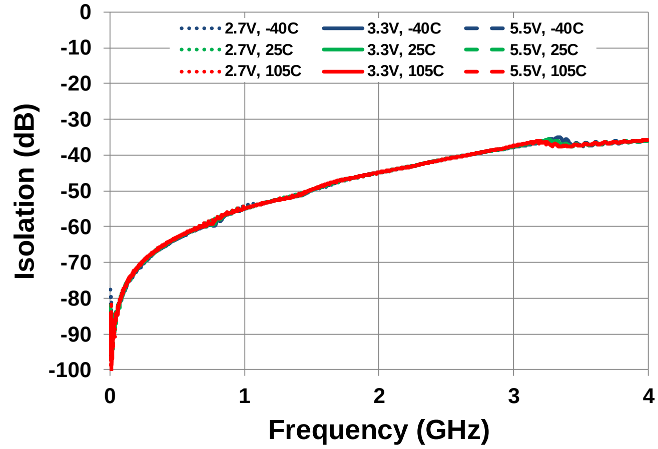


Figure 6. RF1 Port On State Return Loss vs. Frequency over Temp. and Voltage

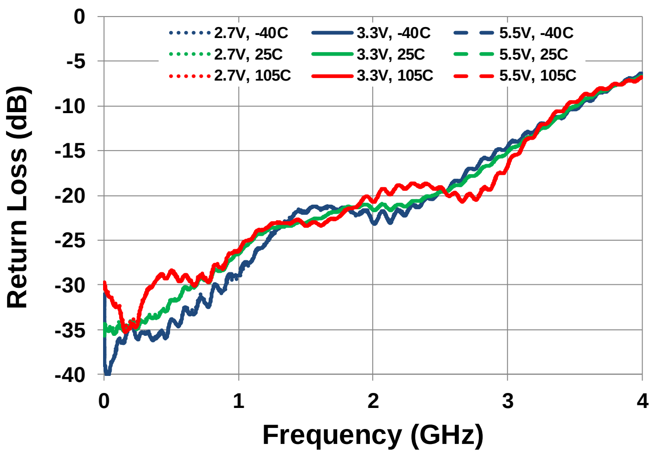


Figure 7. RF2 Port On State Return Loss vs. Frequency over Temp. and Voltage

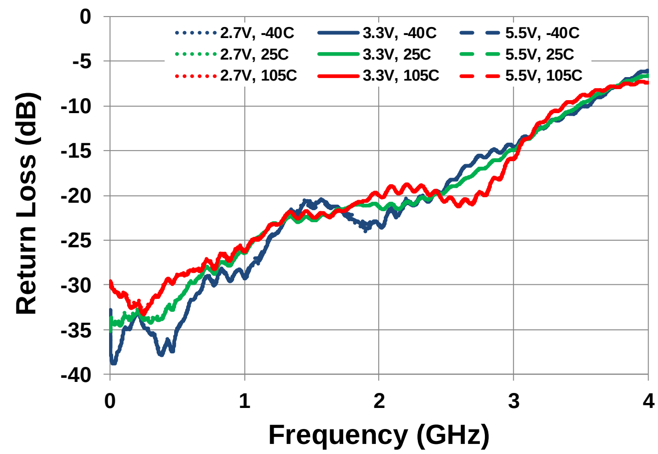
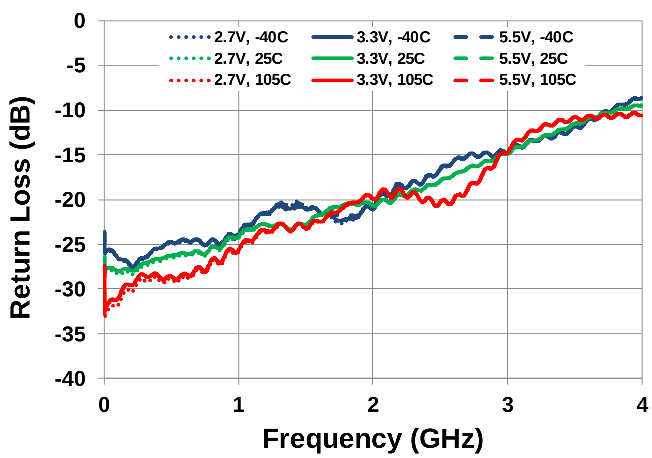


Figure 8. RF2 Port Off State Return Loss vs. Frequency over Temp. and Voltage



Typical Performance Characteristics [2]

Figure 9. Switching Time Isolation to Insertion Loss State

Figure 10. Switching Time Insertion Loss to Isolation State

Figure 11. EVKit PCB and Connector Thru Loss vs. Frequency over Temperature

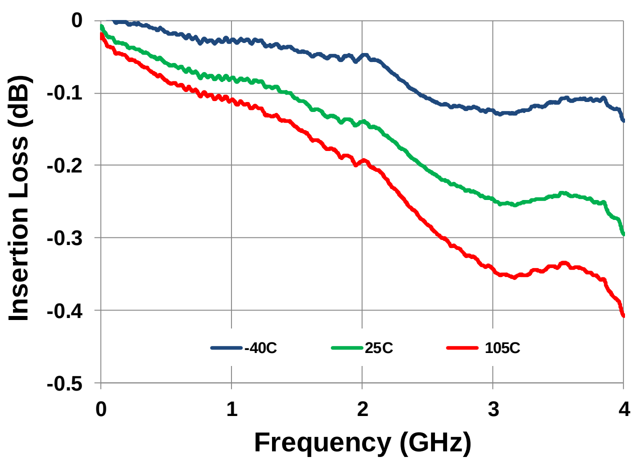
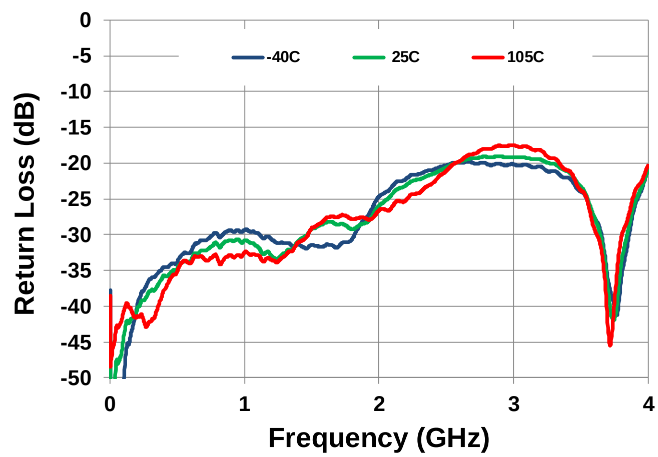


Figure 12. EVKit PCB and Connector Return Loss vs. Frequency over Temp.



Control Mode

Table 7. Switch Control Truth Table

V1	State	RFC to RF2
LOW	Isolation	RF1 port reflective, RF2 port matched to 75Ω
HIGH	Insertion Loss	RF1 and RF2 port matched to 75Ω

Application Information

Default Start-up

The V1 control pin includes no internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH.

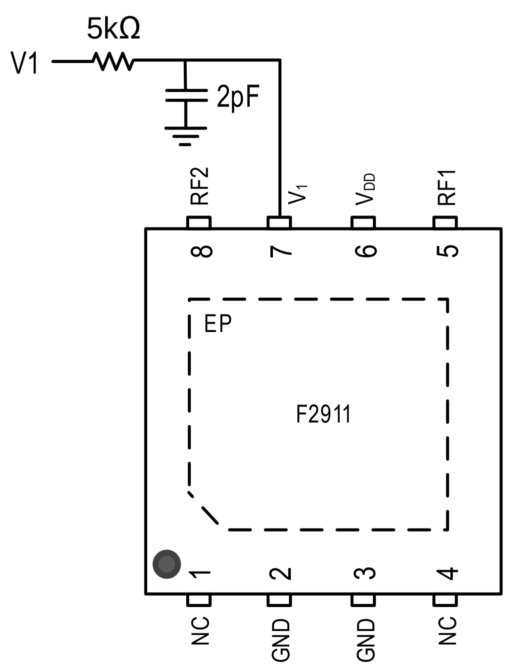
Power Supplies

A common V_{DD} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate slower than 1V/20µs. In addition, all control pins should remain at 0V (± 0.3V) while the supply voltage ramps up or while it returns to zero.

Control Pin Interface

If a clean control signal cannot be guaranteed due to overshoot, undershoot, or ringing, etc., the following circuit at the input of the control pin is recommended.

Figure 13. Control Pin Signal Integrity Improvement Circuit



Evaluation Kit Pictures

Figure 14. Top View

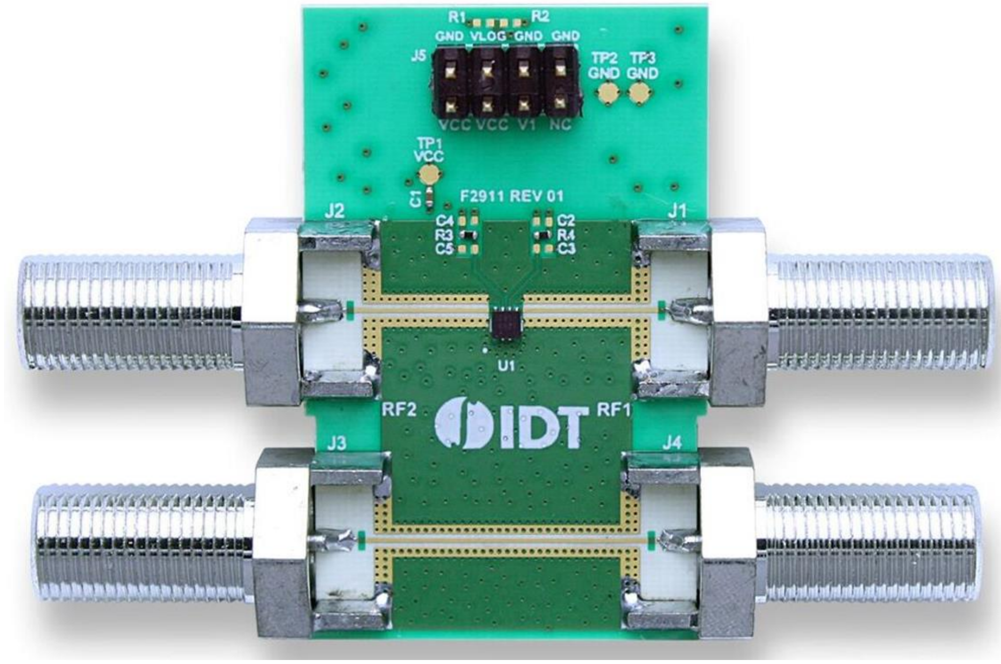
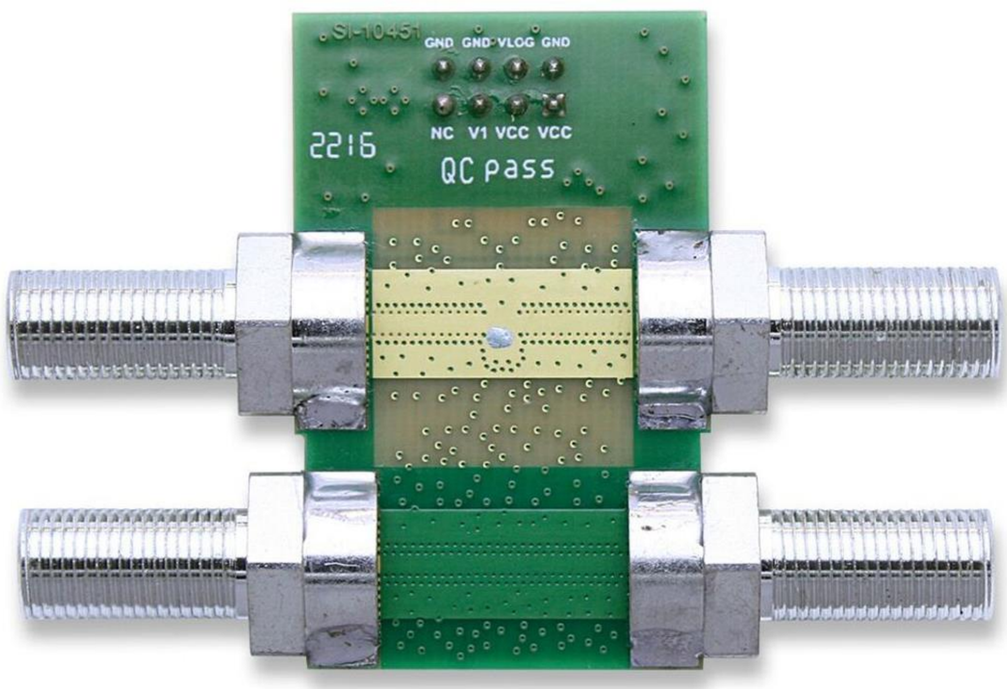


Figure 15. Bottom View



Evaluation Kit / Applications Circuit

Figure 16. Electrical Schematic

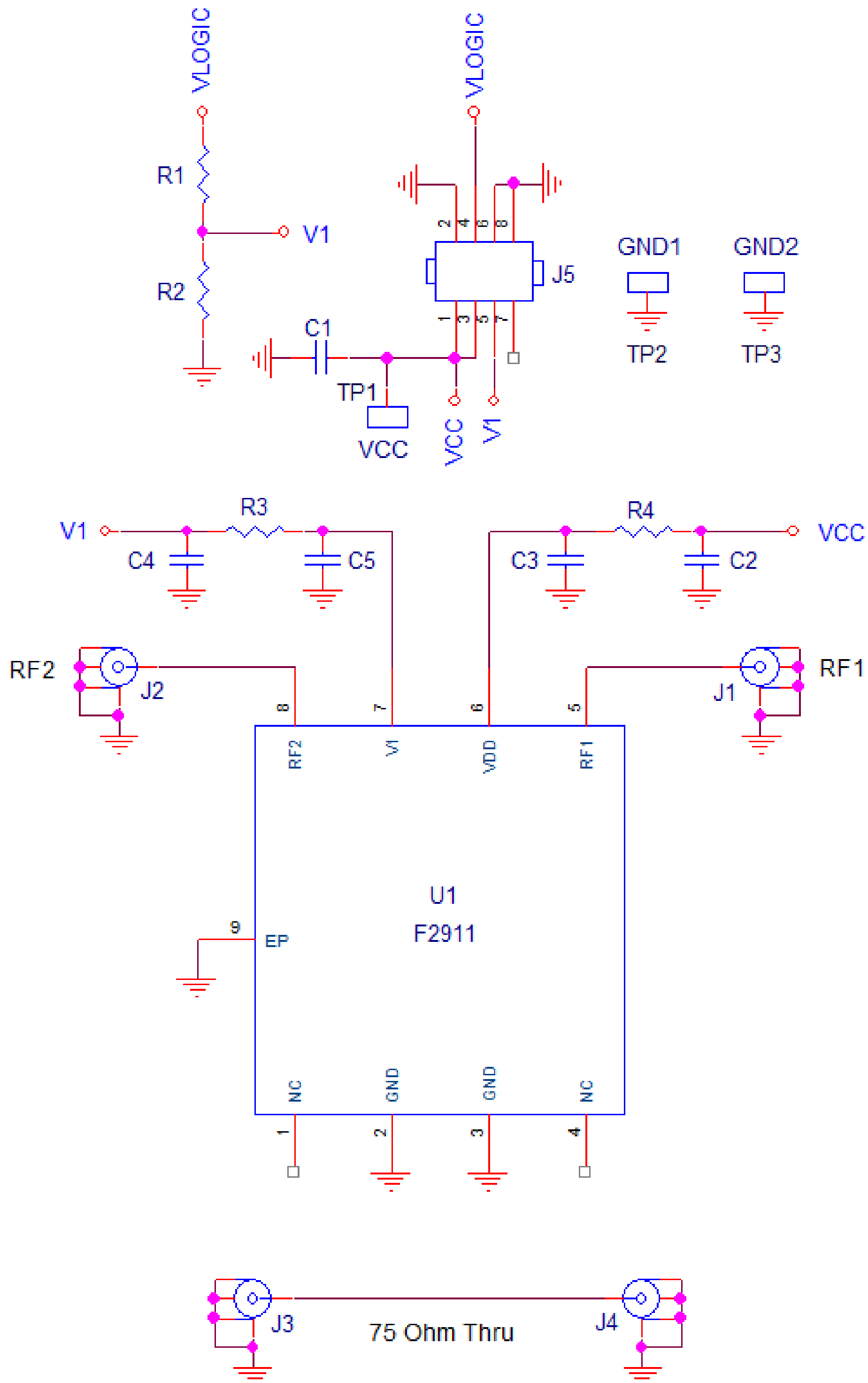


Table 8. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	0.1µF ±10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104K	Murata
C2 – C5	4	Not Installed (0402)		
R1	1	15kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1502X	Panasonic
R2	1	18kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1802X	Panasonic
R3, R4	2	0Ω, 1/10W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
J1 – J4	4	F-Type Edge Mount	531-40039	Amphenol
J5	1	CONN HEADER VERT 4x2 POS GOLD	67997-108HLF	Amphenol FCI
TP1	0	Not Installed (Red Test Point Loop)		
TP2, TP3	0	Not Installed (Black Test Point Loop)		
U1	1	SPST Switch 2mm x 2mm 8-pin DFN	F2911NBGP	IDT
	1	Printed Circuit Board	F2911EVBI	IDT

Evaluation Kit (EVKit) Operation

External Supply Setup

Set up a main power supply in the voltage range of 2.7V to 5.5V with the power supply output disabled.

Connect the disabled power supply to J5 pin 1 (VCC) and ground to J5 pin 8 (GND).

Logic Control Setup

Using the EVKIT to set the control logic:

On connector J5, connect a 2-pin shunt from pin 3 (VCC) to pin 4 (VLOGIC). This connection allows the main power supply to power the EVKit logic control network (R1 and R2). Resistors R1 and R2 form a voltage divider to set the V_{IH} level over the 2.7V to 5.5V supply range for manual logic control.

See Table 7 for Switch Control Truth Table states. With the logic control network enabled (as noted above), pin 5 can be left open to provide a logic HIGH through pull-up resistor R1. To set a logic LOW for V1, connect a 2-pin shunt on J5 from pin 5 (V1) to pin 6 (GND).

Note that when using the on-board R1/R2 voltage divider, the current draw from the power supply will be higher by approximately the main power supply voltage divided by 33kΩ.

Using external control logic:

Remove any jumpers from connector J5. Connect the disabled external logic control to V1 (pin 5) of connector J5. See Table 7 for the Switch Control Truth Table settings. Note that even with the R1/R2 divider network disabled, R2 will still be a load (18kΩ to GND) for an external control signal applied to V1.

Turn On Procedure / Operation

Setup the supplies and EVKit as noted in the External Supply Setup and Logic Control Setup sections above.

Enable the power supply.

If using the EVKIT to manually set the control logic: Set the logic setting to achieve the desired Table 7 configuration by placing a shunt between J5 pins 5 and 6 for a logic LOW or leave pins 5 and 6 open for a logic HIGH.

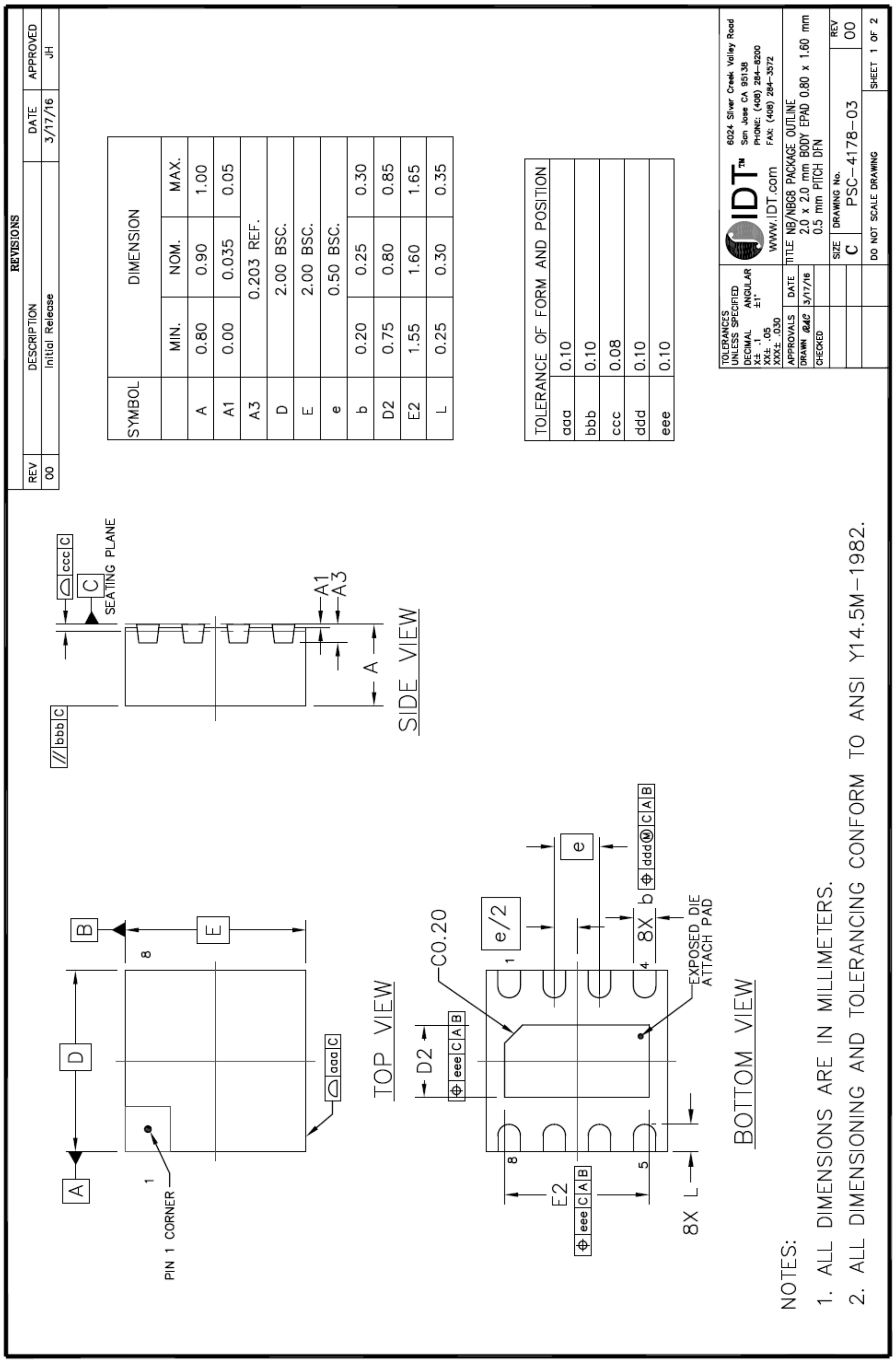
If using the external control logic setup above: Enable the logic control signal. Set the logic signal level to achieve the desired Table 7 configuration. Note that external control logic should not be applied without the main power supply being present.

Turn Off Procedure

Set any external logic control to 0V.
Disable the main power supply.

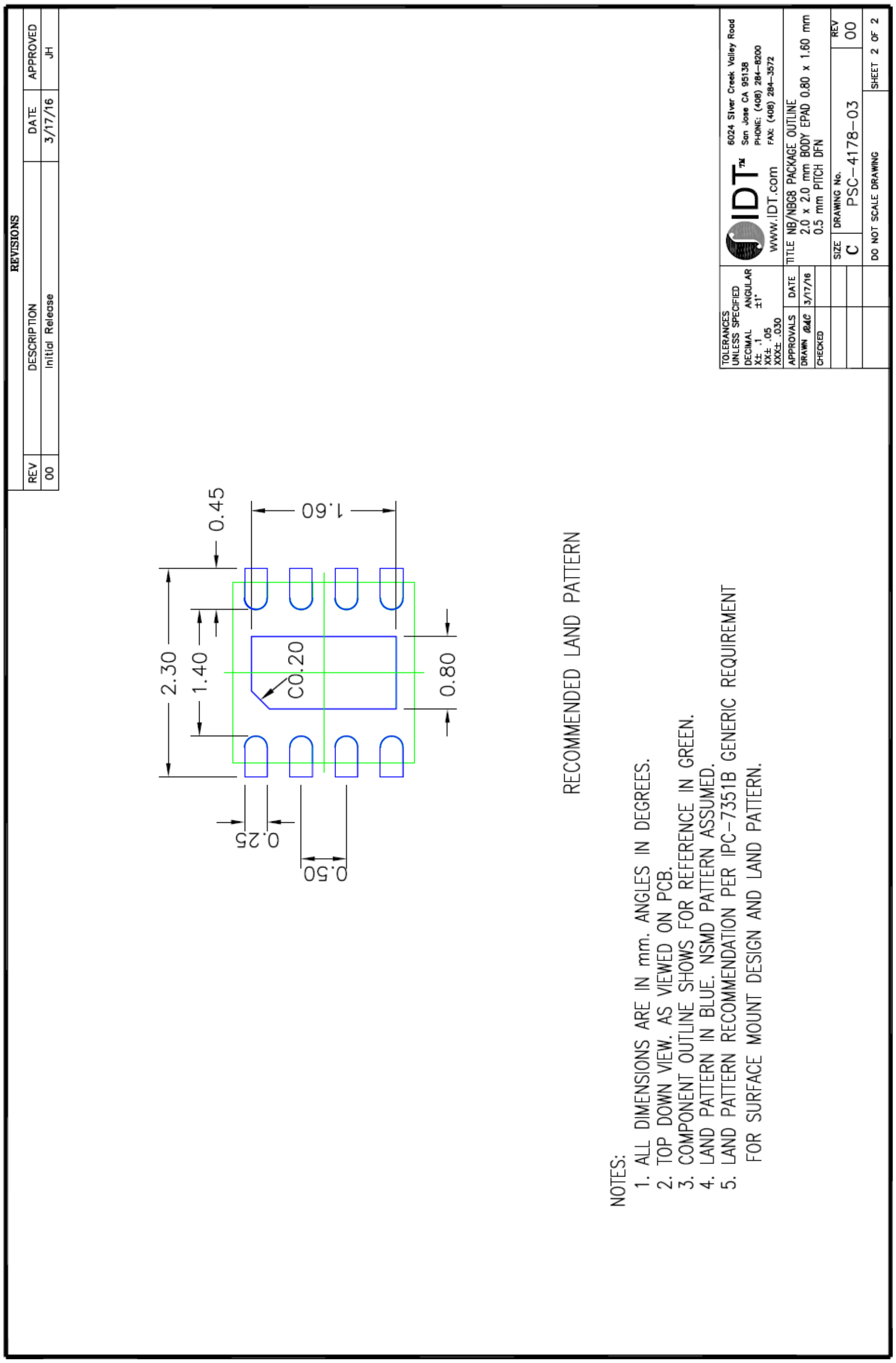
Package Drawings

Figure 17. Package Outline Drawing – NBG8P3 Package



Recommended Land Pattern

Figure 18. Recommended Land Pattern – NBG8P3 Package



Marking Diagram

Line 1 and 2 are the part number.
Line 3 - “Z” are for die version.
Line 3 - “412” is one digit for the year and week that the part was assembled.
Line 3 - “AKG” denotes the production process.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2911NBGP	2mm x 2mm x 0.9mm 8-VFQFP-N	MSL1	Cut Tape	-40°C to +105°C
F2911NBGP8	2mm x 2mm x 0.9mm 8-VFQFP-N	MSL1	Reel	-40°C to +105°C
F2911EVBI	Evaluation Board			

Revision History

Revision	Revision Date	Description of Change
Rev O	2017-Sept-21	Initial release.

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