eX Family FPGAs

Leading Edge Performance

- 240 MHz System Performance
- 350 MHz Internal Performance
- 3.9 ns Clock-to-Out (Pad-to-Pad)

Specifications

- 3,000 to 12,000 Available System Gates
- Maximum 512 Flip-Flops (Using CC Macros)
- 0.22µm CMOS Process Technology
- Up to 132 User-Programmable I/O Pins

Features

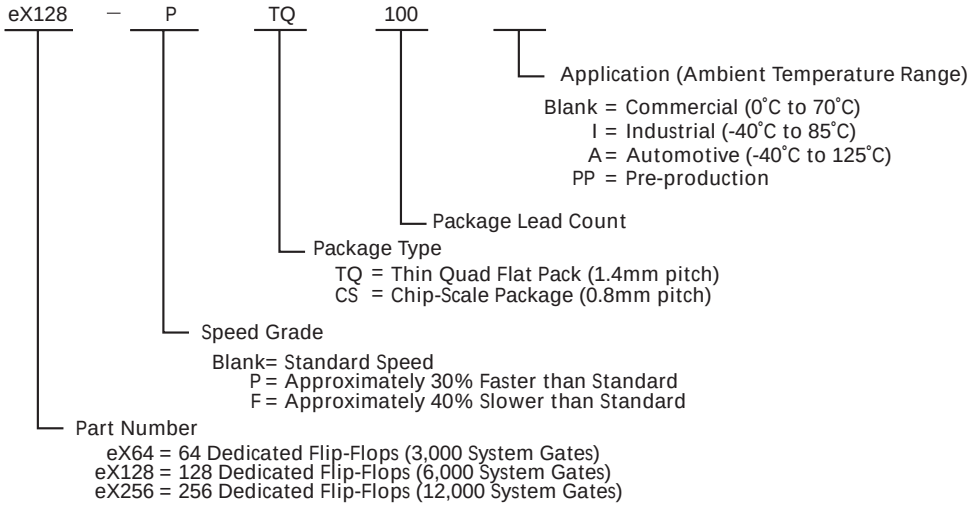
- High-Performance, Low-Power Antifuse FPGA
- LP/Sleep Mode for Additional Power Savings
- Advanced Small-Footprint Packages
- Hot-Swap Compliant I/Os
- Single-Chip Solution
- Nonvolatile
- Live on Power-Up
- No Power-Up/Down Sequence Required for Supply Voltages
- Configurable Weak-Resistor Pull-Up or Pull-Down for Tristated Outputs during Power-Up
- Individual Output Slew Rate Control
- 2.5V, 3.3V, and 5.0V Mixed-Voltage Operation with 5.0V Input Tolerance and 5.0V Drive Strength
- Software Design Support with Actel Designer and Libero™ Integrated Design Environment (IDE) Tools
- Up to 100% Resource Utilization with 100% Pin Locking
- Deterministic Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Fuselock™ Secure Programming Technology Prevents Reverse Engineering and Design Theft

Product Profile

Device	**eX64**	**eX128**	**eX256**
Capacity			
System Gates	3,000	6,000	12,000
Typical Gates	2,000	4,000	8,000
Register Cells			
Dedicated Flip-Flops	64	128	256
Maximum Flip-Flops	128	256	512
Combinatorial Cells	128	256	512
Maximum User I/Os	84	100	132
Global Clocks			
Hardwired	1	1	1
Routed	2	2	2
Speed Grades	–F, Std, –P	–F, Std, –P	–F, Std, –P
Temperature Grades*	C, I, A	C, I, A	C, I, A
Package (by pin count)			
TQFP	64, 100	64, 100	100
CSP	49, 128	49, 128	128, 180

Note: **Refer to the eX Automotive Family FPGAs datasheet for details on automotive temperature offerings.*

Ordering Information



Plastic Device Resources

	User I/Os (Including Clock Buffers)				
Device	**TQFP 64-Pin**	**TQFP 100-Pin**	**CSP 49-Pin**	**CSP 128-Pin**	**CSP 180-Pin**
eX64	41	56	36	84	—
eX128	46	70	36	100	—
eX256	—	81	—	100	132

Note: ***Package Definitions:****TQFP = Thin Quad Flat Pack, CSP = Chip Scale Package*

Temperature Grade Offerings

Device\Package	**TQFP 64-Pin**	**TQFP 100-Pin**	**CSP 49-Pin**	**CSP 128-Pin**	**CSP 180-Pin**
eX64	C, I, A	C, I, A	C, I, A	C, I, A	C, I, A
eX128	C, I, A	C, I, A	C, I, A	C, I, A	C, I, A
eX256	C, I, A	C, I, A	C, I, A	C, I, A	C, I, A

Notes: *C = Commercial*
I = Industrial
A = Automotive

Speed Grade and Temperature Grade Matrix

	–F	**Std**	**–P**
C	✓	✓	✓
I		✓	✓
A		✓	

Notes:
P = Approximately 30% faster than Standard
–F = Approximately 40% slower than Standard
Refer to the eX Automotive Family FPGAs datasheet for details on automotive temperature offerings.

Contact your local Actel representative for device availability.

Table of Contents

eX Family FPGAs

General Description

The eX family of FPGAs is a low-cost solution for low-power, high-performance designs. The inherent low power attributes of the antifuse technology, coupled with an additional low static power mode, make these devices ideal for power-sensitive applications. Fabricated with an advanced 0.22µm CMOS antifuse technology, these devices achieve high performance with no power penalty.

eX Family Architecture

Actel's eX family is implemented on a high-voltage twin-well CMOS process using 0.22µm design rules. The eX family architecture uses a “sea-of-modules” structure where the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Interconnection among these logic modules is achieved using Actel’s patented metal-to-metal programmable antifuse interconnect elements. The antifuse interconnect is made up of a combination of amorphous silicon and dielectric material with barrier metals and has an "on" state resistance of 25Ω with a capacitance of 1.0fF for low-signal impedance. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection. Actel’s eX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-1). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the eX FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to five inputs (Figure 1-2 on page 1-2). Inclusion of the DB input and its associated inverter function enables the implementation of more than 4,000 combinatorial functions in the eX architecture in a single module.

Two C-cells can be combined together to create a flip-flop to imitate an R-cell via the use of the CC macro. This is particularly useful when implementing non-timing-critical paths and when the design engineer is running out of R-cells. More information about the CC macro can be found in Actel’s *Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros* application note.

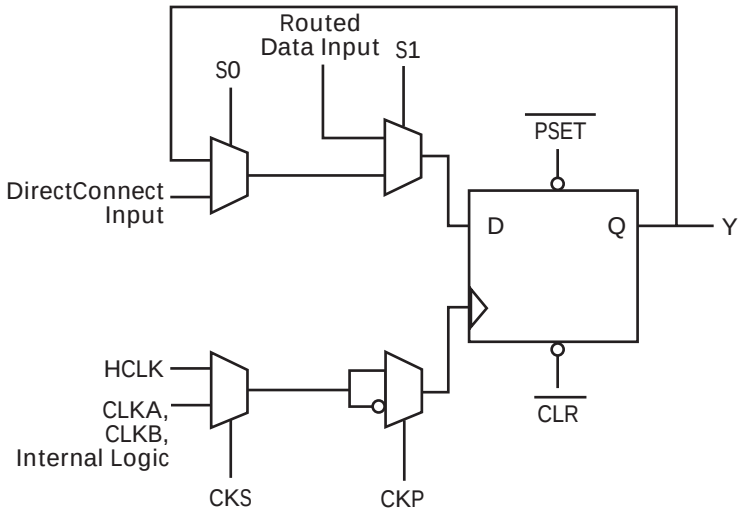


Figure 1-1 • **R-Cell**

Module Organization

C-cell and R-cell logic modules are arranged into horizontal banks called Clusters, each of which contains two C-cells and one R-cell in a C-R-C configuration.

Clusters are further organized into modules called SuperClusters for improved design efficiency and device performance, as shown in Figure 1-3. Each SuperCluster is a two-wide grouping of Clusters.

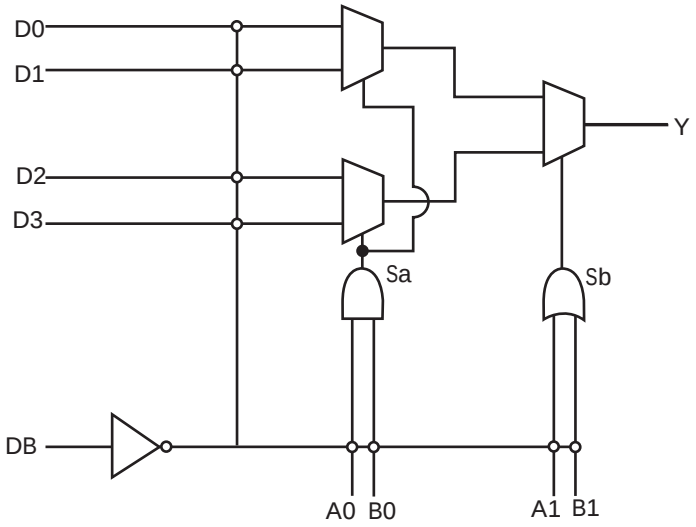


Figure 1-2 • **C-Cell**

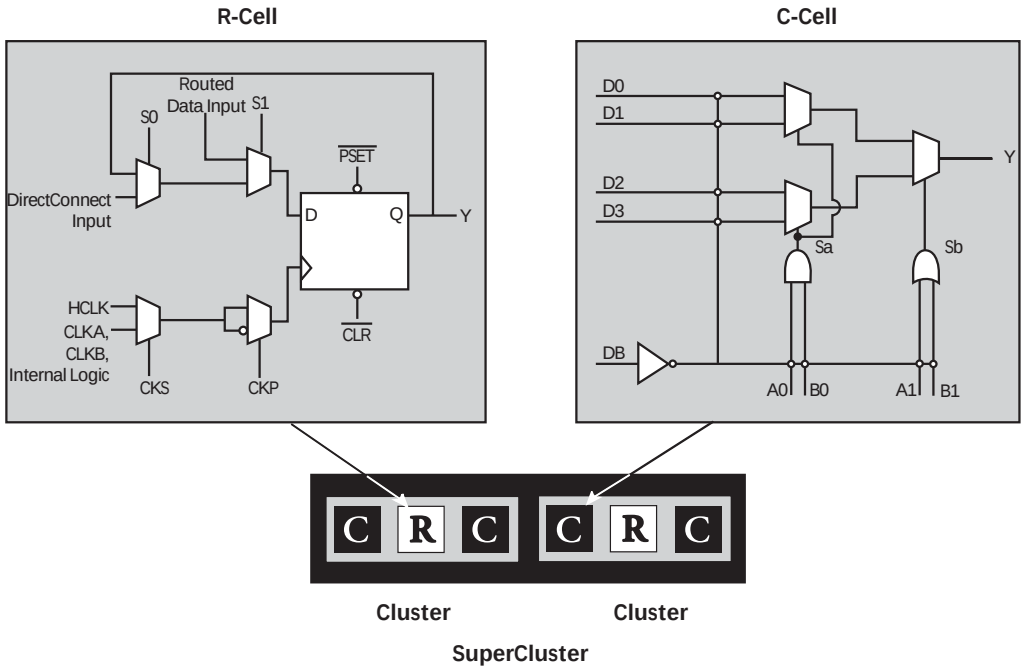


Figure 1-3 • **Cluster Organization**

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns (–P speed grade).

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.3 ns (–P speed grade).

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the fully automatic place-and-route software to minimize signal propagation delays.

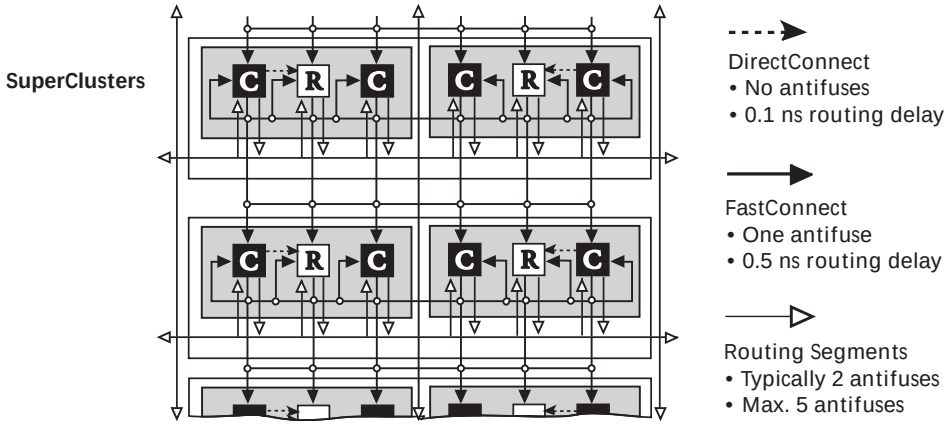


Figure 1-4 • **DirectConnect and FastConnect for SuperClusters**

Clock Resources

eX's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-Cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 3.9 ns clock-to-out (pad-to-pad) performance of the eX devices. The hard-wired clock is tuned to provide a clock skew of less than 0.1 ns worst case. If not used, the HCLK pin must be tied LOW or HIGH and must not be left floating. Figure 1-5 describes the clock circuit used for the constant load HCLK.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board. (See the "TRST, I/O Boundary Scan Reset Pin" on page 1-26).

The remaining two clocks (CLKA, CLKB) are global routed clock networks that can be sourced from external pins or from internal logic signals (via the CLKINT routed clock buffer) within the eX device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals, the external clock pin cannot be used for any other input and must be tied LOW or HIGH and must not float. Figure 1-6 describes the CLKA and CLKB circuit used in eX devices.

Table 1-1 describes the possible connections of the routed clock networks, CLKA and CLKB.

Unused clock pins must not be left floating and must be tied to HIGH or LOW.

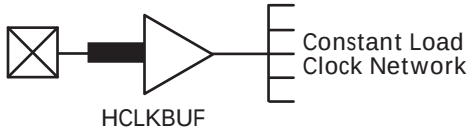


Figure 1-5 • **eX HCLK Clock Pad**

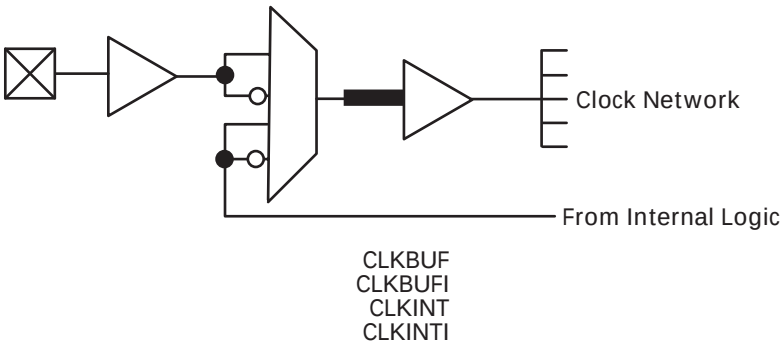


Figure 1-6 • **eX Routed Clock Buffer**

Table 1-1 • **Connections of Routed Clock Networks, CLKA and CLKB**

Module	Pins
C-Cell	A0, A1, B0 and B1
R-Cell	CLKA, CLKB, S0, S1, PSET, and CLR
I/O-Cell	EN

Other Architectural Features

Performance

The combination of architectural features described above enables eX devices to operate with internal clock frequencies exceeding 350 MHz for very fast execution of complex logic functions. The eX family is an optimal platform upon which the functionality previously contained in CPLDs can be integrated. eX devices meet the performance goals of gate arrays, and at the same time, present significant improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located such that they cannot be accessed or bypassed without destroying the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure.

FuseLock

Figure 1-7 • **Fuselock**

For more information, refer to *Actel's Implementation of Security in Actel Antifuse FPGAs* application note.

I/O Modules

Each I/O on an eX device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.9 ns. I/O cells in eX devices do not contain embedded latches or flip-flops and can be inferred directly from HDL code. The device can easily interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

All unused I/Os are configured as tristate outputs by Actel's Designer software, for maximum flexibility when designing new boards or migrating existing designs. Each I/O module has an available pull-up or pull-down resistor of approximately 50kΩ that can configure the I/O in a known state during power-up. Just shortly before V_{CCA} reaches 2.5V, the resistors are disabled and the I/Os will be controlled by user logic.

Table 1-2 describes the I/O features of eX devices. For more information on I/Os, refer to *Actel eX, SX-A, and RT54SX-S I/Os* application note.

Table 1-2 • **I/O Features**

Function	Description
Input Buffer Threshold Selection	• 5.0V TTL • 3.3V LVTTL • 2.5V LVCMOS2
Nominal Output Drive	• 5.0V TTL/CMOS • 3.3V LVTTL • 2.5V LVCMOS 2
Output Buffer	"Hot-Swap" Capability • I/O on an unpowered device does not sink current • Can be used for "cold sparing" Selectable on an individual I/O basis Individually selectable low-slew option
Power-Up	Individually selectable pull ups and pull downs during power-up (default is to power up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

The eX family supports mixed-voltage operation and is designed to tolerate 5.0V inputs in each case.

A detailed description of the I/O pins in eX devices can be found in "Pin Description" on page 1-26.

Hot Swapping

eX I/Os are configured to be hot-swappable. During power-up/down (or partial up/down), all I/Os are tristated, provided V_{CCA} ramps up within a diode drop of V_{CCI}. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and they do not require a specific power-up or power-down sequence in order to avoid damage to the eX devices. In addition, all outputs can be programmed to have a weak resistor pull-up or pull-down for output tristate at power-up. After the eX device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Please see the application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*, which also applies to the eX devices, for more information on hot swapping.

Power Requirements

Power consumption is extremely low for the eX family due to the low capacitance of the antifuse interconnects. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power FPGA architecture available today.

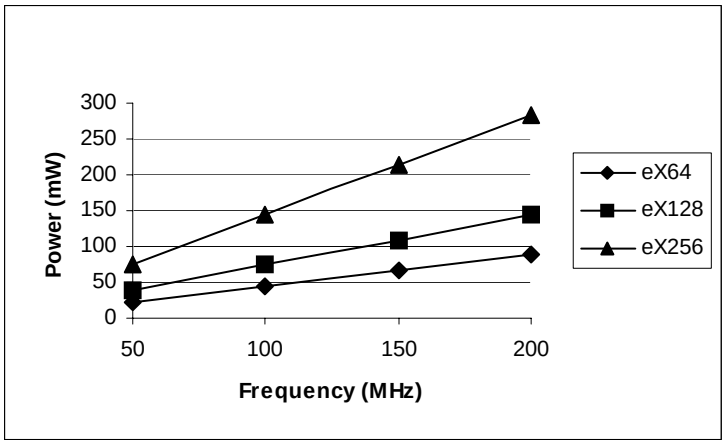
Low Power Mode

The eX family has been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated when the device enters this mode. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when returning to normal operating mode. I/Os can be driven during LP mode. For details, refer to the *Design For Low Power in Actel Antifuse FPGAs* application note under the section Using the LP Mode Pin on eX Devices. Clock pins should be driven either HIGH or LOW and should not float; otherwise, they will draw current and burn power. The device must be re-initialized when exiting LP mode. To exit the LP mode, the LP pin must be driven LOW for over 200µs to allow for the charge pumps to power-up and device initialization can begin. Table 1-3 illustrates the standby current of eX devices in LP mode.

Table 1-3 • **Standby Power of eX Devices in LP Mode**
Typical Conditions, V_{CCA}, V_{CCI} = 2.5V, T_J = 25°C

Product	Low Power Standby Current	Units
eX64	100	µA
eX128	111	µA
eX256	134	µA

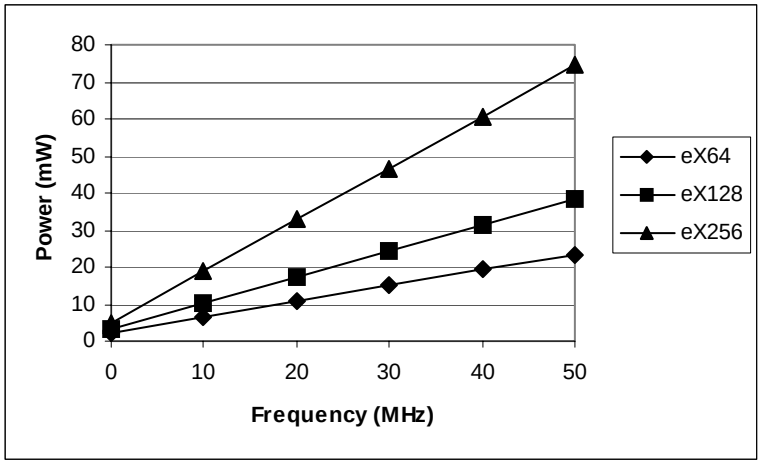
Figure 1-8 to Figure 1-11 on page 1-8 show some sample power characteristics of eX devices.



Notes:

1. *Device filled with 16-bit counters.*
2. *V_{CCA}, V_{CCI} = 2.7V, device tested at room temperature.*

Figure 1-8 • **eX Dynamic Power Consumption – High Frequency**



Notes:

1. *Device filled with 16-bit counters.*
2. *V_{CCA}, V_{CCI} = 2.7V, device tested at room temperature.*

Figure 1-9 • **eX Dynamic Power Consumption – Low Frequency**

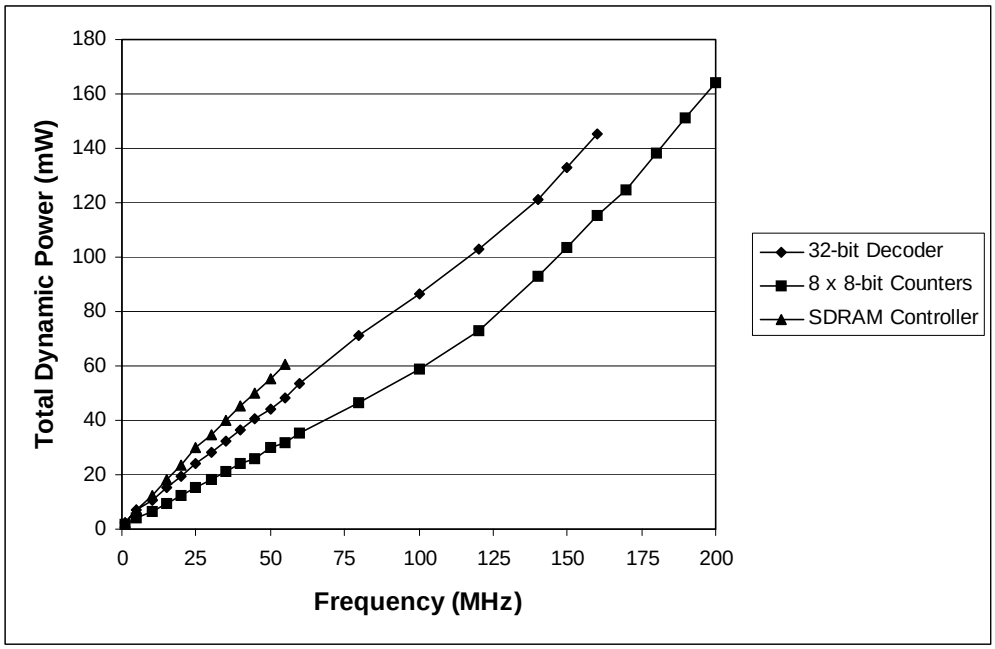


Figure 1-10 • **Total Dynamic Power (mW)**

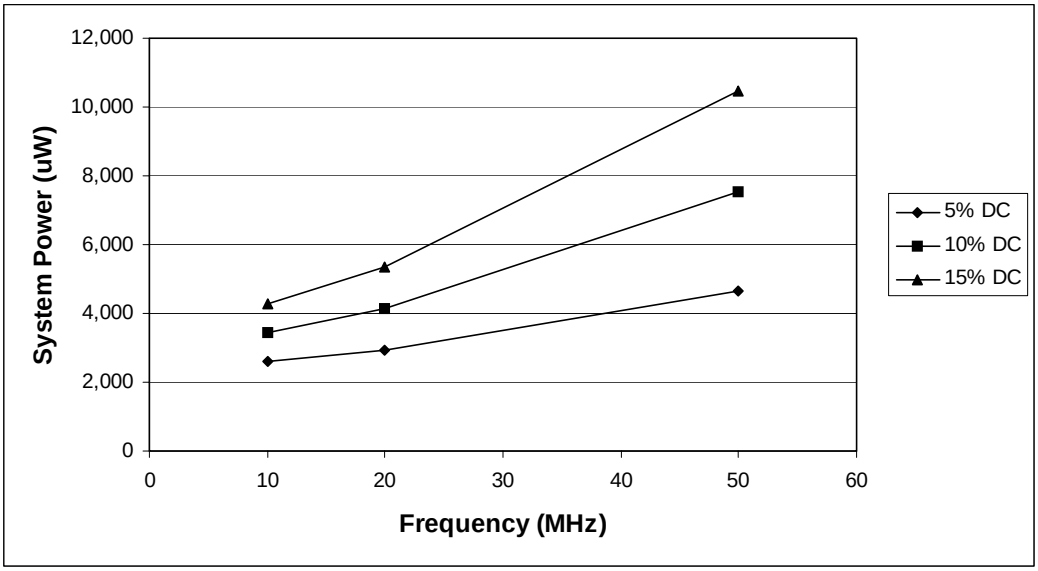


Figure 1-11 • **System Power at 5%, 10%, and 15% Duty Cycle**

Boundary Scan Testing (BST)

All eX devices are IEEE 1149.1 compliant. eX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins (TMS, TDI, TCK, TDO and TRST). The functionality of each pin is defined by two available modes: Dedicated and Flexible, and is described in Table 1-4. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode (default mode), TMS should be set HIGH through a pull-up resistor of 10kΩ. TMS can be pulled LOW to initiate the test sequence.

Table 1-4 • **Boundary Scan Pin Functionality**

Dedicated Test Mode	Flexible Mode
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS and TDI	Use a pull-up resistor of 10kΩ on TMS

Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software by checking the "Reserve JTAG" box in "Device Selection Wizard" (Figure 1-12).

Figure 1-12 • **Device Selection Wizard**

Flexible Mode

In Flexible Mode, TDI, TCK and TDO may be used as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are disabled in flexible JTAG mode, and an external 10kΩ pull-resistor to V_{CCI} is required on the TMS pin.

To select the Flexible mode, users need to uncheck the "Reserve JTAG" box in "Device Selection Wizard" in Actel's Designer software. The functionality of TDI, TCK, and TDO pins is controlled by the BST TAP controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when the TMS pin is LOW at the first rising edge of TCK. The TDI, TCK, and TDO pins return to user I/Os when TMS is held HIGH for at least five TCK cycles.

Table 1-5 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-5 • **Boundary-Scan Pin Configurations and Functions**

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the "Reserve JTAG Test Reset" option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. It is recommended to connect this pin to GND in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or be driven HIGH.

When the "Reserve JTAG Test Reset" option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

JTAG Instructions

Table 1-6 lists the supported instructions with the corresponding IR codes for eX devices.

Table 1-6 • **JTAG Instruction Code**

Instructions (IR4: IR0)	Binary Code
EXTEST	00000
SAMPLE / PRELOAD	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
BYPASS	11111
Reserved	All others

Table 1-7 lists the codes returned after executing the IDCODE instruction for eX devices. Note that bit 0 is always "1." Bits 11-1 are always "02F", which is Actel's manufacturer code.

Table 1-7 • **IDCODE for eX Devices**

Device	Revision	Bits 31-28	Bits 27-12
eX64	0	8	40B2, 42B2
eX128	0	9	40B0, 42B0
eX256	0	9	40B5, 42B5
eX64	1	A	40B2, 42B2
eX128	1	B	40B0, 42B0
eX256	1	B	40B5, 42B5

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the *Programming Actel Devices* application note and the *Silicon Sculptor II User's Guide*.

Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the "Reserve Probe Pin" box as shown in Figure 1-12 on page 1-9, the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This "reserve" option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the "Reserve Probe Pin" option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. Table 1-8 on page 1-11 summarizes the possible device configurations for probing once the device leaves the "Test-Logic-Reset" JTAG state.

Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Actel's Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer

II's non-invasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Since these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry. It is recommended to use a series 70Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

Table 1-8 • **Device Configuration Options for Probe Capability (TRST pin reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	LOW	No	User I/O[3]	Probing Unavailable
Flexible	LOW	No	User I/O[3]	User I/O[3]
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *If TRST pin is not reserved, the device behaves according to TRST=HIGH in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by Actel's Designer software.*

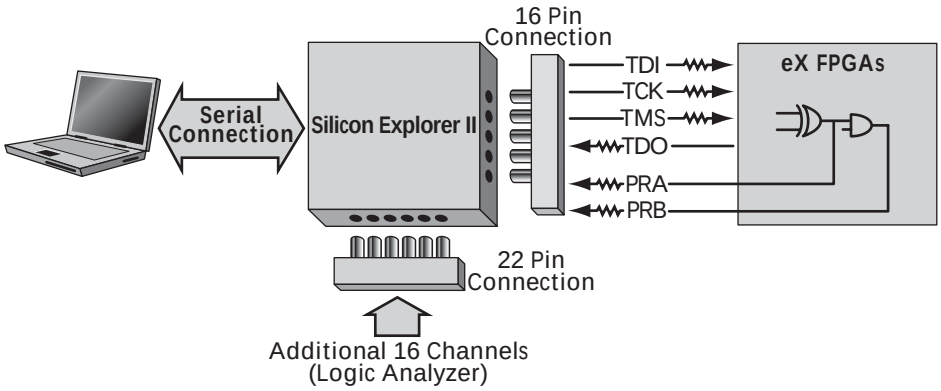


Figure 1-13 • **Silicon Explorer II Probe Setup**

Development Tool Support

The eX family of FPGAs is fully supported by both Actel's Libero™ Integrated Design Environment and Designer FPGA Development software. Actel Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw for Actel from Mentor Graphics, ModelSim™ HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* (located on Actel's website) diagram for more information.

Actel's Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Related Documents

Datasheet

eX Automotive Family FPGAs

http://www.actel.com/documents/eXAutoDS.pdf

Application Notes

Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros

http://www.actel.com/documents/MaxLogicUtil.pdf

Actel's Implementation of Security in Actel Antifuse FPGAs

http://www.actel.com/documents/AntifuseSecurityAN.pdf

Actel eX, SX-A, and RT54SX-S I/Os

http://www.actel.com/documents/antifuseIOan.pdf

Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications

http://www.actel.com/documents/HotSwapColdSparing.pdf

Design For Low Power in Actel Antifuse FPGAs

http://www.actel.com/documents/lowpower.pdf

Programming Actel Devices

http://www.actel.com/documents/ProgrammingGuide.pdf

User Guides

Silicon Sculptor II User's Guide

http://www.actel.com/techdocs/manuals/default.asp#programmers

Miscellaneous

Libero IDE flow

http://www.actel.com/products/tools/libero/flow.html

2.5V/3.3V/5.0V Operating Conditions

Table 1-9 • **Absolute Maximum Ratings***

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage for I/Os	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage for Array	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to +5.75	V
V_O	Output Voltage	–0.5 to +V_{CCI}	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-10 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Units
Temperature Range*	0 to +70	–40 to +85	°C
2.5V Power Supply Range (V_{CCA}, V_{CCI})	2.3-2.7	2.3-2.7	V
3.3V Power Supply Range (V_{CCI})	3.0-3.6	3.0-3.6	V
5.0V Power Supply Range (V_{CCI})	4.75-5.25	4.75-5.25	V

Note: **Ambient temperature (T_A).*

Table 1-11 • **Typical eX Standby Current at 25°C**

Product	V_{CCA}= 2.5V V_{CCI} = 2.5V	V_{CCA} = 2.5V V_{CCI} = 3.3V	V_{CCA} = 2.5V V_{CCI} = 5.0V
eX64	397µA	497µA	700µA
eX128	696µA	795µA	1,000µA
eX256	698µA	796µA	2,000µA

2.5V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Units
V_{OH}	V_{CCI} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = -100µA)	2.1		2.1		V
	V_{CCI} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = -1 mA)	2.0		2.0		V
	V_{CCI} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = -2 mA)	1.7		1.7		V
V_{OL}	V_{CCI} = MIN, V_I = V_{IH} or V_{IL}	(I_{OL}= 100µA)		0.2		0.2	V
	V_{CCI} = MIN, V_I = V_{IH} or V_{IL}	(I_{OL}= 1mA)		0.4		0.4	V
	V_{CCI} = MIN,V_I = V_{IH} or V_{IL}	(I_{OL}= 2 mA)		0.7		0.7	V
V_{IL}	Input Low Voltage, $V_{OUT} \le V_{OL(max)}$		–0.3	0.7	-0.3	0.7	V
V_{IH}	Input High Voltage, $V_{OUT} \ge V_{OH(min)}$		1.7	V_{CCI} + 0.3	1.7	V_{CCI} + 0.3	V
I_{IL}/ I_{IH}	Input Leakage Current, V_{IN} = V_{CCI} or GND		–10	10	–10	10	µA
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–10	10	–10	10	µA
t_R, t_F[1,2]	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}[3,4]	Standby Current			1.0		3.0	mA
IV Curve	Can be derived from the IBIS model at www.actel.com/custsup/models/ibis.html.						

Notes:

1. *t_R is the transition time from 0.7 V to 1.7V.*
2. *t_F is the transition time from 1.7V to 0.7V.*
3. *I_{CC} max Commercial –F = 5.0mA*
4. *I_{CC} = I_{CCI} + I_{CCA}*

3.3V LVTTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V_{OH}	V_{CCI} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = –8mA)	2.4		2.4		V
V_{OL}	V_{CCI} = MIN, V_I = V_{IH} or V_{IL}	(I_{OL}= 12mA)		0.4		0.4	V
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0	V_{CCI} +0.5	2.0	V_{CCI} +0.5	V
I_{IL}/ I_{IH}	Input Leakage Current, V_{IN} = V_{CCI} or GND		–10	10	–10	10	µA
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–10	10	–10	10	µA
t_R, t_F[1,2]	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}[3,4]	Standby Current			1.5		10	mA
IV Curve	Can be derived from the IBIS model at www.actel.com/custsup/models/ibis.html.						

Notes:

1. *t_R is the transition time from 0.8 V to 2.0V.*
2. *t_F is the transition time from 2.0V to 0.8V.*
3. *I_{CC} max Commercial –F=5.0mA*
4. *I_{CC} = I_{CCI} + I_{CCA}*

5.0V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V_{OH}	V_{CCI} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = –8mA)	2.4		2.4		V
V_{OL}	V_{CCI} = MIN, V_I = V_{IH} or V_{IL}	(I_{OL}= 12mA)		0.4		0.4	V
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0	V_{CCI} +0.5	2.0	V_{CCI} +0.5	V
I_{IL}/ I_{IH}	Input Leakage Current, V_{IN} = V_{CCI} or GND		–10	10	–10	10	µA
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–10	10	–10	10	µA
t_R, t_F[1,2]	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}[3,4]	Standby Current			15		20	mA
IV Curve	Can be derived from the IBIS model at www.actel.com/custsup/models/ibis.html						

Note:

1. *t_R is the transition time from 0.8 V to 2.0V.*
2. *t_F is the transition time from 2.0V to 0.8V.*
3. *I_{CC} max Commercial –F=20mA*
4. *I_{CC} = I_{CCI} + I_{CCA}*

Power Dissipation

Power consumption for eX devices can be divided into two components: static and dynamic.

Static Power Component

The power due to standby current is typically a small component of the overall power. Typical standby current for eX devices is listed in the Table 1-11 on page 1-13. For example, the typical static power for eX128 at 3.3V V_{CCI} is:

$I_{CC} * V_{CCA}$ = 795µA x 2.5V = 1.99mW

Dynamic Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. This component is frequency-dependent and a function of the logic and the external I/O. Dynamic power dissipation results from charging internal chip capacitance due to PC board traces and load device inputs. An additional component of the dynamic power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent dynamic power dissipation.

Dynamic power dissipation = CEQ * V_{CCA}^2 x F

where:

CEQ = Equivalent capacitance

F = switching frequency

Equivalent capacitance is calculated by measuring I_{CCA} at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

CEQ Values for eX Devices

Combinatorial modules (Ceqcm)	1.70pF
Sequential modules (Ceqsm)	1.70pF
Input buffers (Ceqi)	1.30pF
Output buffers (Ceqo)	7.40pF
Routed array clocks (Ceqcr)	1.05pF

The variable and fixed capacitance of other device components must also be taken into account when estimating the dynamic power dissipation.

Table 1-12 shows the capacitance of the clock components of eX devices.

Table 1-12 • **Capacitance of Clock Components of eX Devices**

	eX64	eX128	eX256
Dedicated array clock – variable (Ceqhv)	0.85pF	0.85pF	0.85pF
Dedicated array clock – fixed (Ceqhf)	18.00pF	20.00pF	25.00pF
Routed array clock A (r1)	23.00pF	28.00pF	35.00pF
Routed array clock B (r2)	23.00pF	28.00pF	35.00pF

The estimation of the dynamic power dissipation is a piece-wise linear summation of the power dissipation of each component.

Dynamic power dissipation
$= V_{CCA}^2 * [(m_c * C_{eqcm} * fm_C)_{Comb\ Modules} + (m_s * C_{eqsm} * fm_S)_{Seq\ Modules} + (n * C_{eqi} * fn)_{Input\ Buffers} + (0.5 * (q1 * C_{eqcr} * fq1) + (r1 * fq1))_{RCLKA} + (0.5 * (q2 * C_{eqcr} * fq2) + (r2 * fq2))_{RCLKB} + (0.5 * (s1 * C_{eqhv} * fs1)+(C_{eqhf} * fs1))_{HCLK}] + V_{CCI}^2 * [(p * (C_{eqo} + C_L) * fp)_{Output\ Buffers}]$

where:

m_c = Number of combinatorial cells switching at frequency fm, typically 20% of C-cells

m_s = Number of sequential cells switching at frequency fm, typically 20% of R-cells

n = Number of input buffers switching at frequency fn, typically number of inputs / 4

p = Number of output buffers switching at frequency fp, typically number of outputs / 4

q1 = Number of R-cells driven by routed array clock A

q2 = Number of R-cells driven by routed array clock B

r1 = Fixed capacitance due to routed array clock A

r2 = Fixed capacitance due to routed array clock B

s1 = Number of R-cells driven by dedicated array clock

C_{eqcm} = Equivalent capacitance of combinatorial modules

C_{eqsm} = Equivalent capacitance of sequential modules
C_{eqi} = Equivalent capacitance of input buffers
C_{eqcr} = Equivalent capacitance of routed array clocks
C_{eqhv} = Variable capacitance of dedicated array clock
C_{eqhf} = Fixed capacitance of dedicated array clock
C_{eqo} = Equivalent capacitance of output buffers
C_L = Average output loading capacitance, typically 10pF
fm_c = Average C-cell switching frequency, typically F/10
fm_s = Average R-cell switching frequency, typically F/10
fn = Average input buffer switching frequency, typically F/5
fp = Average output buffer switching frequency, typically F/5
fq1 = Frequency of routed clock A
fq2 = Frequency of routed clock B
fs1 = Frequency of dedicated array clock

The eX, SX-A and RTSX-S Power Calculator can be used to estimate the total power dissipation (static and dynamic) of eX devices and can be found at http://www.actel.com/products/rescenter/power/calculators.asp.

Thermal Characteristics

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. EQ 1-1, shown below, can be used to calculate junction temperature.

EQ 1-1

$$\text{Junction Temperature} = \Delta T + T_a \quad (1)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient = $\theta_{ja} * P$

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section below.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates. θ_{jc} is provided for reference.

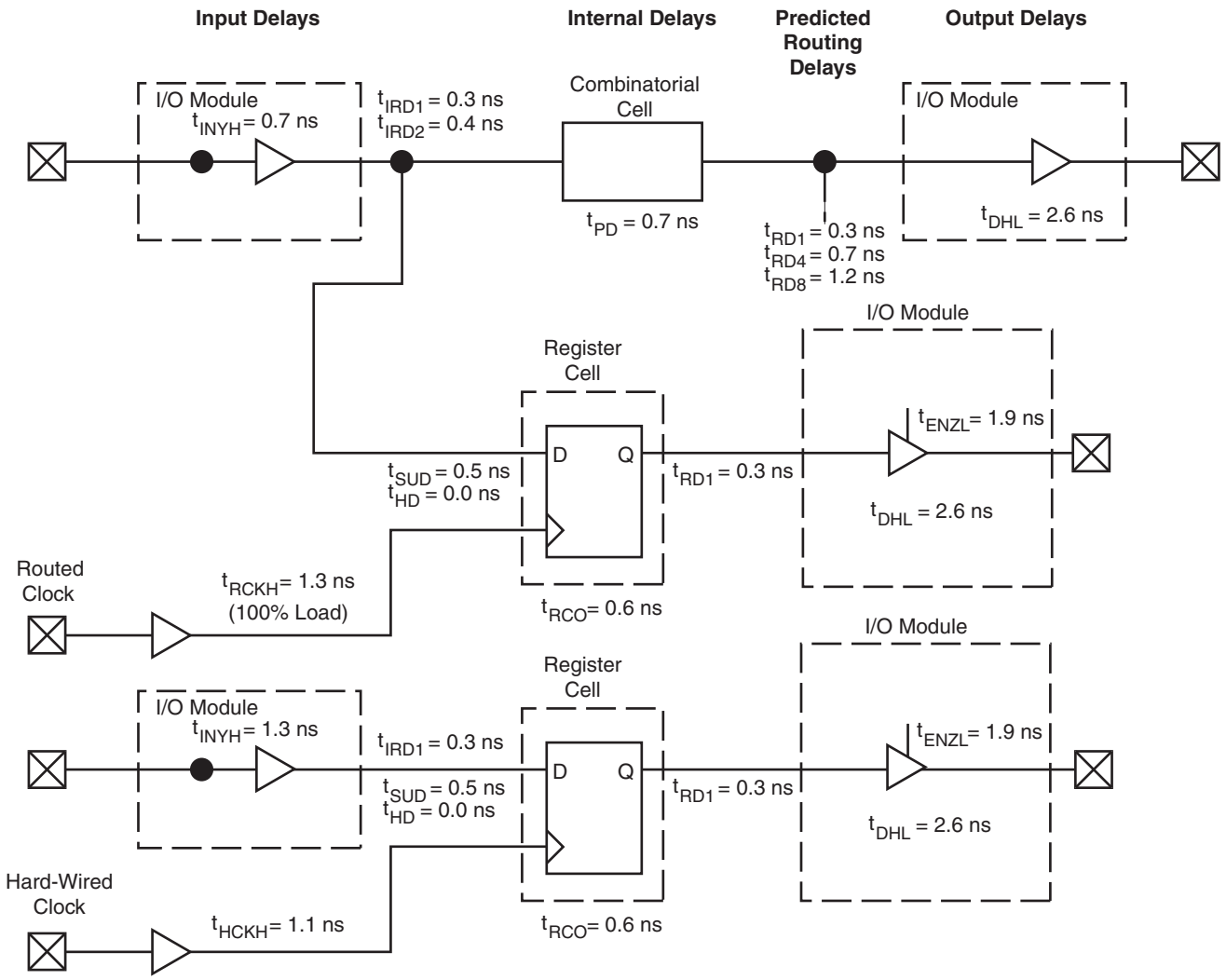
The maximum junction temperature is 150°C.

The maximum power dissipation allowed for eX devices is a function of θ_{ja}. A sample calculation of the absolute maximum power dissipation allowed for a TQFP 100-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{33.5\text{°C/W}} = 2.39\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0 m/s 200 ft/min	θ_{ja} 2.5 m/s 500 ft/min	Units
Thin Quad Flat Pack (TQFP)	64	12.0	42.4	36.3	34.0	°C/W
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W
Chip Scale Package (CSP)	49		72.2	59.5	54.1	°C/W
Chip Scale Package (CSP)	128		54.1	44.6	40.6	°C/W
Chip Scale Package (CSP)	180		57.8	47.6	43.3	°C/W

eX Timing Model



Note: *Values shown for eX128–P, worst-case commercial conditions (5.0V, 35pF Pad Load).*

Figure 1-14 • **eX Timing Model**

Hardwired Clock

External Setup = $t_{INYH} + t_{IRD1} + t_{SUD} – t_{HCKH}$

= 0.7 + 0.3 + 0.5 – 1.1 = 0.4 ns

Clock-to-Out (Pad-to-Pad), typical

= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.1 + 0.6 + 0.3 + 2.6 = 4.6 ns

Routed Clock

External Setup = $t_{INYH} + t_{IRD2} + t_{SUD} – t_{RCKH}$

= 0.7 + 0.4 + 0.5 – 1.3= 0.3 ns

Clock-to-Out (Pad-to-Pad), typical

= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.3+ 0.6 + 0.3 + 2.6 = 4.8 ns

Output Buffer Delays

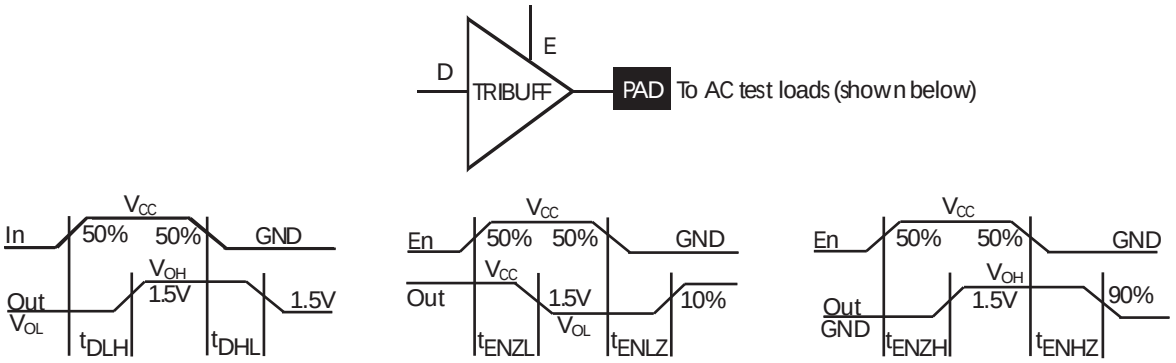


Table 1-13 • **Output Buffer Delays**

AC Test Loads

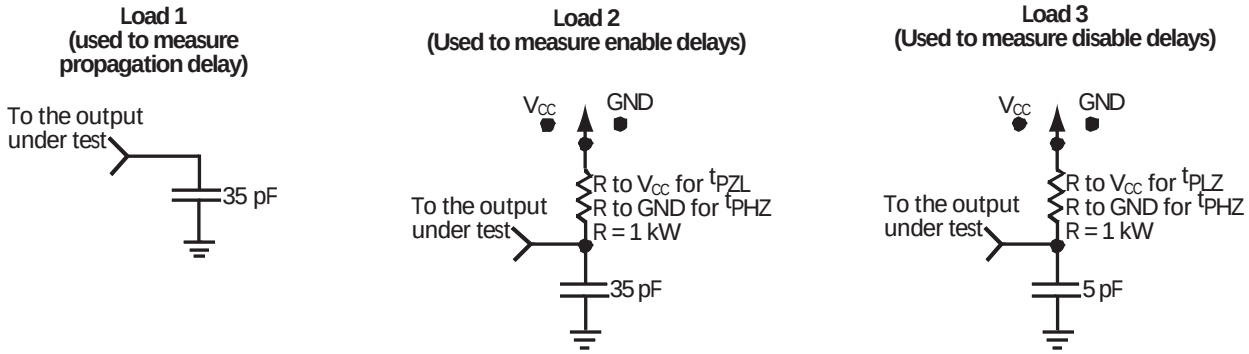


Figure 1-15 • **AC Test Loads**

Input Buffer Delays

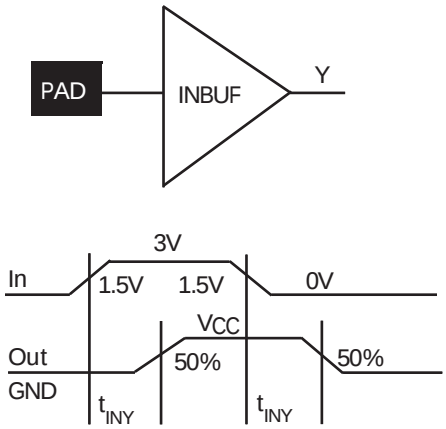


Table 1-14 • **Input Buffer Delays**

C-Cell Delays

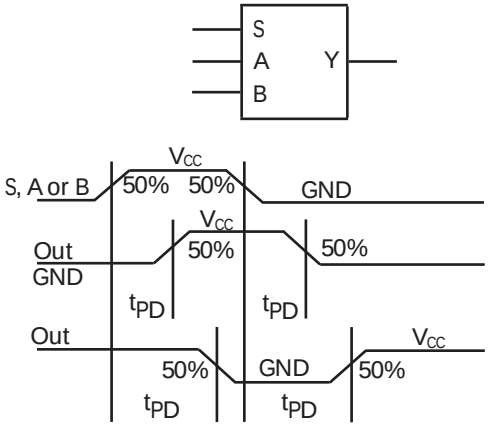


Table 1-15 • **C-Cell Delays**

Cell Timing Characteristics

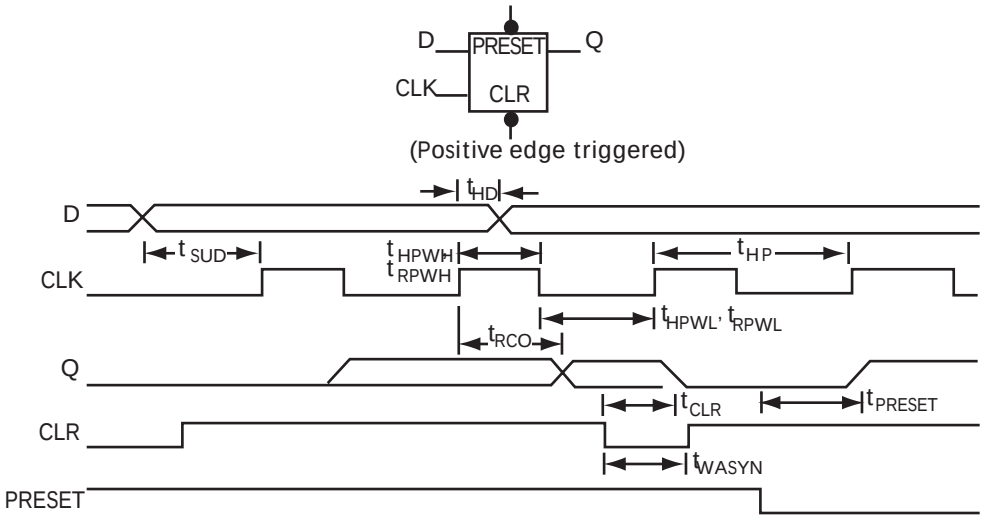


Figure 1-16 • **Flip-Flops**

Timing Characteristics

Timing characteristics for eX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all eX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to six percent of the nets in a design may be designated as critical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, no more than six percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

eX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 1-16 • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.3V)**

V_{CCA}	Junction Temperature (T_J)						
	–55	**–40**	**0**	**25**	**70**	**85**	**125**
2.3	0.79	0.80	0.87	0.88	1.00	1.04	1.13
2.5	0.74	0.74	0.81	0.83	0.93	0.97	1.06
2.7	0.69	0.70	0.76	0.78	0.88	0.91	1.00

eX Family Timing Characteristics

Table 1-17 • **eX Family Timing Characteristics (Worst-Case Commercial Conditions, V_{CCA} = 2.3V, T_J = 70°C)**

		‘–P’ Speed		‘Std’ Speed		‘–F’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]								
t_{PD}	Internal Array Module		0.7		1.0		1.4	ns
Predicted Routing Delays[2]								
t_{DC}	FO=1 Routing Delay, DirectConnect		0.1		0.1		0.2	ns
t_{FC}	FO=1 Routing Delay, FastConnect		0.3		0.5		0.7	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.5		0.7	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{RD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns
R-Cell Timing								
t_{RCO}	Sequential Clock-to-Q		0.6		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.9		1.3	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.7		1.0		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.9		2.6		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.5		0.7		ns
2.5V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.6		0.9		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.1		1.5	ns
3.3V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
5.0V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
Input Module Predicted Routing Delays[2]								
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{IRD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

Table 1-18 • **eX Family Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)**

		‘–P’ Speed		‘Std’ Speed		‘–F’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	2.8		4.0		5.6		ns
f_{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.1		1.6		2.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.5		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.5		2.1		3.0		ns
t_{RCKSW}[1]	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}[1]	Maximum Skew (50% Load)		0.1		0.2		0.3	ns
t_{RCKSW}[1]	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

Note:

1. Clock skew improves as the clock network becomes more heavily loaded.

Table 1-19 • **eX Family Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V or 3.0V, T_J = 70°C)**

		'–P' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	2.8		4.0		5.6		ns
f_{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		2.0		2.8		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		2.0		2.8		ns
t_{RCKSW}[1]	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}[1]	Maximum Skew (50% Load)		0.2		0.2		0.3	ns
t_{RCKSW}[1]	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

Note:

1. Clock skew improves as the clock network becomes more heavily loaded.

Table 1-20 • **eX Family Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.3V, T_J = 70°C)**

		'–P' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5V LVCMOS Output Module Timing[1] (V_{CCI} = 2.3V)								
t_{DLH}	Data-to-Pad LOW to HIGH		3.3		4.7		6.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.5		5.0		7.0	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		11.6		16.6		23.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		3.6		5.1	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		11.8		16.9		23.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.9		6.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		3.0		4.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.4		5.67		7.94	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.034		0.046		0.066	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
3.3V LVTTL Output Module Timing[1] (V_{CCI} = 3.0V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		4.0		5.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.7		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		9.7		13.9		19.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		3.2		4.4	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		9.7		13.9		19.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		4.0		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.8		4.0		5.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.8		5.3	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.02		0.03		0.046	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
5.0V TTL Output Module Timing[1] (V_{CCI} = 4.75V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.9		4.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.7		5.2	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		6.8		9.7		13.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.9		2.7		3.8	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		6.8		9.8		13.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		3.0		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.3		4.8		6.6	ns

Note:

1. Delays based on 35 pF loading.

Pin Description

CLKA/B **Routed Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL or LVTTL specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

GND **Ground**

LOW supply voltage.

HCLK **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL or LVTTL specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL or LVTTL specifications. Unused I/O pins are automatically tristated by the Designer software.

LP **Low Power Pin**

Controls the low power mode of the eX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation 200µs after the LP pin is driven to a logic LOW.

NC **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA/PRB, I/O **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This diagnostic pin can be used independently or in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-4 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer is being used, TDO will act as an output when the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-4 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached five TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the "Reserve JTAG Reset Pin" is not selected in the Designer software.

V_{CCI} **Supply Voltage**

Supply voltage for I/Os.

V_{CCA} **Supply Voltage**

Supply voltage for Array.

Package Pin Assignments

64-Pin TQFP

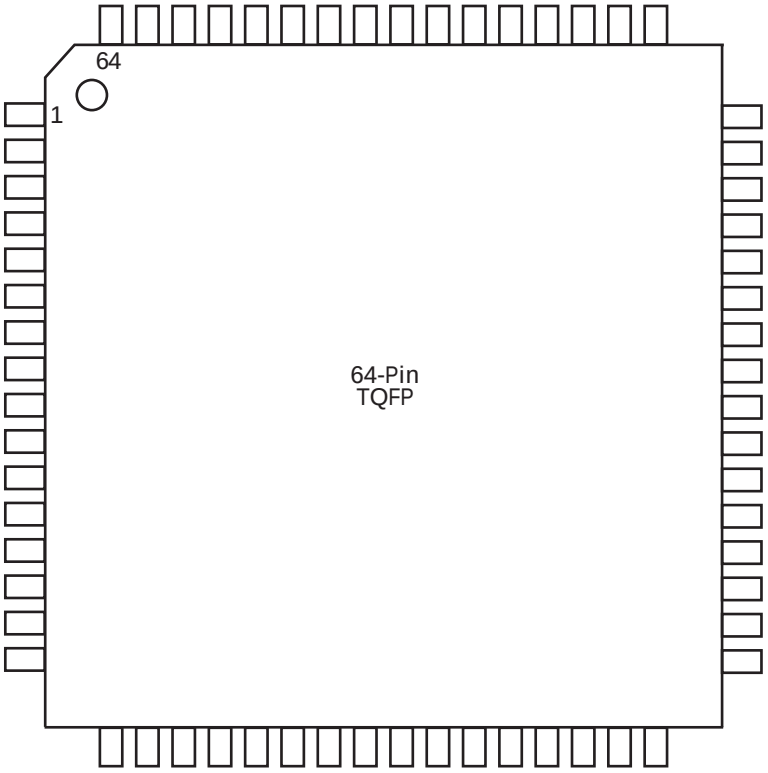


Figure 2-1 • **64-Pin TQFP**

64-Pin TQFP		
Pin Number	eX64 Function	eX128 Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	TMS	TMS
5	GND	GND
6	V_{CCI}	V_{CCI}
7	I/O	I/O
8	I/O	I/O
9	NC	I/O
10	NC	I/O
11	TRST, I/O	TRST, I/O
12	I/O	I/O
13	NC	I/O
14	GND	GND
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	V_{CCI}	V_{CCI}
20	I/O	I/O
21	PRB, I/O	PRB, I/O
22	V_{CCA}	V_{CCA}
23	GND	GND
24	I/O	I/O
25	HCLK	HCLK
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	TDO, I/O	TDO, I/O

Note: **Please read the LP pin descriptions for restrictions on their use*

64-Pin TQFP		
Pin Number	eX64 Function	eX128 Function
33	GND	GND
34	I/O	I/O
35	I/O	I/O
36	V_{CCA}	V_{CCA}
37	V_{CCI}	V_{CCI}
38	I/O	I/O
39	I/O	I/O
40	NC	I/O
41	NC	I/O
42	I/O	I/O
43	I/O	I/O
44	V_{CCA}	V_{CCA}
45*	GND/LP	GND/ LP
46	GND	GND
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	V_{CCI}	V_{CCI}
53	I/O	I/O
54	I/O	I/O
55	CLKA	CLKA
56	CLKB	CLKB
57	V_{CCA}	V_{CCA}
58	GND	GND
59	PRA, I/O	PRA, I/O
60	I/O	I/O
61	V_{CCI}	V_{CCI}
62	I/O	I/O
63	I/O	I/O
64	TCK, I/O	TCK, I/O

Note: **Please read the LP pin descriptions for restrictions on their use*

100-Pin TQFP

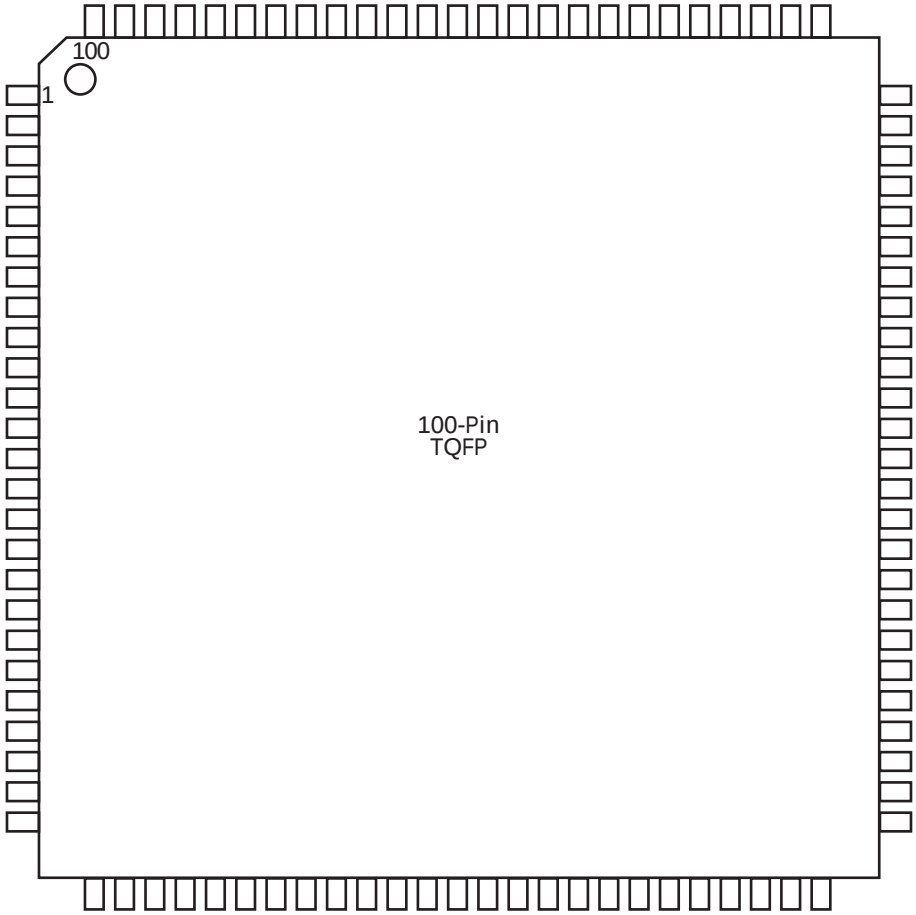


Figure 2-2 • **100-Pin TQFP (Top View)**

100-Pin TQFP			
Pin Number	eX64 Function	eX128 Function	eX256 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	NC	I/O
4	NC	NC	I/O
5	NC	NC	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V_{CCI}	V_{CCI}	V_{CCI}
9	GND	GND	GND
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	I/O	I/O
14	I/O	I/O	I/O
15	NC	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	NC	I/O	I/O
20	V_{CCI}	V_{CCI}	V_{CCI}
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	NC	NC	I/O
24	NC	NC	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O

Note: **Please read the LP pin descriptions for restrictions on their use*

100-Pin TQFP			
Pin Number	eX64 Function	eX128 Function	eX256 Function
35	V_{CCA}	V_{CCA}	V_{CCA}
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	NC	I/O	I/O
51	GND	GND	GND
52	NC	NC	I/O
53	NC	NC	I/O
54	NC	NC	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V_{CCA}	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}	V_{CCI}
59	NC	I/O	I/O
60	I/O	I/O	I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	NC	I/O	I/O
64	I/O	I/O	I/O
65	NC	I/O	I/O
66	I/O	I/O	I/O
67	V_{CCA}	V_{CCA}	V_{CCA}
68	GND/LP	GND/LP	GND/LP

Note: **Please read the LP pin descriptions for restrictions on their use*

100-Pin TQFP			
Pin Number	**eX64 Function**	**eX128 Function**	**eX256 Function**
69	GND	GND	GND
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	NC	I/O	I/O
73	NC	NC	I/O
74	NC	NC	I/O
75	NC	NC	I/O
76	NC	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V_{CCI}	V_{CCI}	V_{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V_{CCA}	V_{CCA}	V_{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

Note: **Please read the LP pin descriptions for restrictions on their use*

49-Pin CSP

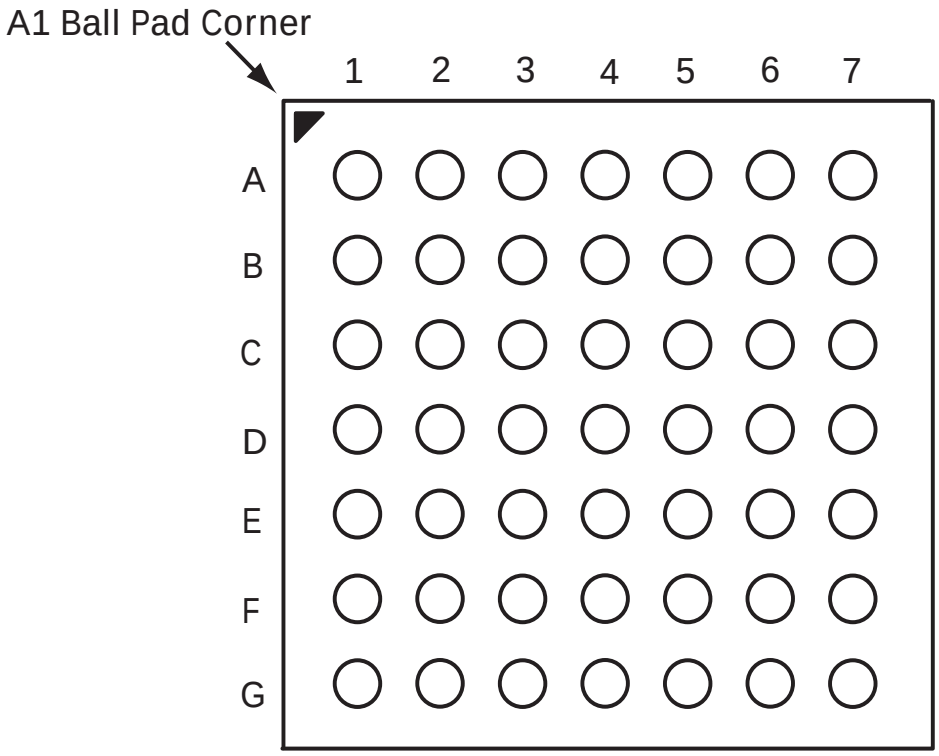


Figure 2-3 • **49-Pin CSP (Top View)**

49-Pin CSP		
Pin Number	**eX64 Function**	**eX128 Function**
A1	I/O	I/O
A2	I/O	I/O
A3	I/O	I/O
A4	I/O	I/O
A5	V_{CCA}	V_{CCA}
A6	I/O	I/O
A7	I/O	I/O
B1	TCK, I/O	TCK, I/O
B2	I/O	I/O
B3	I/O	I/O
B4	PRA, I/O	PRA, I/O
B5	CLKA	CLKA
B6	I/O	I/O
B7*	GND/LP*	GND/LP*
C1	I/O	I/O
C2	TDI, I/O	TDI, I/O
C3	V_{CCI}	V_{CCI}
C4	GND	GND
C5	CLKB	CLKB
C6	V_{CCA}	V_{CCA}
C7	I/O	I/O
D1	I/O	I/O
D2	TMS	TMS
D3	GND	GND
D4	GND	GND

Note: **Please read the LP pin descriptions for restrictions on their use.*

49-Pin CSP		
Pin Number	**eX64 Function**	**eX128 Function**
D5	V_{CCA}	V_{CCA}
D6	I/O	I/O
D7	I/O	I/O
E1	I/O	I/O
E2	TRST, I/O	TRST, I/O
E3	V_{CCI}	V_{CCI}
E4	GND	GND
E5	I/O	I/O
E6	I/O	I/O
E7	V_{CCI}	V_{CCI}
F1	I/O	I/O
F2	I/O	I/O
F3	I/O	I/O
F4	I/O	I/O
F5	HCLK	HCLK
F6	I/O	I/O
F7	TDO, I/O	TDO, I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	PRB, I/O	PRB, I/O
G5	V_{CCA}	V_{CCA}
G6	I/O	I/O
G7	I/O	I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

128-Pin CSP

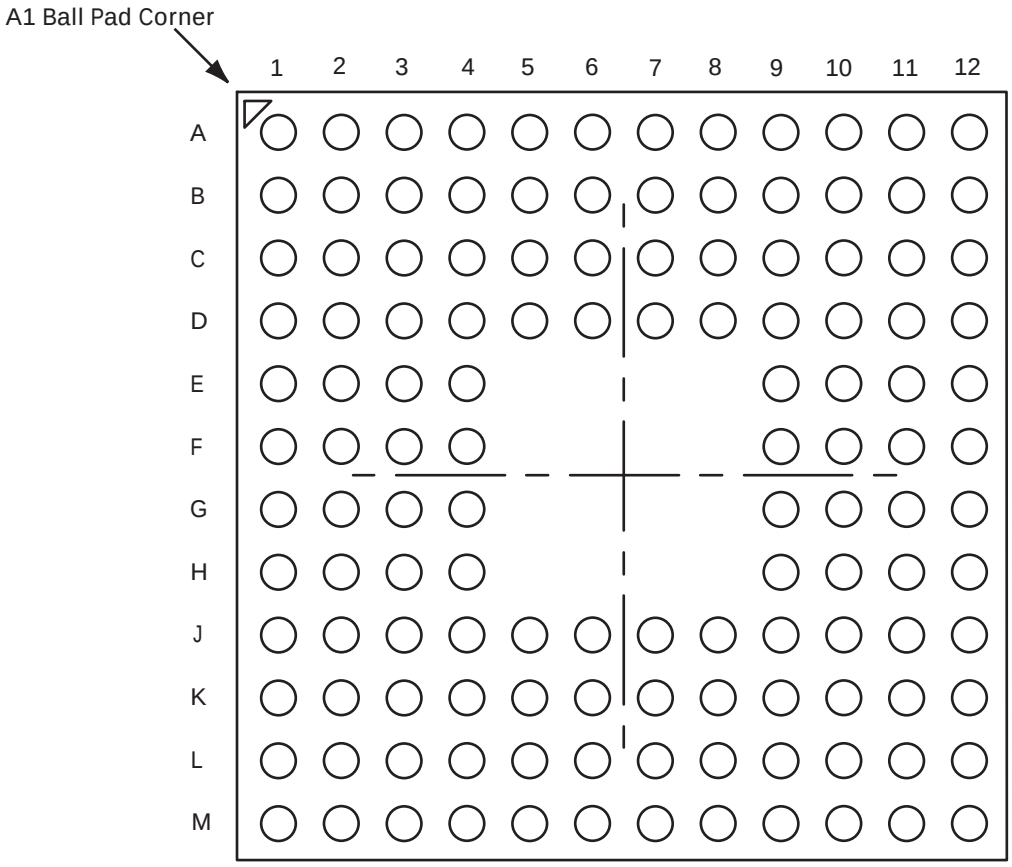


Figure 2-4 • **128-Pin CSP (Top View)**

128-Pin CSP			
Pin Number	eX64 Function	eX128 Function	eX256 Function
A1	I/O	I/O	I/O
A2	TCK, I/O	TCK, I/O	TCK, I/O
A3	V_{CCI}	V_{CCI}	V_{CCI}
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	V_{CCA}	V_{CCA}	V_{CCA}
A7	I/O	I/O	I/O
A8	I/O	I/O	I/O
A9	V_{CCI}	V_{CCI}	V_{CCI}
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	TMS	TMS	TMS
B2	I/O	I/O	I/O
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	PRA, I/O	PRA, I/O	PRA, I/O
B7	CLKB	CLKB	CLKB
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	TDI, I/O	TDI, I/O	TDI, I/O
C3	I/O	I/O	I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	CLKA	CLKA	CLKA
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

128-Pin CSP			
Pin Number	eX64 Function	eX128 Function	eX256 Function
C10	NC	I/O	I/O
C11	NC	I/O	I/O
C12	I/O	I/O	I/O
D1	NC	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	GND	GND	GND
D7	I/O	I/O	I/O
D8	GND	GND	GND
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	V_{CCI}	V_{CCI}	V_{CCI}
E1	NC	I/O	I/O
E2	V_{CCI}	V_{CCI}	V_{CCI}
E3	I/O	I/O	I/O
E4	GND	GND	GND
E9	GND	GND	GND
E10	I/O	I/O	I/O
E11*	GND/LP*	GND/LP*	GND/LP*
E12	V_{CCA}	V_{CCA}	V_{CCA}
F1	NC	I/O	I/O
F2	NC	I/O	I/O
F3	NC	I/O	I/O
F4	I/O	I/O	I/O
F9	GND	GND	GND
F10	NC	I/O	I/O
F11	I/O	I/O	I/O
F12	I/O	I/O	I/O
G1	NC	I/O	I/O
G2	TRST, I/O	TRST, I/O	TRST, I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

128-Pin CSP			
Pin Number	eX64 Function	eX128 Function	eX256 Function
G3	I/O	I/O	I/O
G4	GND	GND	GND
G9	GND	GND	GND
G10	NC	I/O	I/O
G11	I/O	I/O	I/O
G12	NC	I/O	I/O
H1	GND	GND	GND
H2	I/O	I/O	I/O
H3	V_{CCI}	V_{CCI}	V_{CCI}
H4	GND	GND	GND
H9	I/O	I/O	I/O
H10	V_{CCI}	V_{CCI}	V_{CCI}
H11	V_{CCA}	V_{CCA}	V_{CCA}
H12	NC	I/O	I/O
J1	NC	NC	V_{CCA}
J2	I/O	I/O	I/O
J3	V_{CCI}	V_{CCI}	V_{CCI}
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	I/O	I/O	I/O
J7	GND	GND	GND
J8	I/O	I/O	I/O
J9	GND	GND	GND
J10	I/O	I/O	I/O
J11	I/O	I/O	I/O
J12	NC	I/O	I/O
K1	NC	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	PRB, I/O	PRB, I/O	PRB, I/O
K7	HCLK	HCLK	HCLK

Note: **Please read the LP pin descriptions for restrictions on their use.*

128-Pin CSP			
Pin Number	eX64 Function	eX128 Function	eX256 Function
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O
K10	I/O	I/O	I/O
K11	TDO, I/O	TDO, I/O	TDO, I/O
K12	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	NC	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	I/O	I/O	I/O
L8	I/O	I/O	I/O
L9	I/O	I/O	I/O
L10	I/O	I/O	I/O
L11	NC	I/O	I/O
L12	V_{CCI}	V_{CCI}	V_{CCI}
M1	GND	GND	GND
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	V_{CCA}	V_{CCA}	V_{CCA}
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	I/O	I/O	I/O
M12	I/O	I/O	I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

180-Pin CSP

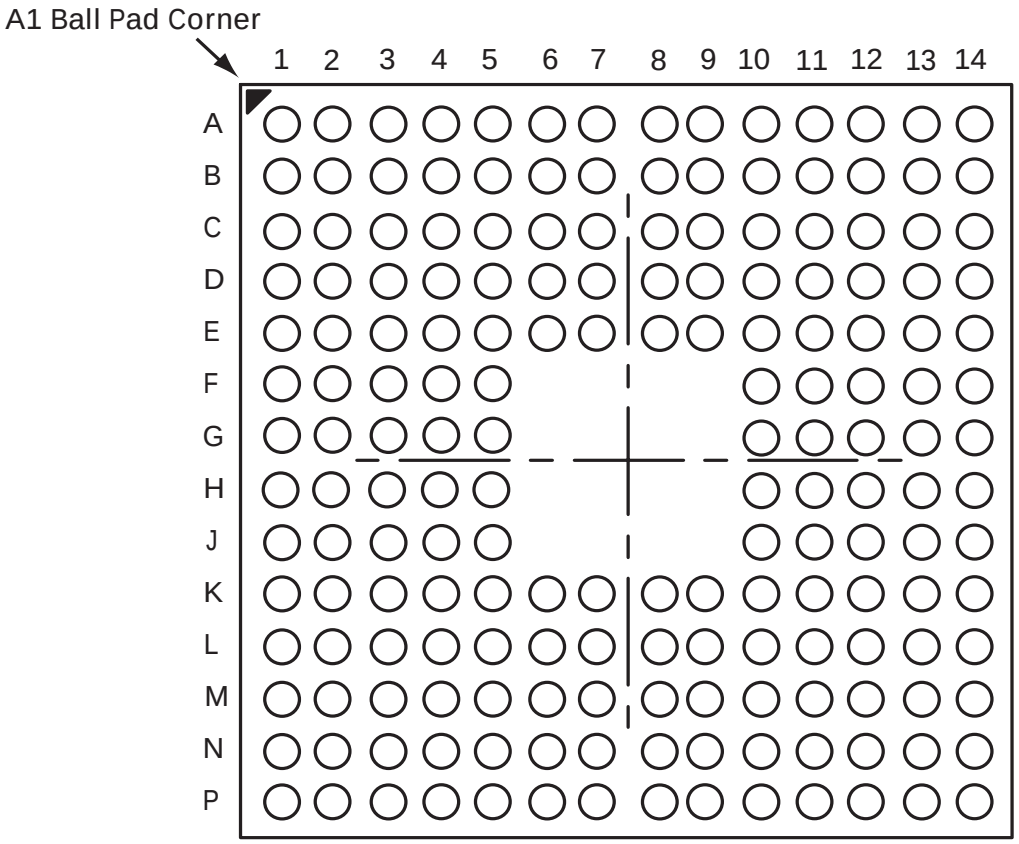


Figure 2-5 • **180-Pin CSP**

180-Pin CSP	
Pin Number	eX256 Function
A1	I/O
A2	I/O
A3	GND
A4	NC
A5	NC
A6	NC
A7	NC
A8	NC
A9	NC
A10	NC
A11	NC
A12	I/O
A13	I/O
A14	I/O
B1	I/O
B2	I/O
B3	TCK, I/O
B4	V_{CCI}
B5	I/O
B6	I/O
B7	V_{CCA}
B8	I/O
B9	I/O
B10	V_{CCI}
B11	I/O
B12	I/O
B13	I/O
B14	I/O
C1	I/O
C2	TMS
C3	I/O
C4	I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

180-Pin CSP	
Pin Number	eX256 Function
C5	I/O
C6	I/O
C7	PRA, I/O
C8	CLKB
C9	I/O
C10	I/O
C11	I/O
C12	GND
C13	I/O
C14	I/O
D1	I/O
D2	I/O
D3	TDI, I/O
D4	I/O
D5	I/O
D6	I/O
D7	CLKA
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O
D13	I/O
D14	I/O
E1	I/O
E2	I/O
E3	I/O
E4	I/O
E5	I/O
E6	I/O
E7	GND
E8	I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

180-Pin CSP	
Pin Number	eX256 Function
E9	GND
E10	I/O
E11	I/O
E12	I/O
E13	V_{CCI}
E14	I/O
F1	I/O
F2	I/O
F3	V_{CCI}
F4	I/O
F5	GND
F10	GND
F11	I/O
F12*	GND/LP*
F13	V_{CCA}
F14	I/O
G1	V_{CCA}
G2	I/O
G3	I/O
G4	I/O
G5	I/O
G10	GND
G11	I/O
G12	I/O
G13	I/O
G14	V_{CCA}
H1	I/O
H2	I/O
H3	TRST, I/O
H4	I/O
H5	GND
H10	GND

Note: **Please read the LP pin descriptions for restrictions on their use.*

180-Pin CSP	
Pin Number	eX256 Function
H11	I/O
H12	I/O
H13	I/O
H14	I/O
J1	I/O
J2	GND
J3	I/O
J4	V_{CCI}
J5	GND
J10	I/O
J11	V_{CCI}
J12	V_{CCA}
J13	I/O
J14	I/O
K1	I/O
K2	V_{CCA}
K3	I/O
K4	V_{CCI}
K5	I/O
K6	I/O
K7	I/O
K8	GND
K9	I/O
K10	GND
K11	I/O
K12	I/O
K13	I/O
K14	I/O
L1	I/O
L2	I/O
L3	I/O
L4	I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

180-Pin CSP	
Pin Number	**eX256 Function**
L5	I/O
L6	I/O
L7	PRB, I/O
L8	HCLK
L9	I/O
L10	I/O
L11	I/O
L12	TDO, I/O
L13	I/O
L14	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M5	I/O
M6	I/O
M7	I/O
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	I/O
M13	V_{CCI}
M14	I/O
N1	I/O
N2	GND
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	I/O
N8	V_{CCA}

Note: **Please read the LP pin descriptions for restrictions on their use.*

180-Pin CSP	
Pin Number	**eX256 Function**
N9	I/O
N10	I/O
N11	I/O
N12	I/O
N13	I/O
N14	I/O
P1	I/O
P2	I/O
P3	I/O
P4	NC
P5	NC
P6	NC
P7	NC
P8	NC
P9	NC
P10	NC
P11	NC
P12	GND
P13	I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v4.2)	Page
v4.1	The "eX Timing Model" was updated.	1-18
v4.0	The "Development Tool Support" section was updated.	1-12
	The "Package Thermal Characteristics" section was updated.	1-17
v3.0	The "Product Profile" section was updated.	1-i
	The "Ordering Information" section was updated.	1-ii
	The "Temperature Grade Offerings" section is new.	1-ii
	The "Speed Grade and Temperature Grade Matrix" section is new.	1-ii
	The "General Description" section was updated.	1-1
	The "Clock Resources" section was updated.	1-4
	Table 1-1 • Connections of Routed Clock Networks, CLKA and CLKB is new.	1-4
	The "User Security" section was updated.	1-5
	The "I/O Modules" section was updated.	1-5
	The "Hot Swapping" section was updated.	1-6
	The "Power Requirements" section was updated.	1-6
	The "Low Power Mode" section was updated.	1-6
	The "Boundary Scan Testing (BST)" section was updated.	1-9
	The "Dedicated Test Mode" section was updated.	1-9
	The "Flexible Mode" section was updated.	1-9
	Table 1-5 • Boundary-Scan Pin Configurations and Functions is new.	1-9
	The "TRST Pin" section was updated.	1-9
	The "Probing Capabilities" section is new.	1-10
	The "Programming" section was updated.	1-10
	The "Probing Capabilities" section was updated.	1-10
	The "Silicon Explorer II Probe" section was updated.	1-10
	The "Design Considerations" section was updated.	1-11
	The "Development Tool Support" section was updated.	1-12
	The "Absolute Maximum Ratings*" section was updated.	1-13
	The "Temperature and Voltage Derating Factors" section was updated.	1-21
	The "TDI, I/O Test Data Input" section was updated.	1-26
	The "TDO, I/O Test Data Output" section was updated.	1-26
	The "TMS Test Mode Select" section was updated.	1-26
	The "TRST, I/O Boundary Scan Reset Pin" section was updated.	1-26

v3.0	All VSV pins were changed to V_{CCA}. The change affected the following pins: 64-Pin TQFP –Pin 36 100-Pin TQFP –Pin 57 49-Pin CSP –Pin D5 128-Pin CSP–Pin H11 and Pin J1 for eX256 180-Pin CSP –Pins J12 and K2	
v2.0.1	The "Recommended Operating Conditions" section has been changed.	1-13
	The "3.3V LVTTL Electrical Specifications" section has been updated.	1-15
	The "5.0V TTL Electrical Specifications" section has been updated.	1-15
	The "Total Dynamic Power (mW)" section is new.	1-8
	The "System Power at 5%, 10%, and 15% Duty Cycle" section is new.	1-8
	The "eX Timing Model" section has been updated.	1-18
Advanced v0.4	The I/O Features table, Table 1-2 on page 1-5, was updated.	1-5
	The table, "Standby Power of eX Devices in LP Mode Typical Conditions, VCCA, VCCI = 2.5V, TJ = 25× C" section, was updated.	1-6
	"Typical eX Standby Current at 25°C" section is a new table.	1-13
	The table in the section, "Package Thermal Characteristics" section has been updated for the 49-Pin CSP.	1-17
	The "eX Timing Model" section has been updated.	1-18
	The timing numbers found in, "eX Family Timing Characteristics" section have been updated.	1-22
	The V_{SV} pin has been added to the "Pin Description" section.	1-26
	Please see the following pin tables for the V_{SV} pin and an important footnote including the pin: "64-Pin TQFP","100-Pin TQFP",, ,"128-Pin CSP", and "180-Pin CSP".	2-1, 2-3, 2-6, 2-11
	The figure, "64-Pin TQFP" section has been updated.	2-1
Advanced v0.3	In the Product Profile, the Maximum User I/Os for eX64 was changed to 84.	1-i
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-i
Advanced v0.2	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, “Package Characteristics and Mechanical Drawings,” available on the Actel web site.	
	A new section describing "Clock Resources"has been added.	1-4
	A new table describing "I/O Features"has been added.	1-5
	The "Pin Description"section has been updated and clarified.	1-26
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL}.	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the "100-Pin TQFP"table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages 27, 31
Advanced v.1	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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