8A, 30V, Synchronous Step-Down Converter with Programmable Frequency

DESCRIPTION

The EUP3288 is a synchronous, step-down constant on-time buck regulator capable of driving 8A continuous load current. The EUP3288 can operate with an input range 4.5V to 30V and the output can be externally set down to 0.8V. The EUP3288 provides excellent transient response with constant on-time control method while maintaining a nearly constant frequency. The switching frequency can be externally programmed from 100KHz to 1MHz.

Fault condition protection includes VIN under-voltage lockout, cycle-by-cycle current limiting, output over-voltage protection, output under-voltage protection, as well as thermal shutdown. Internal soft-start minimizes the inrush supply current and the output overshoot at initial startup.

The EUP3288 is available in a 4mm x 4mm TQFN-23 package.

FEATURES

- Wide Input Voltage Range: 4.5V to 30V
- 8A Output Current
- Excellent Line and Load Transient Responses
- Integrated 23mΩ N-Channel MOSFET for High Side
- Integrated 13mΩ N-Channel MOSFET for Low Side
- Programmable PWM Frequency from 100KHz to 1MHz
- Internal Soft-Start
- Selectable Forced PWM or Automatic PFM/PWM Mode
- Power Good Monitoring
- Under-Voltage Protection
- Over-Voltage Protection
- Cycle-by-Cycle Current Limit
- Over-Temperature Protection
- Available in TQFN-23 4mmx4mm Package
- RoHS Compliant and Halogen-Free

APPLICATIONS

- Notebook
- Mother Board
- Table PC
- Hand-Held Portable
- AIO PC
- Set-top boxes
- LCD TV
- Telecom/Networking/Datacom equipment

Typical Application Circuit

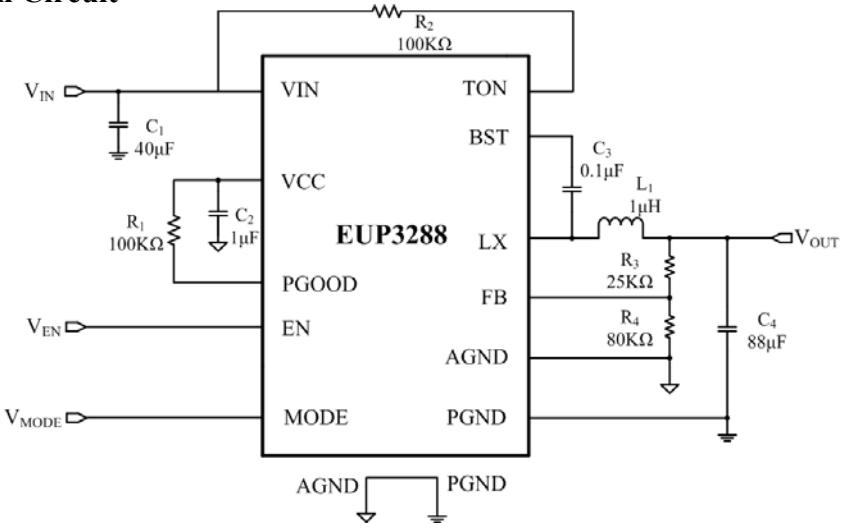
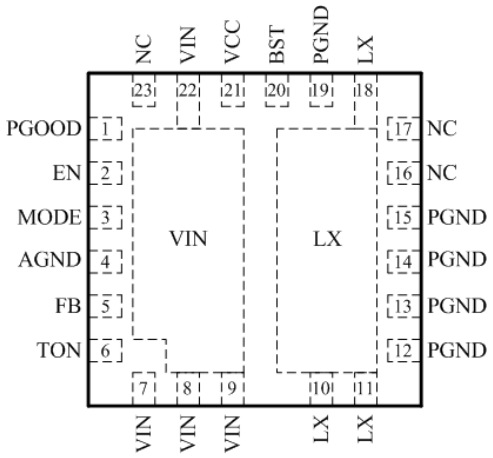


Figure 1. Application Circuit

Pin Configurations

Package Type	Pin Configurations
TQFN-23	(TOP VIEW) 

Pin Description

Pin	Pin Name	Description
1	PGOOD	Power good output pin. PGOOD indicates the status of the output voltage. Connect PGOOD to VCC through pull-up resistor
2	EN	Enable pin. Chip is enabled when EN=1, shutdown when EN=0
3	MODE	Mode selection pin. Connect MODE to high for PWM operation, to low for automatic PFM/PWM mode operation
4	AGND	Signal ground pin
5	FB	Output voltage feedback pin
6	TON	On-time setting pin. Connect TON to VIN with a resistor to set the on-time
16, 17, 23	NC	Not connected
7, 8, 9, 22	VIN	Power supply input pin
10, 11, 18	LX	Switching output pin
12, 13, 14, 15, 19	PGND	Power ground pin
20	BST	Bootstrap capacitor connection pin. BST is power supply for high side gate driver. Connect an external capacitor between BST and LX
21	VCC	5V LDO output pin. Connect a 1uF ceramic capacitor between VCC and AGND

Ordering Information

Order Number	Package Type	Marking	Quantity per Reel	Operating Temperature Range
EUP3288JIR1	TQFN-23	xxxxx P3288	2500	-40 °C to +85°C

EUP3288 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen-Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  J: TQFN

Block Diagram

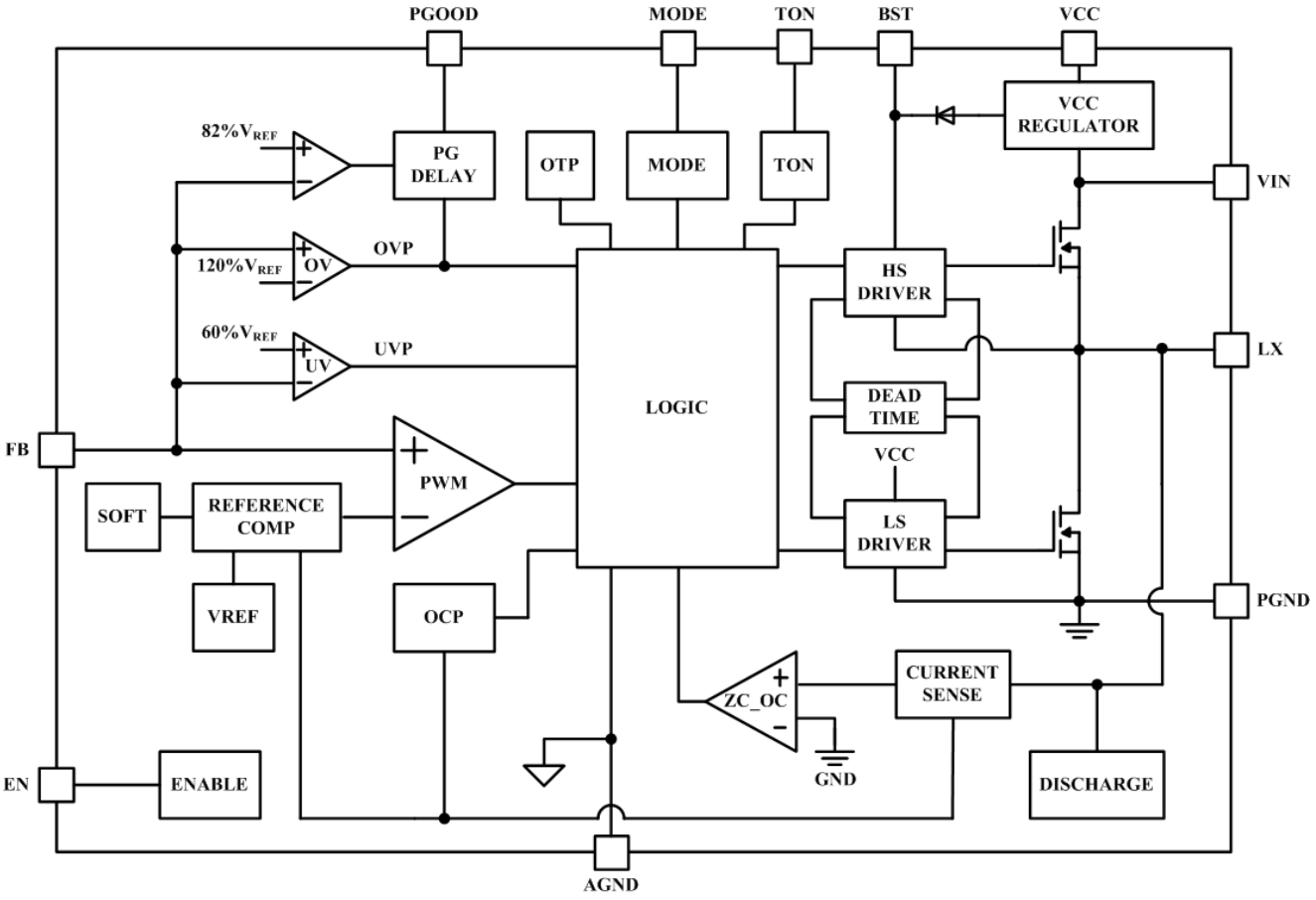


Figure 2. Functional Block Diagram

Absolute Maximum Ratings (1)

- Input Voltage (V_{IN}) ---------- -0.3V to 30V
- Enable Voltage (V_{EN}) ---------- -0.3V to 30V
- Mode Voltage (V_{MODE}) ---------- -0.3V to 30V
- Ton Voltage (V_{TON}) ---------- -0.3V to 30V
- Switch Voltage (V_{LX}) ---------- -1V to V_{IN} +0.3V
- Bootstrap Voltage(V_{BST}) ---------- V_{LX}-0.3V to V_{LX}+6V
- All Other Pins ---------- -0.3V to 6V
- Junction Temperature ---------- 150°C
- Storage Temperature ---------- -65°C to +150°C
- Lead Temp(Soldering, 10sec) ---------- 260°C
- Thermal Resistance θ_{JA} (TQFN-23) ---------- 45°C/W
- Thermal Resistance θ_{JC} (TQFN-23) ---------- 4.5°C/W

Recommend Operating Conditions (2)

- Supply Voltage (V_{IN}) ---------- 4.5V to 28V
- Output Voltage (V_{OUT}) ---------- 0.8V to 20V
- Ambient Operating Temperature ---------- -40°C to +85°C

Note(1):Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note(2):The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

(V_{IN}=12V, T_A=+25°C, unless otherwise specified)

Symbol	Parameter	Conditions	EUP3288			Unit
			Min.	Typ.	Max.	
General Section						
V_{IN}	Input Voltage Range		4.5		30	V
V_{UVLO}	V_{IN} UVLO Threshold	V_{IN} Rising	3.8	4.1	4.4	V
V_{UVLO_HYS}	V_{IN} UVLO Threshold Hysteresis			300		mV
I_Q	Quiescent Current	V_{FB}=105%×V_{REF}, SW open		110		μA
I_{SD}	Shutdown Current	V_{EN}=0V		3.5	10	μA
V_{FB}	Feedback Voltage	T_A=25°C	0.792	0.800	0.808	V
		T_A=0°C ~85°C	0.788	0.800	0.812	V
T_{SS}	Soft Start Time			2		ms
Control Section						
V_{EN}	Enable Threshold	On state	1.5			V
		Off state			0.5	V
V_{MODE}	Mode Select Threshold	Force PWM mode	1.5			V
		Auto PFM/PWM mode			0.5	V
Modulator Section						
T_{ON}	On Time	V_{IN}=12V, R_{TON}=100KΩ	200	250	300	ns
T_{ON_MIN}	Minimum on Time			50		ns
T_{OFF_MIN}	Minimum off Time			250		ns
Power MOS Section						
R_{ONH}	High Side MOS on Resistance	V_{IN}=12V, V_{CC}=5V		23		mΩ
R_{ONL}	Low Side MOS on Resistance	V_{IN}=12V, V_{CC}=5V		13		mΩ
Power Good Section						
V_{PGLR}	PGOOD High to Low Threshold	FB rising	117	120	123	%
V_{PGLF}		FB falling	79	82	85	%
V_{PG_HYS}	PGOOD Threshold Hysteresis			3		%
V_{PG_LOW}	PGOOD Low Voltage	R_{PGOOD}=100KΩ			0.3	V
T_{PG_LOW}	PGOOD Fault Delay Time	FB falling		30		μs

Electrical Characteristics (Continued)

(VIN=12V, T_A=+25°C, VEN=5V, unless otherwise specified)

Symbol	Parameter	Conditions	EUP3288			Unit
			Min.	Typ.	Max.	
Protection Section						
I_{OCP}	Valley Inductor Current Limit			12		A
V_{UV}	Output UVP Threshold	FB falling	57	60	63	%
T_{UV}	Output UVP Delay Time	FB falling		120		µs
V_{OV}	Output OVP threshold	FB rising	117	120	123	%
T_{OV}	Output OVP Delay Time	FB rising		10		µs
T_{SD}	Thermal Shutdown Threshold			150		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			35		°C

External Components for Typical Designs

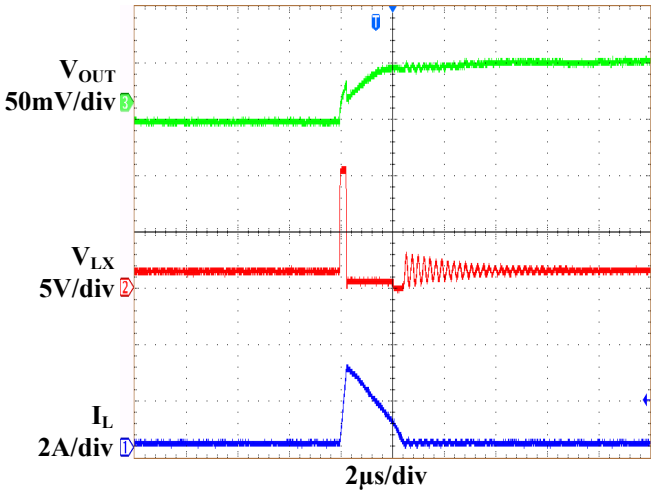
V_{OUT} (V)	F_{LX} (KHz)	R_2 (KΩ)	R_3 (KΩ)	R_4 (KΩ)	L_1 (µH)	C_1 (µF)	C_5 (µF)
1.05	400	100	6.98	22.1	1	10×4	22×4
3.3	400	309	69.5	22.1	3.3	10×4	22×4
5	400	464	63.4	12	4.7	10+100	22×4
9	150	2400	124	12	15	10+100	22×4
12	150	3400	169	12	15	10+100	22×4
20	150	5500	300	12.4	10	10+100	22×4

Typical Operating Characteristics

T_A=25°C, V_{IN}=12V, V_{OUT}=1.05V, F_{LX}=400KHz, unless otherwise specified.

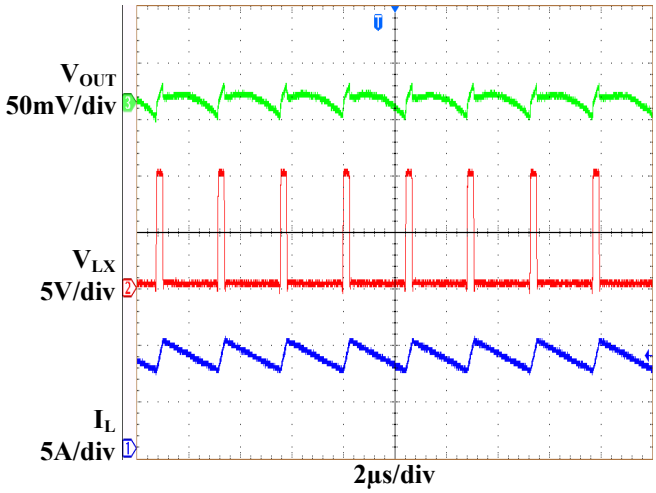
Steady State

V_{IN}=12V, V_{OUT}=1.05V, No load, PFM/PWM



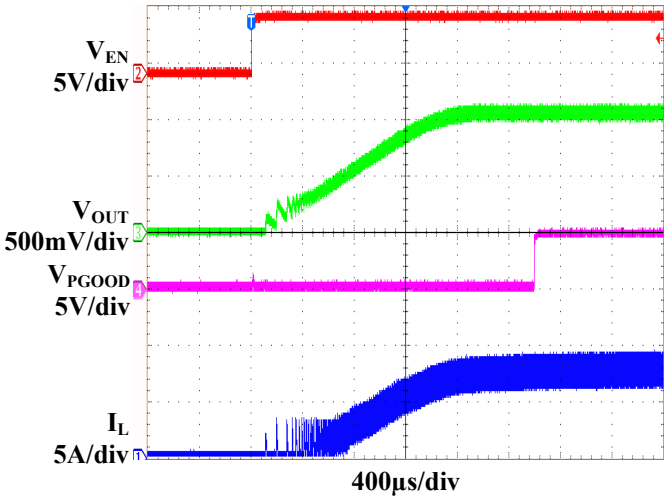
Steady State

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A, PFM/PWM



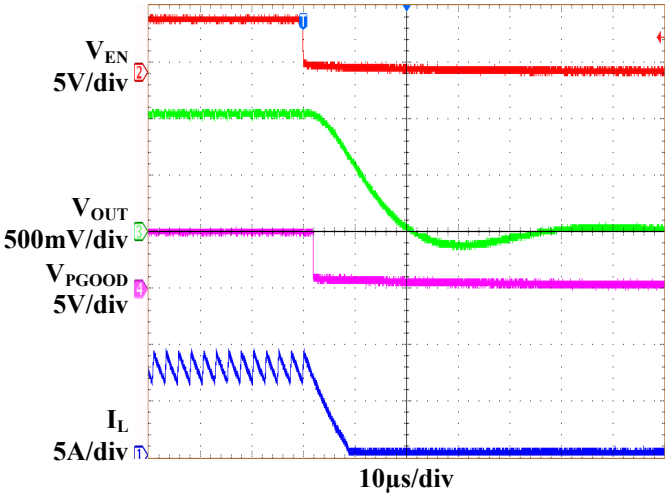
Startup through Enable

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A, PFM/PWM



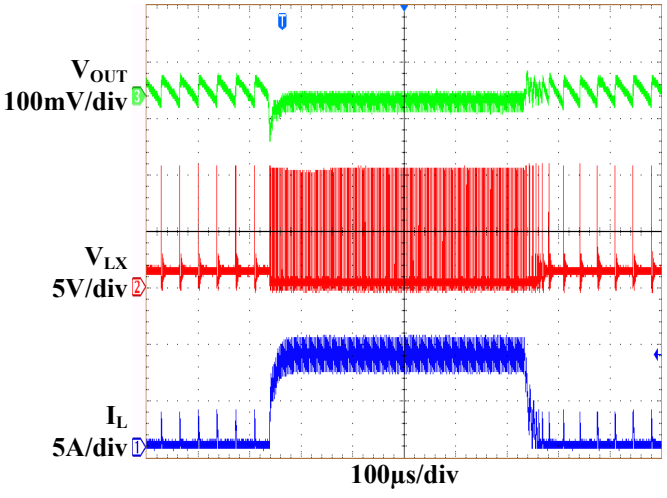
Shutdown through Enable

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A, PFM/PWM



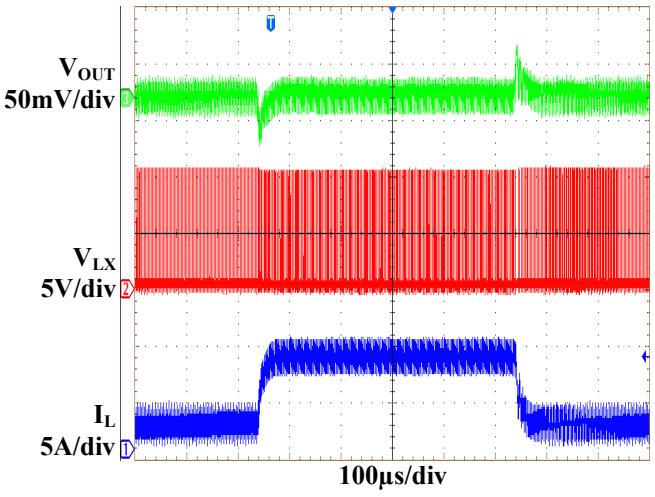
Load Transient Response

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=0.1A to 8A, PFM/PWM



Load Transient Response

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=2A to 8A, PFM/PWM

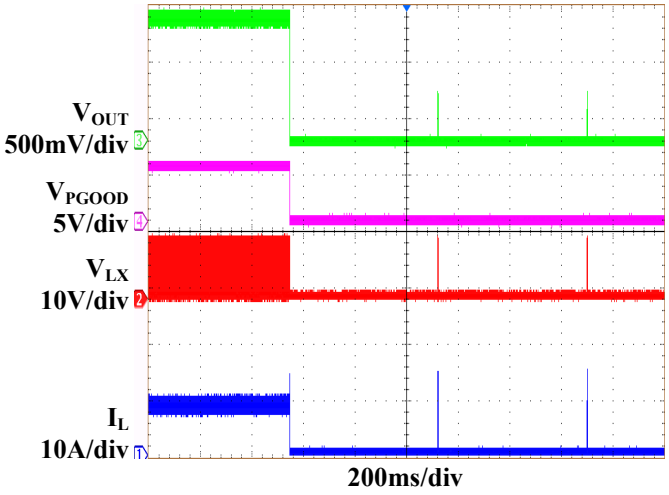


Typical Operating Characteristics

T_A=25°C, V_{IN}=12V, V_{OUT}=1.05V, F_{LX}=400KHz, unless otherwise specified.

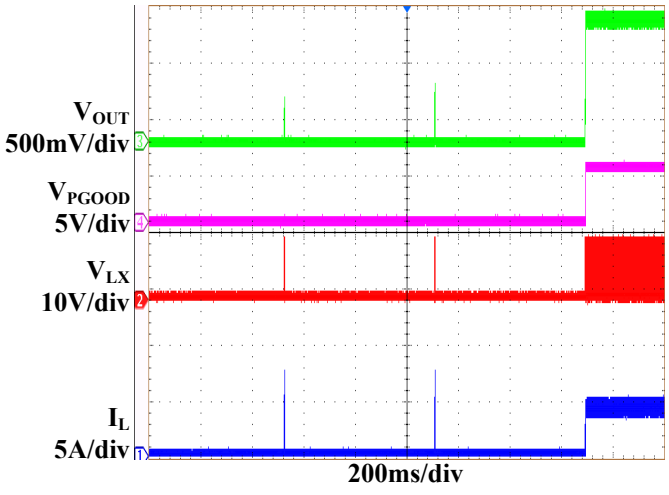
Short Circuit

V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A, PFM/PWM

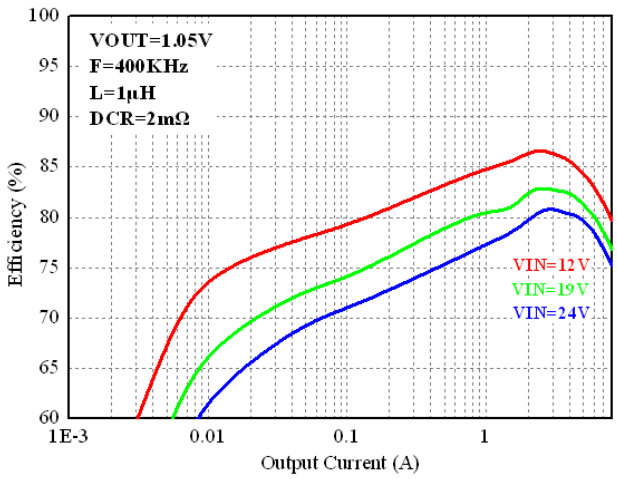


Short Circuit Recovery

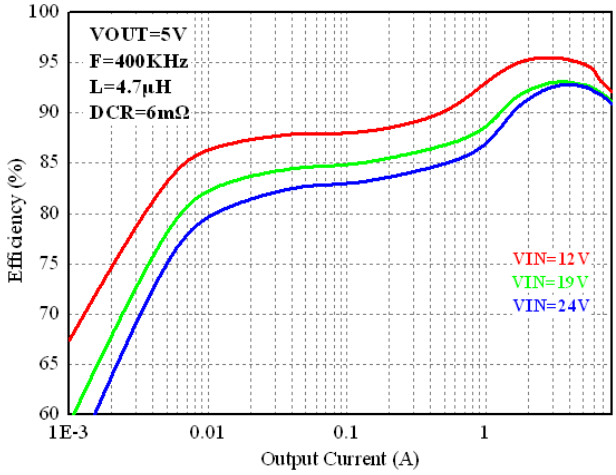
V_{IN}=12V, V_{OUT}=1.05V, I_{OUT}=8A, PFM/PWM



Efficiency vs. Output Current



Efficiency vs. Output Current



Functional Description

The EUP3288 is a constant on-time synchronous step-down converter with 4.5V to 30V input power supply. The device can provide up to 8A continuous current to the output. This architecture provides very fast on-time response to output load transients. The switching frequency can be externally programmed from 100KHz to 1MHz.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between LX and BST is needed to drive the high side gate. The bootstrap capacitor is charged from the internal 5V rail when LX is low. At light loads, the inductor current may reach zero or reverse on each pulse. The bottom MOS is turned off by the current reversal comparator and the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for the switching regulator. At light load, the EUP3288 will automatically skip pulses in pulse frequency modulation (PFM) mode to maintain output regulation and increases efficiency.

When the FB pin voltage exceeds 20% of the nominal regulation value of 0.8V, the over voltage comparator is tripped and forcing the high-side switch off.

Constant On-time Architecture with Reference Compensation

The EUP3288 uses constant on-time control method with reference compensation as shown below:

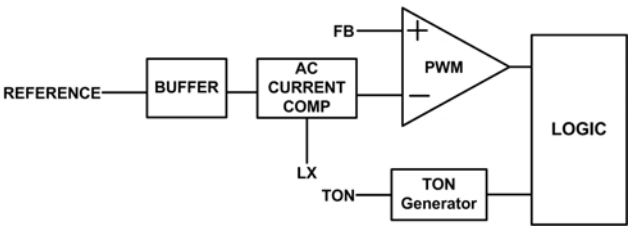


Figure 3. Simplified control topology of EUP3288

The on-time of EUP3288 is determined by TON generator whose pulse width can be programmed by external resistor and is inversely proportional to input voltage (V_{IN}). And this pulse is triggered when the feedback voltage (V_{FB}) reaches the compensation reference voltage, which is the internal reference voltage further processed by the AC current information of inductor. This compensation reference voltage can help the loop stability in pure ceramic output capacitors application, for low ESR of ceramic capacitor would cause unstable condition.

The constant on-time control architecture is a pseudo-fixed frequency and does not use a clock signal to produce trigger signal. The on-time of high-side switch is set by internal circuits, which is proportional to output voltage V_{OUT} and inverse proportional to input voltage V_{IN}:

$$T_{ON} = \frac{26.3 \times 10^{-12} \times R_{TON}(\Omega)}{V_{IN}(V)}$$

Where R_{TON} is the resistor connected from V_{IN} pin to T_{ON} pin. As in buck DC-DC converter we have:

$$T_{ON} = D \times T = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{LX}}$$

Thus, the switching frequency keeps constant and is independent with input voltage as shown below:

$$F_{LX} = \frac{V_{OUT}(V) \times 10^{12}}{26.3 \times R_{TON}(\Omega)}$$

Soft-Start

The EUP3288 has internal soft start feature to minimize the inrush supply current and the output overshoot at initial startup. When the EUP3288 starts up, the internal reference voltage which is compared with V_{FB} ramps up gradually, so the output voltage ramps up as well. The typical soft-start time is 2ms.

Over Current Protection

If the sensed current value is above the over current (OC) setting, the converter delays the next ON pulse until the current drops below the OC limit. Current limiting occurs on a pulse-by-pulse basis. The EUP3288 uses a valley current limiting scheme where the DC current point is the OC limit plus half of the inductor ripple current. The typical valley OC limit is 12A.

$$I_{OC\_DC} = I_{OC\_vally} + \frac{1}{2} \times I_{Peak-to-Peak}$$

Over Voltage Protection

OVP (over voltage protection) function with fixed OV (over voltage) threshold set by the internal resistor divider is provided. When output over voltage occurs, the high-side switch turns off and low-side switch turns on cycle-by-cycle until the output over voltage is released.

Under Voltage Protection

UVP (under voltage protection) function continually monitors the FB voltage after soft-start is completed. If output voltage is lower than 60% of the nominal output voltage by over current or short circuit, the device will enter hiccup mode. In hiccup mode, there is a 450ms delay time period before restart.

Power Good

The EUP3288 has one open-drain power good (PGOOD) pin. The PGOOD pin de-asserts as soon as the EN pin is pulled low, or output voltage is 18% lower or 20% higher than nominal value, or any other faults that require latch off action is detected.

Thermal Shutdown

The EUP3288 stops switching when its junction temperature exceeds 150°C and resumes when the temperature has dropped by 35°C to protect the device.

Application Information

Setting the Output Voltage

The output voltage is set through a resistive voltage divider and can be expressed by the equation as follows

$$V_{OUT} = 0.8 \times \frac{R3 + R4}{R4}$$

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{LX} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{LX} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current. Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times F_{LX} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where I_{LOAD} is the load current. The choice of which style inductor to use mainly depends on the price v.s. size requirements and any EMI constraints.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors. Since the input capacitor (C_1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{C1} = I_{LOAD}/2$. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, or a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C_1 \times F_{LX}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_1 is the input capacitance value. For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

Output Capacitor

The output capacitor (C_5) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{LX} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{LX} \times C_4}\right)$$

Where C_4 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{LX}^2 \times L \times C_4} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{LX} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The EUP3286E can be optimized for a wide range of capacitance and ESR values.

Thermal Considerations

To avoid the EUP3288 from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = P_D \times \theta_{JA}$$

$$P_D = V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT} - I_{OUT}^2 \times R_{DCR}$$

Where P_D is the power dissipated by the regulator; θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature; R_{DCR} is resistor of inductor. Then the junction temperature, T_J, is given by:

$$T_J = T_A \times T_R$$

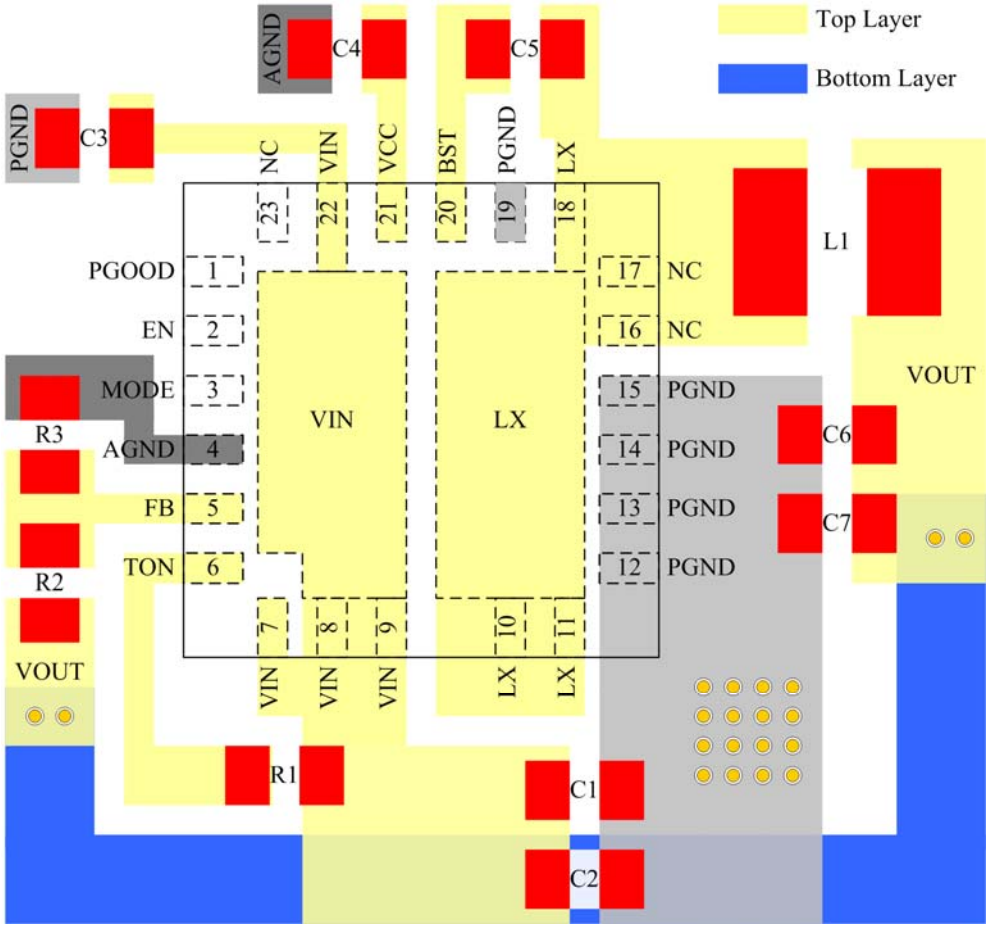
where T_A is the ambient temperature. T_J should be below the maximum junction temperature of 150°C.

PCB Layout Checklist

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems. When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3288.

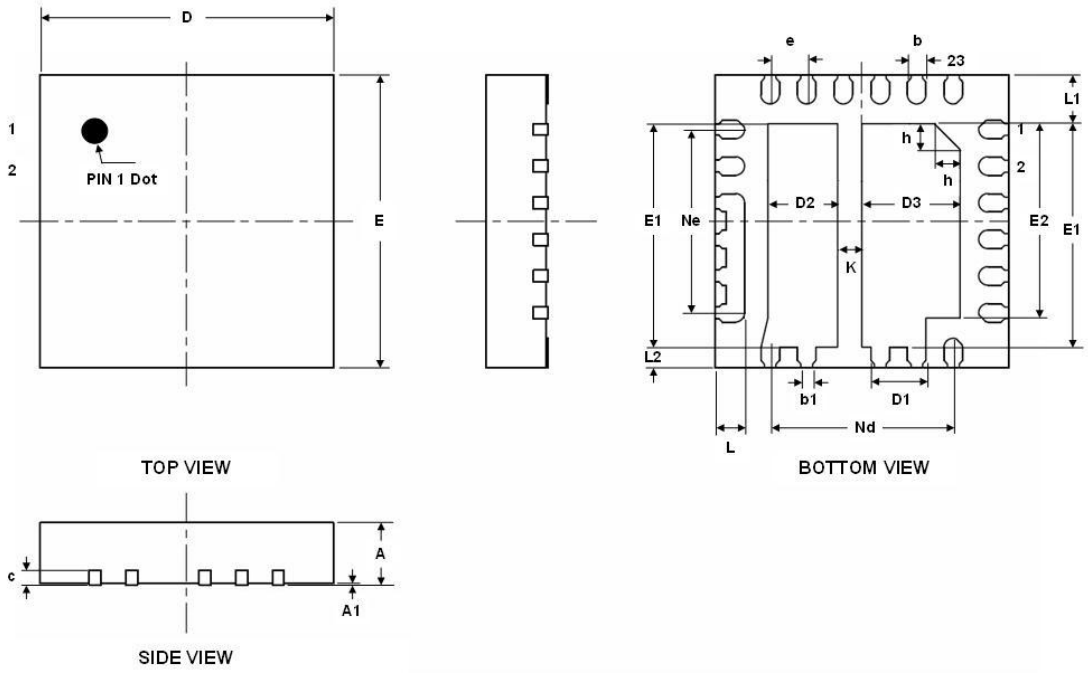
1. The input capacitor C1/C2/C3 should place to VIN pin as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
2. The power traces, consisting of the PGND trace, the LX trace and the VIN trace should be kept short, direct and wide.
3. The VOUT pin should connect directly to the inductor output. The resistive divider R2/R3 must be connected as close as possible between the FB and AGND.
4. Keep the switching node, LX, away from the sensitive VOUT/FB node.

An example of PCB layout guide is shown in the figure below for reference.



Packaging Information

TQFN-23



Note: The exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
b1		0.16 REF			0.006 REF	
D	3.90	4.00	4.10	0.154	0.157	0.161
D1	0.65	0.75	0.85	0.026	0.030	0.033
D2	0.85	0.95	1.05	0.033	0.037	0.041
D3	1.24	1.34	1.44	0.049	0.053	0.057
e		0.50 REF			0.020 REF	
Ne		2.50 REF			0.098 REF	
Nd		2.50 REF			0.098REF	
E	3.90	4.00	4.10	0.154	0.157	0.161
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	2.60	2.65	2.70	0.102	0.104	0.106
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.57	0.62	0.67	0.022	0.024	0.026
L2	0.23	0.28	0.33	0.009	0.011	0.013
K	0.33	-	-	0.013	-	-
h	0.30	0.35	0.40	0.012	0.014	0.016